RF FRONT-END OF A RECEIVER FOR A 3 TESLA MAGNETIC RESONANCE IMAGER

by

Işıl KALAFAT KIZILKAYA

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Throughout my thesis study not just my knowledge about analog design but also a lot of things has evolved in my life. I was a single student who was really thrilling about the word of “analog” at first; but now I am a married woman who is planning to make her academic career on analog design.

I would first like to thank my advisor Assist. Prof. Arda DENİZ YALÇINKAYA who has always relaxed me with his cool attitude and knowledge whenever I came up with a problem.

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Finally; I would like to say that, I have always supported by the best family in the world and a beloved husband. If my family would not dream my academic career as much as I do, I would not be able to finish all those sleepless nights.

ABSTRACT

RF FRONT-END OF A RECEIVER FOR A 3 TESLA MAGNETIC RESONANCE IMAGER

In this study, a front-end circuitry is designed for a 3 Tesla Magnetic Resonance Imager Receiver with UMC 0.18 μm technology. Folded cascode topology is seemed to be the optimum design for our design specifications which are 1.2 V supply voltage, <2 mW power consumption and <1 dB NF. For the designed fully differential folded cascode low-noise amplifiers (FDFC LNAs), layouts are drawn and the layout of the FDFC LNA with NMOS input pair is sent to fabrication. For FDFC LNA with NMOS input pair; 54 dB voltage gain, 34 dB power gain is obtained. A noise figure of 0.4 dB in schematic simulations, 0.7 dB in post-layout simulations is measured. For FDFC LNA with PMOS input pair; 57.5 dB voltage gain, 36.5 dB power gain is obtained. A noise figure of 0.5 dB in schematic simulations, 0.8 dB in post-layout simulations is measured. Both LNAs have power consumption of 1.7 mW. During this study, LNA topologies are observed and compared. Detailed analysis of circuits is done and simulated results are observed to be matching with the mathematical expressions around 93%. Consequently; design of an LNA with low-voltage and low-power requirements heavily depends on the overall system, which means there is not an optimum design way satisfying all of the specifications. Designer should chose one of the best circuit topology which meets most of the application demands, that is folded cascode topology for our case.

ÖZET

3 TESLA MANYETİK REZONANS GÖRÜNTÜLEYİCİ İÇİN RF ALICI ÖN DEVRESİ

Bu çalışmada 3 Tesla Manyetik Rezonans Görüntüleyici alıcısı için UMC 0.18 μm teknolojisi kullanılarak alıcı ön devresi tasarlanmıştr. Çalısmanın tasarım koşulları çerçevesinde; ki bu koşullar 1.2 V besleme gerilimi, <2 mW güç tüketimi, ve <1 dB gürültü faktörü (NF) olarak özetlenebilir; devrik kaskod yapı en uygun tasarım olarak ön görülmüştür. Tasarlanan devrik kaskod farksal kuvvetlendirici yapıdaki LNA'ler için layout çizimleri yapılmış ve NMOS giriş çiftine sahip devrik kaskod farksal kuvvetlendirici için hazırlanan çizim üretime gönderilmiştir. NMOS giriş çiftine sahip devrik kaskod farksal kuvvetlendirici için; 54 dB gerilim kazancı, 34 dB güç kazancı elde edilmiştir. Şematik benzetimlerde 0.4 dB, layout benzetimlerinde 0.7 dB NF ölçülmüştür. PMOS giriş çiftine sahip devrik kaskod farksal kuvvetlendirici için; 57.5 dB gerilim kazancı, 36.5 dB güç kazancı elde edilmiştir. Şematik benzetimlerde 0.5 dB, layout benzetimlerinde 0.8 dB NF ölçülmüştür. Çalışma süresince, düşük gürültülü kuvvetlendirici yapıları incelenmiş ve karşılaştırılmıştır. Devrelerin detaylı çözümlemeleri ve benzetim sonuçları matematiksel ifadelerle % 93 oranında uyum sağlamıştır. Sonuç olarak; düşük gerilimli düşük güçlü LNA tasarım gereksinimleri ağırlıklı olarak sistemin bütünüyle ilintilidir. Yani en uygun tasarım yöntemi diye bir kavram mevcut değildir. Tasarımcı, tasarım gereksinimlerine en çok uyan devre yapısını seçmelidir; ki bizim için bu devrik kaskod yapısıdır.

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A_v	Voltage Gain
F	Noise Factor
K	Rollett's Stability Factor

LIST OF ACRONYMS/ABBREVIATIONS

$CMFB$	Common Mode Feedback
$CMRR$	Common Mode Rejection Ratio
$FDFCA$	Fully Differential Folded Cascode Amplifier
$FDFC\ LNA$	Fully Differential Folded Cascode Amplifier LNA
FID	Free Induction Decay
GM	Gain Margin
$IIP3$	Third Order Intermodulation Distortion
LNA	Low Noise Amplifier
MRI	Magnetic Resonance Imaging
NF	Noise Figure
NMR	Nuclear Magnetic Resonance
PM	Phase Margin
PSD	Power Spectral Density
RF	Radio Frequency
SNR	Signal to Noise Ratio
UHF	Ultra High Frequency
VHF	Very High Frequency

1. INTRODUCTION

Electronics market demands make analog designers' work harder in each passing day; due to required gain, linearity, noise specifications compared to power and voltage limits. Especially portable devices' power limits also deal with analog and digital circuits on same die.

MRI is an authentic technique which provides good soft tissue contrast in a safe way since it does not use harmful ionization [1]. For an MRI device minimally invasive procedures are required in terms of correct diagnosis and patient health. A low noise amplifier (LNA) with already given specifications for a portable Magnetic Resonance Imaging (MRI) system is aimed to design in thesis. The portable MRI system is optically powered, and catheter is used for MR measurements [2]. Catheter localization is done via a chip which actually determines specifications of this thesis. Since the device is portable and optically powered; supply voltages is limited with 1.2 V; and obtainable minimum noise figure (NF) is required, in order to maximize the signal-to-noise ration of the overall receiver.

However, low-voltage low-power analog design is like a small table cloth with which you try to cover a large dinner table. Result is; always a part of the table will not be covered by the table cloth. So throughout thesis study, subject formed itself to a comparison study between LNAs given in literature ([3]- [5]) to get an optimum point for the given specifications that are listed in Section 7.1.

In Chapter 2 basics of MRI is discussed. Chapter 3 explains theoretic background of the design specifications. Chapters 4, 5 analyze circuit topologies needed to form LNAs. In Chapter 7 detailed analysis of the designed LNAs are done and they are compared in Chapter 8.

In the result of comparison two merits of figure, gain and NF, are determined to be major markers for topology. In terms of gain, folded cascode topology was really

helpful whereas it consumes much power to obtain linearity and proper DC-levels. Basic CMOS topology is a solution for power budget, but it can not reach same amount of gain because of linearity and stability concerns.

An other very important aim is to attain NF objective; which is required to be below 1 dB. A good noise matching is needed to obtain low noise figure [6] and details are explained in Section 3.1.7.1. NMOS input pairs tend to have a better matching compared to PMOS input pairs regarding device sizes for same amount of gain and drain-source voltages. Also UMC 0.18 μm NMOS devices have less intrinsic noise than PMOS devices which are used in this thesis.(See Section 3.1.6)

In the light of the foregoing knowledge, in Section 7.1 four of designed LNAs are observed to reach a design way regarding the given design specifications for the analog designers which is sumarized in conclusion section.

This thesis is a part of TÜBİTAK 1001 project (108E119) and main contributions of the designed LNAs to the project with respect to the already designed LNA published in [2] are increased gain by an amount of 3-6 dB, decreased NF by an amount of 0.2 dB with help of a better matching whilst providing neither advantage nor disadvantage in terms of linearity. The only worsened case is power budget. Two of the designed LNAs, fully differential folded-cascode LNA with NMOS/PMOS input pairs consume 1.44 mA whereas LNA in [2] consumes 1.39 mA.

2. MAGNETIC RESONANCE IMAGING

Magnetic Resonance Imaging (MRI), is an imaging technique, based on Nuclear Magnetic Resonance (NMR), used for monitoring inside of the human body. It is advantageous since it does not use ionizing radiation while monitoring soft tissue. Detailed MRI images help with diagnosis of certain diseases that may not be identified with other body imaging methods. To understand MRI, basics of NMR should be identified clearly.

2.1. Basics of NMR

NMR is based on the movements of nuclei. Since the simplest nuclei are protons, NMR basically works on water which consists of one hydrogen and two oxygen atoms. Human body contains water and tissue proteins a lot which makes it suitable for NMR technique. Throughout this chapter, nuclei are considered to be body tissue.

A nucleus with spin is mostly like a small magnet which has magnetic moment including both magnitude and direction.

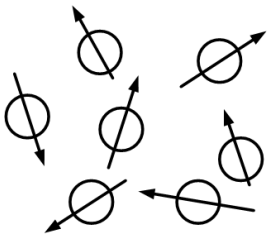


Figure 2.1. Nuclei with Random Spins.

As shown in Figure 2.1 natural behavior of spins is random and total magnetic moment would converge zero. If any magnetic field B_0 is applied to these nuclei, a net magnetic moment will occur even only a fraction of vast number of nuclei magnetized [7].

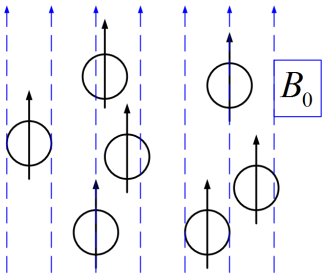


Figure 2.2. Nuclei Under B_0 Magnetic Field.

On the other hand a nucleus would naturally resonate even under static magnetic field. Note that frequency of this resonation depends on the applied magnetic field B_0, which is called Larmor Frequency.

$$\omega_{Larmor} = 2\pi f_{Larmor} = \gamma B_0 \tag{2.1}$$

where γ is called gyromagnetic ratio which is a nuclei specific constant. Larmor frequency at 3-Tesla static magnetic field is calculated to be 127.8 MHz for Hydrogen atoms.

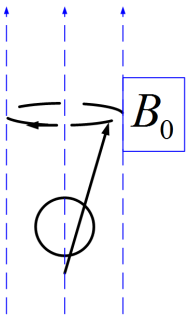


Figure 2.3. Nucleus Resonating with Larmor Frequency under Static B_0 Magnetic Field.

However, in order to have a uniform magnetic wave; the MR device used in this work operates at 3 Tesla Magnetic Field with a frequency of 123 MHz which is the frequency of interest for this thesis.

Due to the applied magnetic field, nuclei have same direction of magnetic moment and same frequency of resonation, but their precession is random. Now, net phase of

the spins converges zero.

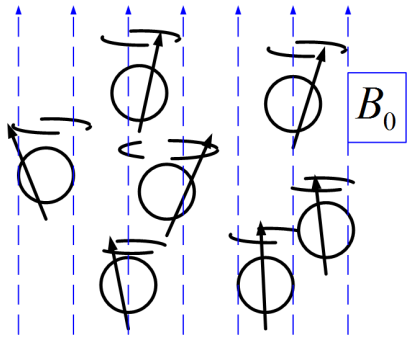


Figure 2.4. Nuclei Resonating with Different Phase.

2.1.1. Free Induction Decay

Let us consider the applied static magnetic field is in Z-direction; so, total magnetic moment becomes M_Z. If an RF pulse ($RF_{\text{pulse}} = B_1 sin(\omega_L t)$) is applied to the nucleus at Larmor Frequency; energy state of each nucleus would change, since at resonance frequency maximum energy is transferred. The major stimulus is; they would precess in the same phase. Generally $B_0 \gg B_1$.

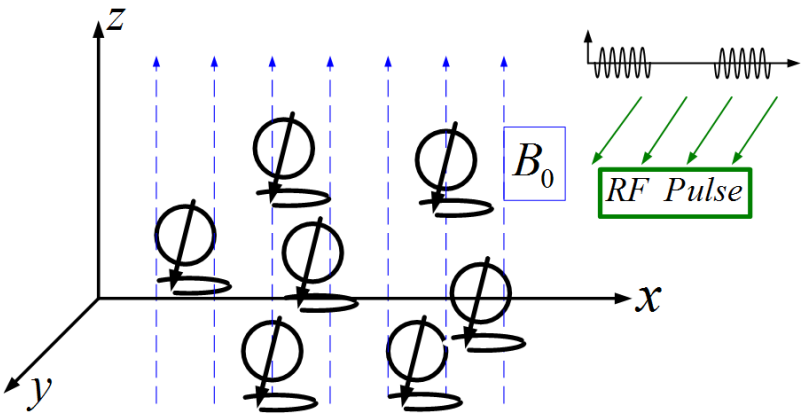


Figure 2.5. Nuclei Phase Behavior Under RF Pulse.

As seen in Figure 2.5, with an applied RF pulse nuclei gain energy, and they flip over -Z direction. The time it takes net phase to be 90° is called T_{90° and the time it takes net phase to be 180° is called T_{180°.

After RF pulse, these nuclei will relax and turn their equilibrium state shown in Figure 2.4, since B_0 still stands. Relaxation signal characteristic is called Free Induction Decay (FID), and it is the main signal that will be observed. Decay time gives information about the tissue.

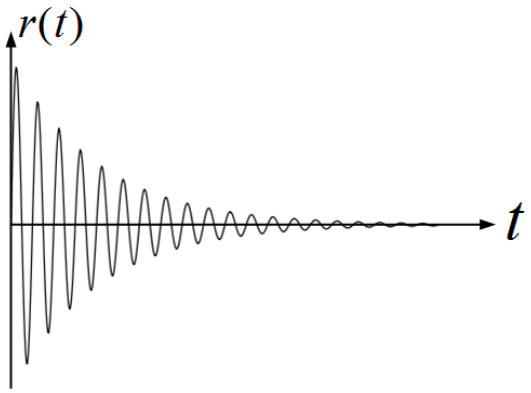


Figure 2.6. FID Signal in t-domain.

If this relaxation flux of nuclei is measure via an antenna, observed signal $v(t)$ heavily depends on the size of the antenna. FID signal which gives characteristic of tissue will be in Larmor Frequency. So, aim of this thesis is to design front-end circuits regarding this basic knowledge of MRI applications. Output frequency of the MRI device determines our operating frequency which is 123 MHz and output signal's amplitude determines our system's input voltage range which is received by roughly 4-6 mm^2 of antenna and is around 50-100 μV.

3. DESIGN SPECIFICATIONS

Today's technology includes both analog and digital signals in many applications. Low voltage, low power analog design is a competitive field of electronics due to shrinking dimensions of devices and supply voltage.

On the other hand, chips that involve both digital and analog circuits may require separate supply voltages, because mostly analog circuits operate with higher supply voltages than digital circuits. Separate supply results in high cost chips.

Lowering supply voltage cause output swing problem; since, threshold voltage does not shrink proportionally with device sizes. Also it is getting harder to form reasonable currents with low supply voltages. that would lead to noisy currents in analog designs.

There are several limitations of low voltage applications. Throughout this chapter basic limitations and sources of these limitations are defined shortly.

3.1. Noise

Noise performance of a circuit determines two limits of the specifications; the lower limit of device sizes and the upper limit of available gain [8].

There are two main noise concepts; inherent noise and interference noise. Interference noise is caused by signal interference in the circuit and may not be random, whereas inherent noise is caused by device and it is random. We are mostly interested in random inherent noise.

3.1.1. Noise in Time Domain

If noise is random, then mean value of the signal is zero in terms of both current and voltage noise. While taking the mean value of a random noise signal, the root mean square value of noise signals is considered.

$$\begin{aligned} V_{n(rms)} &= \sqrt{\frac{1}{T}\int_0^T v_n(t)^2 dt} \\ I_{n(rms)} &= \sqrt{\frac{1}{T}\int_0^T i_n(t)^2 dt} \end{aligned} \tag{3.1}$$

It is obvious that a long T would lead to a more realistic RMS value. RMS value of a noise signal defines its normalized power dissipated on 1 Ω.

$$\begin{aligned} P_{delivered} &= \frac{V_{n(rms)}^2}{1\ \Omega} = V_{n(rms)}^2 \\ P_{delivered} &= I_{n(rms)}^2\ 1\ \Omega = I_{n(rms)}^2 \end{aligned} \tag{3.2}$$

3.1.2. Noise Summation and Correlation Coefficient

If two voltage noise sources assumed to be summed as shown in Figure 3.1;

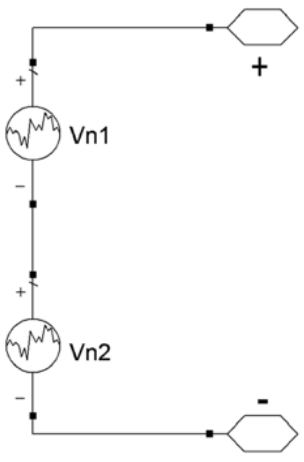


Figure 3.1. Voltage Noise Summation.

then

$$\begin{aligned} v_{nt}(t) &= v_{n1}(t) + v_{n2}(t) \\ V_{nt,rms}^2 &= \frac{1}{T}\int_0^T \big(v_{n1}(t) + v_{n2}(t)\big)^2 dt \\ V_{nt,rms}^2 &= V_{n1,rms}^2 + V_{n2,rms}^2 + \frac{2}{T}\int_0^T \big(v_{n1}(t) + v_{n2}(t)\big) dt. \end{aligned}$$

Correlation coefficient is defined as in Equation 3.3.

$$\begin{aligned} C &= \frac{\frac{1}{T}\int_0^T \big(v_{n1}(t) + v_{n2}(t)\big) dt}{V_{n1,rms} \ . \ V_{n2,rms}} \\ V_{nt,rms}^2 &= V_{n1,rms}^2 + V_{n2,rms}^2 + 2C \ V_{n1,rms} \ . \ V_{n2,rms} \end{aligned} \tag{3.3}$$

It is obvious that $-1 \leq C \leq 1$. If $C = \pm 1$ signals are said to be fully correlated; whilst if $C = 0$, signals are said to be uncorrelated.

3.1.3. Signal to Noise Ratio (SNR)

Signal to noise ratio (SNR) is a parameter to measure how much signal is corrupted by noise. It is apparent that SNR value is required to be higher than 1.

$$\begin{aligned} SNR &= \frac{P_{signal}}{P_{noise}} \\ SNR_{dB} &= 10 \ \log\Big(\frac{P_{signal}}{P_{noise}}\Big) \\ SNR_{dB} &= 10 \ \log\Big(\frac{V_{signal,rms}^2}{V_{noise,rms}^2}\Big) \\ SNR_{dB} &= 20 \ \log\Big(\frac{V_{signal,rms}}{V_{noise,rms}}\Big) \end{aligned} \tag{3.4}$$

Using SNR values, a term called noise factor (F) is defined.

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{3.5}$$

Another term called noise figure (NF) is defined as in Equation 3.6. NF determines how much noise is added to the signal in the circuit. Note that SNR_{out} would be smaller than SNR_{in}.

$$NF = 10 \ \log\left(\frac{SNR_{in}}{SNR_{out}}\right) = SNR_{in,dB} - SNR_{out,dB} \tag{3.6}$$

3.1.3.1. Noise Factor in Multistage Amplifiers. Understanding multistage amplifier's noise factor behavior is important, since first stage of an overall system is designed in this thesis. Let G_1 and G_2 be the power gain of the staged of the two stage amplifier as shown in Figure 3.2. P_{n1} and P_{n2} are the noise powers added in amplifiers [9].

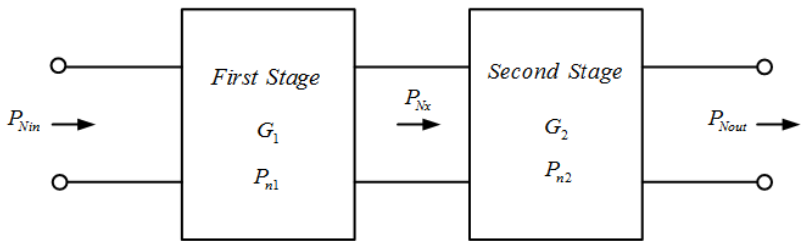


Figure 3.2. Noise Factor of a Two Stage Amplifier.

$$\begin{aligned} P_{Nx} &= G_1 P_{Nin} + P_{n1} \\ P_{Nout} &= G_2 P_{Nx} + P_{n2} \\ P_{Nout} &= G_2 G_1 P_{Nin} + G_2 P_{n1} + P_{n2} \end{aligned} \tag{3.7}$$

$$\begin{aligned} F &= \frac{P_{Sin}/P_{Nin}}{P_{Sout}/P_{Nout}} \\ F &= \frac{P_{Sin}/P_{Nin}}{(G_1 G_2 P_{Sin})/P_{Nout}} \\ F &= \frac{P_{Nout}}{G_1 G_2 P_{Nin}} = 1 + \frac{P_{n1}}{P_{Nin} G_1} + \frac{P_{n2}}{P_{Nin} G_1 G_2} \\ F &= F_1 + \frac{F_2 - 1}{G_1} \end{aligned} \tag{3.8}$$

F_1 and F_2 are the noise factors of first stage and second stage respectively. If the result is generalized,

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_3 - 1}{G_1 G_2 G_3} \dots \ . \tag{3.9}$$

It is apparent that noise factor of the first stage (receiver stage of MRI system) contributes to the system effectively.

3.1.4. Noise in Frequency Domain

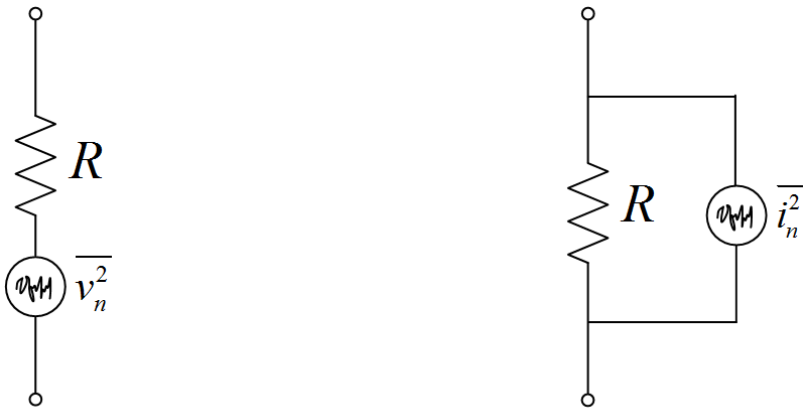
The two terms, power spectral density and normalized noise power, should be known to understand frequency analysis of noise. Power spectral density is the power of the noise signal over a 1 Hz bandwidth; its unit is V^2/Hz. Normalized noise power is the mean squared value over a 1 Hz bandwidth; its unit is $V/\sqrt{Hz}$.

3.1.5. Noise Sources of MOSFET

3.1.5.1. Thermal Noise. If a noise signal has a constant spectral density all over the frequency band, then this signal is said to be white noise.

$$V_n(f) = V_n$$

Thermal noise is generated by random electronic motion related to the temperature of the room. It is a white noise, since it is dependent on temperature and independent of frequency. Thermal noise is modeled by a noisy resistor. Equivalent circuits are shown in Figure 3.3.



(a) Voltage Source Thermal Noise Model. (b) Current Source Thermal Noise Model.

Figure 3.3. Thermal Noise Models

Power spectral density of thermal noise is $[W^2]$

$$P_{th} = kT\Delta f \tag{3.10}$$

where k is the Boltzman Constant $[1.38 \times 10^{-23}\text{J/K}]$, T is temperature in Kelvin and Δf is the bandwidth of the signal in Hz.

$$\begin{aligned} P_{th} &= kT\Delta f = \frac{V_n^2}{4R} \\ \overline{V_n^2} &= 4kTR\Delta f \ [\text{V}^2] && (3.11) \\ \overline{i_n^2} &= 4kT\frac{1}{R}\Delta f \ [\text{A}^2] && (3.12) \end{aligned}$$

Thermal noise on a 1 kΩ resistor at room temperature is 4 nV/$\sqrt{\text{Hz}}$. MOSFET drain current leads to thermal noise due to drain-source channel resistance. Thermal noise of MOSFET's channel is given by the Equation 3.13.

$$\overline{i_{nd_{th}}^2} = 4kT\gamma g_{ds}\Delta f \ [\text{A}^2] \tag{3.13}$$

where g_{ds} is drain-source conductance [$\mho$] and γ is a coefficient whose value depends on basic device parameters and bias conditions. In long devices $0.67 \leq \gamma \leq 1$, whereas in short channel devices γ can even rise up to 2-3. Due to higher electric field in short channel devices, carriers cause more heating and as well thermal noise [$\sqrt{\text{V}}$].

Thermal noise on channel, capacitively couples itself to gate terminal of the device which is negligible at low frequencies but can be important at RF frequencies. Since Larmor Frequency of 3-Tesla MRI system is in ultra high frequency (UHF) band as explained in Chapter 2; this noise source is effective. So; thermal noise of channel and gate are correlated. Note that thermal noise in gate is frequency dependent.

$$\begin{aligned} \overline{i^2_{ng_{th}}} &= 4kT\delta g_g \, \Delta f \\ g_g &= \frac{\omega^2 C^2_{gs}}{5 g_{ds}} \end{aligned} \tag{3.14}$$

where δ is gate noise coefficient.

3.1.5.2. Shot Noise. Shot noise is generated by electric charge packets flowing through the channel; which means it is directly proportional to the biasing of the device and independent of frequency.

$$\overline{i^2_{nd_s}} = 2qI_{DC}\Delta f \tag{3.15}$$

where q electronic charge [C].

Shot noise of a device biased at 1 mA is approximately 18 pA/$\sqrt{\text{Hz}}$.

3.1.5.3. Flicker Noise (1/f Noise). Main source of 1/f noise cannot be described exactly; but it is generally assumed that flicker noise is cause by traps associated with contamination and crystal defects. These traps capture and release the carriers randomly; so this noise exits in all active devices.

Main idea is spectral density of this noise degrades with rising frequency. Mathematical derivations are done empirically for flicker noise [8].

3.1.6. MOSFET Noise Modeling

As already explained MOSFET has three main noise sources. But major noise sources that dominate are thermal noise and flicker noise.

Thermal noise of a MOSFET is

$$\overline{i_{nd_{th}}^2} = 4kT\gamma g_{ds}\Delta f.$$

However if MOSFET operates in active region the channel is not homogenous so thermal noise source becomes

$$\overline{i_{nd_{th}}^2} = 4kT\frac{2}{3}g_m\Delta f. \tag{3.16}$$

For easy calculation, Thévenin equivalent of thermal noise source at gate of the device can be obtained.

$$\overline{V_{nd_{th}}^2} = 4kT\frac{2}{3}\frac{1}{g_m}\Delta f \tag{3.17}$$

On the other hand, gate thermal noise should be taken into account which couples itself through C_{gs}. Its current noise source formula is given in Equation 3.14. If Thévenin equivalent is taken, then

$$\overline{v_{ng_{th}}^2} = \frac{4kT\delta\Delta f}{g_g}. \tag{3.18}$$

So total thermal noise becomes

$$\overline{V_{Mosfet_{th}}^2} = 4kT\frac{2}{3}\frac{1}{g_m}\Delta f + \frac{4kT\delta\Delta f}{g_g}. \tag{3.19}$$

Flicker noise of mosfet is modeled as a voltage source at gate of the device; and given for MOSFET as in Equation 3.20.

$$\overline{v^2_{Mosfet_f}} = \frac{K}{WLC^2_{ox}f} \tag{3.20}$$

where K is a technology dependent constant, W is the device width, L is the device length and C_{ox} is the gate capacitance per unit area.

It is obvious that large devices tend to have less flicker noise. Total noise at gate terminal is calculated to be

$$\overline{V^2_{Mosfet}} = \frac{K}{WLC^2_{ox}f} + 4kT\frac{2}{3}\frac{1}{g_m}\Delta f + \frac{4kT\delta\Delta f}{g_g}. \tag{3.21}$$

$\overline{V^2_{Mosfet}}$ is called input-referred noise of MOSFET.

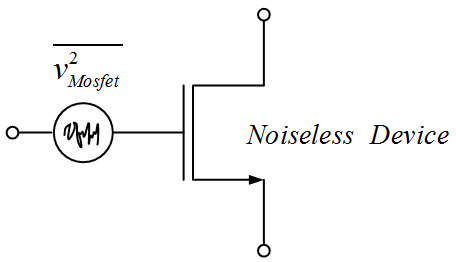


Figure 3.4. Noise Model of Mosfet.

Regarding the definitions of noise sources of a MOSFET, a noise figure characteristic as seen Figure 3.5 is expected.

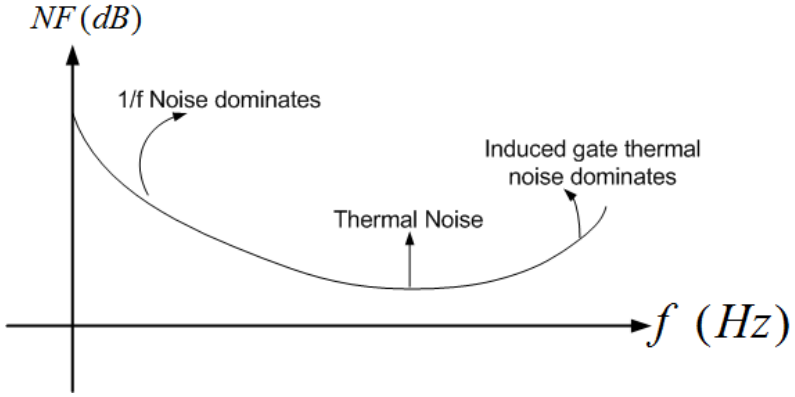


Figure 3.5. Noise Figure of MOSFET vs. Frequency.

But when simulations are done to determine UMC 0.18 μm MOSFET noise characteristics of both PMOS and NMOS, Figure 3.6 is obtained.

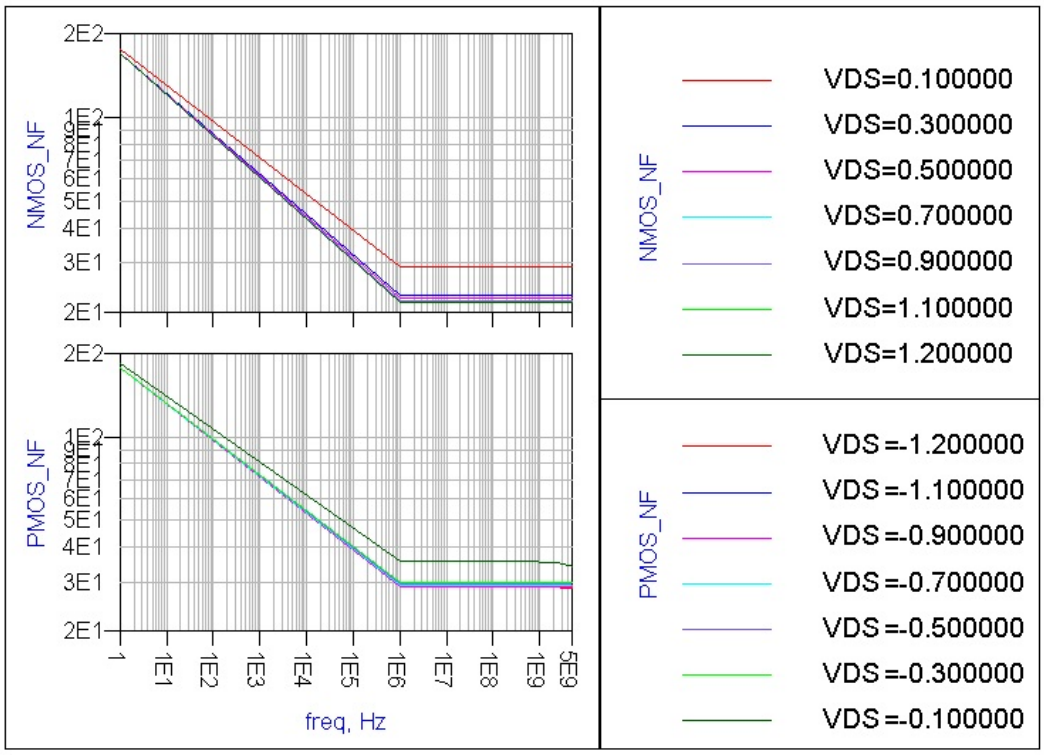


Figure 3.6. Noise Figure Simulation of UMC 0.18 μm MOSFETs.

It is obvious from simulation output that, transistors that will be used for LNA design do not suffer from induced gate thermal noise. There is another result that 1/f noise is dead at 123 MHz (corner frequency of 1/f noise is 1 MHz). So during this design, following noise model of MOSFET in Equation 3.22 is used.

$$\overline{V_{Mosfet}^2} = 4kT\frac{2}{3}\frac{1}{g_m}\Delta f \tag{3.22}$$

Also note that higher biasing voltage lowers noise figure. There is not an optimum biasing point for a minimum noise figure.

3.1.7. Noise Matching

An amplifier is a two-port network; and noise figure of a two-port network is [9]

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{s,opt}|^2 \tag{3.23}$$

where F_{min} is intrinsic minimum noise factor of the network, R_n is noise resistance, Y_s is source admittance, $Y_{s,opt}$ is source admittance that provides minimum noise factor and G_s= $Re\{Y_S\}$.

For a minimum noise figure $Y_{s,opt}$ should be obtained. This is generally done via a passive matching network as it is called *Noise Matching*.

MOSFET noise figure effectively depends on its biasing, since channel resistance and other AC characteristics are determined by biasing. To get F_{min}, NF should be simulated versus drain current V_{DS} and V_{GS}. As already explained larger bias voltages result in lower NF for our MOSFETs.

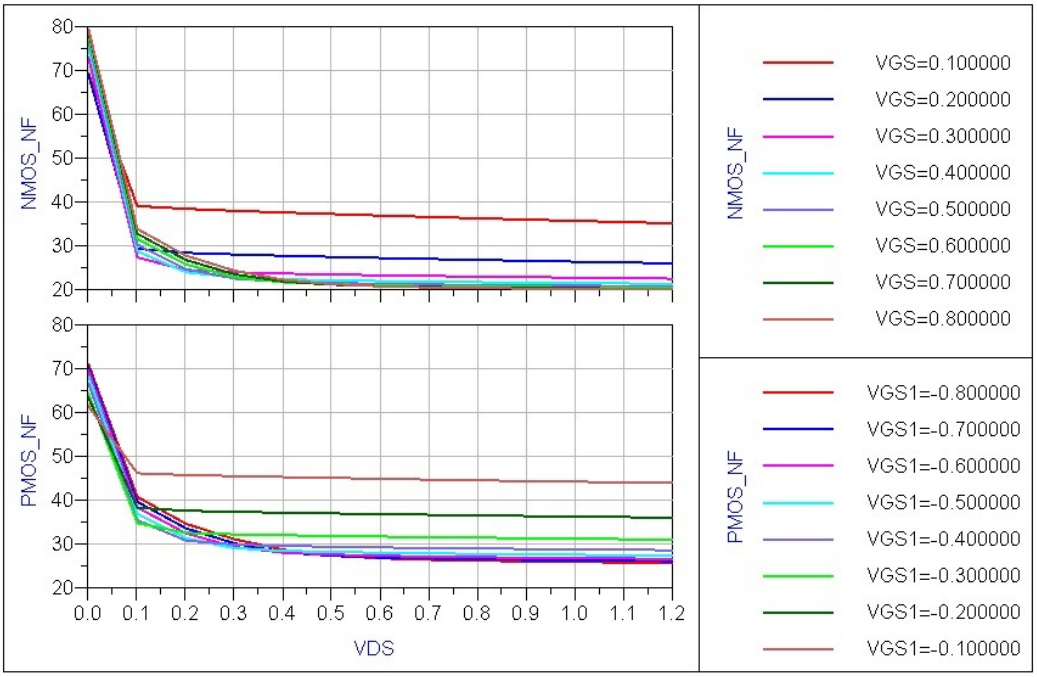


Figure 3.7. MOSFET NF Simulation of Bias Point.

3.1.7.1. Noise Matching Network. Designed LNA is connected to an antenna and it is basically an inductor which is 282 nH with an intrinsic resistance of 5 Ω. Quality factor (Q) of this inductor at 123 MHz is

$$Q = \frac{\omega_L L}{R} \tag{3.24}$$
$$Q \simeq 43.6.$$

Let us assume a designed LNA seen in Figure 3.8. Z_1 is the output impedance of matching network whereas Z_2 is the input impedance of LNA.

Inductors and capacitors are assumed to be noiseless. It is obvious that antenna's intrinsic resistance R_L would have a thermal noise of $\overline{v_n^2}$ which have a power spectral density of $\overline{v_n^2}/\Delta f$. Now there is the power of signal and thermal noise power at the input of the matching network

$$P_t = P_s + P_n.$$

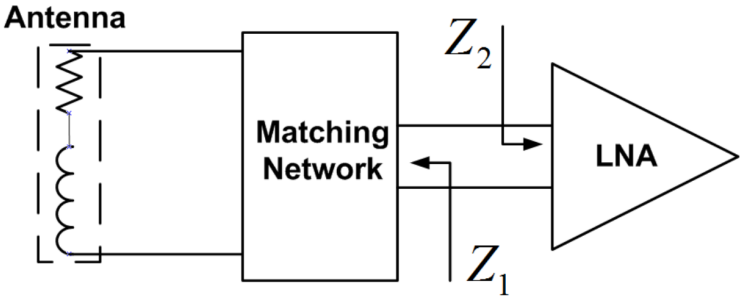


Figure 3.8. Block Diagram of Matching Network Connected to LNA.

Since passive network will be designed via passive elements it would have a transfer function

$$H(\omega) = A\angle\theta^{\circ}.$$

The signal at the input of the matching network will be amplified by a factor of A.

$$P_{MN_{output}} = (A.V_s)^2 + (A.V_n)^2 \tag{3.25}$$

$(A.V_n)^2$ will be added to the power spectral density of the input-referred noise of LNA. If amplification is high enough, SNR system's output would not be affected by LNA that much.

Now system's NF is defined such as in Equation 3.26.

$$NF = 10\ \log\left(\frac{A^2\overline{V^2_{matching-network}} + \overline{V^2_{in-LNA}}}{A^2\overline{V^2_{matching-network}}}\right) \tag{3.26}$$

For passive network just a capacitor is used such that it would also resonate with the inductor at 123 MHz which is the frequency of interest.

It is also known that maximum available gain occurs in an RLC circuit when resonance occurs [6],

$$A = \frac{1}{\sqrt{(1-\omega_L RCQ)^2(\omega_L RC)^2}} \tag{3.27}$$

$$A_{max} \simeq Q \tag{3.28}$$

when

$$\begin{aligned} \frac{1}{j\omega C} &= j\omega L \\ \omega &= \frac{1}{\sqrt{LC}} \\ L &= 282x10^{-9}, \ \frac{\omega}{2\pi} = 123 \times 10^6 \text{ Hz} \\ C &\simeq 5.9 \text{ pF}. \end{aligned} \tag{3.29}$$

On the other hand, this passive network will be connected to LNA input. To obtain available gain of passive network; Z_2 which is defined as LNA input impedance should be infinity. So for a good noise matching; there is a second requirement such that $Z_2 = \infty$ (See Appendix A).

All designed differential amplifiers' input MOSFETs are in common source configuration (Section 7.1) which means they have a pure capacitive input. Capacitive input helps to obtain infinite input resistance.

Designed LNAs' input-referred noise sources are all defined and detailed NF analysis is done in Section 7.1. But final matching network is seen in Figure 3.9 where C_1 is resonating capacitor, C_2 and C_3 are DC-block capacitors.

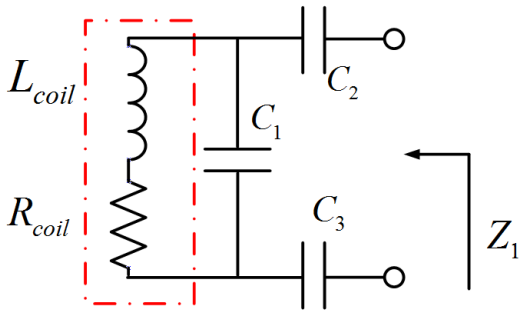


Figure 3.9. Noise Matching Circuit.

3.2. S-Parameters

Systems can be identified via various parameters regarding system properties such as z-parameters, y-parameters and h-parameters. Scattering parameters (S-parameters) is one way to define input-output characteristics of a two-port system at high frequencies. Let us define a two port system as shown in Figure 3.10;

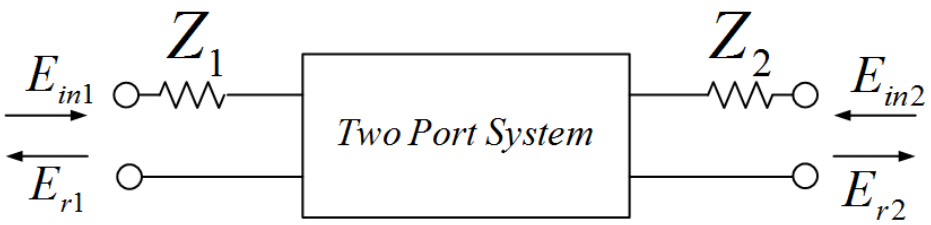


Figure 3.10. Two Port System at High Frequencies.

Inputs and outputs are defined in terms of incident and reflected voltage waves [10]. S-parameters are defined as;

$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{3.30}$$

where

$$\begin{aligned} a_1 &= E_{in1}/\sqrt{Z_1} \\ a_2 &= E_{in2}/\sqrt{Z_2} \\ b_1 &= E_{r1}/\sqrt{Z_1} \\ b_2 &= E_{r2}/\sqrt{Z_2}. \end{aligned} \tag{3.31}$$

So

$$\begin{aligned} S_{11} &= \frac{b_1}{a_1}\Big|_{Z_2=0} \\ S_{21} &= \frac{b_2}{a_1}\Big|_{Z_2=0} \\ S_{12} &= \frac{b_1}{a_2}\Big|_{Z_1=0} \\ S_{22} &= \frac{b_2}{a_2}\Big|_{Z_1=0} \end{aligned} \tag{3.32}$$

where s_{11} is the voltage reflection coefficient of port 1, s_{12} is the reverse voltage gain, s_{21} is the forward voltage gain and s_{22} is the voltage reflection coefficient of port 2. S-parameters are important in terms of determining major system specification such as gain and stability.

3.3. Stability

Designing RF amplifier requires great attention on stability. The most effective way to see if a circuit would oscillate or not; is to calculate its Rollett's Stability factor which is known as K, stability factor [9].

$$\mathrm{K} = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.33}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{3.34}$$

A two-port system is said to be unconditionally stable if K$\geq$ 1 and $S_{11}, S_{22} < 1$. Stability factor also helps us to calculate maximum available gain which is

$$G_{MAX} = \frac{S_{21}}{S_{12}}(K - \sqrt{K^2 - 1}). \tag{3.35}$$

It is obvious that if K$<$ 1, than maximum available gain becomes infinity. Also K$=$ 1 states maximum available gain which is

$$G_{MAX} = \frac{S_{21}}{S_{12}}. \tag{3.36}$$

3.4. 1-dB Compression Point

1-dB compression point is a metric used for extracting linearity of an electronic system which depends on the input range of the system/device. Increasing input would eventually cause system to go in saturation in terms of gain. The input power which causes a 1 dB gain loss is called 1-dB Compression Point [9], shown in Figure 3.11.

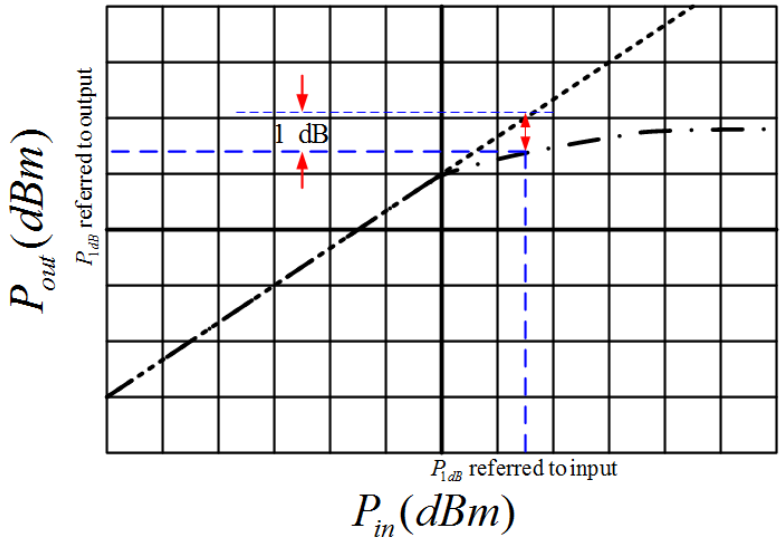


Figure 3.11. 1-dB Compression Point of a Non-linear Amplifier.

3.5. Intermodulation Distortion

Intermodulation distortion is a way to measure linearity of a system/device under two inputs of different frequencies. In order to make this analysis two inputs with different frequencies are applied to the input; and outputs of 3rd, 5th and 7th order products of these inputs are measured.

Let us describe a non-linear circuit's transfer function in Taylor series expansion

$$f(x) = a_0 + a_1x(t) + a_2x^2(t) + a_3x^3(t) + a_4x^4(t) + \dots \ . \tag{3.37}$$

If we define a term as the ratio of the third order product to the carrier signal as IM3; and then imply two inputs as

$$x(t) = Usin(\omega_1 t) + Usin(\omega_2 t). \tag{3.38}$$

$$IM3 = \frac{4}{3} \left| \frac{a_3}{a_1} \right| U^2 \tag{3.39}$$

It is obvious that with an increasing input, IM3 will increase much faster than the fundamental signal. The amplitude where IM3 equals to 1 is called input referred third order intermodulation intercept point (IIP3).

$$IIP3 = \sqrt{\frac{3}{4} \left| \frac{a_1}{a_3} \right|} \tag{3.40}$$

For each 1 dB increase in the input power, the third order products will increase 3 dB. IP3 is a figure of merit that determines the circuit's tolerance to multi inputs outside the desired band. It is also a good way to measure the linearity of the device. The input power up to IIP3 will give us the input range where the device acts more linear.

4. CURRENT MIRRORS

Current mirrors are major building blocks in analog design. Depending on the output current direction they can be used as current sources or current sinks. An ideal current source is defined as; a component which supplies constant amount of current regardless the voltage drop between its terminals. This definition connotes infinite output impedance as seen in Figure 4.1;

Figure 4.1. Ideal Current Source Output Characteristic.

While designing a current mirror, to obtain high output impedance is one of the major specifications. Secondly, in order to get large output swing, low output voltage is required. Throughout this chapter, circuits supplying these demands are investigated.

4.1. Basic Current Mirror

Basic current mirror topology is seen in Figure 4.2.

$$\begin{aligned} V_{GS1} &= V_{DS1} \\ V_{DS1} &> V_{GS1} - V_{th1} \end{aligned}$$

It is seen that M_1 always operates in active region. M_1 structure is also called *diode connected transistor*.

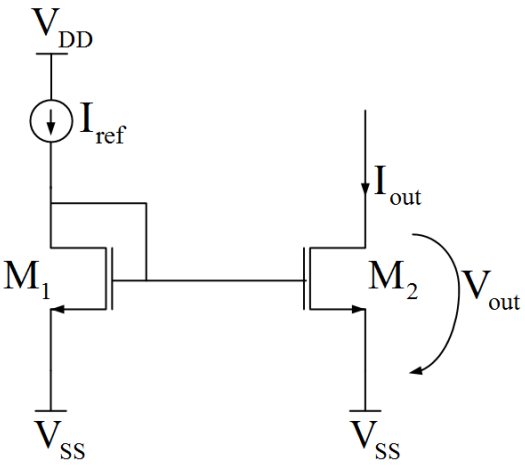


Figure 4.2. Basic Current Mirror Topology.

Assuming M_2 operating in saturation and transistors M_1 and M_2 are matched, then

$$\begin{aligned} I_{D1} &= \frac{1}{2}\frac{W}{L}\mu_n C_{ox}(V_{GS1} - V_{th})^2 \\ I_{D2} &= \frac{1}{2}\frac{W}{L}\mu_n C_{ox}(V_{GS2} - V_{th})^2 \\ I_{D1} &= \frac{(W/L)_1}{(W/L)_2}. \end{aligned} \tag{4.1}$$

Main idea is V_{GS1} copied to V_{GS2} and if transistors are matched $I_{D1} = I_{D2}$ is obtained. On the other hand; if finite output resistance is taken into account, the transistor with larger V_{DS} would have larger drain current. In other words, a mismatch would cause unequal drain currents that would result in different V_{DS} values.

Output resistance of this current mirror simply equals to r_{ds2}. So, keeping M_2 in saturation also enlarges the output impedance. Output voltage becomes; $V_{out} = V_{DS2}$. Basic current mirror structure is good in terms of low output voltage, but it has a major disadvantage of low output impedance.

Output characteristic of a basic current mirror is seen in Figure 4.3. Simulated basic current mirror has a supply voltage of 1.2 V and $W/L_1 = W/L_2$. 0.1 mA reference current is mirrored to the output.

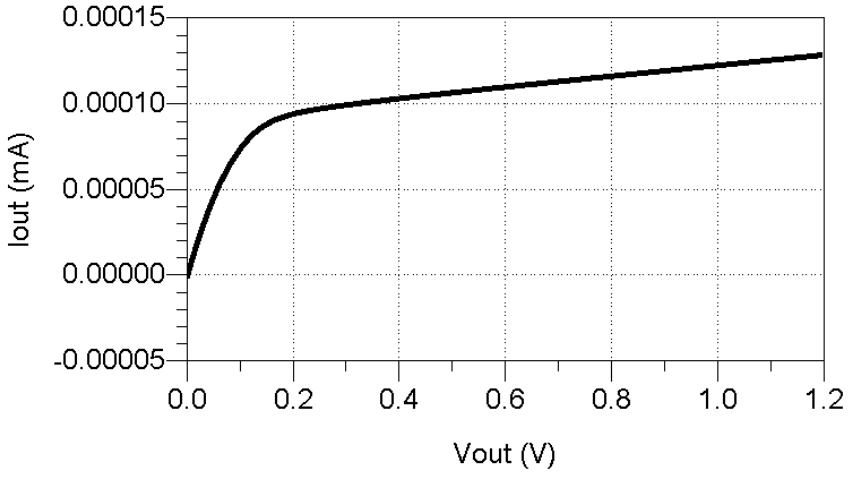


Figure 4.3. Basic Current Mirror Output Characteristic.

4.2. Cascode Current Mirror

Cascode current mirror seen in Figure 4.4 is designed to have high output resistance [11].

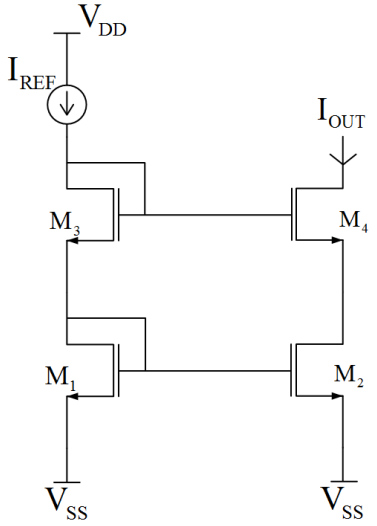


Figure 4.4. Cascode Current Mirror Topology.

$$r_{out} = r_{ds4}[1 + r_{ds2}(g_{m4} + g_{ds4})] \simeq r_{ds4} r_{ds2} g_{m4} \tag{4.2}$$

$$V_{out} = 2V_{DS} + V_{th} \tag{4.3}$$

Output characteristic of a cascode current mirror is seen in Figure 4.5.

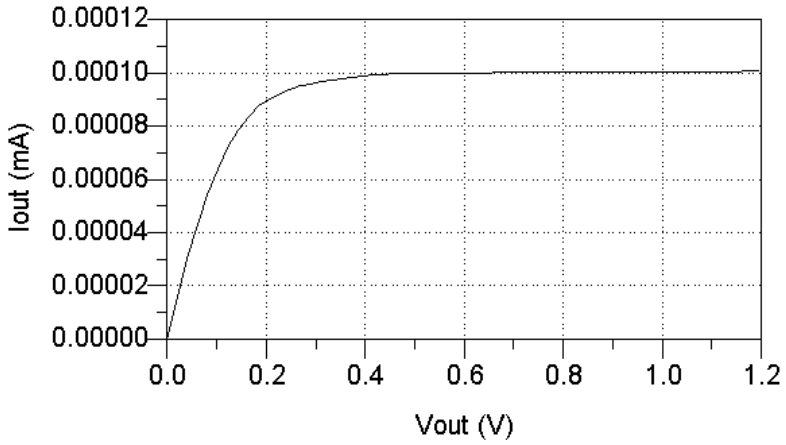


Figure 4.5. Output Characteristic of Cascode Current Mirror.

0.1 mA reference current is mirrored to the output with unity gain which means $W/L_1 = W/L_2 = W/L_3 = W/L_4$. Supply voltage is chosen to be 1.2 V.

High output impedance of cascode current mirror results in high gain in many stages. But cascode current mirrors suffer from low output swing due to their high output voltage requirement; such that they are not feasible in low voltage applications. Threshold term of output voltage cause a significant loss in voltage swing when current mirror is used as an active load. Also if there is body effect in the circuit, threshold voltage may even get higher.

It is apparent that output voltage should be made smaller while keeping the output impedance high. One way to obtain this circuit requirement is to do level shifting such as in Figure 4.6.

The circuit seen in Figure 4.7 is designed to perform the level shifting. Transistor M_6 does level shifting since it is a source follower. Disadvantage of this configuration is the extra current that will be used in the level shifter branch.

$$r_{out} \simeq r_{ds4} r_{ds2} g_{m4} \tag{4.4}$$

$$V_{out} = 2V_{DS} \tag{4.5}$$

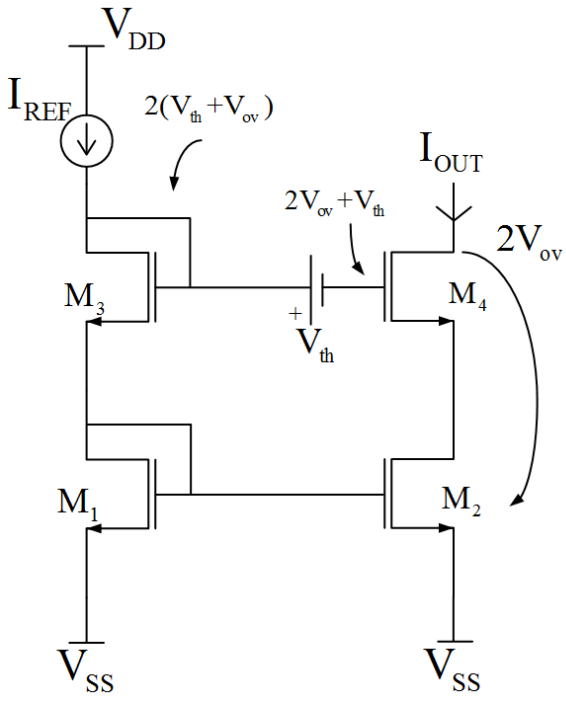


Figure 4.6. Level Shifting Method for Cascode Current Mirror.

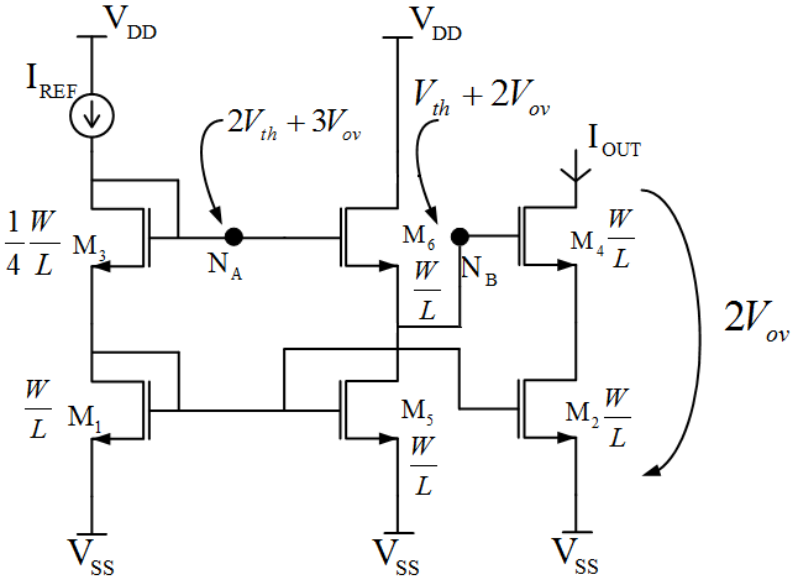


Figure 4.7. Level Shifting with Source Follower.

For a good level shifting device sizes gain importance. In Figure 4.7 M_3 has different sizing than other transistors. Making its device size $W/4L$ doubles its V_{DS}. In other words; if its sizing would be same with the others, M_1 would have no drain-source voltage, such that it would not operate in active region; and high output impedance could not be obtained. Note that, in this analysis body effect is not considered. When body effect considered, sizing of M_3 should even be smaller to obtain higher overdrive voltage [11].

A level-shifted cascode current mirror is simulated with a supply voltage of 1.2 V. Device sizes are chosen to be equal whereas M_3 is chosen to be $W/4L$, as explained above. 0.1 mA input current is mirrored to the output.

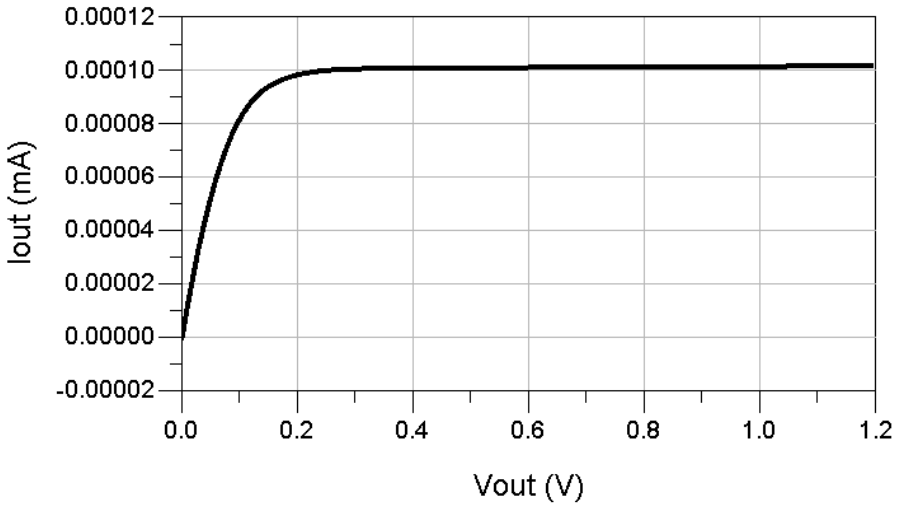


Figure 4.8. Output Characteristic of Level-Shifted Cascode Current Mirror.

5. AMPLIFIER TOPOLOGIES USED in LNA DESIGNS

Two basic topologies, differential pair topology and folded cascode topology are used in designs. In this section these topologies are examined.

5.1. Differential Pair

Basic differential amplifier consists of two matched transistors M_1 and M_2, two matched loads $R_{D1} = R_{D2} = R_D$, and a current source I_{bias}.

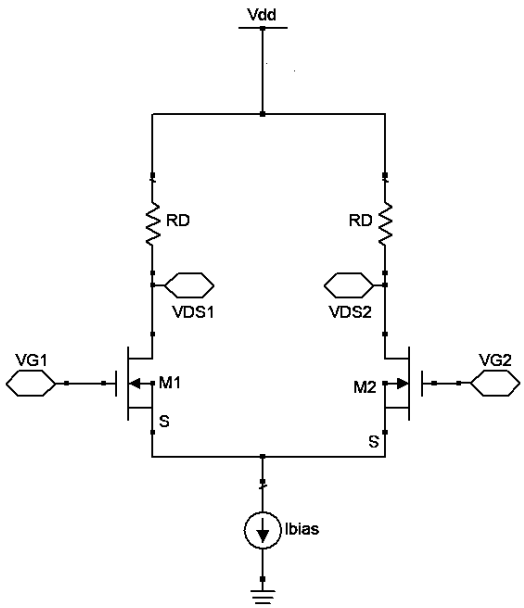


Figure 5.1. Basic Differential Amplifier Configuration.

If a perfect match is assumed between M_1-M_2, R_{D1}-R_{D2} and a common-voltage is applied to the gates of M_1 and M_2, then

$$\begin{aligned} V_{GS1} &= V_{GS2} = V_{cm} \\ V_{id} &= V_{GS1} - V_{GS2} = 0 \\ I_{D1} &= I_{D2} = \frac{I_{bias}}{2} \\ V_{DS1} &= V_{DS2} \qquad (5.1) \\ V_{od} &= V_{DS1} - V_{DS2} = 0. \qquad (5.2) \end{aligned}$$

It is obvious that differential pair suppresses common mode signals. On the other hand; if a differential mode signal is applied to the amplifier it will be seen that a differential output can be obtained.

$$\begin{aligned} V_{GS1} &= V_{id}, V_{GS2} = 0 \\ I_{D1} &= I_{bias}, I_{D2} = 0 \\ V_{D2} &= 0 \\ V_{od} &= V_{D1} - V_{D2} = V_{D1} \end{aligned} \tag{5.3}$$

If body effect is not considered, then drain currents are defined as [12];

$$\begin{aligned} i_{D1} &= \frac{I_{bias}}{2} + \frac{I_{bias}}{V_{ov}} . \frac{v_{id}}{2} \sqrt{1 - \left(\frac{v_{id}/2}{V_{ov}}\right)^2} \\ i_{D2} &= \frac{I_{bias}}{2} - \frac{I_{bias}}{V_{ov}} . \frac{v_{id}}{2} \sqrt{1 - \left(\frac{v_{id}/2}{V_{ov}}\right)^2} . \end{aligned} \tag{5.4}$$

Note that $i_{D1} + i_{D2} = I_{bias}$.

5.1.1. Differential Gain and Common Mode Rejection Ration (CMRR)

If differential input is applied, and output is taken from one drain $V_{out} = V_{DS1}$ or $V_{out} = V_{DS2}$ it is called a single-ended differential pair; whereas if output is taken from both drains $V_{out} = V_{DS1} - V_{DS2}$ or $V_{out} = V_{DS2} - V_{DS1}$ then it is called a fully-differential pair. Voltage gain of these topologies are defined as [12];

$$A_{single-ended} = -\frac{1}{2} g_{m1} R_{Deq} \tag{5.5}$$

$$A_{fully-\text{differential}} = -g_{m1} R_{Deq} \tag{5.6}$$

where R_{Deq} is the equivalent resistance seen at drains of the transistors.

Another important metric of differential amplifiers is common mode rejection ratio (CMRR) which helps to determine how good common mode signals are rejected. Mathematically CMRR is defined as the ratio of differential mode and common-mode gain.

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right|$$

A_{cm} is defined as

$$A_{cm} = \frac{R_D}{2R_{ss}}.$$

where R_{ss} is the output resistance of the current source. Due to parallelity of sources of M_1 and M_2; its effect on one half circuit is $2R_{ss}$. In differential-mode operation drain currents are complementary; which means no differential signal passes through R_{ss}. As a result R_{ss} has no effect on differential gain. In other words; the node where source terminals are connected is called *virtual ground*.

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right| = g_{m1}R_{ss} \tag{5.7}$$

If a perfect match is assumed and output is taken differentially; then, CMRR=∞. If there exists a mismatch between drain resistors,

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right| = 2g_{m1}R_{ss} \Big/ \frac{\Delta R_D}{R_D}. \tag{5.8}$$

If there exists a mismatch between input transistors,

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right| = 2g_{m1}R_{ss} \Big/ \frac{\Delta g_m}{g_m}. \tag{5.9}$$

5.1.2. Differential Pair with Active Loads

Drain resistances has negative effects on differential pair in terms of chip area and DC voltage limit. To overcome these problems active loads are used. If PMOS active loads are used with NMOS input pairs or vice versa, then the structure is said to be a *CMOS differential pair*.

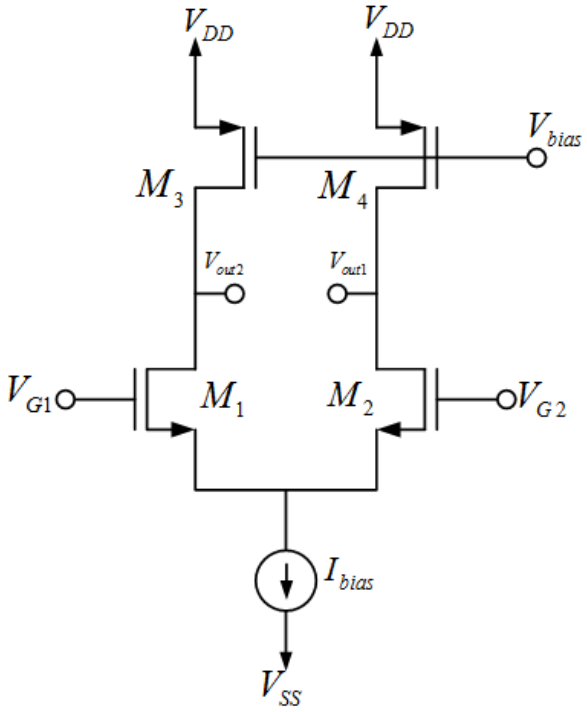


Figure 5.2. CMOS Differential Amplifier with Active Load.

Gain formula given in Equation 5.6 remains same. Now equivalent drain resistance should be determined. Since the node where sources of M_1 and M_2 is said to be virtual ground; there exists parallel resistances between drains and ground.

$$\begin{aligned} R_{Deq} &= r_{out1}//r_{out3} = r_{out2}//r_{out4} \\ A_{\text{fully-differential}} &= -g_{m1}(r_{out2}//r_{out4}) \end{aligned} \tag{5.10}$$

In terms of common-mode gain $R_{Deq} \neq r_{out2}//r_{out4}$, because R_{ss} comes into account as already explained.

$$A_{cm} = -\frac{1}{2g_{m1}R_{ss}} \tag{5.11}$$

$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right| = [g_{m1}r_{out1}//r_{out3}][2g_{m3}R_{ss}] \tag{5.12}$$

5.1.3. Frequency Analysis of CMOS Differential Amplifier

Since designs are done with active loads, frequency analysis of differential amplifier with active load is investigated. Since we consider differential response of the pair; in Figure 5.3, high frequency equivalent model of half circuit is seen in differential mode.

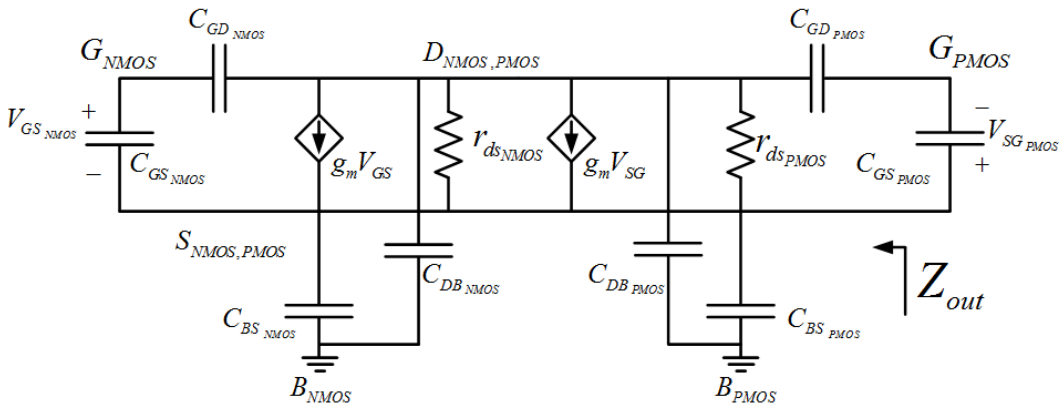


Figure 5.3. High Frequency Equivalent Model for Half Circuit of the Differential Pair.

$$Z_{out} = (r_{ds_{NMOS}}//r_{ds_{PMOS}}) + j\omega C_{eq} \tag{5.13}$$

$$C_{eq} = C_{gd2} + C_{bd2} + C_{bs2} + C_{gd4} + C_{bd4} + C_{bs4} \tag{5.14}$$

If the circuit is loaded by another capacitance C_L

$$C_{L_{total}} = C_{eq} + C_L. \tag{5.15}$$

Transfer function of the pair is now defined as

$$A_{fully-\text{differential}} = (-g_{m1}R_{out})\Big(\frac{1}{1+sC_LR_{out}}\Big)\Big(\frac{1-s\frac{C_{eq}}{2g_{m4}}}{1+s\frac{C_{eq}}{g_{m4}}}\Big). \tag{5.16}$$

Dominant pole of the circuit becomes

$$f_{cut-off,lf} = \frac{1}{2\pi C_{L_{total}}R_{out}}. \tag{5.17}$$

The frequency at which gain becomes unity is defined in Equation 5.18 [8]. Unity gain frequency is important in terms of determining stability as will be explained in Section 6.1.

$$f_{unity} = A_{\text{fully}-\text{differential}}.f_{cut-off,lf} \tag{5.18}$$

5.2. Cascode Gain Stage

Cascode stage actually consists of two different stages one operating common source, the other operating common gate; and behaves as an amplifier by itself. Due to its popularity cascode amplifier is called as *cascode stage* as if it is just one stage.

Cascode stage is popular because of its high gain, high output impedance and good input-output isolation properties. DC voltage level of the input transistors is limited by the common gate structure; therefore short channel effects are reduced due to lower electric field. A telescopic cascode gain stage is shown in Figure 5.4. Transistor M_1 operates as a common source stage while transistor M_2 operates as a common gate stage.

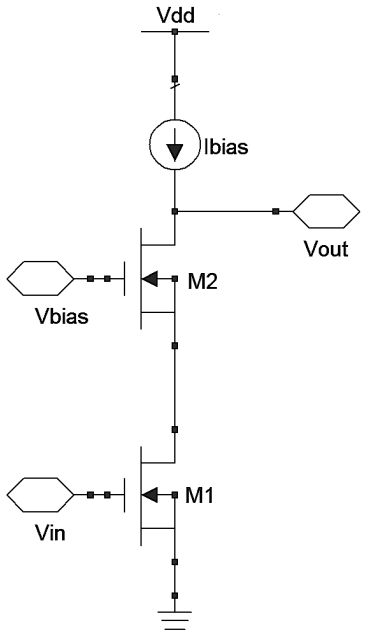


Figure 5.4. Telescopic Cascode Stage.

Output impedance of a cascode stage is

$$R_{out} = g_{m2}[r_{ds1}.r_{ds2}]. \tag{5.19}$$

If a differential amplifier is considered as in Figure 5.5 which is also called a telescopic cascode fully-differential amplifier.

Gain of this differential amplifier is again $A_v = -g_{m1}R_{out}$ but now output resistance is extremely high compared to basic CMOS differential pair. So, in terms of gain telescopic cascode amplifier is advantageous.

It is obvious that telescopic differential pair has bad output-swing since on one DC line there exist four MOSFETs. If current source is also used a cascode current mirror, this number would increase.

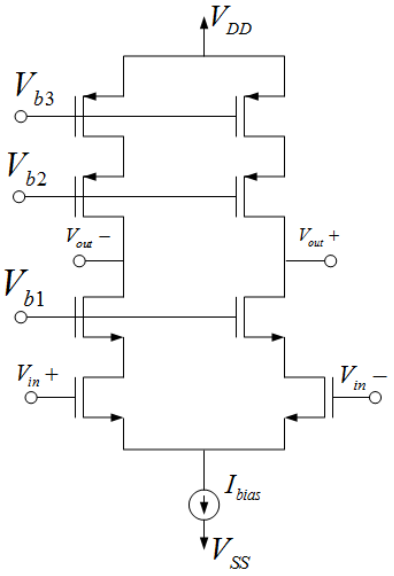


Figure 5.5. Telescopic Cascode Fully Differential Amplifier.

To solve output swing problem folded-cascode stages are used. Basic folded cascode gain stage is seen in Figure 5.6.

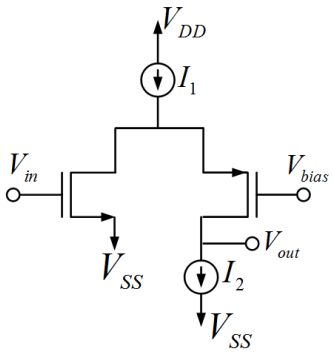


Figure 5.6. Folded Cascode Gain Stage.

Folded cascode stage is taken its name since the current $g_{m1}V_{in}$ is folded when it passes through M_2. Output resistance is same as given in Equation 5.19. Again gain of this stage is defined as $A_v = -g_{m1}R_{out}$.

Frequency analysis of folded cascode stage is done in Section 7.1.1.

6. FEEDBACK

Understanding the main idea of feedback is important for a good circuit design. In this chapter negative feedback is considered.

Negative feedback is advantageous since it stabilizes overall gain against changes in the active devices caused by such as temperature, voltage supply variations, transistor aging. On the other hand negative feedback reduces gain which can be compensated by extra gain stages. Actually potential problem of negative feedback is that undesired oscillations may occur.

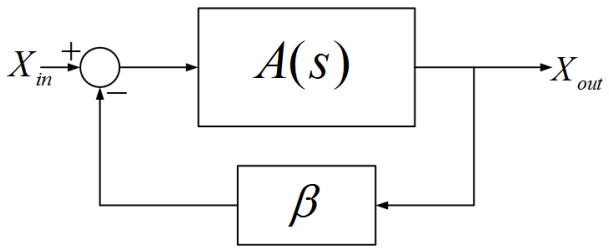


Figure 6.1. Block Diagram of a Feedback System.

Let $H(s)$ be closed loop transfer function, then

$$H(s) = \frac{A(s)}{1 + \beta A(s)}. \tag{6.1}$$

where $A(s)$ is called open-loop transfer function. If we make $\beta A(s)$ product very much larger than unity, then

$$H(s) \simeq 1/\beta. \tag{6.2}$$

Feedback network is generally realized via linear and passive elements such as resistors. As a result closed-loop transfer function would be linear although open-loop transfer function is not.

The very important advantage of feedback is that it helps the overall system to be insensitive to the various distortions.

$$\begin{aligned}\frac{dH(s)}{d\beta} &= \frac{d}{d\beta}\left\{\frac{A(s)}{1+\beta A(s)}\right\} \\ &= -\frac{H}{d\beta}\frac{A(s)}{1+\beta A(s)} \\ \frac{dH(s)}{H} &= -\frac{d\beta}{\beta}\frac{A(s)}{1+\beta A(s)}\end{aligned}$$

Changes in closed loop gain due to changes in open loop gain related to temperature, device non-linearities are extremely suppressed.

Now let us consider $A(s)$ as a one pole transfer function, then

$$\begin{aligned}A(s) &= \frac{a_0}{1-s/p_1} \\ H(s) &= \frac{a_0/(1-s/p_1)}{\beta\ a_0/(1-s/p_1)} \\ &= \frac{a_0}{1+a_0 f}\frac{1}{\frac{s}{p_1}\frac{1}{a_0 f}}.\end{aligned}$$

So, feedback increases bandwidth of the system. It does not provide more gain at high frequencies, whereas low frequency gain is reduced.

6.1. Stability of Systems with Feedback

Major problem with feedback systems is the stability concern. If gain of the system exceed, then instabilities may occur. One way to measure stability of the system is measuring the phase and gain margin of the system.

Stability is determined via the poles of the systems as shown in Figure 6.2. So, if closed loop stability is searched $P(s)$ should be analyzed.

$$P(s) = 1 + \beta A(s) \tag{6.3}$$

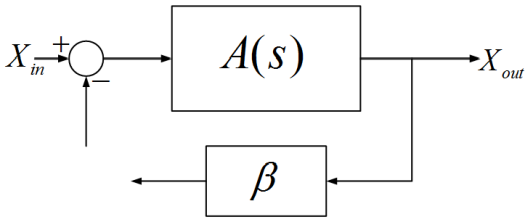


Figure 6.2. Poles of the Feedback System.

First step is to cut the system through feedback and apply a sine wave at the non-inverting input of the summing node. Output is taken from the open node where loop was broken. At the output node now exists $F(s) = \beta A(s)$.

If $\beta A(s) = -1$, then

$$H(s) = \frac{A(s)}{1-1} = \infty.$$

System is said to unstable in this condition. This occurs when

$$\begin{aligned} |\beta A(s)| &= -1 \\ \angle \beta A(s) &= 180^o. \end{aligned}$$

6.1.1. Phase and Gain Margins

As already mentioned; in order to measure a closed-loop system's stability we need to see the angle and magnitude of the product $\beta A(s)$. Gain and phase margin helps us to determine if a system is BIBO (Bounded Input Bounded Output) stable or not.

Gain margin of a closed loop system is defined in Equation 6.4. ω_π is the frequency where $\angle\beta A(\omega_\pi) = 180°$.

$$GM = \frac{1}{|\beta.A(\omega_\pi)|} \tag{6.4}$$

Phase margin of a closed loop system is defined in Equation 6.5. ω_c is the frequency where $1/|\beta.A(\omega_c)| = 1$. A phase margin of $30° - 60°$ is acceptable.

$$PM = 180° + \angle\beta A(\omega_c) \tag{6.5}$$

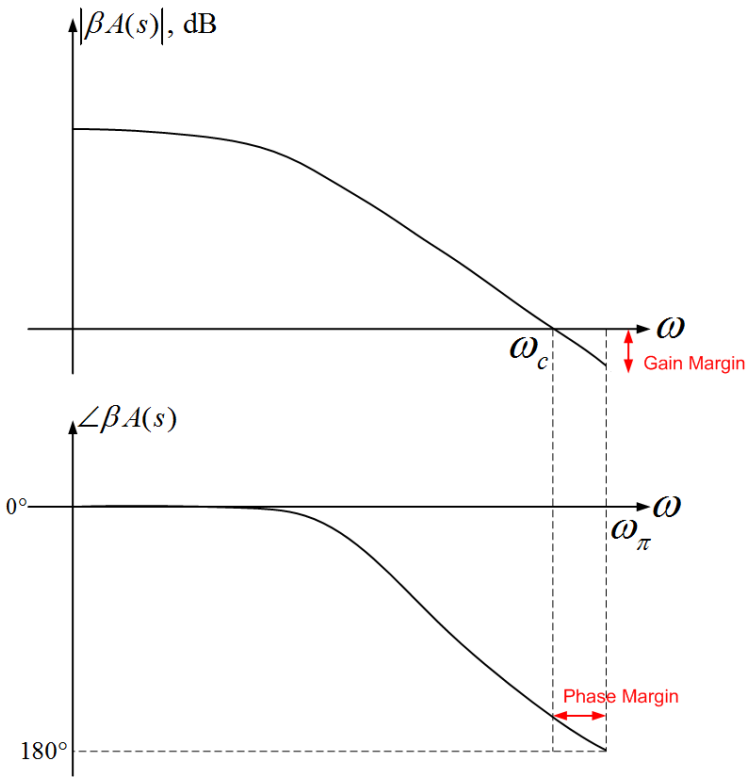


Figure 6.3. Gain and Phase Margins.

6.2. Compensation

Main idea of compensation is to differentiate the phase margin and gain margin such that phase margin performance of the overall circuit improves. Since two stage LNAs are designed in this thesis (Section 7.1), compensation is considered for two-stage fully differential amplifiers.

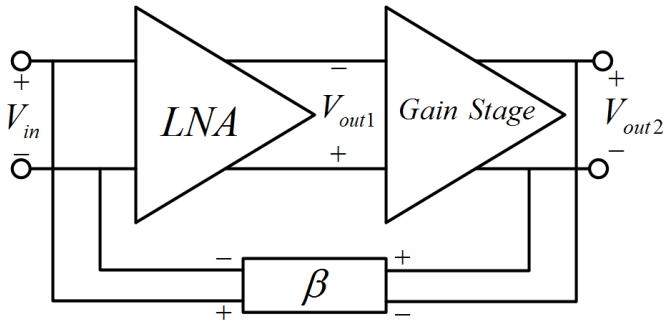


Figure 6.4. Two Stage Fully Differential Amplifier with Negative Feedback.

One way to compensate a two-stage Opamp is to do Miller compensation (may also be referred as pole splitting compensation) as seen in Figure 6.5. A compensation

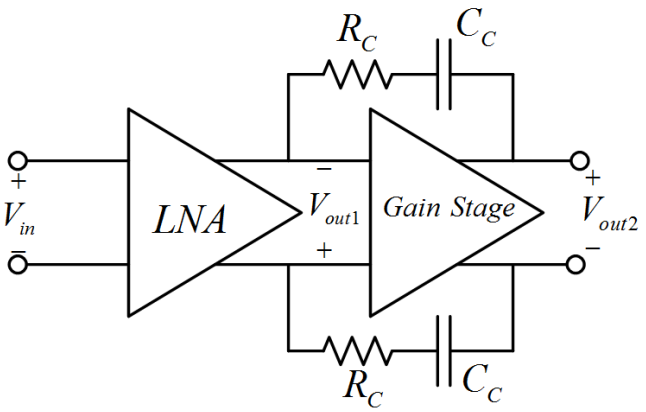


Figure 6.5. Miller Compensation.

capacitor is included to the circuit such that dominant pole frequency decreases whereas non-dominant pole frequency increases. Detailed analysis of Miller compensation is done in Appendix B.

6.3. Common Mode Feedback

Common mode feedback (CMFB) is used to set common mode signals in a fully differential amplifier, which is DC output level. CMFB stabilizes fully differential amplifiers common mode signals by means of adjusting output currents which cannot be done by differential negative feedback. Basic idea is shown in Figure 6.6;

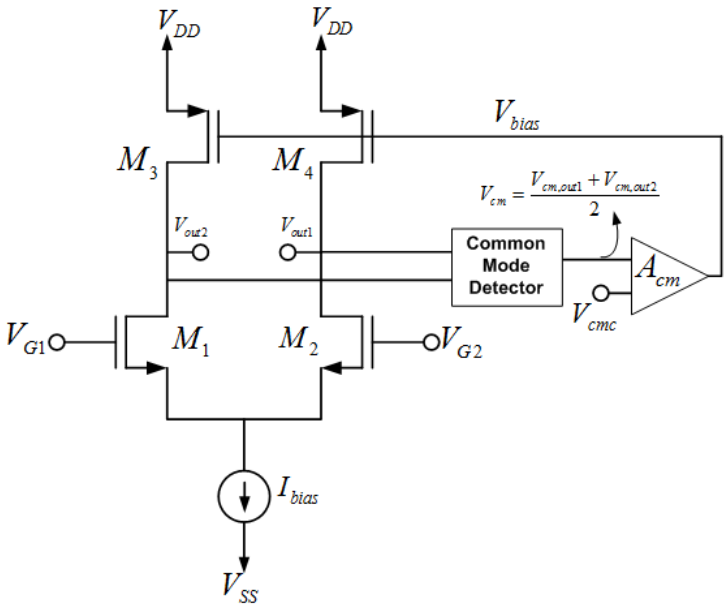


Figure 6.6. CMFB Block Diagram.

Two common mode output DC levels are averaged and V_{cm} is generated, then V_{bias} is set to a desired value via an error amplifier. V_{bias} is used for biasing active loads of the fully differential stage, such that output current and voltage would stabilize.

For a voltage amplifier common mode diode connection can be used; and V_{cm} can be obtained by two resistors as seen in Figure 6.7.

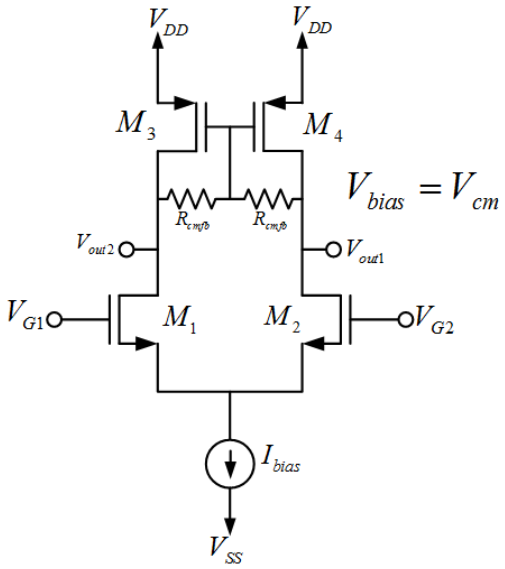


Figure 6.7. Resistive CMFB.

This connection ensures $I_{bias} = I_{D1} + I_{D2}$

There are two main disadvantages of resistive CMFB; increase of chip area since high resistances are needed, decrease of gain since circuit is extra loaded. Let us consider the circuit seen in Figure 6.8.

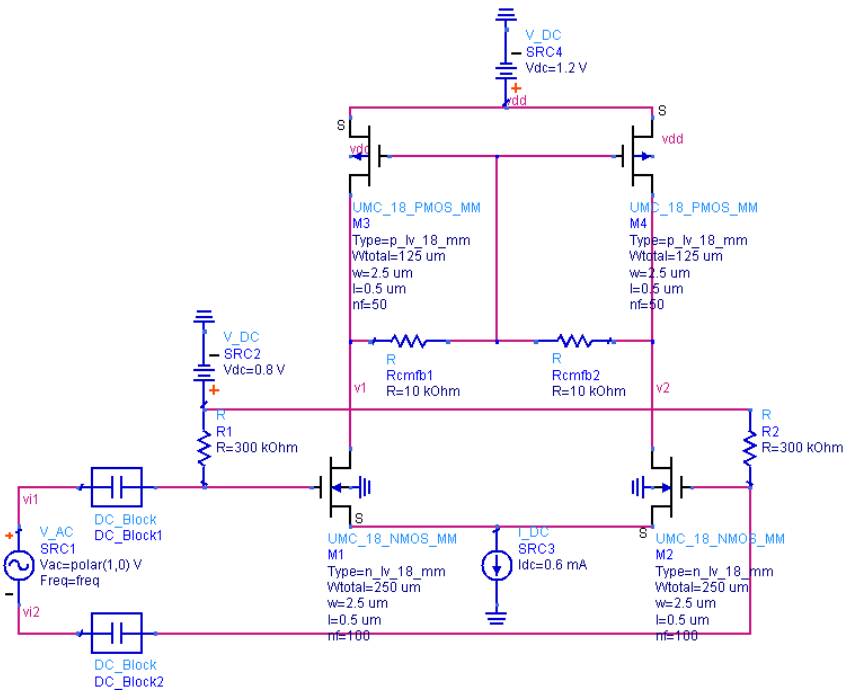


Figure 6.8. Resistive CMFB Example.

$$
\begin{aligned}
g_{m1} &= \sqrt{\mu_n C_{ox} \frac{W_1}{L_1} I_{D1}} = \sqrt{\mu_n C_{ox} \frac{W_1}{L_1} \frac{I_{bias}}{2}} \simeq 0.0076 \ \mho \\
r_{ds1} &= \frac{1}{\lambda I_{D1}} = \frac{1}{\lambda I_{bias}/2} \simeq 7.5 \ \text{k}\Omega \\
r_{ds3} &= \frac{1}{\lambda I_{D2}} = \frac{1}{\lambda I_{bias}/2} \simeq 18.8 \ \text{k}\Omega \\
A_v &= g_{m1}(r_{ds1} // r_{ds3}) \simeq 40.8 \simeq 32 \ \text{dB}
\end{aligned}
$$

But when simulation is done the obtained gain is much lower than expected as seen in Figure 6.9.

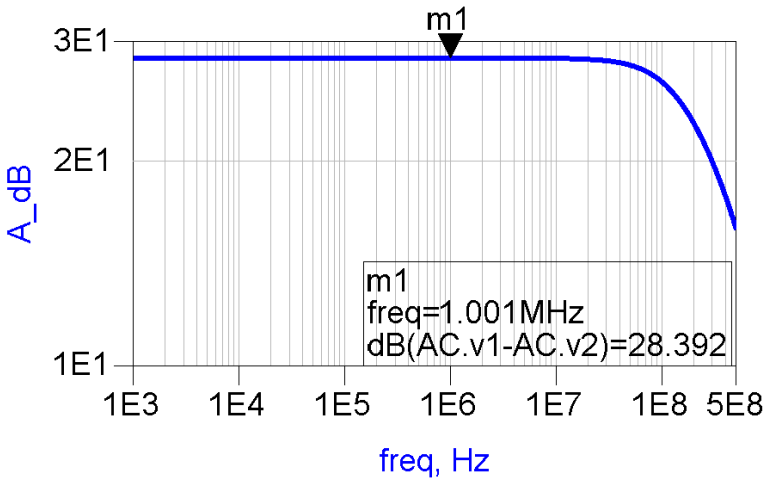


Figure 6.9. CMFB Example's Simulation.

This much of gain reduction is not surprising since common mode feedback resistors are comparable with the output resistance of M_3.

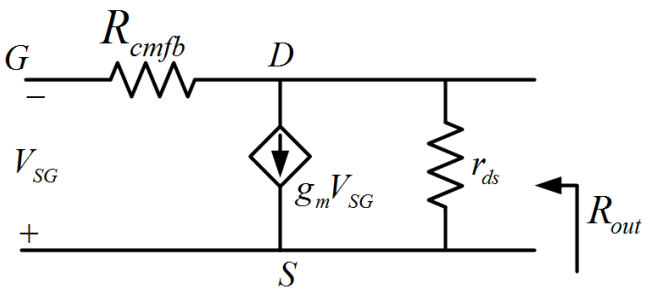


Figure 6.10. Equivalent Circuit of Active Load with Resistive CMFB.

$$R_{out} = R_{\text{cmfb}}//r_{ds} \tag{6.6}$$

Let us calculate gain of the differential pair with CMFB under this circumstance;

$$\begin{aligned} g_{m3} &= \frac{I_{bias}}{V_{ov3}} \simeq 0.003\ \text{℧} \\ R_{out3} &= (10\ \ k\Omega//18.8\ \text{k}\Omega) \simeq 6.5\ \text{k}\Omega \\ A_v &= g_{m1}(r_{ds1}//R_{out3}) \simeq 26.5 \simeq 28.4\ \text{dB} \end{aligned}$$

If R_{cmfb} would not be comparable with r_{ds3}, for instance $R_{\text{cmfb}} = 100\ \text{k}\Omega$ gain becomes $A_v = \simeq 28.67 \simeq 31.7$ dB. This result converges to the gain without CMFB. But, using high resistance would reduce the capability of averaging DC output levels. So, in our designs 10 kΩ resistances are used.

To avoid gain loss, another common-mode sensing method should be developed. There are various CMFB circuits for voltage amplifiers for those who are interested [11], [13], [14]. But for our case; since current budget is limited, an extra feedback circuit means extra dissipated power. So CMFB is done via resistances with loss of gain and chip area. The advantage of resistive CMFB is that, linearity is not effected.

7. LNAs in LITERATURE and DESIGNED LNAs in THIS THESIS

In literature, LNA design is mostly considered for operating frequencies of microwave or above whereas noise mostly occurs at low frequencies due to 1/f noise. Our operating frequency (123 MHz) is considered to be at very high frequency (VHF) band.

Methods derived to design microwave LNAs such as matching networks with inductors, can not be used at 123 MHz. Impedance matching methods are generally used to eliminate capacitive circuit behaviors resulting from parasitic capacitances of transistors [15]. However; at VHF band, inductors needed to compensate capacitive behaviors should be really high because of the low capacitance values at these frequencies.

Actually there exists a gap about VHF and UHF LNA design in literature. So; during design process mostly amplifier design strategies are applied while considering high frequency requirements such as noise matching.

7.1. Designed LNAs

Aim of this thesis is formed by a number of specifications seen in Table 7.1. Since a portable device is being designed, our DC voltage is limited to 1.2 V by the designed charge-pump already published in [2]. Due to this low-voltage DC supply limit, output swing gains extra importance.

Table 7.1. Design Spesifications.

Total Dissipated Power	< 2 mW
NF	$< 1\ dB$
Voltage Gain	> 50 dB
S_{21}	> 25 dB
V_{DD}	$= 1.2$ V
Operating Frequency	$= 123$ MHz
$\text{PSD}_{\text{input}}$	$\simeq$ -80 dBm

High output swing brings load in terms of gain, linearity, and noise figure. Consequently, designs are done to obtain the optimum results for each specification.

7.1.1. Fully-Differential Folded Cascode (FDFC) LNA with NMOS Input Pair

A two stage fully differential folded cascode LNA designed as shown in Figure 7.1. Detailed component values are also given in Table 7.2.

First stage which provides us low noise has FDFCA topology with NMOS input pair; whereas gain stage has fully differential CMOS amplifier topology.

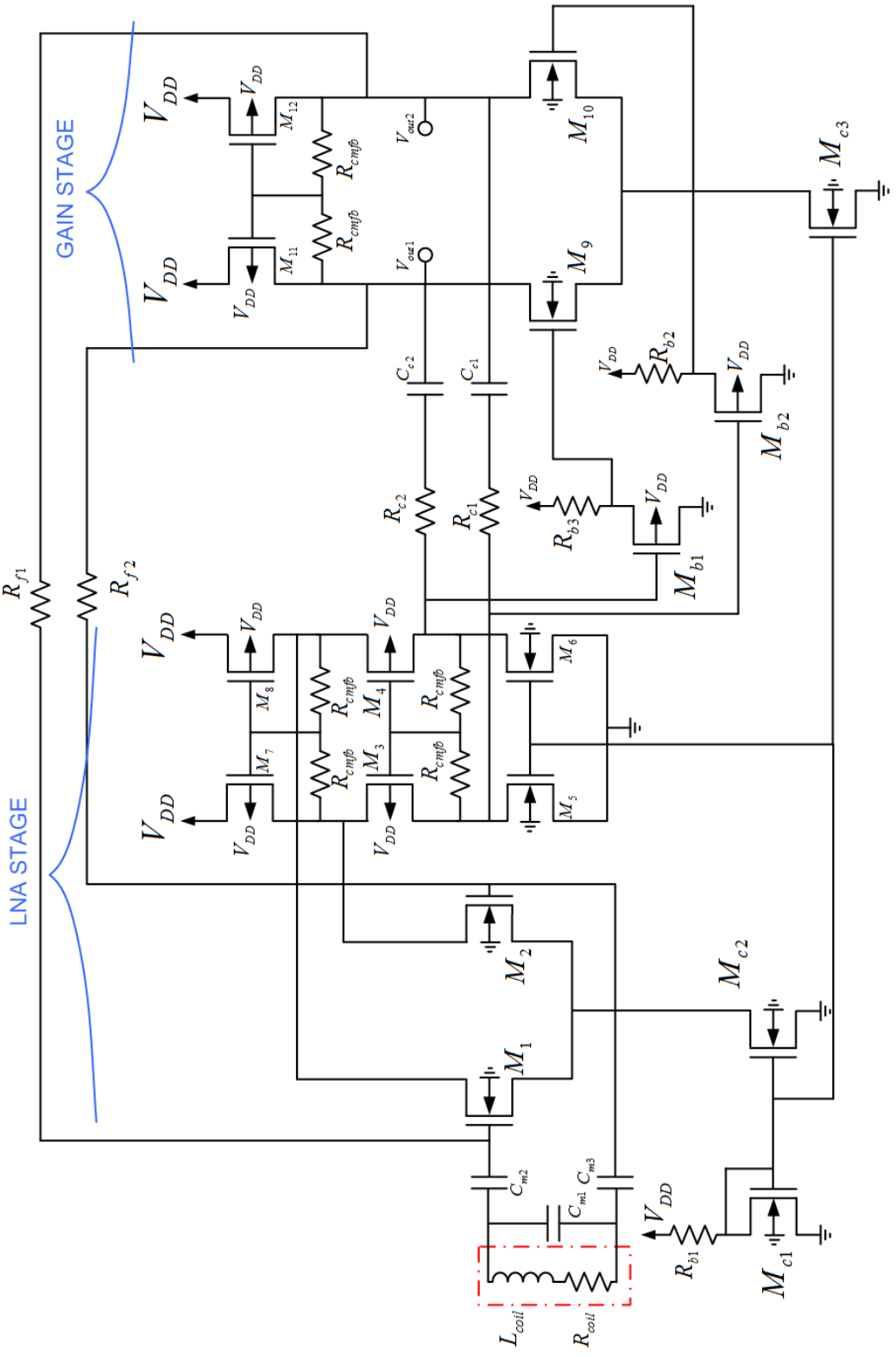


Figure 7.1. Folded Cascode LNA Design.

Table 7.2. Component Values of Fully Differential Folded Cascode LNA with NMOS Input Pair.

$W/L_{1,2}$	60 μm/0.5 μm
$W/L_{3,4}$	20 μm/0.5 μm
$W/L_{5,6}$	4 μm/0.5 μm
$W/L_{7,8}$	260 μm/0.5 μm
$W/L_{9,10}$	8 μm/0.5 μm
$W/L_{11,12}$	40 μm/0.5 μm
$W/L_{M_{c1}}$	10 μm/0.5 μm
$W/L_{M_{c2}}$	110 μm/0.5 μm
$W/L_{M_{c3}}$	20 μm/0.5 μm
$W/L_{M_{b1},M_{b2}}$	10 μm/0.5 μm
R_{b1}	10 kΩ
$R_{b1,b2}$	20 kΩ
R_{cmfb}	10 kΩ
$R_{f1,f2}$	600 kΩ

7.1.1.1. Voltage Gain Calculations of the FDFC LNA with NMOS Input Pair. Gain calculation of a basic CMOS differential stage with CMFB is already shown in Section 6.3. A detailed gain calculation of fully differential folded-cascode amplifier is a little bit complicated.

Note that; M_5 and M_6 are part of basic current mirror and they bias $M_{3,4,7,8}$. In this design folded current $g_m v_{in}$ would pass through $M_{3,5}$ and $M_{4,6}$. Output resistance of basic folded cascode gain stage is already given in Equation 5.19. Now output resistance of folded cascode stage becomes

$$R_{out_{fc}} = g_{m3} r_{out3} (r_{ds1} // r_{out7}). \tag{7.1}$$

Output resistance of overall FDFC stage becomes [16]

$$\begin{aligned} R_{out_{fc}} &= g_{m3} r_{out3} (r_{ds1} // r_{out7}) // r_{ds5} \\ r_{out3} &= r_{ds3} // R_{\text{cmfb}} \\ r_{out7} &= r_{ds7} // R_{\text{cmfb}}. \end{aligned} \tag{7.2}$$

Gain is as usual $g_{m1} R_{out}$. Due to low DC-voltage limitations a cascode current mirror cannot be used in this design. This would limit our output swing.

On the other hand; all MOSFETs needs to have proper V_{DS} and V_{GS} voltages to remain in active region. First of all; proper V_{DS} voltages are set for various biasing currents since we do know; $V_{ov} = 2I_D / \sqrt{2\mu_n (W/L) C_{ox} I_D}$.

Biasing currents are determined via current mirrors formed by $M_{c1,c2,c3}$ and $M_{5,6}$. Input pairs $M_{1,2}$ are biased with 1.05 mA via M_{c2} such that; $I_{D1} = I_{D2} \simeq 524\ \mu$A. $M_{3,4}$ are biased with 43.2 μA via $M_{5,6}$ such that; $I_{D3} = I_{D4} = I_{D5} = I_{D6} \simeq 43.2\ \mu$A. As a result, $M_{7,8}$ are biased with $I_{D1} + I_{D3}$ such that $I_{D7} = I_{D8} \simeq 568\ \mu$A.

$$\begin{aligned} g_{m1} &= \sqrt{\mu_n C_{ox} \frac{W_1}{L_1} I_{D1}} \simeq 0.0063\ \text{℧}, \quad g_{m3} \simeq 0.00045\ \text{℧} \\ r_{ds1} &= \frac{1}{\lambda I_{D1}} = 5.26\ \text{k}\Omega \\ r_{ds3} &= \frac{1}{\lambda I_{D3}} = 11.25\ \text{k}\Omega, \quad r_{out3} = r_{ds3} // R_{\text{cmfb}} = 5.3\ \text{k}\Omega \\ r_{ds5} &= \frac{1}{\lambda I_{D5}} = 65.6\ \text{k}\Omega \\ r_{ds7} &= \frac{1}{\lambda I_{D7}} = 10\ \text{k}\Omega, \quad r_{out7} = r_{ds3} // R_{\text{cmfb}} = 5\ \text{k}\Omega \\ R_{out_{fc}} &= g_{m3} r_{out3} (r_{ds1} // r_{out7}) // r_{ds5} \simeq 5\ \text{k}\Omega \\ A_{v-1^{st}stage} &= -g_{m1} (R_{out}) \simeq -31.5 \simeq 29.9\ \text{dB} \end{aligned}$$

Simulation also confirms our result as seen in Figure 7.11.

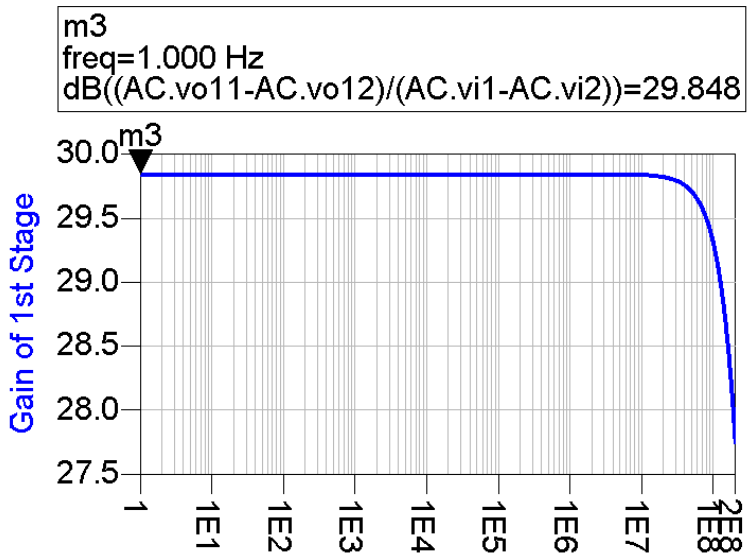


Figure 7.2. Simulated Voltage Gain of the First Stage.

A gain stage (whose structure is given in Section 6.3) biased with 189 μA is designed. A voltage gain of 6.3 is obtained.

First stage and second stage connection is important for our design. DC level of first stage's output is 382 mV which is insufficient for the second stage and may lead M_{c3} to go out of active region. If M_{c3} will operate in triode region, it would cause errors in mirroring the bias current; which would change all bias points and also overall AC characteristic of the designed circuit.

Source followers M_{b1} and M_{b2} are used to overcome this problem; and a DC level of 814 mV is obtained at gates of M_9 and M_{10}. Used source followers are designed with loss of voltage gain such that they would not consume much power. They are only biased with 19.3 μA, and they have 0.7 voltage gain.

Consequently; overall gain is calculated to be

$$A_v = 31 \times 0.7 \times 6.5 = 141 \simeq 42.9 \text{ dB}.$$

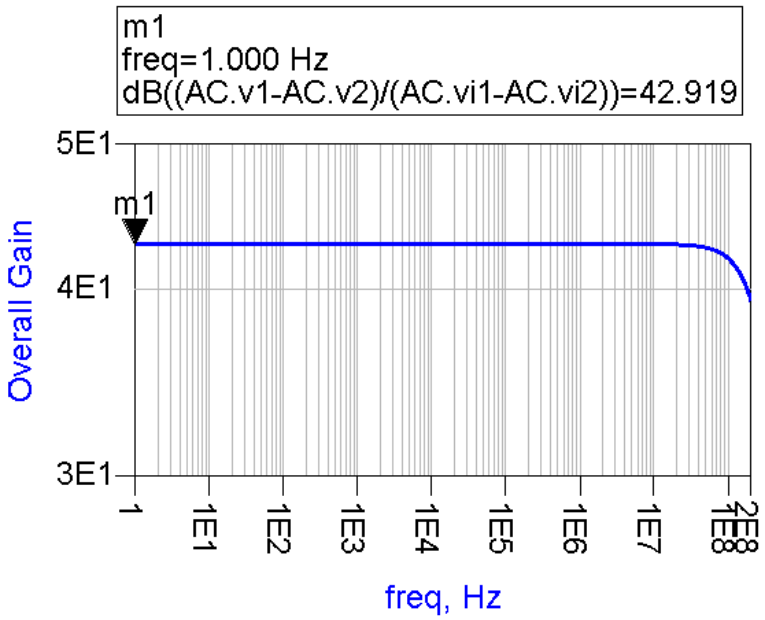


Figure 7.3. Overall Voltage Gain Simulation of the FDFC LNA with NMOS Input Pair.

This gain is of course reduced by load resistance. Designed LNA will be loaded by a mixer which is modeled by its 2.5 kΩ thevenin input resistance [2]. This resistance will be connected to the differential output such that each output will be loaded by 1.25 kΩ resistor. This load resistance lowers the second stage's voltage gain to 1.09. With load included, overall gain becomes $A_v = 31 \times 0.7 \times 1.09 = 23.65 \simeq 27$ dB. This problem can be solved via a buffer that will prevent the circuit to be loaded.

Finally, FDFC LNA with these biasing currents consumes 1.4 mA current which leads 1.68 mW power dissipation.

7.1.1.2. Frequency Analysis and Compensation of the FDFC LNA with NMOS Input Pair.

Dominant pole of the first stage is given as [17]

$$p_{1^{st\ stage}} \simeq \frac{1}{2\pi r_{out7} C_{out-1^{st\ stage}}} \tag{7.3}$$

$$C_{out-1^{st\ stage}} = C_{bd7} + C_{gd7} + C_{bd3} + C_{gd3} + C_{gs-Mb1}. \tag{7.4}$$

Dominant pole of the second stage is given as [12]

$$p_{2^{nd\ stage}} \simeq \frac{1}{2\pi R_{out2} C_{out-2^{nd\ stage}}} \tag{7.5}$$

$$C_{out-2^{nd\ stage}} = C_{bd9} + C_{gd9} + C_{bd11} + C_{gd11}. \tag{7.6}$$

However with compensation, dominant and non-dominant poles change. For compensation technique used in this design see Appendix B. An RC network ($R_{c1,2} - C_{c1,2}$) is used. A high resistance (100 kΩ) is used such that it would not effect the output resistance of the first stage.

In simulations, a phase margin of 13° is observed before compensation whereas it improved to 36° after compensation. (Section 7.1.1.4)

7.1.1.3. Input-Referred Noise of the FDFC LNA with NMOS Input Pair. Noise model of a MOSFET is already given in Equation 3.22. γ coefficient of 0.18 μm is 50% percent higher than long devices [18]. However; with simulations γ for 0.18 μm when $l = 0.5$ μm is found to be $0.8\sqrt{\text{V}}$.

$$\overline{V^2_{Mosfet}} = 4kT\ 0.8\ \frac{1}{g_m}\Delta f \tag{7.7}$$

For modelling the input-referred noise only first stage of the amplifier is considered since 2^{nd} stage NF contribution to the overall amplifier is negligible (Section 3.1.3.1).

$$\overline{V^2_{FDFC\ LNA}} \simeq 4kT\ \Delta f \left[2\Big(0.8\frac{1}{g_{m1}} + 0.8\frac{g_{m7}}{(g_{m1})^2} + \frac{1}{R_{\text{cmfb}}\ g^2_{m1}} \Big) \right] \tag{7.8}$$

Note that contribution of M_3 to the input-referred noise can be neglected; this is another advantage of folded-cascode amplifiers [18]. Calculated input referred noise is; $\overline{V^2_{FDFC\ LNA}}/\Delta f \simeq 1.97$ nV/$\sqrt{\text{Hz}}$.

Let us make a simple analysis of NF with matching network designed in Section 3.1.7.1. Noise generated in the coil is calculated from the intrinsic resistance is; $\overline{V^2_{coil}}/\Delta f \simeq 0.02$ nV/$\sqrt{\text{Hz}}$. We have found that for a perfect match voltage gain (A) of the matching network is 43.6.

$$NF = 10\ log\ \left(\frac{A^2\overline{V^2_{matching-network}} + \overline{V^2_{in-LNA}}}{A^2\overline{V^2_{matching-network}}}\right) \simeq 0.22 \text{ dB}$$

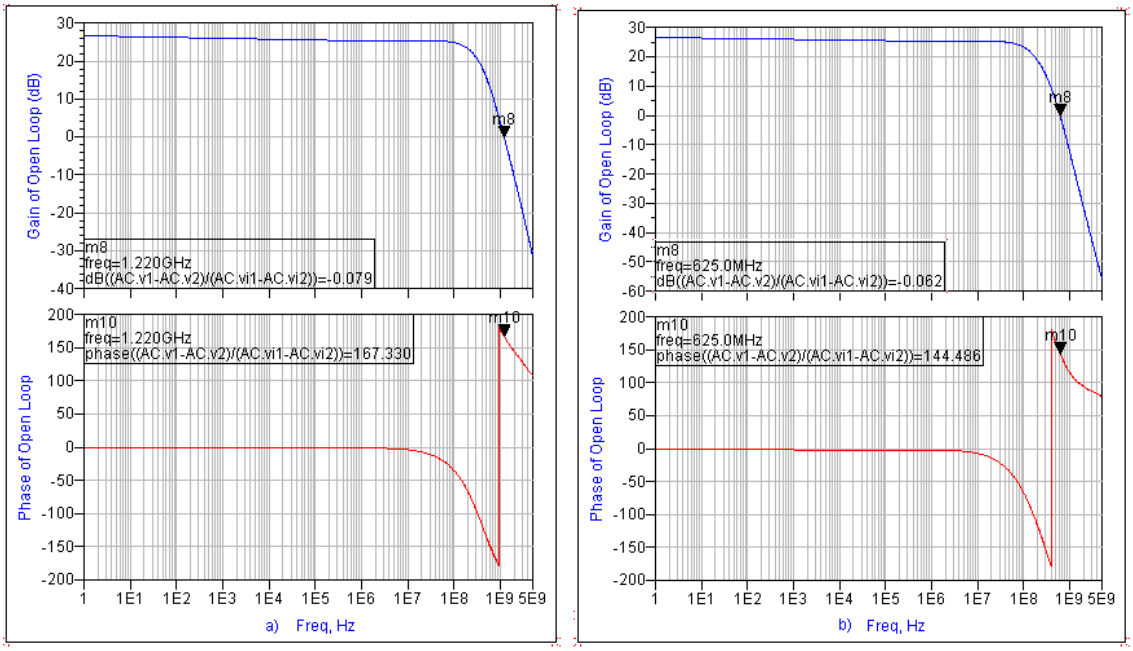
However simulation in Section 7.1.1.4 shows that NF≃0.39 dB. It is known that to obtain the best NF; $Z_{LNA} = \infty$. Our LNA has a finite input impedance at 123 MHz which is; 1899-7435j Ω. Finite input impedance leads the gain of the matching network 32.75 (See Appendix A). So NF is recalculated to be 0.387 dB.

7.1.1.4. Simulation Results of the FDFC LNA with NMOS Input Pair. Simulations of overall system support our analysis and specifications.

1-dB Compression Point

freq	inpwr	outpwr
0.0000 Hz	-38.99 dBm	-18.87 dBm
123.0 MHz	-38.99 dBm	-18.87 dBm
246.0 MHz	-38.99 dBm	-18.87 dBm

Figure 7.4. 1-dB Compression Point Simulation of the FDFC LNA with NMOS Input Pair.



(a) Before Compensation. (b) After Compensation.

Figure 7.5. Phase Margin Simulations of the FDFC LNA with NMOS Input Pair.

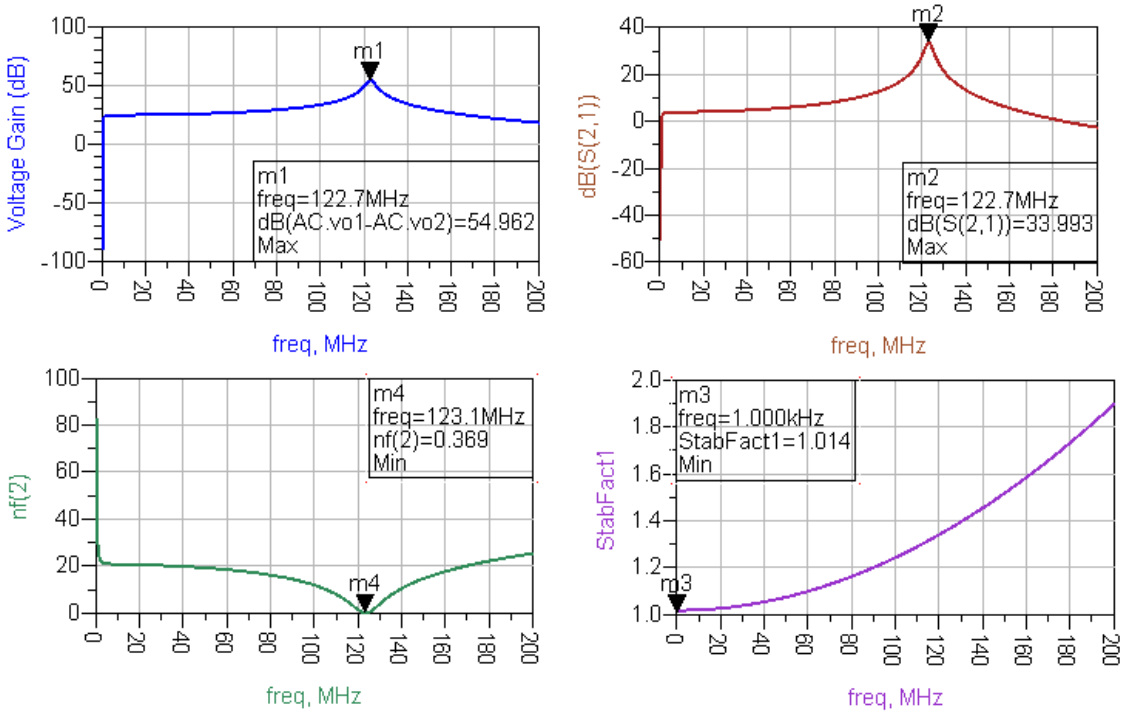


Figure 7.6. Result Set of the FDFC LNA with NMOS Input Pair.

7.1.1.5. Post-Layout Simulations of the FDFC LNA with NMOS Input Pair. Since a differential circuit is to be drawn, common centroid method is used to obtain a good matching; and to suppress fabrication process variations [19]. Chip area is 468 μm $\times$ 223 μm.

When post-layout simulations are compared with schematic simulations, it is observed that gain is same whereas there is an increment in NF. Schematic simulation is indicating a NF of 0.37 dB. Due to resistive parasitics at gates of the input-pairs; NF of post layout simulation is 0.7 dB.

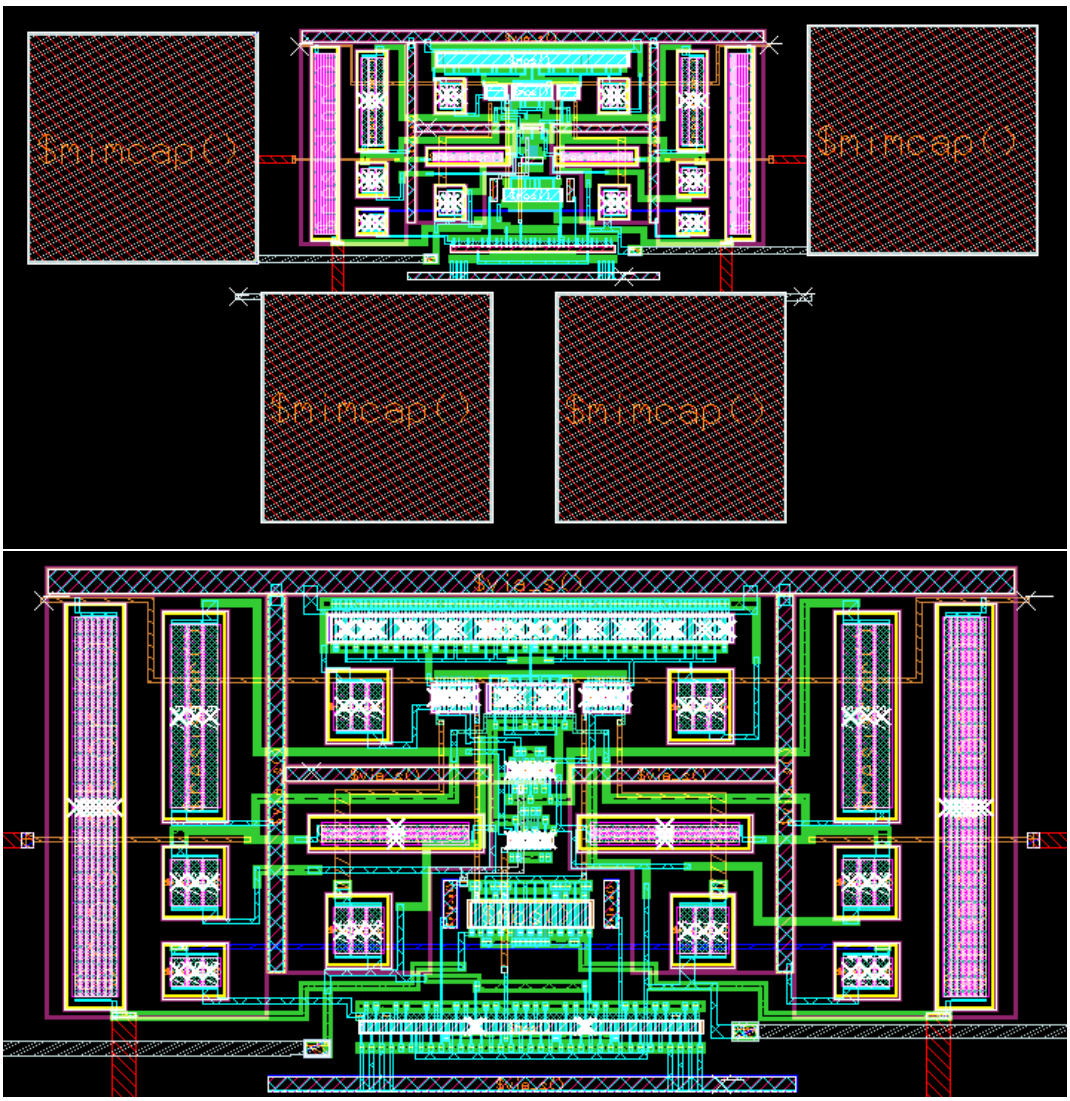


Figure 7.7. Layout Views of the FDFC LNA with NMOS Input Pair.

Gain is calculated from transient analysis such that a 1 μV input voltage is applied.

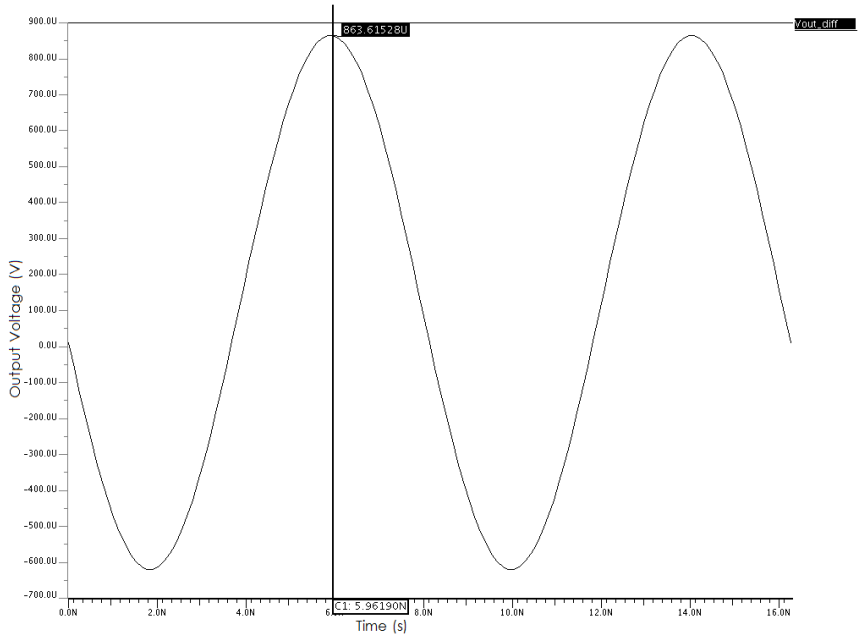


Figure 7.8. Post-Layout Transient Simulation of the FDFC LNA with NMOS Input Pair.

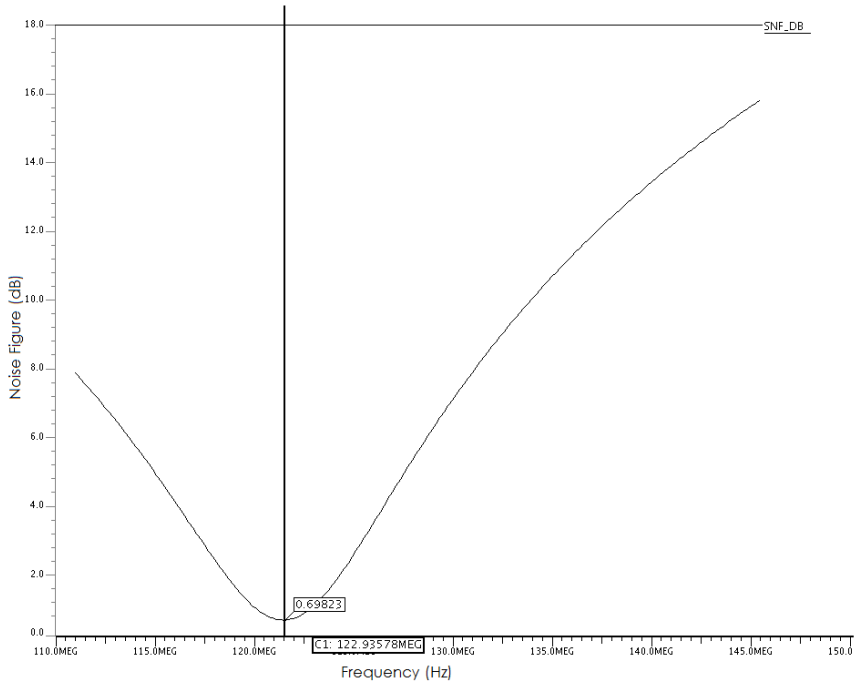


Figure 7.9. Post-Layout Noise Figure Simulation of the FDFC LNA with NMOS Input Pair.

7.1.2. Fully-Differential Folded Cascode (FDFC) LNA with PMOS Input Pair

A two stage fully differential folded cascode LNA designed as shown in Figure 7.10. Detailed component values are also given in Table 7.3.

Table 7.3. Component Values of Fully Differential Folded Cascode LNA with PMOS Input Pair.

$W/L_{1,2}$	200 μm/0.5 μm
$W/L_{3,4}$	4 μm/0.5 μm
$W/L_{5,6}$	16 μm/0.5 μm
$W/L_{7,8}$	20 μm/0.5 μm
$W/L_{9,10}$	10 μm/0.5 μm
$W/L_{11,12}$	20 μm/0.5 μm
$W/L_{M_{c1}}$	40 μm/0.5 μm
$W/L_{M_{c2}}$	8 μm/0.5 μm
$W/L_{M_{c3}}$	500 μm/0.5 μm
$W/L_{M_{c4}}$	24 μm/0.5 μm
$W/L_{M_{b1},M_{b2}}$	4 μm/0.5 μm
R_{b1}	7 kΩ
$R_{b1,b2}$	20 kΩ
R_{cmfb}	10 kΩ
$R_{f1,f2}$	600 kΩ

First stage which provides us low noise has FDFCA topology with PMOS input pair; whereas gain stage has fully differential CMOS amplifier topology.

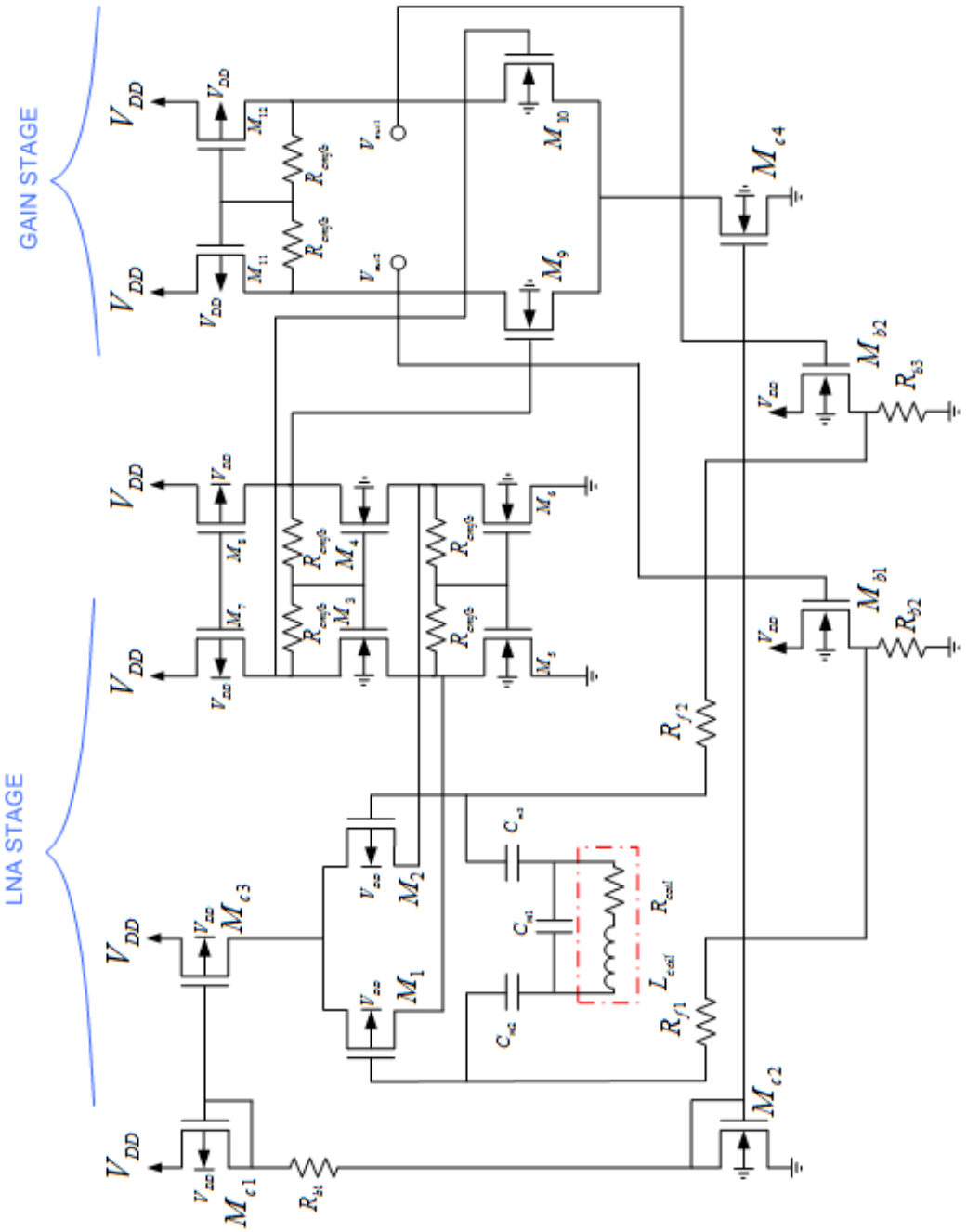


Figure 7.10. Folded Cascode LNA Design.

7.1.2.1. Voltage Gain Calculations of the FDFC LNA with PMOS Input Pair. For FDFC topology which is the first stage of this amplifier, detailed voltage gain analysis is done in Section 7.1.1.1. For a PMOS input paired FDFCA output resistance becomes

$$R_{out_{fc}} = g_{m3} r_{out3} (r_{ds1} // r_{out5}) // r_{ds7}. \tag{7.9}$$

Biasing currents are determined via current mirrors formed by $M_{c1,c2,c3,4}$ and $M_{7,8}$. Input pairs $M_{1,2}$ are biased with 960 μA via M_{c2} such that; $I_{D1} = I_{D2} \simeq 480$ μA. $M_{3,4}$ are biased with 38.7 μA via $M_{7,8}$ such that; $I_{D3} = I_{D4} = I_{D7} = I_{D8} \simeq 43.2$ μA. As a result, $M_{5,6}$ are biased with $I_{D1} + I_{D3}$ such that $I_{D5} = I_{D6} \simeq 518$ μA.

$$\begin{aligned}
g_{m1} &= \sqrt{\mu_n C_{ox} \frac{W_1}{L_1} I_{D1}} \simeq 0.0021 \text{ } \mho \\
g_{m3} &= \sqrt{\mu_n C_{ox} \frac{W_3}{L_3} I_{D1}} \simeq 0.00044 \text{ } \mho \\
r_{ds1} &= \frac{1}{\lambda I_{D1}} = 13 \text{ k}\Omega \\
r_{ds3} &= \frac{1}{\lambda I_{D1}} = 69.4 \text{ k}\Omega, r_{out3} = 10 \text{ k}\Omega // r_{ds3} = 8.7 \text{ k}\Omega \\
r_{ds5} &= \frac{1}{\lambda I_{D5}} = 6.1 \text{ k}\Omega, r_{out5} = r_{ds5} // R_{\text{cmfb}} = 3.8 \text{ k}\Omega \\
r_{ds7} &= \frac{1}{\lambda I_{D1}} = 163.6 \text{ k}\Omega \\
R_{out_{fc}} &= g_{m3} r_{out3} (r_{ds1} // r_{out5}) // r_{ds7} \simeq 10 \text{ k}\Omega \\
A_{v-1^{st}stage} &= -g_{m1}(R_{out}) \simeq -23.5 \simeq 27.42 \text{ dB}
\end{aligned}$$

Gain calculation of the second stage has already been explained in Section 6.3. A gain stage with 6.9 voltage gain is designed with a bias current of 240 μA. Again 2.5 kΩ differential load which affects each output node as a 1.25 kΩ resistor, decreases second stage's voltage gain around 1.2.

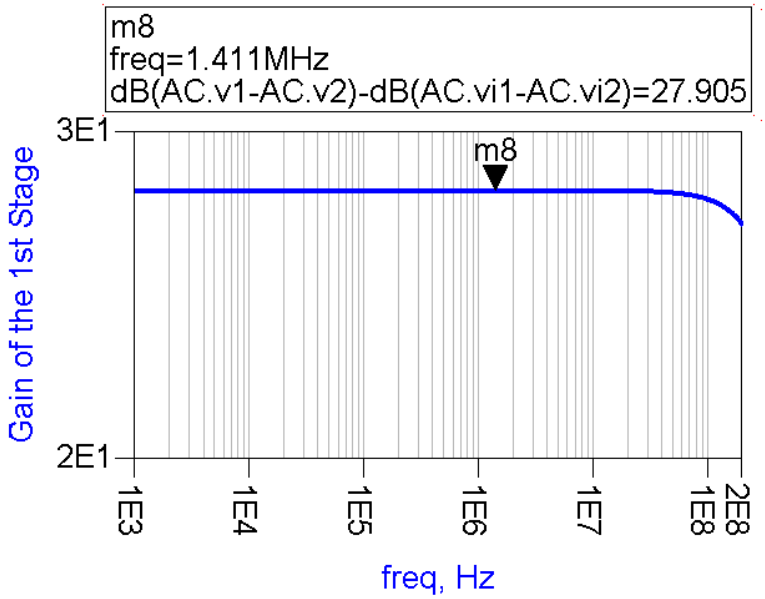


Figure 7.11. Voltage Gain Simulation of First Stage of the FDFC LNA with PMOS Input Pair.

In Section 7.1.1.1 it is explained that for DC level requirements, source followers are used as level shifters. In this design, there is no need to use level shifters between 1st and 2nd stage; whereas 1st stage's DC-input level is determined by DC-output level of the second which is too high for our case. NMOS level shifters are used to lower DC level; which has also helped us with compensation.(See Section 7.1.2.2)

These level shifters are designed such that they have 1.27 voltage gain. As a result overall gain becomes

$$A_v = 23.5 \times 1.2 \times 1.27 =\simeq 29 \text{ dB}.$$

Note that with PMOS input pair obtainable gain decreases due to lower mobility of carriers. Actually this is the main reason why NMOS differential pairs are used for gain stages.

Consequently; 1.4 mA is consumed resulting in 1.68 mW power dissipation.

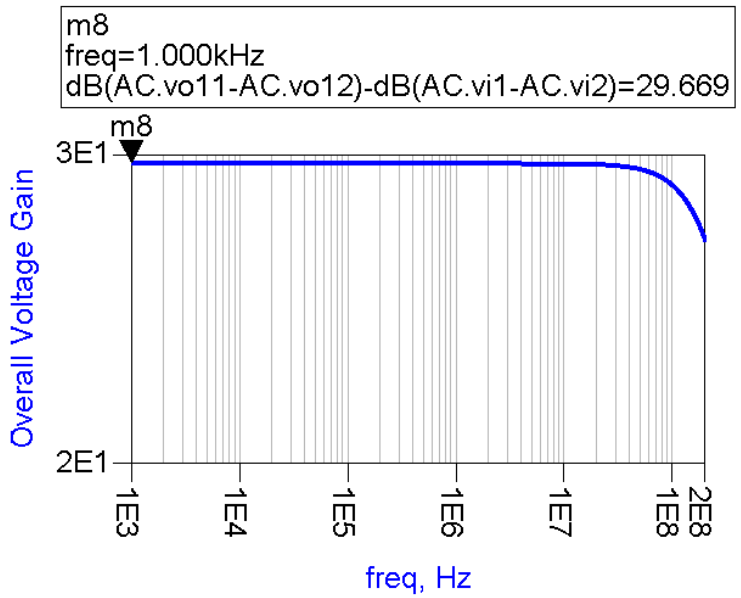


Figure 7.12. Overall Voltage Gain Simulation of the FDFC LNA with PMOS Input Pair.

7.1.2.2. Frequency Analysis of the FDFC LNA with PMOS Input Pair. Dominant pole of the first stage is given as [17]

$$\begin{aligned} p_{1^{st}\ stage} &\simeq \frac{1}{2\pi r_{out5} C_{out-1^{st}\ stage}} \\ C_{out-1^{st}\ stage} &= C_{bd5} + C_{gd5} + C_{bd3} + C_{gd3}. \end{aligned}$$

Dominant pole of the second stage is given as [12]

$$\begin{aligned} p_{2^{nd}\ stage} &\simeq \frac{1}{2\pi R_{out2} C_{out-2^{nd}\ stage}} \\ C_{out-2^{nd}\ stage} &= C_{bd9} + C_{gd9} + C_{bd11} + C_{gd11} + C_{gs-M_{b2}}. \end{aligned}$$

Source followers form a series RC network with feedback resistors and biasing resistors of the source followers. This RC network determines dominant pole of the amplifier.

Dominant pole of the amplifier becomes

$$p_{amplifier} \simeq \frac{1}{R_{eq}C_{out-2^{nd}\ stage}} \tag{7.10}$$

$$R_{eq} = R_f//R_{b3} \simeq R_{b3}. \tag{7.11}$$

7.1.2.3. Input-Referred Noise of the FDFC LNA with PMOS Input Pair. Input-referred noise of the amplifier is given as

$$\overline{V^2_{FDFC\ LNA}} \simeq 4kT\ \Delta f \left[2\Big(0.8\frac{1}{g_{m1}} + 0.8\frac{g_{m5}}{(g_{m1})^2} + \frac{1}{R_{\text{cmfb}}\ g^2_{m1}}\Big)\right]. \tag{7.12}$$

Calculated input referred noise is; $\overline{V^2_{FDFC\ LNA}}/\Delta f \simeq 2.26$ nV/$\sqrt{\text{Hz}}$. $V^2_{matching-network} =$ 0.02 nV/$\sqrt{\text{Hz}}$.

If matching network gain is assummed to be transferred without loss (A=43.6), then

$$NF = 10\ \log\Big(\frac{A^2\overline{V^2_{matching-network}} + \overline{V^2_{in-LNA}}}{A^2\overline{V^2_{matching-network}}}\Big) \simeq 0.25 \text{ dB}.$$

Simulation in Section 7.1.2.4 shows that NF≃0.57 dB. Z_{LNA}=200-2381j Ω which leads the gain of the matching network 28.3 (See Appendix A). So NF is recalculated to be 0.573 dB.

7.1.2.4. Simulation Results of the FDFC LNA with PMOS Input Pair. Simulations of over- all system support our analysis and specifications.

1-dB Compression Point

freq	inpwr	outpwr
0.0000 Hz	-38.96 dBm	-16.32 dBm
123.0 MHz	-38.96 dBm	-16.32 dBm
246.0 MHz	-38.96 dBm	-16.32 dBm

Figure 7.13. 1-dB Compression Point Simulation of the FDFC LNA with PMOS Input Pair.

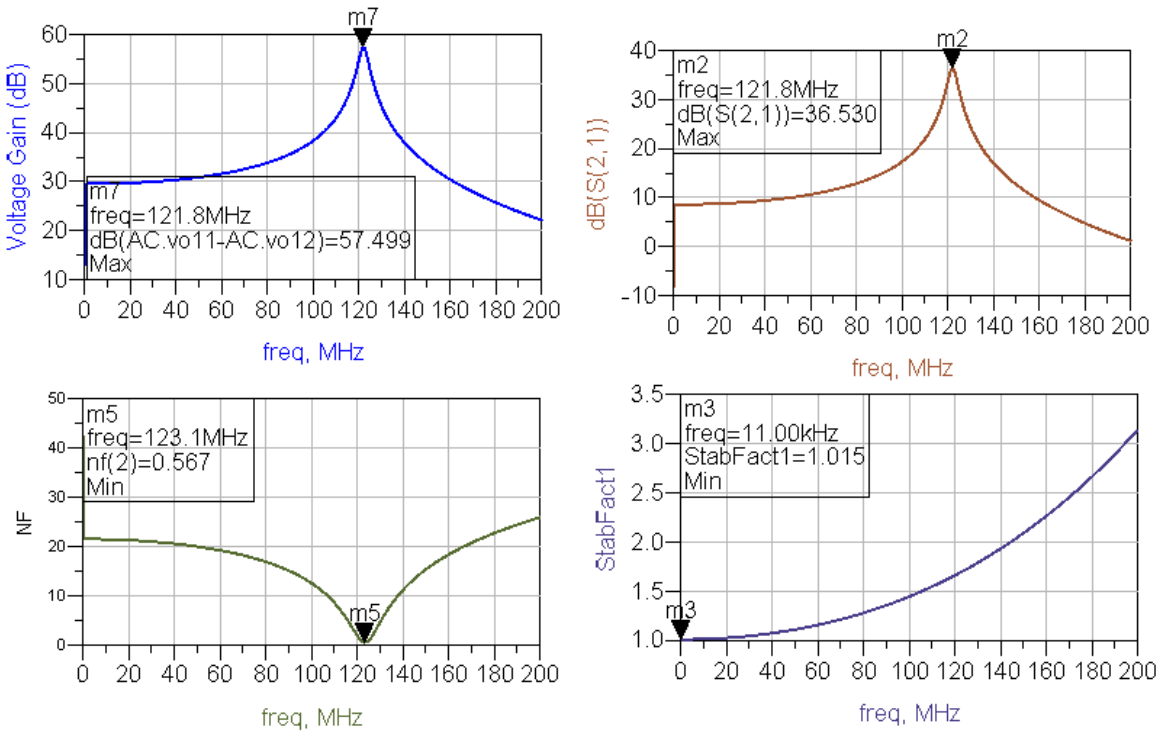


Figure 7.14. Simulation Result Set of the FDFC LNA with PMOS Input Pair.

7.1.2.5. Post-Layout Simulations of the FDFC LNA with PMOS Input Pair. Layout is of the circuit drawn with common-centroid method; and it is seen in Figure 7.15. Note that area of the chip is 200 μm $\times$ 120 μm; with elimination of compensation capacitors layout area significantly decreases.

Simulation results shows a NF of 0.8 dB which results from parasitic resistances. However post-layout voltage gain simulation match with schematic simulation. Gain is calculated from transient analysis such that a 1 μV input voltage is applied.

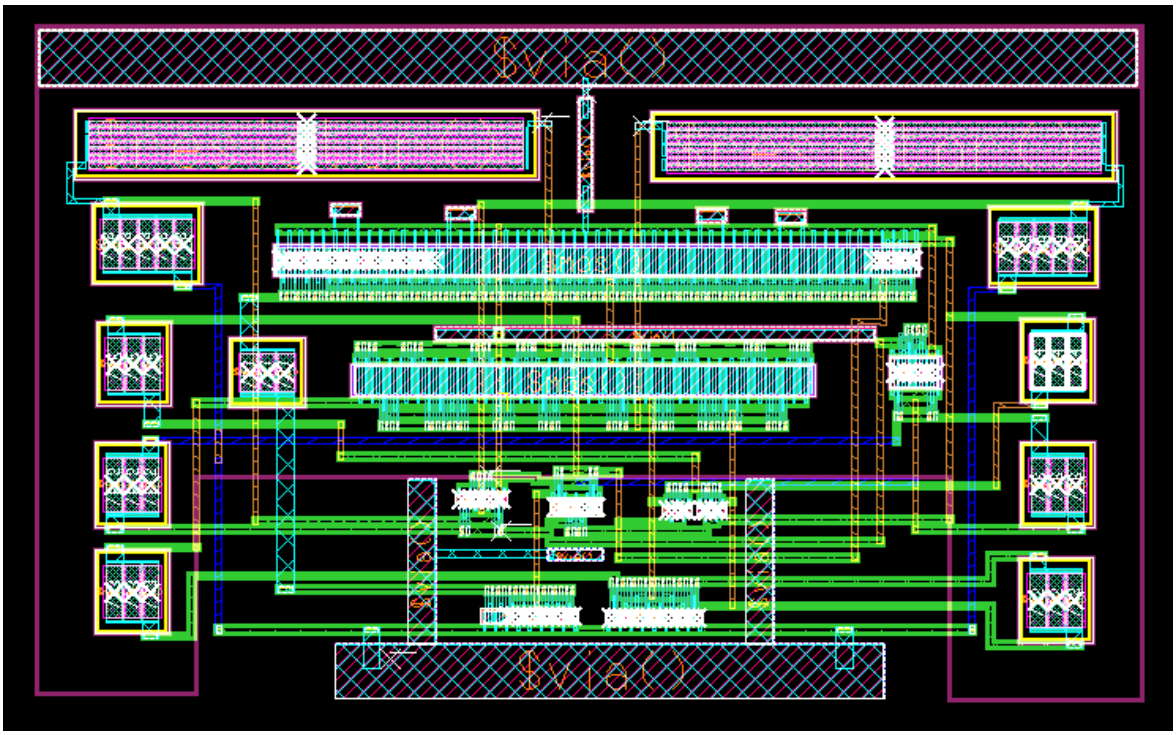


Figure 7.15. Layout View of the FDFC LNA with PMOS Input Pair.

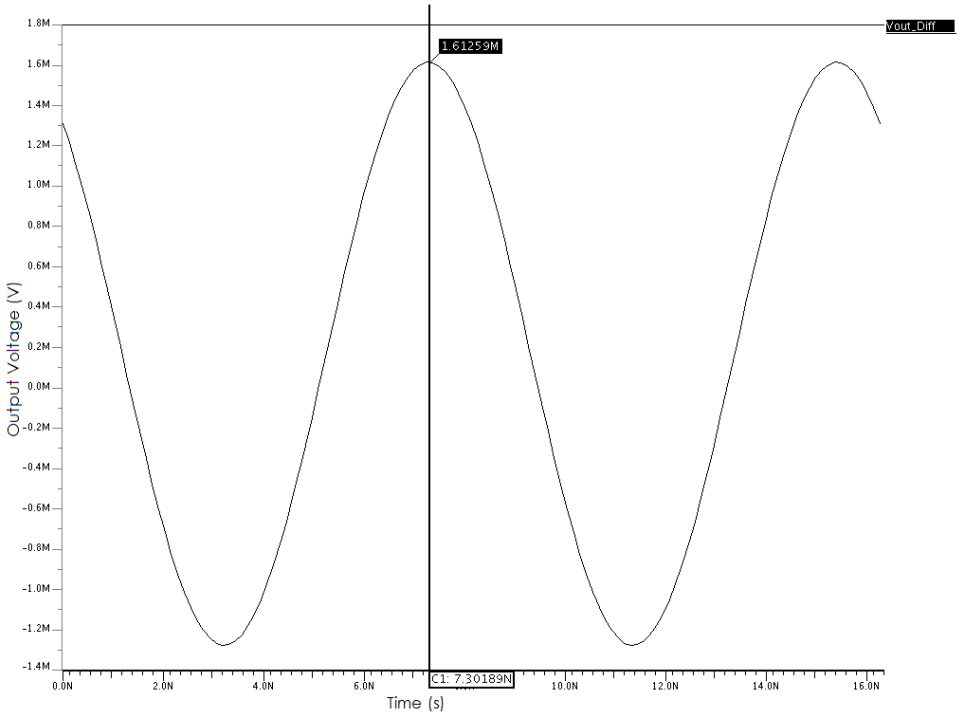


Figure 7.16. Post-Layout Transient Simulation of the FDFC LNA with PMOS Input Pair.

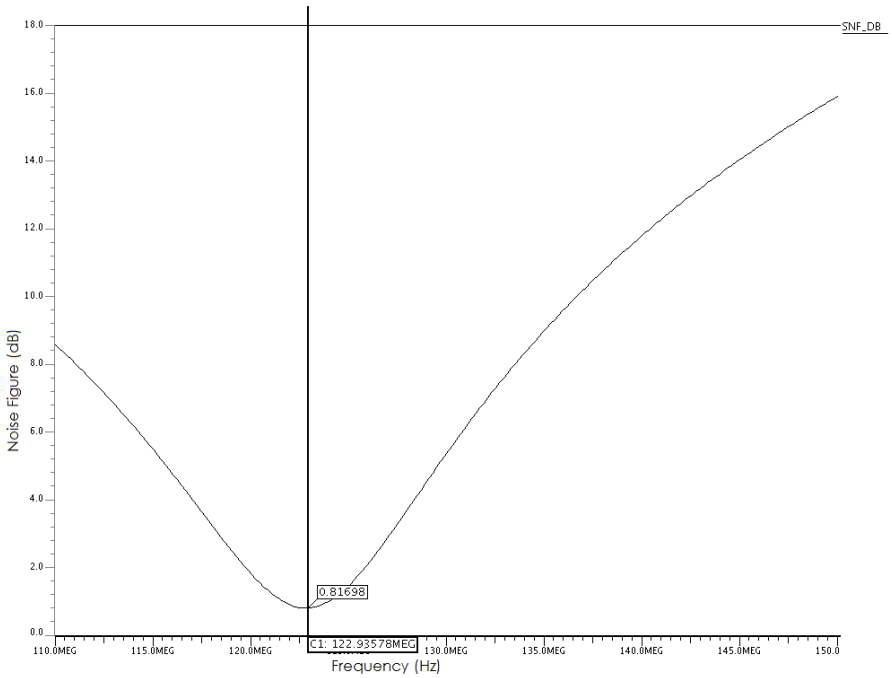


Figure 7.17. Post-Layout Noise Figure Simulation of the FDFC LNA with PMOS Input Pair.

7.1.3. Fully Differential CMOS LNA with PMOS Input Pair

This circuit is designed of CMOS topology with PMOS input pairs both in the first stage and second stage. Designed LNA is seen in Figure 7.18.

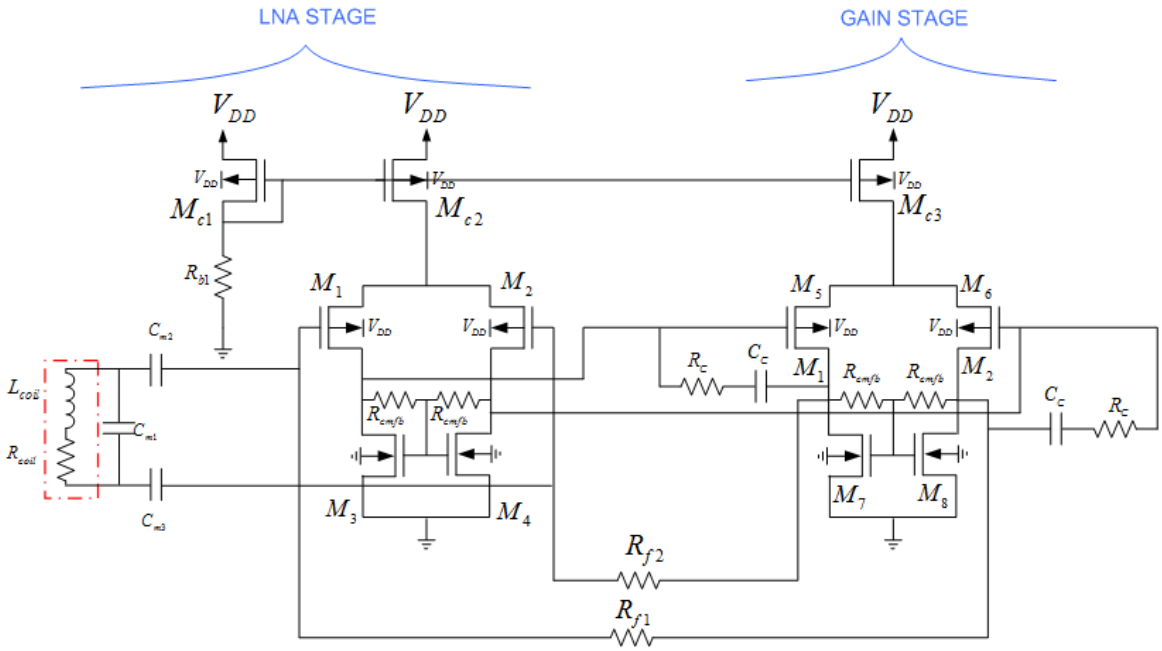


Figure 7.18. Fully Differential CMOS LNA with PMOS Input Pair.

Same circuit with NMOS input pairs has already been designed in [2] with different compensation technique. It is obvious from simulations given in Section 3.1.7 PMOS devices of 0.18 μm technology tend to have higher thermal noise. Designed circuit proves this point as explained below.

Gain of the two stages are calculated as explained in Section 6.3. First stage is biased with a current of 885 μA and 24.3 dB voltage gain is obtained. Second stage is biased with 276 μA and 3.6 dB voltage gain is obtained with the load resistance.

Table 7.4. Component Values of Fully Differential CMOS LNA with PMOS Input Pair.

$W/L_{1,2}$	310 μm/0.5 μm
$W/L_{3,4}$	20 μm/0.5 μm
$W/L_{5,6}$	70 μm/0.5 μm
$W/L_{7,8}$	10 μm/0.5 μm
$W/L_{M_{c1}}$	30 μm/0.5 μm
$W/L_{M_{c2}}$	380 μm/0.5 μm
$W/L_{M_{c3}}$	120 μm/0.5 μm
R_{b1}	12 kΩ
R_{cmfb}	10 kΩ
$R_{f1,f2}$	600 kΩ
R_C	100 kΩ
C_C	10 pF

Since there is no source followers in this design (DC levels of two stages are comparable) overall voltage gain becomes; A_v=24.3 dB+3.6 dB=27.9 dB. Consumed current is 1.2 mA which causes 1.44 mW power dissipation.

Input-referred noise of this LNA is defined as [18] in Equation 7.13. Note that $\gamma = 0.8$.

$$\overline{V^2_{CMOS\ LNA}} \simeq 4kT\ \Delta f \left[2\Big(0.8\frac{1}{g_{m1}} + 0.8\frac{g_{m3}}{(g_{m1})^2} + \frac{1}{R_{\text{cmfb}}\ g^2_{m1}} \Big) \right] \tag{7.13}$$

Input-referred noise of the LNA is 0.32 nV/$\sqrt{\text{Hz}}$. We do know that; to calculate the overall NF, we need to determine the input impedance of the LNA such that we can calculate voltage gain transferred to the input of the LNA from matching network. Z_{LNA} is simulated and found to be 604-1288j Ω. This finite input impedance results in 11.5$\simeq$21 dB voltage gain of matching network. Final NF is calculated 0.49 dB.

Miller compensation technique is applied to the circuit. (See Appendix A). For load capacitance calculations see Section 5.1.3. Simulation results can be seen in Figure 7.19 and 7.20.

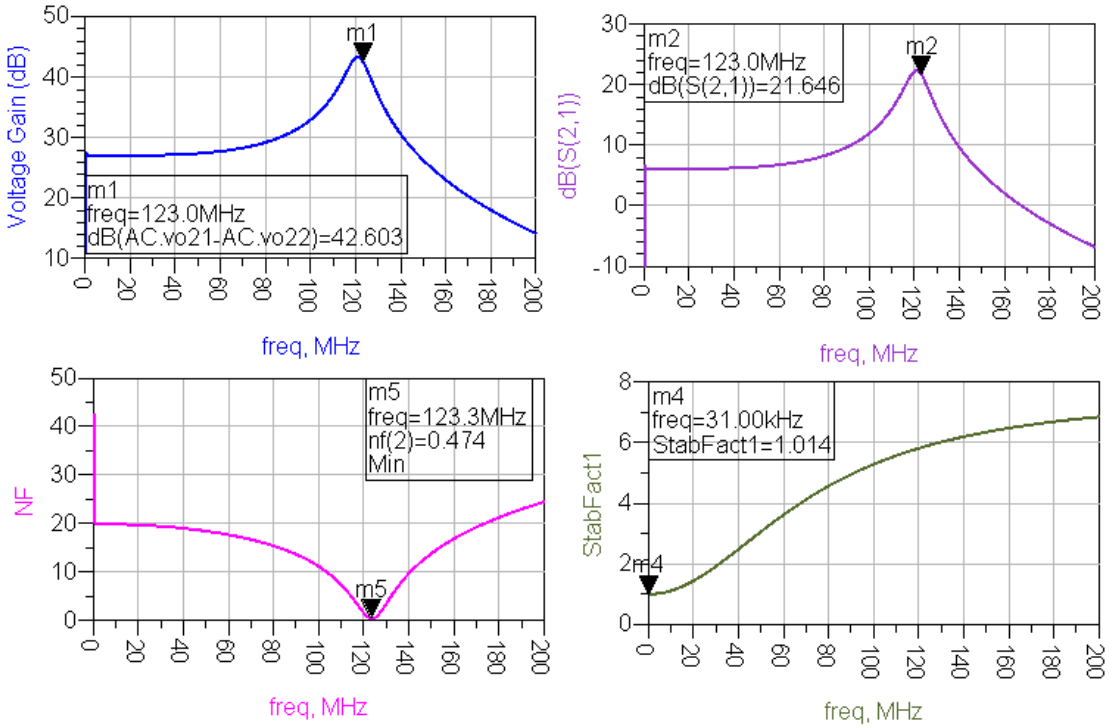


Figure 7.19. Simulation Results of Fully Differential CMOS LNA with PMOS Input Pair.

1-dB Compression Point

freq	inpwr	outpwr
0.0000 Hz	-37.32 dBm	-17.79 dBm
123.0 MHz	-37.32 dBm	-17.79 dBm
246.0 MHz	-37.32 dBm	-17.79 dBm
369.0 MHz	-37.32 dBm	-17.79 dBm

Figure 7.20. 1-dB Compression Point Simulation of Fully Differential CMOS LNA with PMOS Input Pair.

7.1.4. Fully Differential CMOS LNA with NMOS Input Pair

Same circuit seen in Figure 7.21 with different compensation and of course device sizes was designed in [2]. Actually throughout this section effects of current mirrors are searched. A fully differential circuit with low-voltage cascode current mirror is designed.

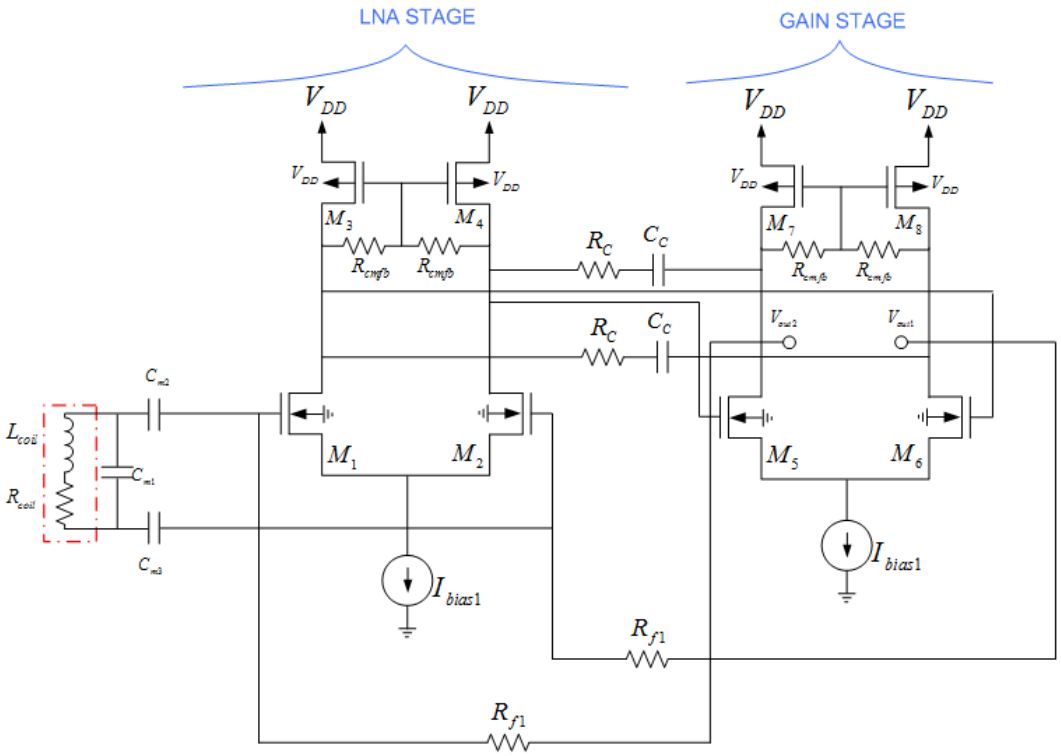


Figure 7.21. Fully Differential CMOS LNA with NMOS Input Pair.

7.1.4.1. Fully Differential CMOS LNA Biased with Basic Level-Shifted Current Mirror. Used current mirror is seen in Figure 7.22; and used component values are seen in Table 7.5. Details of the level-shifted current mirror was explained in Section 4.2.

LNA stage is biased with 946 μA, gain stage is biased with 189 μA. To obtain these currents a 240 μA reference current is used; which is really high for our power limit. On the other hand; 42.7 μA current is used to bias level shifter branch. Obtained results are calculated in Table 7.6.

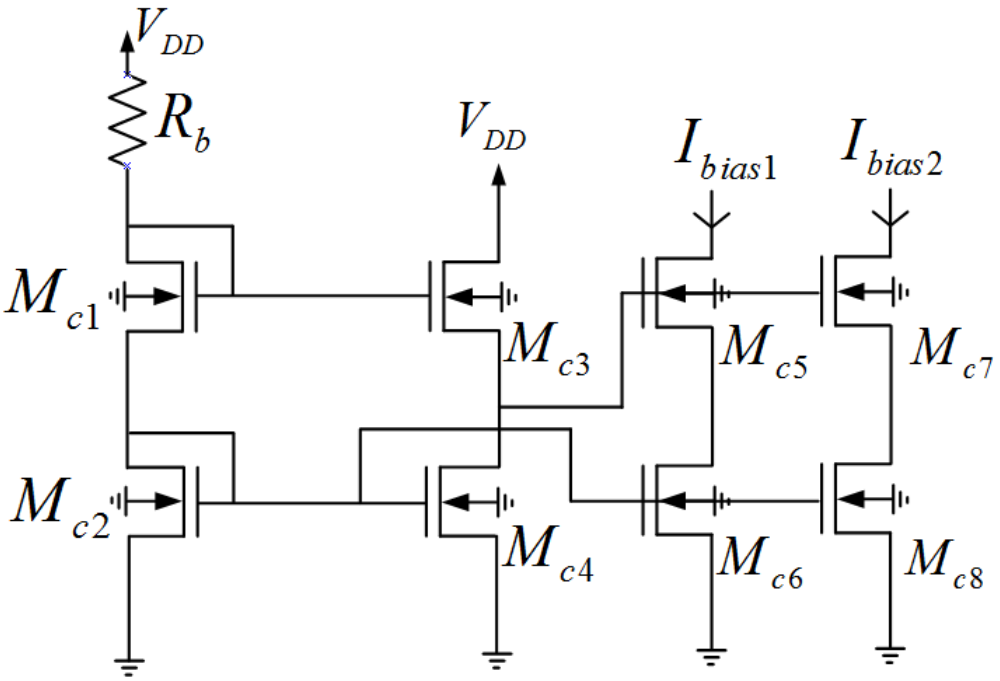


Figure 7.22. Basic Level-Shifted Cascode Curent Mirror.

Table 7.5. Component Values of Fully Differential CMOS LNA with NMOS Input Pair Biased with Basic Level-Shifted Current Mirror.

$W/L_{1,2}$	50 μm/0.5 μm
$W/L_{3,4}$	250 μm/0.5 μm
$W/L_{5,6}$	10 μm/0.5 μm
$W/L_{7,8}$	50 μm/0.5 μm
$W/L_{M_{c1,c2}}$	200 μm/0.5 μm
$W/L_{M_{c3,c4}}$	8 μm/0.5 μm
$W/L_{M_{c5}}$	8 μm/0.5 μm
$W/L_{M_{c6}}$	48 μm/0.5 μm
R_b	2 kΩ
R_{cmfb}	10 kΩ
$R_{f1,f2}$	600 kΩ
R_C	100 kΩ
C_C	10 pF

Table 7.6. Calculated results for the Fully Differential CMOS LNA Biased with Basic Level-Shifted Current Mirror.

$H_{v-1^{st}\ stage}$	$\simeq$ 23 dB
$H_{v-2^{nd}\ stage}$	$\simeq$ 1.2 dB
$H_{v-matching\ network}$	$\simeq$ 29 dB
$H_{v-over\ all}$	$\simeq$ 52.2 dB
Z_{LNA}	$\simeq$ 2930-6634j
$\overline{V^2_{CMOS\ LNA}}$	$\simeq$ 1.2 V/$\sqrt{\text{Hz}}$
NF	$\simeq$ 0.32 dB
$I_{consumed}$	= 1.42 mA
$P_{dissipated}$	= 1.7 mW

It is obvious from Table 7.6 that results does not provide a significant advantage of cascode current mirrors. Also with same currents obtained by basic current mirror; almost same results are observed as can be seen in Figure 7.25 and 7.26. This is not surprising, since current mirror's output resistance and capacitance is effective at common mode operation. As already explained in Section 5.1.2, there exists a virtual ground for differential signals, where current mirror is connected to the circuit. So, in terms of CMRR a cascode current mirror results better as seen in Figure 7.27.

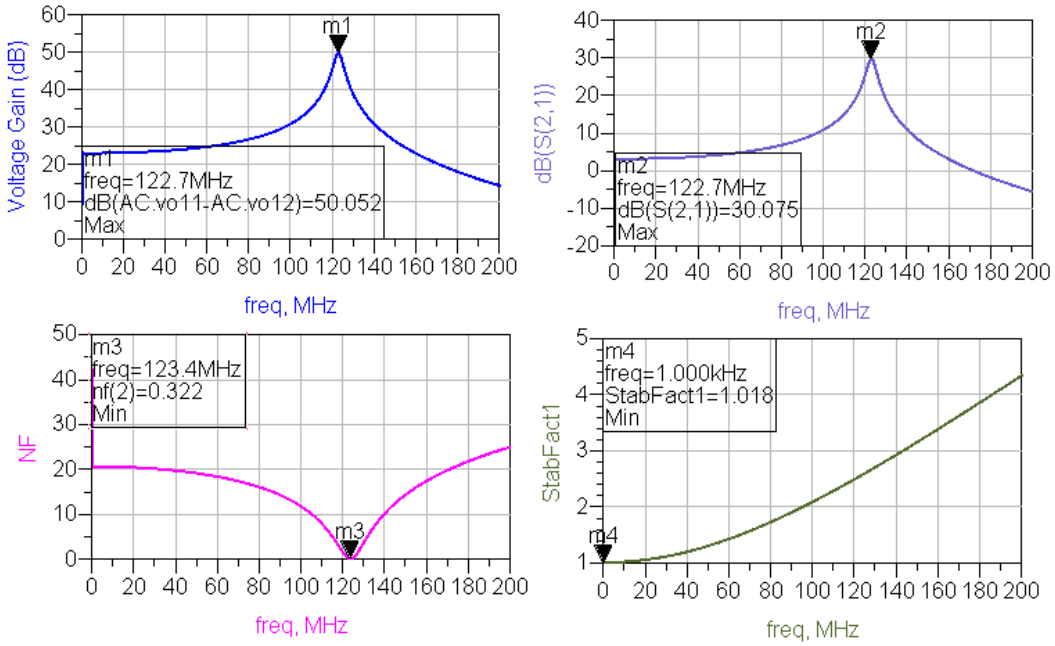


Figure 7.23. Simulation Result Set of CMOS LNA Biased with Basic Level-Shifted Current Mirror.

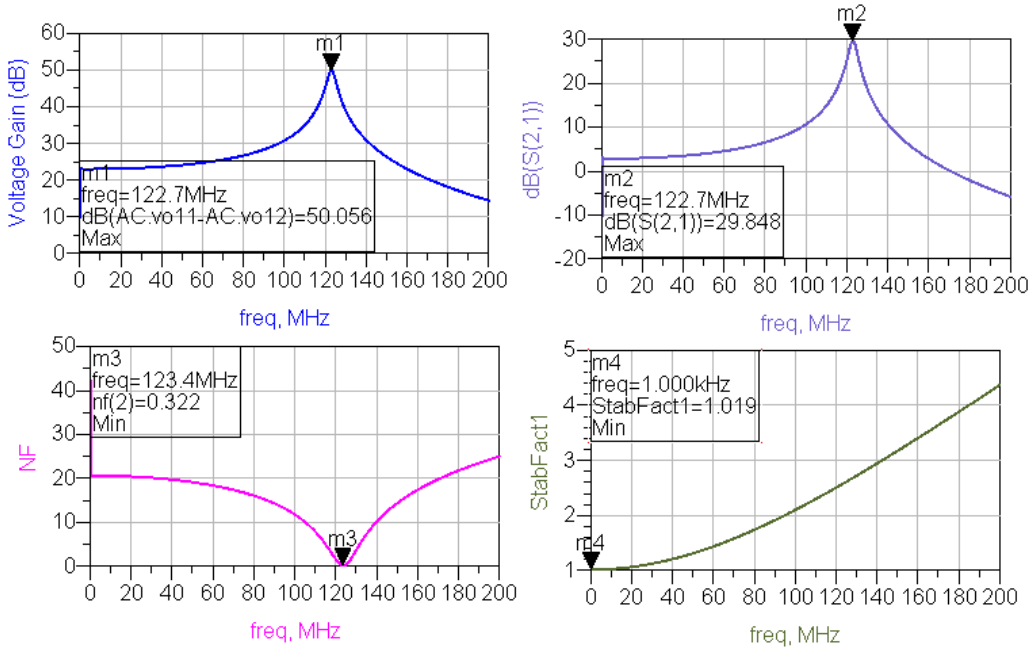


Figure 7.24. Simulation Result Set of Fully Differential CMOS LNA Biased with Basic Current Mirror.

1-dB Compression Point

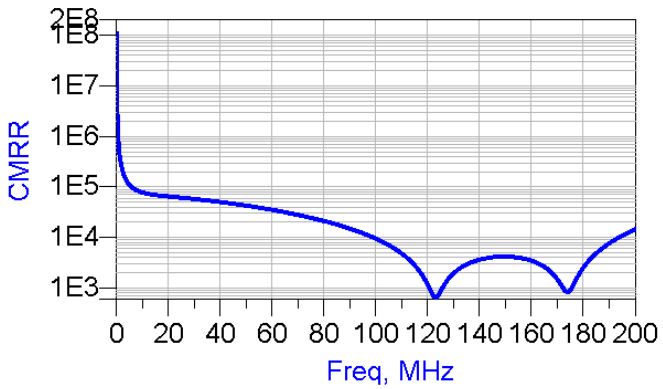
freq	inpwr	outpwr
0.0000 Hz	-38.85 dBm	-19.04 dBm
123.0 MHz	-38.85 dBm	-19.04 dBm

Figure 7.25. 1-dB Compression Point Simulation of CMOS LNA Biased with Basic Level-Shifted Current Mirror.

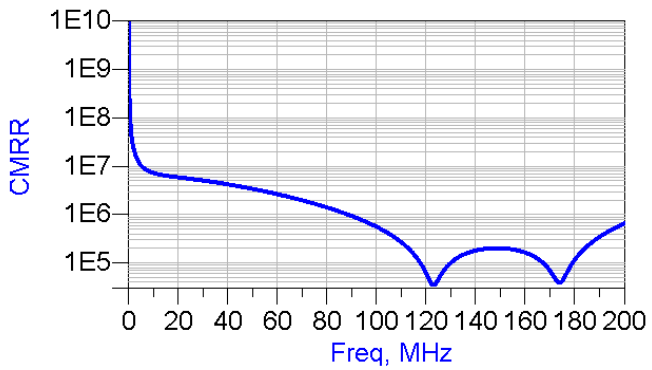
1-dB Compression Point

freq	inpwr	outpwr
0.0000 Hz	-38.83 dBm	-19.34 dBm
123.0 MHz	-38.83 dBm	-19.34 dBm

Figure 7.26. 1-dB Compression Point Simulation of CMOS LNA Biased with Basic Current Mirror.



(a) Biased with Basic Current Mirror.



(b) Biased with Basic Level-Shifted Current Mirror.

Figure 7.27. CMRR Simulation of Fully Differential CMOS LNA.

8. CONCLUSIONS

Four different LNAs are designed to meet an optimum point for our design specs. Layouts are drawn for two of these designs, and one of these layouts (Layout of the FDFC LNA with NMOS Input Pair) is sent to fabrication. Related mathematical analysis and simulations are done. Simulations and calculations are in 93% match.

We require minimum obtainable NF which can be done via high input impedance of the LNA. Large devices tend to have less noise, although their impedance is lower compared to their smaller counterparts. If designer have an antenna with a good quality factor and low intrinsic resistance, high input impedance should be major aim for a good NF performance which was our case. But if antenna does not provide a good performance in terms of quality factor and intrinsic resistance, larger devices should be preferred for minimum input-referred noise. Actually this was the main reason why PMOS input pairs provided worsened NF matching. In order to obtain comparable voltage gain with PMOS input pairs, they need to be large enough due to lower mobility of positive carriers.

On the other hand; higher currents provides higher output resistances which increases voltage gain and decreases NF, whereas it is limited by power limits of the low-voltage low-power applications. This problem can be solved by folded-cascode topology which provides higher gain compared to its CMOS differential counterpart. If a larger DC-supply voltage would be available; a cascode active load can be used in FDFC LNAs which would lead even higher gain. But because of our limited DC-supply this method would limit output swing and linearity of the LNA, so we could not use it.

Another main consideration would be chip area which is limited mostly by compensation capacitors. Chip area was not one of the limits of this thesis; but FDFC LNA with PMOS input pair provides a better area performance since it is compensated via source followers.

CMRR is mostly neglected by designers as long as it converges to infinity compared to the differential voltage gain. Biasing current mirror with high output impedances produce a better CMRR. But CMRR provided by the basic current mirror is also high enough for most designs including this one.

In Table 8.1 comparison of the designed LNAs is done.

Table 8.1. Comparison of Designed LNAs.

Spec	D1	D2	D3	D4	D5
NF	√	X	X	√	X
Power Dissipated	X	X	√	X	X
Linearity	√	√	√	X	√
GAIN	√	√	X	X	X
CMRR	X	X	X	√	X
Chip Area	X	√	X	X	√

FDFC LNA with NMOS Input Pair : D1
FDFC LNA with PMOS Input Pair : D2
Fully Differential CMOS LNA with PMOS Input Pair : D3
Fully Differential CMOS LNA Biased with Basic Level-Shifted Current Mirror : D4
Fully Differential CMOS LNA Biased with Current Mirror Designed in [2] : D5

Consequently; FDCFC LNA with NMOS/PMOS input pair are chosen to be the optimum designs for our specs, since it has better noise matching while providing higher gain.

APPENDIX A: EFFECT OF Z_{LNA} IN NOISE MATCHING

Consider the given Figure A.1. Z_{C2} and Z_{C3} are impedances of DC block capacitors. If C_2 and C_3 are chosen to be infinite; then their impedances will be zero and the will not effect the overall gain. As already mentioned; if we can obtain $Z_{LNA} = \infty$, transferred voltage gain of the matching network will be equal to Q. (Section 3.1.7)

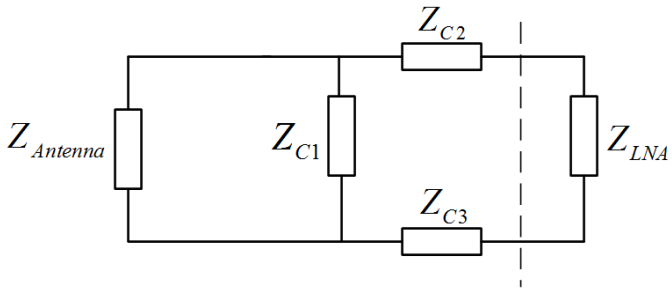


Figure A.1. Equivalent Circuit of Noise Matching Network with Finite Z_{LNA} Included.

Now a simplified circuit shown in Figure A.2 is used where C_2 and C_3 are short circuited and an input voltage is added to calculate the gain of matching network.

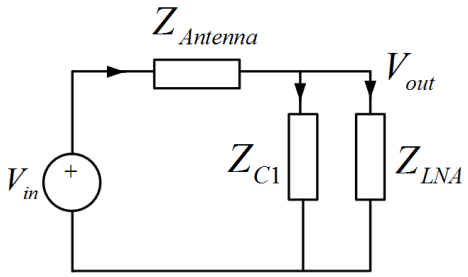


Figure A.2. Equivalent Circuit of Noise Matching Network with Finite Z_{LNA} Included and DC-Block Capacitors are Short Circuited.

If Kirchoff's current law is applied to the output node, gain of the circuit can easily be obtained.

$$H_v = \frac{Z_{C1}Z_{LNA}}{Z_{C1}Z_{LNA} + Z_{Antenna}Z_{LNA} + Z_{C1}Z_{Antenna}} \tag{A.1}$$

APPENDIX B: MILLER COMPENSATION

In Figure B.1 equivalent circuit for a two stage amplifier is considered.

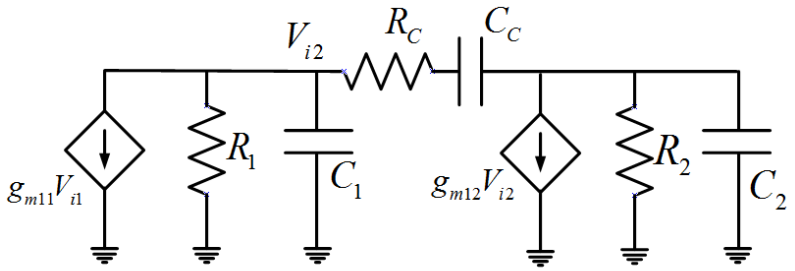


Figure B.1. Equivalent Circuit of Two Stage Amplifier.

If we consider $R_c = 0$, transfer function becomes

$$\begin{aligned} A_{fc}(s) &= \frac{-(g_{m1} - sC_1)R_{out}}{bs^2 + as + 1} \\ P(s) &= bs^2 + as + 1 = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right). \end{aligned} \tag{B.1}$$

where R_1 and R_2 are output resistances, C_1 and C_2 are output capacitances of first and second stages respectively. p_1 is the dominant pole and p_2 is the non-dominant pole of the system and they are defined as [8]

$$p_1 = \frac{1}{g_{m12}R_1R_2C_c} \tag{B.2}$$

$$p_2 = \frac{g_{m12}}{C_1 + C_2}. \tag{B.3}$$

Also there exists a zero at $z = g_{m11}/C_1$. To eliminate this zero R_c is added such that new zero becomes

$$\omega_z = \frac{1}{C_c(1/g_{m12} - R_c)}.$$

REFERENCES

1. Schulz, T., J.P. Schneider, W. Hirsch, S. Puccini, F. Schmidt and T. Kahn, "Pediatric MR-guided Interventions", *European Journal of Radiology*, vol. 53, no. 1, pp. 57-66, 2005.

2. Aktan, O., *The Design and Aspects of an Optically Powered CMOS Receiver Front-End for Electrically Isolated Applicaitons*, PhD. Thesis, Boğaziçi University, 2011.

3. Wattanapanitch, W., M. Fee and R. Sarpeshkar, "An Energy-Efficient Micropower Neural Recording Amplifier", *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, p. 2, 2007.

4. Corsi, F., C. Marzocca, "An Approach to the Analysis of the CMOS Differential Stage With Active Load and Single-Ended Output", *IEEE Transactions on Education*, vol. 46, p. 3, 2003.

5. Bazes, M., "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", *IEEE Solid-State Circuits*, vol. 26, p. 2, 1991.

6. Sun, N., Y. Liu, H. Lee, R. Weissieder and D. Ham, "CMOS RF Biosensor Utilizing Nuclear Magnetic Resonance", *IEEE Journal of Solid-State Circuits*, vol. 44, p. 5, 2009.

7. Bushong, S. C., *Magnetic Resonance Imaging*, 2^{nd} ed., Mosby-Year Book, U.S.A, 1996.

8. David, J., M. Ken, *Analog Integrated Circuit Design*, University of Toronto Press, 2000.

9. Gonzales, G., *Microwave Transistor Amplifiers*, 2^{nd} ed., Prentice Hall, 1996.

10. Lee, T.H., *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, U.S.A., 1998.

11. Gray, P. R., P. J. Hurst, S. H. Lewis and R. G. MEYER, *Analysis and Design of Analog Integrated Circuits*, 4^{th} ed., LeihghPress, U.S.A., 2001.

12. Sedra, A. S., K. C. Smith, *Microelectronic Circuits*, 5^{th} ed., Oxford University Press, New York, 2004.

13. Babanezhad, J. N., "A Low-output-impedance Fully Differential OPAMP with Large Output Swing and Continuous-time Common-Mode Feedback", *IEEE J. Solid-State Circuits*, vol. SC-26, no. 12, pp. 1825-1833, 1991,

14. Czarnul, Z., S. Takagi and N. Fujii, "Common-mode Feedback Circuit with Differential-Difference Amplifier", *IEEE Trans. Circuits Systems I*, vol. 41, no. 3, pp. 243-246, 1994.

15. Bowick, C., *RF Circuit Design*, Newnes, 1997.

16. Bhargav, S., J. Peretzman, *Design of a MOS double casode Op-Amp with* 61 *dB of gain and* 128 MHz *of unity gain bandwidth for a Low-Pass Filter application*, ELEN 4321, Analog Electronics Circuits, Columbia University, 2007.

17. Alen, P. E., D. R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, U.S.A., 2002.

18. Sansen, W.M.C., *Analog Design Essentials*, Springer, 2006.

19. Hastings, A., *The Art of Analog Layout*, Prentice Hall, 2001.

20. Cherifi, T., N. Abounchi, G. Lu, L. Fakri, L. Quiquerez, J. F. Chataeaux and P. Morin, "A CMOS Microcoil-Associated Preamplifier for NMR Spectroscopy", *IEEE Transactions on Circuits and SystemsI*: Regular Papers, vol. 52, p. 12, 2005.

21. Fan, X., H. Zhang and E. Sánchez-Sinencio, "A Noise Reduction and Linearity Improvement Technique for a Differential Cascode LNA", *IEEE Journal of Solid-State Circuits*, vol. 43, p. 3, 2008.

22. Fandrey, S., S. Weiss, J. Müller, "Development of an Active Intravascular MR Device With an Optical Transmission System", *IEEE Transactions on Medical Imaging*, vol. 27, p. 12, 2008.

23. Harrison, R.R., C. Charles, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications", *IEEE Journal of Solid-State Circuits*, vol. 38, p. 6, 2003.

24. Hu, Y., M. Sawan, "CMOS Front-end Amplifier Dedicated to Monitor Very Low Amplitude Signal from Implantable Sensors", *Analog Integrated Circuits and Signal Processing*, Kluwer Academic Publishers. Manufactured in The Netherlands, 2002.

25. Lundberg, K. H., "Internal and External Op-Amp Compensation: A Control-Centric Tutorial", *American Control Conference*, U.S.A., 2004.

26. Moreno, R.L., E. C. Rodriguf, *A CMOS Low Noise Amplifier for Biomedical Telemetry Applications*, Design, Test, Integration 8 Packaging of MEMS/lMOEMS, 2003.

27. Ock, S., K. Han and J. Ryul, *A Modified Cascode Type Low Noise Amplifier Using Dual Common Source Transistors*, IEEE, 2002.

28. Pernici, S., G. Nicollini and R. Castello,"A CMOS Low-Distortion Fully Differential Power Amplifier with Double Nested Miller Compensation", *IEEE J. Solid-State Circuits*, vol. 28. p., 1993.

29. Steyaert, M., S. Willy and A. Zhongyuan, "A Micropower Low-Noise Monolithic Instrumentation Amplifier for Medical Purposes", *IEEE Journal of Solid-State Circuits*, vol. sc-22, p. 6, 1987.

30. Szczepański, S., S. Kozieł, "Phase Compensation Scheme for Feedforward Linearized CMOS Operational Transconductance Amplifier", *Bulletin of the Polish Academy of Sciences, Technical Sciences*, vol. 52, p. 2, 2004.

31. Youssef, A. A., "Design Guidelines for the Noise Optimization of a 0.18 μm CMOS Low-Noise Amplifier", *Analog Integrated Circuits and Signal Processing*, Springer Science and Business Media, Inc. Manufactured in The Netherlands, 2006.