REALIZATION AND MODELING OF WATER-GATED FIELD EFFECT TRANSISTORS (WG-FET) USING 16-NM-THICK SINGLE CRYSTALLINE SILICON FILM AND THEIR CIRCUIT APPLICATIONS

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ABSTRACT

REALIZATION AND MODELING OF WATER-GATED FIELD EFFECT TRANSISTORS (WG-FET) USING 16-NM-THICK SINGLE CRYSTALLINE SILICON FILM AND THEIR CIRCUIT APPLICATIONS

This thesis covers realization and modeling of novel water-gated field effect transistors (WG-FETs) which use 16-nm-thick single crystalline silicon film as active layer. WG-FET devices utilize electrical double layer (EDL) structure as a replacement of gate insulator and operate in the non-Faradaic region (under 1 V) without causing any oxidation/reduction reactions. Performance parameters based on voltage distribution on EDL are extracted and current-voltage relations are modeled. Various WG-FET devices with both probe- and planar-gate setups are simulated, fabricated and tested. Effects of gate distance, gate topology, field and source/drain electrode insulation on transistor performance are investigated. Best ON/OFF ratios are measured with probe-gate devices for both insulated and uninsulated source/drain electrodes. Performance of probe-gate devices with uninsulated source/drain electrodes are superior to the ones with insulated source/drain due to absence of parasitic resistances related with the overlapping area of insulation layer. Planar-gate devices with source/drain insulation have lower ON/OFF ratios compared to probe-gate counterparts and device performance tends to deteriorate with increasing gate distance. Without source/drain electrode insulation, proper transistor operation is not obtained with planar-gate devices. Measurement results are in agreement with theoretical models. Inverters and ring oscillators are realized as circuit applications. WG-FET is a promising device platform for microfluidic applications where sensors and read-out circuits can be integrated at transistor level.

ÖZET

16 NM KALINLIĞINDA TEK KRİSTALLİ SİLİSYUM FİLM KULLANAN SU-KAPILI ALAN ETKİLİ TRANZİSTÖRLERİN GERÇEKLENMESİ MODELLENMESİ VE DEVRE UYGULAMALARI

Bu tezde 16 nm kalınlığında tek kristalli silisyum film kullanan su-kapılı alan etkili tranzistörlerin (WG-FET) gerçeklenmesi ve modellenmesi ele alınmıştır. WG-FET aygıtları elektriksel çift katman (EDL) yapısını kapı yalıtkanı olarak kullanırlar ve non-Faradaik rejimde (1 V altı) yükseltgenme/indirgenme reaksiyonlarına sebebiyet vermeden çalışırlar. EDL üzerindeki voltaj dağılımına dayanan performans parametreleri çıkartılarak akım-voltaj ilişkileri modellenmiştir. Çeşitli WG-FET aygıtları hem prob- hem de düzlemsel-kapılı sistemlerle simule edilmiş, üretilmiş ve test edilmiştir. Kapı uzaklığı, kapı şekli, alan ve kaynak/savak elektrodlarının yalıtımının tranzistör performansı üzerindeki etkileri incelenmiştir. En iyi $AÇIK/KAPALI$ oranları hem yalıtılmış hem de yalıtılmamış kaynak/savak elektrotları ile prob-kapılı aygıtlarda ölçülmüştür. Yalıtılmamış kaynak/savak elektrotlu prob-kapılı aygıtların performansı, yalıtım katmanının aktif alanı örtmesi sonucu oluşan parazitik dirençlerin olmaması nedeniyle, yalıtılmış kaynak/savak elektrotlu benzerlerine göre üstündür. Düzlemsel-kapılı yalıtılmış kaynak/savak elektrotlu aygıtlar, prob-kapılı benzerlerine göre daha düşük $AÇIK/KAPALI$ oranlarına sahiptir ve aygıt performansı artan kapı uzaklığı ile kötüleşme eğilimindedir. Kaynak/savak elektrot yalıtımı olmadığında, düzlemsel-kapılı aygıtlarda düzgün tranzistör davranışı elde edilememiştir. Ölçüm sonuçları teorik modellerle uyumludur. Eviriciler ve halka salınıcılar, aygıt uygulamaları olarak gerçeklenmiştir. WG-FET, sensörlerin ve okuma devrelerinin tranzistör seviyesinde entegrasyonuna imkan veren, mikroakışkan uygulamaları için gelecek vadeden bir aygıt platformudur.

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LIST OF SYMBOLS

Ag	Silver
AgCl	Silver chloride
Al	Aluminum
Al_2O_3	Aluminum oxide
Au	Gold
C_d	Differential capacitance
C_{EDL}	Capacitance of EDL
C_{GC}	Gouy-Chapman capacitance
C_H	Helmholtz capacitance
C_i	Capacitance per unit area
C_{OX}	Oxide capacitance per area
Cl	Chlorine
CO_2	Carbon dioxide
Cu	Copper
d	Insulator thickness
e	Electronic charge
E_B	Energy bandgap
E_c	Semiconductor conduction band
E_{Fm}	Metal Fermi level
E_{Fs}	Semiconductor Fermi level
E_i	Semiconductor intrinsic level
E_{ref}	Potential of reference electrode
E_v	Semiconductor valence band
HNO_3	Nitric acid
H_2O	Water
HfO_2	Hafnium dioxide
I_0	Ion concentration in mol/L
I_D	Channel current

$I_{D,max}$	Maximum channel current
$I_{D,res}$	Channel current in resistive region
$I_{D,sat}$	Channel current in saturation region
I_{DS}	Drain to source current
I_{OFF}	Off current
I_{ON}	On current
k_B	Boltzmann's constant
L	Channel length
n	Electron density
N_a	Doping concentration of p-type semiconductor
n_i	Concentration of ion i; intrinsic concentration
n_i^0	Bulk ion concentration
NaCl	Sodium chloride
NH_4	Ammonium
NH_4F	Ammonium fluoride
p	Hole density
Pt	Platinum
Q_{acc}	Accumulation charge
Q_B	Accumulated charge in the depletion region
Q_{OX}	Accumulated charge on the oxide
Q_S	Gate-induced charge-carrier density
Q_{SS}	Accumulated charge at the oxide/Si interface
R_{px}	Series parasitic resistance
Si	Silicon
SiO_2	Silicon dioxide
Si_3N_4	Silicon nitride
T	Absolute temperature
t_f	Fall time
t_r	Rise time
Ta_2O_5	Tantalum pentoxide
V	Potential difference

V_{BS}	Bulk to source voltage
V_{DD}	Supply voltage
V_{DS}	Drain to source voltage
V_{g_EDL}	Potential on EDL
V_{GS}	Gate to source voltage
V_i	Applied voltage on insulator
V_{IH}	Input high voltage
V_{IL}	Input low voltage
V_{IN}	Input voltage
V_M	Switching threshold voltage
V_{OH}	Output high voltage
V_{OL}	Output low voltage
V_{OUT}	Output voltage
V_{th}	Threshold voltage
V_{thc}	Threshold constant
W	Channel width
Y_2O_3	Yttrium(III) oxide
z_i	Signed charge of ion i
ZrO_2	Zirconium dioxide
β_S	Surface buffer capacity
δ	Parallel plate separation distance
ϵ_0	Permittivity of free space
$\mathcal{E}_i$	Applied electric field
ϵ_i	Permittivity of insulator
$\mathcal{E}_{ox}$	Electric field in the oxide
ϵ_{ox}	Relative permittivity of oxide
ϵ_r	Relative permittivity
$\mathcal{E}_{Si}$	Electric field on the semiconductor surface
ϵ_{Si}	Relative permittivity of Si
κ	Dielectric constant; Debye-Hückel parameter

λ_D	Debye screening length
μ_n	Electron mobility in Si
μ_p	Hole mobility in Si
ρ	Total charge per volume
σ	Stored charge density
σ_E	Charge density of electrolyte
σ_S	Surface charge
$\varPhi_B$	Schottky barrier potential
ϕ_F	Fermi potential
$\varPhi_m$	Electrostatic potential of metal with respect to oxide
$\varPhi_s$	Electrostatic potential of sc with respect to oxide
$\varPhi_{Si}$	Work function of Si
χ_s	Electron affinity of semiconductor
χ^{sol}	Surface dipol potential of the solvent
ψ	Potential function with respect to bulk
ψ_{bulk}	Bulk potential
ψ_S	Surface potential with respect to bulk electrolyte
ψ_δ	Stern potential

LIST OF ACRONYMS/ABBREVIATIONS

2DEG	Two-Dimensional Electron Gas
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
EDL	Electric Double Layer
EDLC	Electric Double Layer Capacitance
EDLT	Electric Double Layer Transistor
FET	Field Effect Transistor
GCS	Gouy-Chapman-Stern
ISFET	Ion-Sensitive Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OFET	Organic Field Effect Transistor
P3HT	Polythiophene
PEG	Poly(Ethylene Glycol)
PR	Photoresist
SOI	Silicon-On-Insulator
TFT	Thin Film Transistor
TMAH	Tetramethylammonium Hydroxide
VNM	Voltage Noise Margin
WG-FET	Water-Gated Field Effect Transistor
WGOFET	Water-Gated Organic Field Effect Transistor

1. INTRODUCTION

Despite the unlucky debut in 1948, field-effect devices started to become popular in the market in 1970s with the integrated-circuit concept. Especially metal-oxide-semiconductor field-effect-transistors (MOSFET) made the integrated-circuit process comparably easy. Then, it took barely a decade the silicon MOSFET to dominate the market. [1] Since then, MOSFET technology has been used in almost all electronic devices.

In MOSFETs, single crystalline silicon has been used as semiconductor material. It has a natural oxide, SiO_2, which makes the production easier. However, today's needs challenge the current MOSFET technology in many ways. Device dimensions are shrinking to improve cost, speed and power per function. As channel length scales down, oxide thickness should also decrease to handle channel control. [2] Yet, gate oxide thickness for 90 nm channel is approximately 2 nm. For further development, SiO_2 will not suffice and other insulator materials with higher dielectric constants should be used which requires more difficult and costly processes. [3]

High performance issues are not the only challenging factor for MOSFET technology. For several applications like wide displays, sensors or disposable detectors, mediocre performance is acceptable as long as production cost stays low enough. Conventional MOSFET production facilities are not suitable for such devices. Thin film transistors (TFTs) are proposed as a solution to this problem. They use amorphous Si layers instead of single crystalline ones, [4] which decreases production cost in some degree. However, the resultant performance deterioration is drastic. Electron mobility value is approximately 4 cm^2/Vs in TFTs which is really poor compared to 1500 cm^2/Vs of the single crystalline case. Utilization of organic semiconductor materials decreases production cost further. Cheap process methods which include spin-coating, inkjet-printing and drop-casting make organic and polymer semiconductors better options especially for large area applications and disposable devices. [5–7] Their electrical conductivity is greatly affected by environmental factors. Although this can

be considered as a drawback for conventional MOSFET technology, it turns out to be a great advantage for sensing applications. [8, 9] However, performance is even lower in these devices. Despite the fact that charge carrier mobilities around 5 cm^2/Vs are reported for organic semiconductor pentacene, [10] general trend is around 1 cm^2/Vs for organic ones and 0.1 cm^2/Vs for polymer ones.

Technological progress requires different ways for development, because natural limits for current technology are almost reached. SiO_2 gates cannot be made thinner and other high-κ materials are increasing cost and process complexity. Some cheap and flexible ways are needed for making transistors with high performance and application flexibility which is the motivation for this thesis.

Here, a novel water-gated field effect (WG-FET) device is introduced. It combines the high performance of single crystalline silicon with cheap fabrication techniques. Electric double layer is used as gate insulator which provides an ultra-thin dielectric layer with a relatively high dielectric constant. Devices are fabricated with lithographic techniques using SOI wafers. Therefore, they are also compatible with existing MOSFET fabrication facilities. Moreover, WG-FET device has a fluidic interface on top of the Si channel area which can be exploited for sensor applications. These features make WG-FET a flexible device platform especially for applications which involve electronic circuits and sensory parts.

In this work, WG-FET devices are investigated in detail.Their operation principles are explained and theoretical models are obtained. Fabrication steps are demonstrated for various device topologies. Electrical measurements are performed for fabricated samples and compared with theoretical results. Effects of environmental and structural variations on transistor performance are examined. Also, some circuit applications of WG-FET devices are demonstrated.

Outline of the thesis is as follows:

Chapter 2 details the physical background of the work. EDL concept and its theoretical modeling approaches are analyzed. EDL-based devices and their applications are also investigated.

Chapter 3 extensively explains the WG-FET concept. Motivation behind the device design is stated. Fabrication process is explained in detail. Experimental measurement results are given for various WG-FET devices. Mathematical models are proposed and compared with experimental data.

Chapter 4 discusses some circuit applications of WG-FET. Inverter and ring oscillator circuits are implemented, and characterized.

Chapter 5 summarizes and concludes this thesis. Possible developments and future work on the topic are discussed.

2. BACKGROUND

When we apply Gauss' law on the channel region of a MOSFET, gate-induced charge-carrier density at the channel, Q_S, can be written as

$$Q_S = -\epsilon_i \mathcal{E}_i \tag{2.1}$$

where ϵ_i is the permittivity of the insulator and $\mathcal{E}_i$ is the applied electric field. If we replace $\mathcal{E}_i$ with V_i/d where V_i is the applied voltage on insulator layer and d is the insulator thickness, it can be seen that charge-carrier density is directly proportional to ϵ_i and inversely proportional to d. For an insulator, ϵ_i/d ratio stands for the capacitance per unit area, C_i. Therefore, we can rewrite Equation 2.1 as

$$Q_S = -C_i V_i. \tag{2.2}$$

For a constant applied voltage, gate-induced carrier density increases with increasing insulator capacitance.

One way of increasing insulator capacitance is decreasing its thickness. With advancing technology nodes, SiO_2 layers got thinner and thinner in MOSFET fabrication. However, ultra-thin SiO_2 films are prone to dielectric breakdown at lower voltages due to their relatively low electric breakdown field (<10 MV/cm), [11] and have high leakage currents (>1 A/cm^2 at 1 V) due to electron tunneling. [12]

Another way of enhancing insulator capacitance is to use high-κ dielectrics. [13] These materials have higher dielectric constants than that of SiO_2 (i.e. $\epsilon_r > 3.9$). Metal oxides like ZrO_2 ($\epsilon_r \approx 23$), HfO_2 ($\epsilon_r \approx 20$), Y_2O_3 ($\epsilon_r \approx 15$), and Al_2O_3 ($\epsilon_r \approx 10$) can be used as high-κ dielectrics. [14] To obtain better interfaces between insulators and Si, silicates of those materials like $(HfO_2)_x(SiO_2)_{1-x}$ are used. Yet, using high-κ dielectrics requires more complicated fabrication techniques compared to SiO_2. Also, Coulomb scattering due to interface traps and phonon scattering due to high dielectric

constant of the insulator result in lower charge-carrier mobility. [15, 16]

An interesting and cheap way of obtaining a thin dielectric layer with high capacitance is using electric double layer (EDL) as gate insulator. When there is an electrolyte between the gate electrode and the channel layer in contact with both, EDLs are formed at solid/electrolyte surfaces. They behave like nano-gap parallel plate capacitors with high dielectric constants. By controlling the applied voltage on gate electrode, charge-carrier density in the channel can be controlled. Extremely large electric fields can be generated on EDLs which are not possible to obtain with solid insulators due to dielectric breakdown. [17, 18] By using EDLs, charge-carrier densities higher than 10^{14} cm^{-2} can be achieved. [19, 20]

2.1. Electric Double Layer (EDL)

2.1.1. Helmholtz Model

When a charged solid surface is immersed into an electrolyte, counter-ions are attracted to the surface to maintain electroneutrality, while co-ions are pushed into bulk liquid. Therefore, a structure which consists of two layers with opposite charges emerges at the solid/electrolyte interface. This phenomenon was first explained by Hermann von Helmholtz. [21] In Helmholtz model, counter-ions in the vicinity of solid surface form a fixed sheet of charge as given in Figure 2.1. He described the double layer system as a parallel plate capacitor with a thickness of counter-ion radius. For this capacitor, stored charge density, σ, is calculated as

$$\sigma = \frac{\epsilon_r \epsilon_0}{\delta} V \tag{2.3}$$

where ϵ_r is the dielectric constant of the electrolyte, ϵ_0 is the permittivity of free space, δ is the parallel plate separation distance, and V is potential difference between plates.

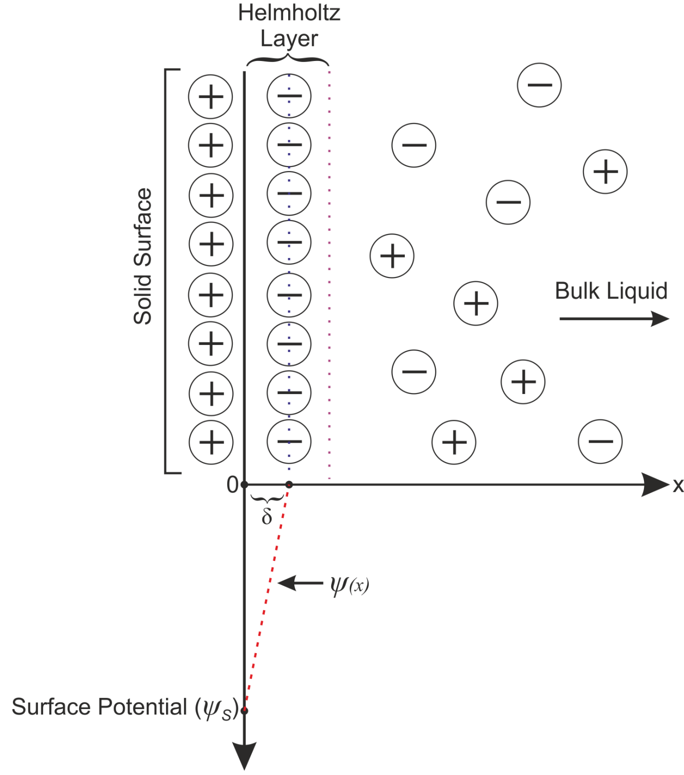

Figure 2.1. EDL structure in Helmholtz model. $\psi(x)$ is the potential at distance x.

Capacitance is defined as stored charge per applied voltage, or surface charge in response to perturbation in surface potential. [22] Latter is called differential capacitance, C_d, and it is used in characterization of non-linear capacitors. For linear systems, two definitions are equivalent. Differential capacitance can be written as

$$C_d = \frac{\partial \sigma_S}{\partial \psi_S} \tag{2.4}$$

where σ_S is the surface charge and ψ_S is the surface potential with respect to bulk electrolyte. Therefore, C_d for Helmholtz model can be calculated as

$$C_d = \frac{\partial \sigma}{\partial V} = \frac{\epsilon_r \epsilon_0}{\delta}. \tag{2.5}$$

From Equation 2.5, it can be seen that C_d of EDL is constant in Helmholtz model, and it only depends on the dielectric constant of the electrolyte and ionic radius of the counter-ion.

2.1.2. Gouy-Chapman Model

Louis Georges Gouy [23] and David Leonard Chapman [24] independently reported that the differential capacitance of EDL is not constant as Helmholtz model suggested, but a function of the surface potential and the ionic concentration of the electrolyte. In a solid/liquid interface, charge of the solid part is confined on the solid surface. This situation does not hold for the liquid part because of Brownian motion. While electrostatic forces attract counter-ions to interface in the electrolyte, Brownian motion imposes a randomized distribution. Therefore, ionic charge needed to neutralize the surface charge of the solid part disperses into a finite distance in the liquid as depicted in Figure 2.2. This diffused layer is the main characteristic of the Gouy-Chapman model.

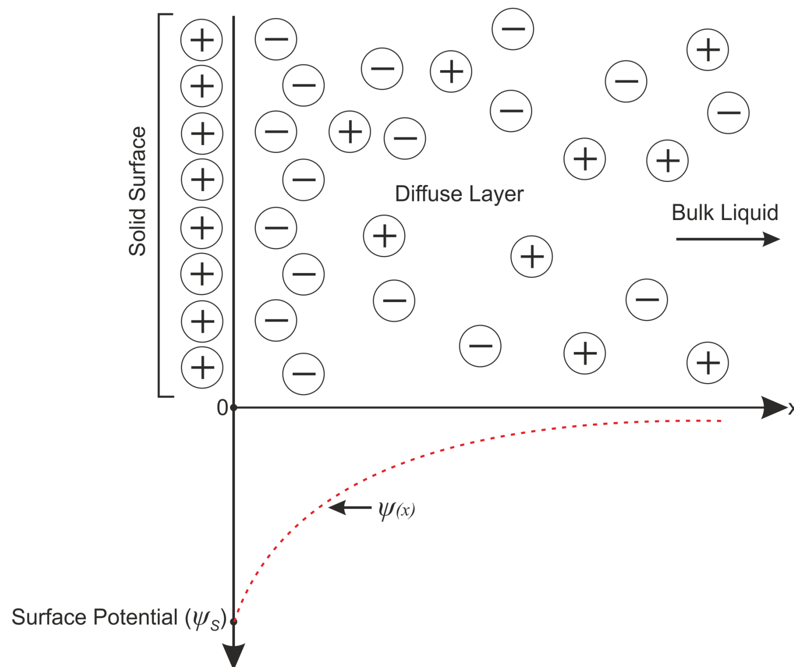

Figure 2.2. EDL structure in Gouy-Chapman model.

Diffuse layer can be considered as successive laminae with thickness of dx as in Figure 2.3. Electrostatic forces are strongest in the vicinity of solid surface which indicates that the concentration of counter-ions is the highest in the nearest lamina. With increasing distance, electrostatic forces get weaker and the effect of Brownian motion increases. Therefore, counter-ion concentration decreases in each successive lamina until it reaches its bulk concentration. The opposite relation is true for concentration of co-ions.

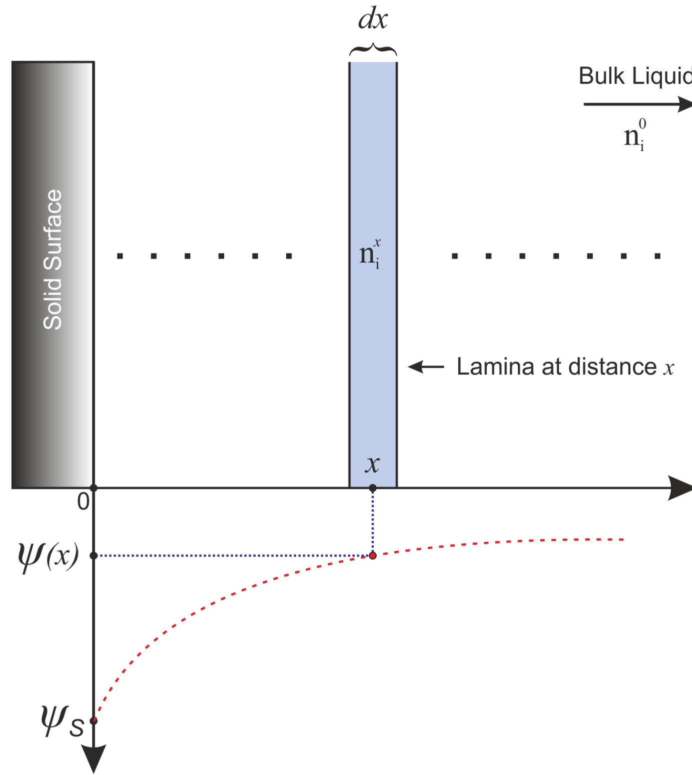

Figure 2.3. Successive laminae approximation of diffuse layer in Gouy-Chapman model.

In Gouy-Chapman model, ions are considered as point-like charges and their distribution follows Maxwell-Boltzmann statistics. In each lamina, concentration of ion i, n_i, can be found as

$$n_i = n_i^0 \exp\left(\frac{-z_i e \psi}{k_B T}\right) \tag{2.6}$$

where n_i^0 is the bulk concentration and z_i is signed charge for ion i. e is electronic charge, k_B is the Boltzmann's constant, T is absolute temperature, and ψ is potential at distance x measured with respect to bulk. Then, total charge per volume for a lamina, $\rho(x)$, can be found as

$$\begin{aligned}\rho(x) &= \sum_i n_i z_i e \\ &= \sum_i n_i^0 z_i e \exp\left(\frac{-z_i e\psi}{k_B T}\right)\end{aligned} \tag{2.7}$$

where i goes for all ion species present in liquid. In electrostatics, ρ and ψ are also related with Poisson equation as

$$\nabla^2\psi = -\frac{\rho}{\epsilon_r\epsilon_0}. \tag{2.8}$$

Since ψ and ρ vary only with x, Equation 2.7 and 2.8 can be combined as

$$\frac{d^2\psi}{dx^2} = -\frac{e}{\epsilon_r\epsilon_0}\sum_i n_i^0 z_i \exp\left(\frac{-z_i e\psi}{k_B T}\right). \tag{2.9}$$

Equation 2.9 is called Poisson-Boltzmann equation and characterizes EDL in Gouy-Chapman model. For small x values, $\exp(-x) \approx 1 - x$. Therefore, if ψ is small everywhere in EDL satisfying $z_i e\psi \ll k_B T$, Poisson-Boltzmann equation becomes

$$\frac{d^2\psi}{dx^2} = -\frac{e}{\epsilon_r\epsilon_0}\left(\sum_i n_i^0 z_i - \sum_i \frac{n_i^0 z_i^2 e\psi}{k_B T}\right). \tag{2.10}$$

The term $\sum_i n_i^0 z_i$ must be equal to zero due to electroneutrality in bulk electrolyte. Then, Equation 2.10 can be written as

$$\frac{d^2\psi}{dx^2} = \kappa^2\psi \tag{2.11}$$

where

$$\kappa = \sqrt{\frac{e^2 \sum_i n_i^0 z_i^2}{\epsilon_r \epsilon_0 k_B T}}. \tag{2.12}$$

The parameter κ is known as Debye-Hückel parameter. [25] Thickness of the EDL layer (also known as Debye length, λ_D) can be found as

$$\lambda_D = \kappa^{-1} = \sqrt{\frac{\epsilon_r \epsilon_0 k_B T}{e^2 \sum_i n_i^0 z_i^2}}. \tag{2.13}$$

From Equation 2.13, it can be seen that there is an inverse relationship between ion concentration of the electrolyte and the EDL thickness.

To calculate differential capacitance, potential distribution in electrolyte should be found. If the Poisson-Boltzmann equation is rearranged [26] by using

$$\frac{d^2\psi}{dx^2} = \frac{1}{2}\frac{d}{d\psi}\left(\frac{d\psi}{dx}\right)^2 \tag{2.14}$$

the result is in the form of

$$d\left(\frac{d\psi}{dx}\right)^2 = -\frac{2e}{\epsilon_r \epsilon_0}\sum_i n_i^0 z_i \exp\left(\frac{-z_i e\psi}{k_B T}\right) d\psi. \tag{2.15}$$

After integration, Equation 2.15 becomes

$$\left(\frac{d\psi}{dx}\right)^2 = \frac{2k_B T}{\epsilon_r \epsilon_0}\sum_i n_i^0 z_i \exp\left(\frac{-z_i e\psi}{k_B T}\right) + \Psi_{constant}. \tag{2.16}$$

Potential should be equal to zero for distances far from solid surface. Therefore, by applying boundary conditions as $\psi = 0$ and $d\psi/dx = 0$ for $x \to \infty$, it can be obtained

that

$$\left(\frac{d\psi}{dx}\right)^2 = \frac{2k_BT}{\epsilon_r\epsilon_0}\sum_i n_i^0 z_i\left[\exp\left(\frac{-z_ie\psi}{k_BT}\right)-1\right]. \tag{2.17}$$

Most of the cases, surface charge is balanced almost entirely by counter-ions at the interface. Role of co-ions in this process is less significant. Therefore, it is safe to assume the electrolyte as symmetric (i.e. $z:z$ electrolyte) for calculations where z equals to valence of counter-ion. [27] For a symmetric electrolyte, Equation 2.17 gives

$$\frac{d\psi}{dx} = -\sqrt{\frac{8k_BTn^0}{\epsilon_r\epsilon_0}}\sinh\left(\frac{ze\psi}{2k_BT}\right). \tag{2.18}$$

For surface charge

$$\begin{aligned}\sigma_S = -\sigma_E &= -\int_0^\infty \rho(x)dx \\ &= \epsilon_r\epsilon_0\int_0^\infty \frac{d^2\psi}{dx^2} \\ &= -\epsilon_r\epsilon_0\left(\frac{d\psi}{dx}\right)_{x=0}\end{aligned} \tag{2.19}$$

where σ_E charge density of electrolyte. By using Equation 2.18 and 2.19, σ_S can be calculated as

$$\sigma_S = \sqrt{8k_BTn^0\epsilon_r\epsilon_0}\sinh\left(\frac{ze\psi_S}{2k_BT}\right). \tag{2.20}$$

Then, by using Equation 2.4, C_d for Gouy-Chapman model can be calculated as

$$C_d = \sqrt{\frac{2\epsilon_r\epsilon_0n^0}{k_BT}}ze\cosh\left(\frac{ze\psi_S}{2k_BT}\right). \tag{2.21}$$

Equation 2.21 shows that differential capacitance varies with surface potential of the solid and ionic concentration of the electrolyte as Gouy and Chapman proposed.

2.1.3. Gouy-Chapman-Stern Model

Although Gouy-Chapman model has a better explanation for the EDL structure, it has its own shortcomings. In Gouy-Chapman model, differential capacitance increases boundlessly with increasing ion concentration or potential values which does not coincide with experimental results. Main reason for this discrepancy is assuming ions as point-like charges. With increasing potential, ions accumulate closer to the solid surface, thus the effective distance which separates solid surface and shielding counter-ions goes down to zero. In reality, ions in solution have finite diameters and their distance to the surface cannot be smaller than ionic radius. Otto Stern [28] was stated it and proposed a model which is a combination of both Helmholtz and Gouy-Chapman models.

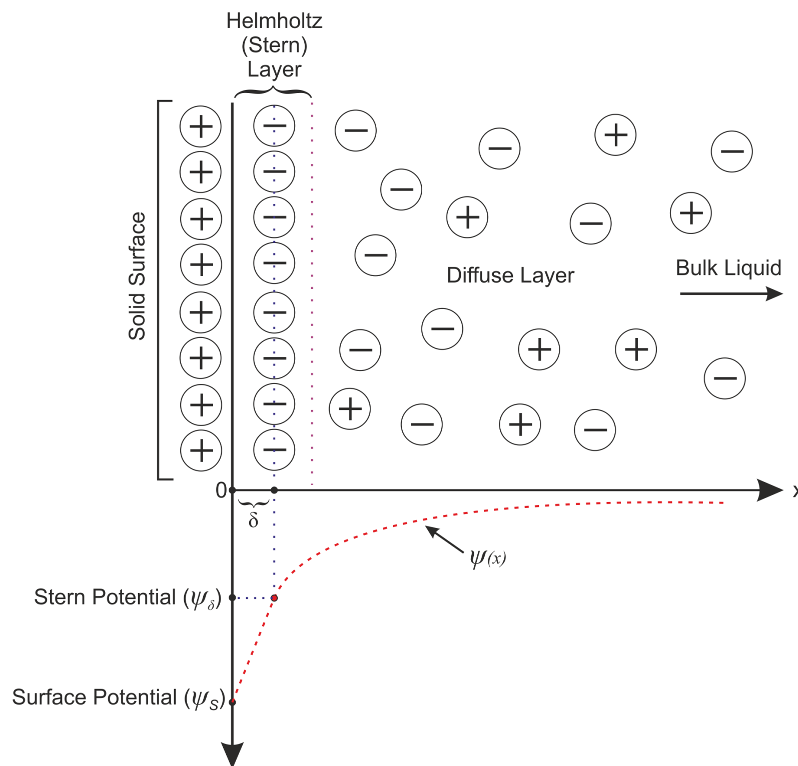

Figure 2.4. EDL structure in Gouy-Chapman-Stern model.

According to Stern, if counter-ion radius is δ, there should be no charge for $x < \delta$ and electric field should be constant at that interval. For $x \geq \delta$, a diffusion

layer is formed as explained in Gouy-Chapman model. The proposed EDL structure is depicted in Figure 2.4.

Since electric field is constant for $x < \delta$, potential drop should be linear, and the potential at $x = \delta$ can be calculated as

$$\psi_\delta = \psi_S + \left(\frac{d\psi}{dx}\right)_{x=\delta} \delta. \tag{2.22}$$

Surface charge can be calculated by slightly modifying Equation 2.19 as

$$\begin{aligned} \sigma_S = -\sigma_E &= -\int_\delta^\infty \rho(x)dx \\ &= \epsilon_r\epsilon_0 \int_\delta^\infty \frac{d^2\psi}{dx^2} \\ &= -\epsilon_r\epsilon_0 \left(\frac{d\psi}{dx}\right)_{x=\delta} \end{aligned} \tag{2.23}$$

since all ionic charges are located beyond δ. Then, Equation 2.22 can be rearranged as

$$\psi_\delta = \psi_S - \left(\frac{\sigma_S}{\epsilon_r\epsilon_0}\right)\delta. \tag{2.24}$$

By using symmetric electrolyte assumption with Equation 2.18 and 2.23, surface charge is found as

$$\begin{aligned} \sigma_S &= \sqrt{8k_BTn^0\epsilon_r\epsilon_0}\,\sinh\left(\frac{ze\psi_\delta}{2k_BT}\right) \\ &= \sqrt{8k_BTn^0\epsilon_r\epsilon_0}\,\sinh\left[\frac{ze}{2k_BT}\left(\psi_S - \frac{\sigma_S\delta}{\epsilon_r\epsilon_0}\right)\right]. \end{aligned} \tag{2.25}$$

Differential capacitance can be obtained by calculating $d\sigma_S/d\psi_S$ as

$$C_d = \frac{\sqrt{2\epsilon_r\epsilon_0 z^2e^2n^0/k_BT}\,\cosh\left(ze\psi_\delta/2k_BT\right)}{1 + \left(\delta/\epsilon_r\epsilon_0\right)\sqrt{2\epsilon_r\epsilon_0 z^2e^2n^0/k_BT}\,\cosh\left(ze\psi_\delta/2k_BT\right)}. \tag{2.26}$$

Equation 2.26 can be written in its reciprocal form as

$$\frac{1}{C_d} = \frac{1}{\epsilon_r \epsilon_0/\delta} + \frac{1}{\sqrt{2\epsilon_r \epsilon_0 z^2 e^2 n^0/k_B T} \cosh\left(ze\psi_\delta/2k_B T\right)}. \tag{2.27}$$

Here, it can be seen that the first term equals to the reciprocal of Helmholtz capacitance, and the second term equals to the reciprocal of Gouy-Chapman capacitance. Therefore, differential capacitance can be calculated as the serial combination of Helmholtz and Gouy-Chapman capacitances as

$$\frac{1}{C_d} = \frac{1}{C_H} + \frac{1}{C_{GC}}. \tag{2.28}$$

For low ionic concentrations, λ_D gets wider and C_{GC} becomes dominant. If ion concentration is increased, counter-ions accumulate tightly near the solid surface and C_H becomes dominant.

With Stern's modifications, this EDL structure is called Gouy-Chapman-Stern (GCS) model and is used to characterize solid/liquid interfaces in non-Faradaic situations (i.e. no oxidation or reduction occurs). Although it broadly accounts for behavior of EDL systems, it has limitations. [29] It assumes that permittivity in the Helmholtz layer is constant [30] and independent of the surface potential. It also ignores ion pairing effects and any non-Colombic ion interactions in diffuse layer. There are further studies [31–40] to explain effects of such mechanisms on EDL structure. However, GCS model provides a neat theoretical background for characterization of solid/liquid interfaces in most of the electronic applications.

2.2. Electric Double Layer Transistors (EDLTs)

By utilizing EDL concept, electric double layer transistors (EDLTs) are designed. For comparison, a sketch of a classical MOSFET structure is given in Figure 2.5. An oxide layer insulates semiconductor surface from gate electrode. With application of proper V_{GS} and V_{DS} voltages, charge carriers are attracted to Si surface and a

conduction channel is formed between source and drain regions. MOSFETs are either n-channel or p-channel devices depending on the majority charge carrier type in the channel region (i.e. electrons or holes). Channel current, I_D, in an n-channel MOSFET can be calculated as

$$I_D = \mu_n C_{OX} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2.29}$$

in linear region where $V_{DS} < V_{GS} - V_{th}$, and as

$$I_D = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{th})^2 \tag{2.30}$$

in saturation region where $V_{DS} \geq V_{GS} - V_{th}$. μ_n is effective electron mobility in Si, C_{OX} is the gate oxide capacitance per unit area, W is the channel width, L is the channel length, and V_{th} is the threshold voltage which stands for the minimum gate voltage required to turn the device on. For values of $V_{GS} < V_{th}$, channel is not formed and the transistor is turned off.

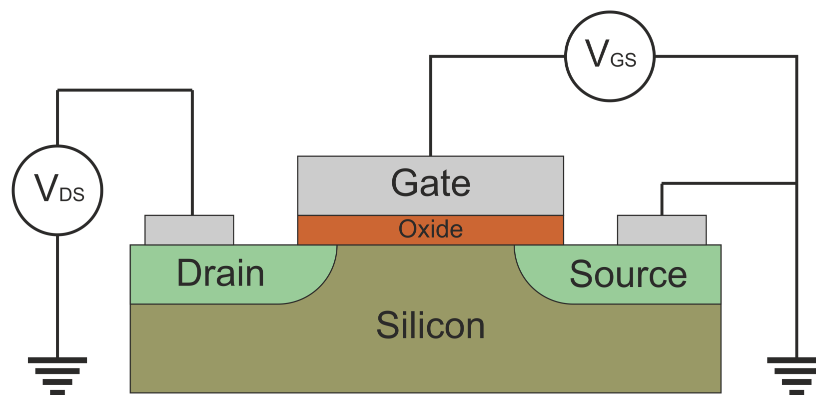

Figure 2.5. A simple sketch of a MOSFET device.

Although $I - V$ characteristics of MOSFET are governed by more complicated equations in real life, this basic model is enough for practical calculations and it gives insight about device operation.

Compared to MOSFET, a general EDLT structure can be depicted as in Figure 2.6. Oxide layer is replaced with electrolyte solution to use EDL capacitance (EDLC) as gate insulator. Gate electrode and semiconductor surfaces are directly in contact with electrolyte which results formation of EDL layers on both. For sensor applications, semiconductor surface can be coated or functionalized to make it sensitive to certain molecules or ions. Ionic liquids, ion-gels, aqueous or solid electrolytes can be used to form EDLs.

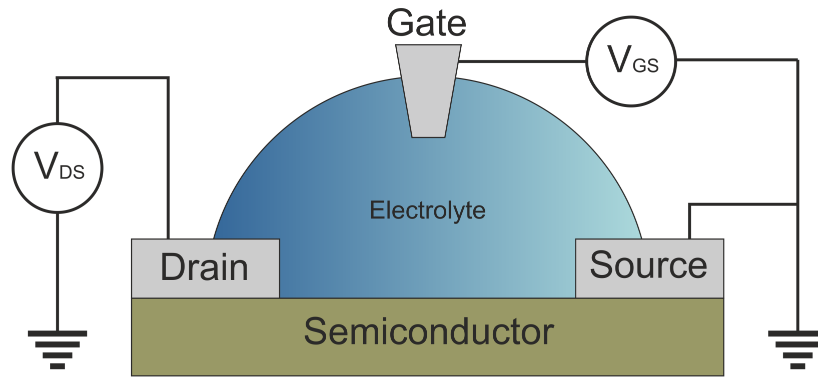

Figure 2.6. A simple sketch of an EDLT device.

There are various types of EDLTs specific to different applications. The oldest [41] and most known type of EDLT device is the ion-sensitive field effect transistor (ISFET). ISFET uses similar structure with MOSFET except the gate electrode. Instead, an electrolyte solution is used in a direct contact with the thin gate dielectric like SiO_2, Al_2O_3, Si_3N_4, or Ta_2O_5. A sketch of an ISFET is given in Figure 2.7.

Interfacial potential at the electrolyte/oxide interface modifies the threshold voltage, V_{th}. Bergveld [42] states the relation as

$$V_{th} = E_{ref} - \psi_S + \chi^{sol} - \frac{\Phi_{Si}}{e} - \frac{Q_{OX} + Q_{SS} + Q_B}{C_{OX}} + 2\phi_F \tag{2.31}$$

where E_{ref} is the potential of reference electrode, ψ_S is the surface potential, χ^{sol} is the surface dipol potential of the solvent, Φ_{Si} is the work function of Si, e is electronic

charge, Q_{OX} is the accumulated charge on the oxide, Q_{SS} is the accumulated charge at the oxide/Si interface, Q_B is the accumulated charge in the depletion region, C_{OX} is the oxide capacitance, and $2\phi_F$ is the required potential for strong inversion at the channel. The surface potential also changes with pH of the solution as

$$\Delta\psi_S = -2.3\alpha\frac{k_BT}{e}\Delta pH \tag{2.32}$$

where

$$\alpha = \left(2.3\frac{k_BT}{e^2}\frac{C_{EDL}}{\beta_S} + 1\right)^{-1}. \tag{2.33}$$

Here, C_{EDL} is the capacitance of EDL, and β_S is the surface buffer capacity. With proper calibration and with the presence of reference electrode, ISFET can be used as a pH sensor.

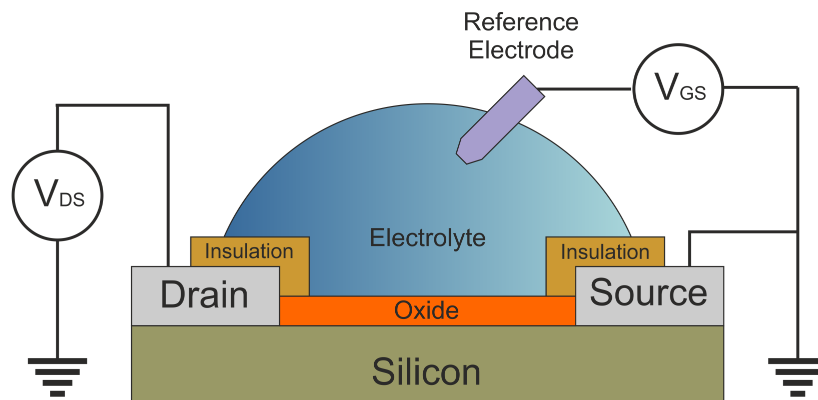

Figure 2.7. A simple sketch of an ISFET device.

Electric current, I_D, flows between source and drain similar to MOSFET. The channel resistance is modified by the interfacial potential, thus direct measurement of this resistance gives a metric about that potential value. Reference electrode seems unnecessary in this case. However, value of the resistance by itself gives no absolute value of interfacial potential. If a feedback system is applied which supplies constant I_D while V_{DS} is kept constant, all changes on the interface potential should be com-

pensated by the reference electrode potential, V_{GS}. Therefore, direct measurement of the electrolyte/oxide interfacial potential is achieved.

In another study, Nikolaides *et al.* built a silicon-on-insulator (SOI) based thin film resistor to detect changes of electrolyte concentrations and small numbers of charged biomolecules [43]. They used SOI wafers with 200 nm buried oxide and 30 nm low doped single crystalline Si layer. 50 nm of p-doped Si layer was grown on top of the 30 nm Si layer with molecular beam epitaxy for experimental purposes. On top of grown Si layer, 2-3 nm of natural SiO_2 layer exists. Si layer was patterned as a Hall bar configuration to apply 4-point probe resistance measurement. An Ag/AgCl reference electrode was used in contact with electrolyte solution and a voltage was applied to the bulk Si as back gate potential to control the charge carrier concentration in the thin Si layer. An illustration of their device is given in Figure 2.8.

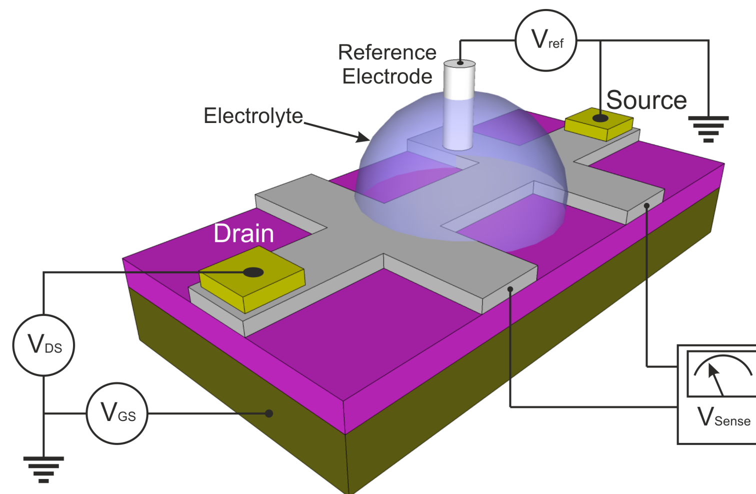

Figure 2.8. Illustration of SOI-based ISFET designed by Nikolaides *et al.* Oxide layer is not shown. After [43].

Nikolaides *et al.* showed that 1 nM (80 ng/mL) of poly-L-lysine concentration was detectable with that setup. That corresponds to detection of one electronic charge variation per 100 nm^2 surface, which is highly attributed to quasi-two-dimensional electron gas (2DEG) nature of SOI. [43] Although this study shows the efficiency of

SOI about sensing surface potential variations, existence of back gate and reference electrode make the integration of such devices harder. Also, the device behaves as a resistance, therefore its application area is limited.

Although ISFET is an established structure as a pH sensor [44, 45], it has some design challenges. Presence of the reference electrode introduces some problems to the system. Reference electrodes are traditionally made of Ag/AgCl because of process compatibility and preferable electrochemical characteristics. Solubility of AgCl is not negligible especially in solutions with high concentration of Cl^-. [46] They are also bulky and fragile which makes the encapsulation process and miniaturization of ISFET harder.

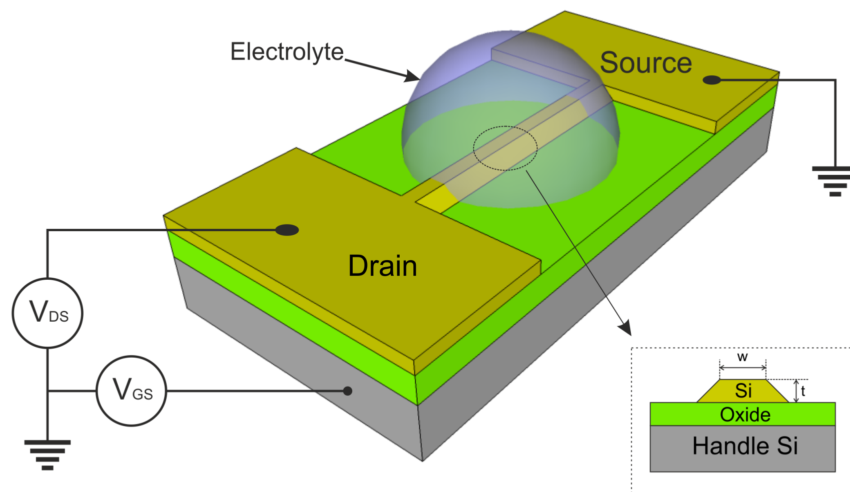

Figure 2.9. Illustration of SOI-based thin film resistor designed by Stern *et al.* After [47].

Sensor applications of EDLTs are not limited with ISFET topology. Stern *et al.*, built a pseudo-nanowire based device with a back gate [47]. They used anisotropic wet etching with tetramethylammonium hydroxide (TMAH) to pattern the thin Si layer of an SOI wafer. Due to the fact that TMAH etches Si (111) planes 100 times slower than other planes, undercuts behind the masking oxide occur and this leads

to a trapezoidal shape nanowire which is narrower than the lithographic limit of the oxide mask. With the fabricated device, they obtained I_D vs. V_{DS} characteristics for varying V_{GS} values. An illustration of their device is given in Figure 2.9.

After that, Stern *et al.* functionalized the surface of Si nanowire structure to achieve label-free antibody detection. For this process, antibodies to mouse IgG and mouse IgA proteins were used, and detection of below 100 fM concentrations achieved. Although the focus on this experiment is sensing application, device structure is important because of the absence of reference electrode and defined transistor operation. CMOS compatible process is another big advantage. [48] Yet, thick oxide layer between back gate and the channel requires high voltage values (i.e. $|V_{GS}|$ up to 40 V) to control the channel flow.

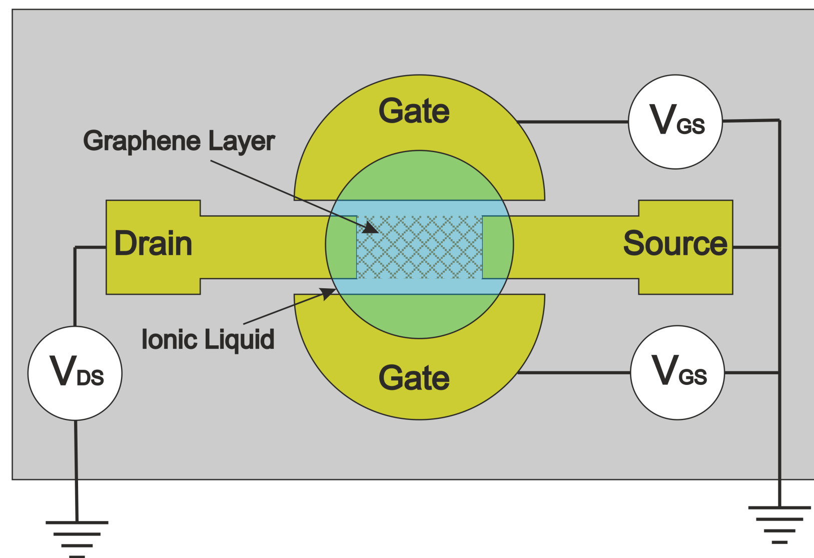

Figure 2.10. Top view of the graphene-FET based gas sensor designed by Inaba *et al.* After [49].

Beside Si, other types of semiconductors are also used in EDLT devices. Inaba *et al.* built an ionic-liquid gate FET based gas sensor using graphene as semiconductor layer. [49–51] They obtained graphene on Cu foil by chemical vapor deposition (CVD) and transferred it onto Au source/drain electrode structure. Ionic-liquid, which is

selective to the target gas type, was placed on top of graphene layer. Top view of their device structure is depicted in Figure 2.10.

They managed to detect 30 ppm of NH_4 and 4000 ppm of CO_2 at V_{GS} values under 1 V. 2DEG feature of graphene combined with thin EDL layer provided high sensitivity at low gate voltages [52]. Inaba *et al.* used planar gate electrodes in this device instead of immersing reference or gate electrodes which makes integration of multiple devices easier. However, using graphene requires a more complicated process and brings compatibility issues which decreases practical advantages of planar gate structure.

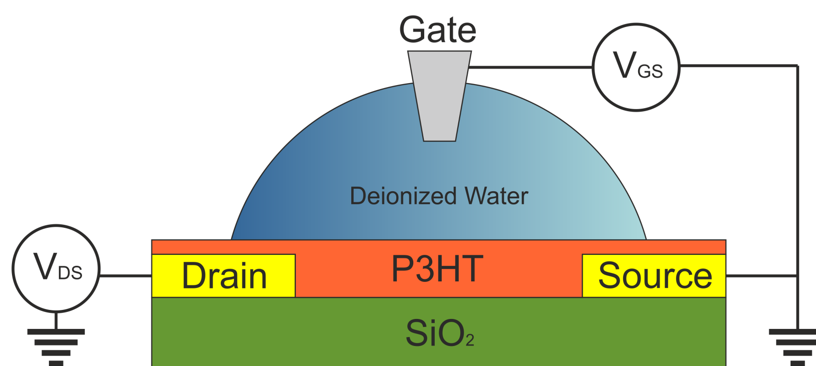

Figure 2.11. A sketch of WGOFET device designed by Kergoat *et al.* Source and drain electrodes are made out of Au, and coated with thin P3HT layer. After [53].

Similar EDLT devices are designed by using metal-oxide semiconductors [54, 55], carbon nanotubes [56–58], and organic semiconductors [59–64] as well. An interesting study was done by Kergoat *et al.* with organic semiconductor, P3HT. [53] They built an EDLT based on organic field-effect transistor (OFET) stucture. Instead of ionic-liquid, de-ionized water was used as electrolyte. By immersing a Pt probe into water as gate electrode, EDLT was completed. Their water-gated OFET (WGOFET) device operated in non-Faradaic region to prevent electrochemical reactions on polymer surface which is an important issue in other electrolyte-gated OFETs. [65] A sketch of WGOFET device is given in Figure 2.11.

Later, Kergoat *et al.* used their WGOFET structure to build biosensors by using different organic semiconductors and gate probes specific to target molecules. [66, 67] Concept of using pure water as gate electrolyte is important because it further simplifies the fabrication process by eliminating complex ionic compounds. Also water-gated devices have low operating voltages and are inherently compatible with aqueous media for sensory applications.

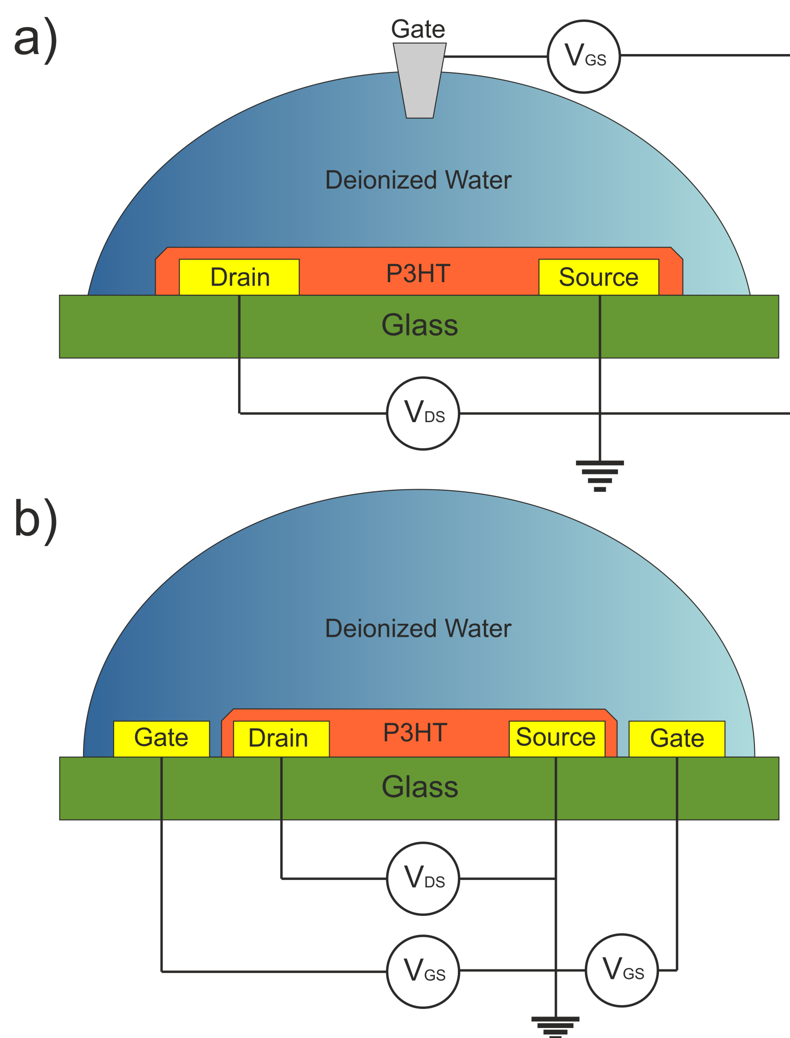

Figure 2.12. Illustrations of WGOFET devices designed by Yaman *et al.* with (a) probe- and (b) planar-gate topologies. After [68].

There are several studies on WGOFETs and its applications. [69–71] A notable one is conducted by Yaman *et al.* with WGOFET devices using P3HT and P3HT-

co-P3PEGT as semiconductor materials. [68, 72, 73] They patterned source-drain electrodes from Au on glass substrate and coated them with thin organic semiconductor. After placing de-ionized water on active area, a probe made out of tungsten was immersed into it to complete device. Also, they fabricated WGOFETs with planar gate electrodes which were patterned with source-drain electrodes from Au. Probe- and planar-gate structures they built are depicted in Figure 2.12.

In experiments, they tested the effect of ion concentration by using aqueous solutions of NaCl instead of de-ionized water. They also used P3HT-co-P3PEGT, which is obtained by functionalization of P3HT with poly(ethylene glycol) (PEG), as organic semiconductor for performance comparison. Yaman *et al.* also built inverter circuits using WGOFETs. Planar-gate structure is advantageous for such applications due to several reasons. It simplifies fabrication process by adding gate electrode while patterning drain-source electrodes. Absence of external probe electrode allows more compact devices. Since all electrodes are placed in the same plane, it is easier to integrate such devices with microfluidic structures.

Despite addressed advantages, EDLT devices with organic semiconductors have some inherent drawbacks. Charge carrier mobilities are lower in organic semiconductors with respect to Si and other inorganic counterparts. They are also prone to ion diffusion which results in electrochemical doping of channel area. [67] It alters channel conductivity, decreases switch speed, and affects transistor performance. [74–76]

There is a growing interest on EDLT devices as seen from aforementioned studies. Beside fabrication flexibility, EDLT structure provides better channel control with respect to classical FET devices with solid gate insulators due to high electric fields obtained at the channel region. Ultra-thin EDL behaves as a capacitor at the solid/liquid interface according to Gouy-Chapman-Stern model, [77] and makes those high electric fields achievable at low gate voltages without the risk of dielectric breakdown. EDLT devices can use various materials such as Si, graphene, metal-oxide semiconductors, carbon nanotubes, and organic semiconductors as active channel layer, and ionic liquids, ion-gels, polymers, aqueous solutions and even de-ionized water as electrolytes

depending on the application. Utilization of EDL layer as gate insulator makes EDLT a promising component for future circuit applications which require flexible and low-voltage devices, whereas its inherent fluidic interface offers new methods for sensor devices. [78–80]

3. WATER-GATED FIELD EFFECT TRANSISTOR (WG-FET)

3.1. Motivation

In Chapter 2, working mechanism and utilization of the EDL in EDLT devices are explained, and some examples of EDLT studies in literature are given. Devices with Si semiconductor layer have advantages of high charge carrier mobility and compatibility with existing fabrication techniques. Especially, SOI-based devices take advantage of 2DEG nature of thin Si which provides better response to surface changes in sensor applications. However, bulky reference electrodes used in those devices make fabrication process harder. Also, using handle Si layer as gate electrode (i.e. back gating) requires considerably high potential values to be applied for device operation due to thick buried oxide layer. Semiconductor layer materials like graphene and carbon nanotubes have advantages of high charge carrier mobility and surface response, yet their processes require elaborate procedures in which small variations can cause repeatability problems in device operation.

Organic and polymer semiconductor materials are low-cost alternatives for EDLTs due to their cheap fabrication methods including spin-coating, inkjet-printing, and drop-casting which also allow these materials to be applied on large areas. Prior studies demonstrated planar-gate EDLTs with polymer semiconductor layers. Planar-gate topology allows patterning of source, drain and gate electrodes at the same layer. It simplifies the fabrication process and paves the way for easier integration with fluidic systems. However, comparably low charge carrier mobility in organic and polymer semiconductors result in inferior device performances. Also, their environmental stability and degradation are important issues for organic EDLTs.

As electrolyte materials, ionic solutions and ion-gels have advantage of higher EDL capacitance, and they are more stable than aqueous solutions due to absence of

solvent. [54] However, they carry the risk of electrochemical doping on channel layer due to ion diffusion. Also, they are prone to environmental degradation. [81] Using pure water greatly simplifies EDLT fabrication and prevents undesirable interactions of ionic compounds with other device parts which decreases compatibility with other electronic components. [80].

Here, we present a water-gated field effect transistor (WG-FET) which uses 16-nm-thick single crystalline Si film as channel layer. It basically combines advantages of aforementioned device structures. Ultra thin and high mobility characteristics of the channel layer provide better surface sensitivity in sensor applications and in-situ amplification in their read-out circuits. 2DEG feature of 16-nm-thick Si layer is exploited to obtain both in the same device. SOI-based design makes it inherently compatible with well established MOSFET fabrication techniques which provide easy integration with other electronic components. Instead of back-gating, it uses a gate electrode directly in contact with de-ionized water. Therefore, low operating voltage levels under 1 V can be achieved. Also, these low voltage levels ensure non-Faradaic operation and prevent electrochemical reactions which otherwise could occur at Si/water or water/electrode interfaces. Either probe- or planar-gate topologies can be used, where the latter is especially suitable for direct integration with fluidic systems. Features of presented WG-FET device can be summarized as:

- Superior charge carrier mobility of single crystalline Si
- 2DEG feature of 16-nm-thick Si layer
- Process advantages of SOI wafer
- Ultra thin, high-κ, pinhole-free EDL layer as gate insulator
- Low operation voltage due to water-gating
- No ionic compounds are required
- Easy manipulation for sensory applications
- Compatibility with fluidic systems with planar-gate topology

WG-FET is designed as a device platform for microfluidic applications where sensors and read-out circuits can be integrated at transistor level.

3.2. Theoretical Modeling

An illustration of WG-FET device is given in Figure 3.1. Single crystalline Si is used as channel layer. Source and drain electrodes patterned from aluminium. Gate electrode is also patterned with them for planar-gate devices. When in contact with water, source and drain electrodes can act as subsidiary gates which is not desirable. Therefore, they are insulated to avoid such effects. By placing a de-ionized water droplet on Si channel region and the planar gate electrode, WG-FET device is completed. If it is a probe-gate device, a gate electrode is immersed into the water droplet.

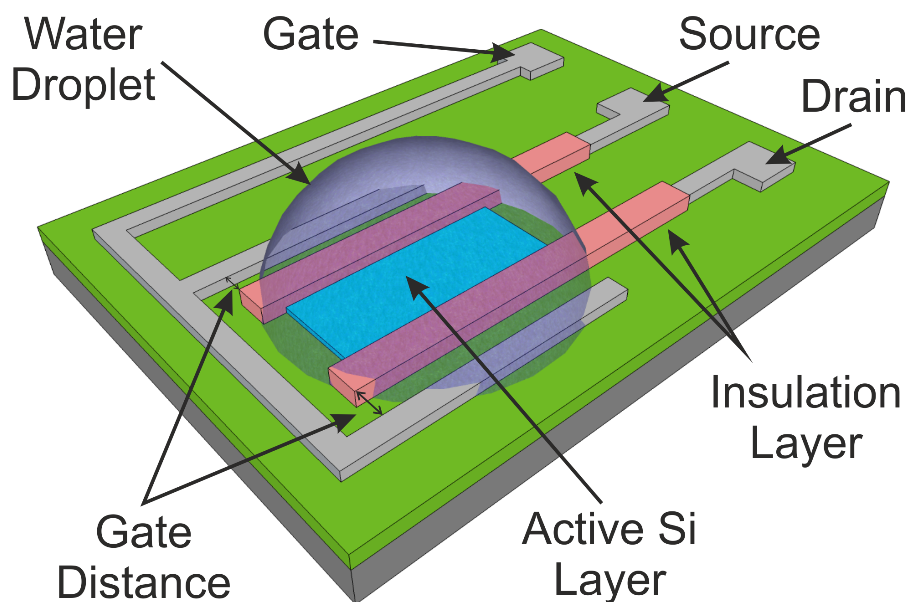

Figure 3.1. An illustration of a WG-FET device with planar gate electrode.

When in contact with water, EDLs are formed at surfaces of Si channel and gate electrode as in Figure 3.2. At each surface, EDL capacitance is the series combination of Helmholtz and Gouy-Chapman capacitances. For low ion densities, Gouy-Chapman capacitance is dominant due to wider diffuse layer, whereas the equivalent capacitance

converges to Helmholtz capacitance with increasing ion density.

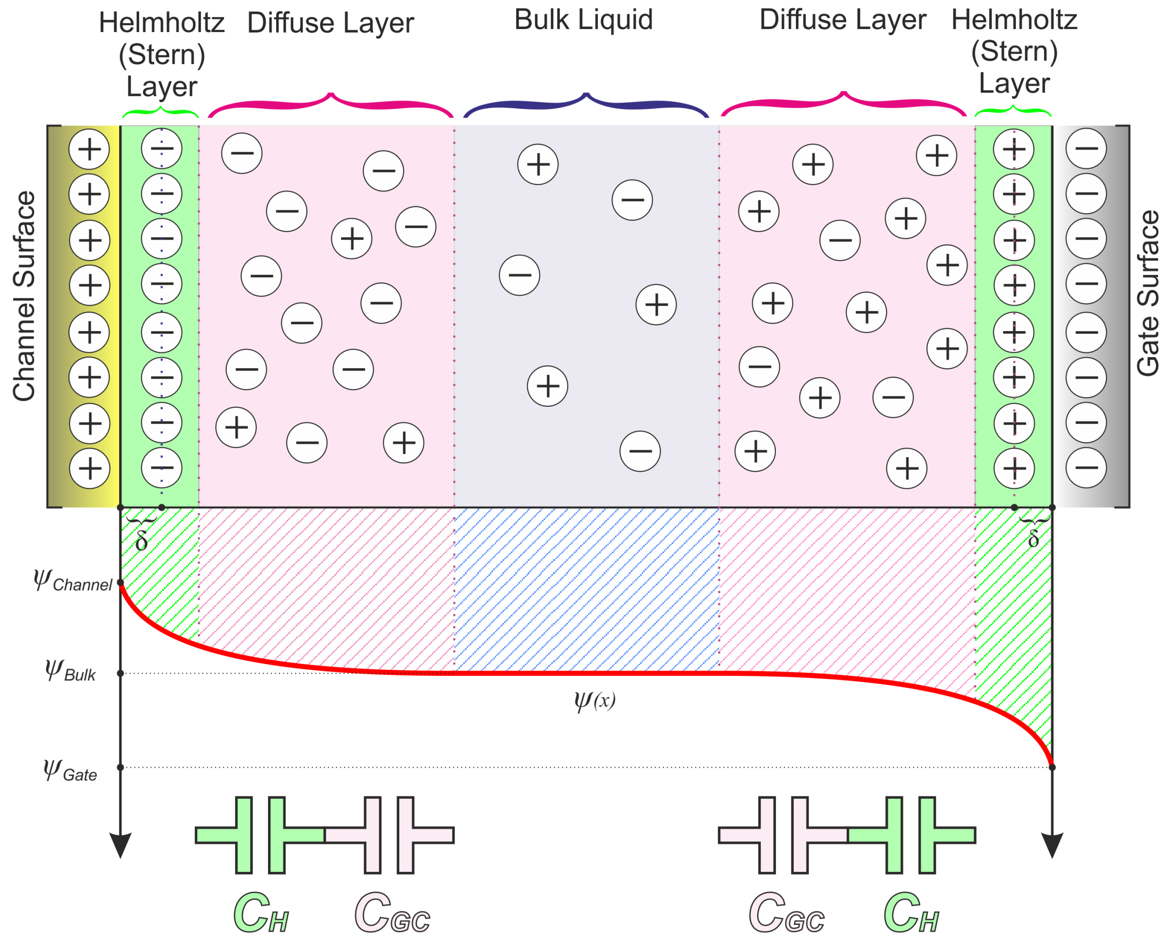

Figure 3.2. EDL formation at Si/water and water/gate electrode interfaces.

Bulk liquid can be modeled as a resistor between channel and gate EDLs. Since the WG-FET device works in non-Faradaic region, gate leakage current is negligible. Therefore, equivalent gate capacitance can be considered as the series combination of two EDL capacitances as

$$\frac{1}{C_{Gate}} = \frac{1}{C_{EDL,Channel}} + \frac{1}{C_{EDL,Gate}}. \tag{3.1}$$

To explain the working mechanism of WG-FET, it is beneficial to examine MOSFET dynamics, first. A general MOSFET device is depicted in the previous chapter, in Figure 2.5. An n-channel MOSFET has a p-doped bulk Si and n-doped diffused source and drain regions. An oxide layer separates the Si channel region and the gate electrode. This metal-oxide-semiconductor (MOS) structure can be considered as a parallel plate capacitor. When there is no external potential applied to gate electrode, energy band diagram of the MOS capacitor can be depicted as in Figure 3.3.

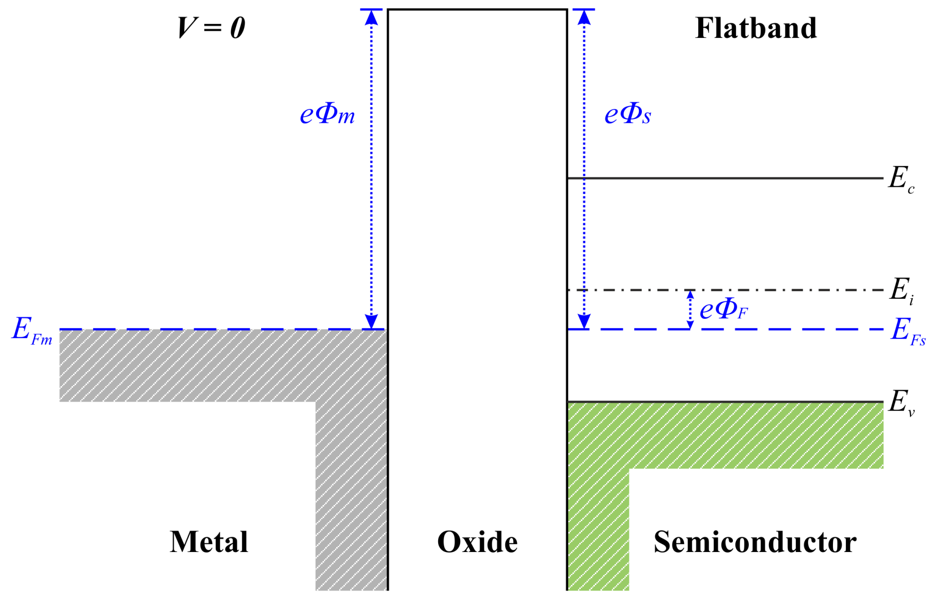

Figure 3.3. Energy band diagram of MOS capacitor in equilibrium. After [82].

In the diagram, $e\Phi_m$ and $e\Phi_s$ are modified work functions of metal and semiconductor, respectively (i.e. energy measured from Fermi level to conduction band of the oxide instead of vacuum level). e stands for the electronic charge. For an ideal system, $e\Phi_m$ and $e\Phi_m$ are equal. Since, Si is p-doped in this case, Fermi level of the semiconductor part is between intrinsic level and valence band. Difference between semiconductor Fermi level, E_{Fs}, and intrinsic level, E_i, is denoted as $e\Phi_F$. It shows the strength of doping, and calculated as

$$e\Phi_F = k_B T \ln \frac{N_a}{n_i} \tag{3.2}$$

where N_a is the doping concentration of p-type semiconductor, and n_i is the intrinsic concentration. Energy levels are flat, so it is also called as flatband situation.

When a negative voltage applied to the gate electrode, potential of the metal decreases and metal Fermi level is elevated by eV relative to its equilibrium position as in Figure 3.4. Difference between Fermi levels of metal and semiconductor causes a bending in the conduction band of oxide. In ideal conditions, there is no charge in the oxide, therefore electric field, $\mathcal{E}_{ox}$, in the oxide region is constant.

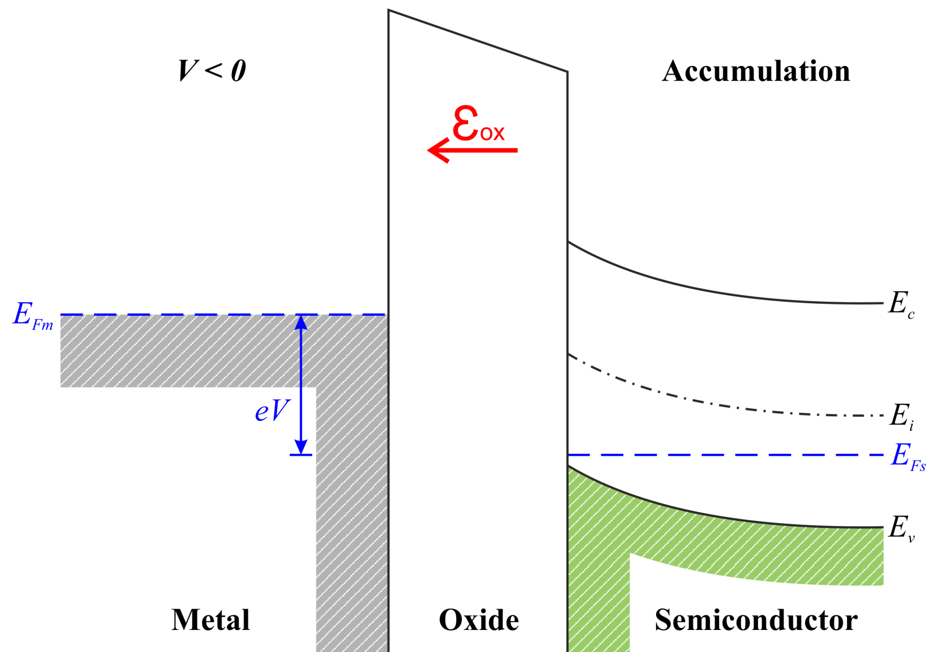

Figure 3.4. Energy band diagram of MOS capacitor in accumulation. After [82].

From Gauss' Law, electric field in the semiconductor region at surface, $\mathcal{E}_{Si}$, can be calculated as

$$\mathcal{E}_{Si} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \mathcal{E}_{ox}. \tag{3.3}$$

Electron potential energy, $E(x)$, is defined as

$$E(x) = -eV(x) \tag{3.4}$$

where $V(x)$ is the electrostatic potential and e is the electronic charge. Electric field, $\mathcal{E}$, can also be written in terms of electrostatic potential as

$$\mathcal{E}(x) = -\frac{dV(x)}{dx} \tag{3.5}$$

and by combining Equation 3.4 and 3.5, it can be expressed as

$$\mathcal{E}(x) = \frac{1}{e}\frac{dE(x)}{dx}. \tag{3.6}$$

Equation 3.6 shows that for $\mathcal{E}_{Si}$ to exist, there should be a gradient in the electron potential energy function. Therefore, energy bands E_i, E_c, and E_v should bend at the the surface of semiconductor region. However, Fermi level, E_{Fs}, remains constant due to absence of current. After band bending, difference between E_i and E_{Fs} increases at the surface. Since hole density is calculated as

$$p = n_i \exp\left((E_i - E_{Fs})/k_B T\right). \tag{3.7}$$

Number of holes increases at the Si surface due to increase in the difference between E_i and E_{Fs} levels, therefore the situation is called as accumulation.

If the applied potential is positive, potential of the metal increases and metal Fermi level drops by eV relative to its equilibrium position as in Figure 3.5. Again, difference between metal and semiconductor Fermi levels causes a bending in the conduction band of oxide. This time, electric field in the oxide region is in the opposite direction relative to accumulation case. Energy bands bend at the surface of semiconductor region and E_i gets closer to semiconductor Fermi level. Due to decrease in the

difference between E_i and E_{Fs}, number of holes starts to decrease at the surface by the Equation 3.7. Therefore, the situation is called depletion. For a specific voltage, E_i bends down to E_{Fs} such that $E_i - E_{Fs} = 0$. At that point, number of holes falls to intrinsic levels.

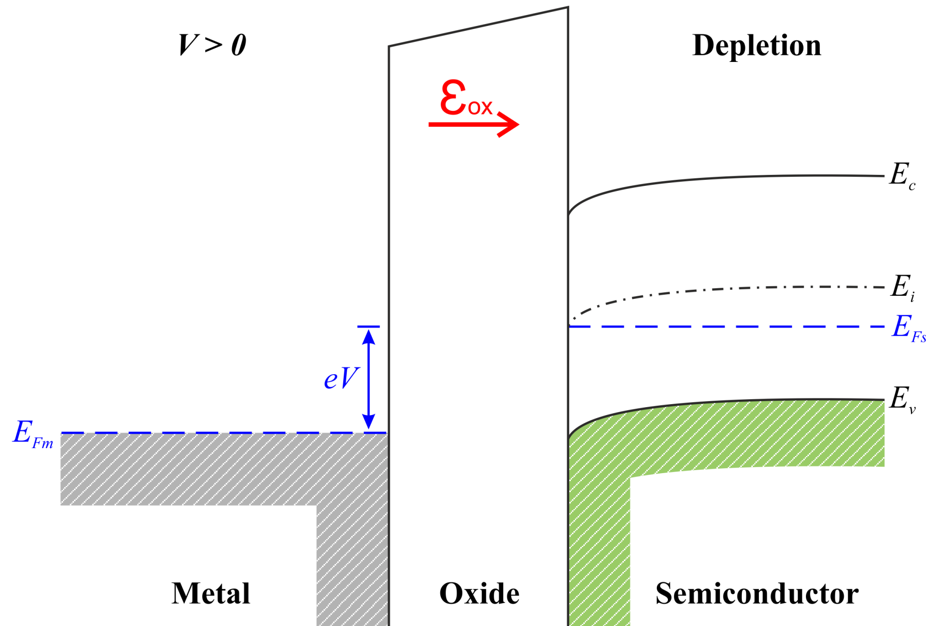

Figure 3.5. Energy band diagram of MOS capacitor in depletion. After [82].

If the applied potential is increased further, E_i bends down below E_{Fs} as in Figure 3.6, and $(E_i - E_{Fs})$ becomes negative. After that point, number of electrons is larger than number of holes as in an n-type semiconductor, and the situation is called inversion. Electron density can be calculated as

$$n = n_i \exp\left((E_{Fs} - E_i)/k_B T\right) \tag{3.8}$$

which shows that number of electrons increases with further bending of E_i below E_{Fs}. This phenomenon is called electrostatic doping [83], and it is essential for field-effect device operation. Although the number of electrons is already larger than the number of holes, semiconductor surface is not assumed completely inverted until it is n-type as strong as it was p-type. This situation is called strong inversion and it requires

bending down of E_i as $2\Phi_F$. [82]

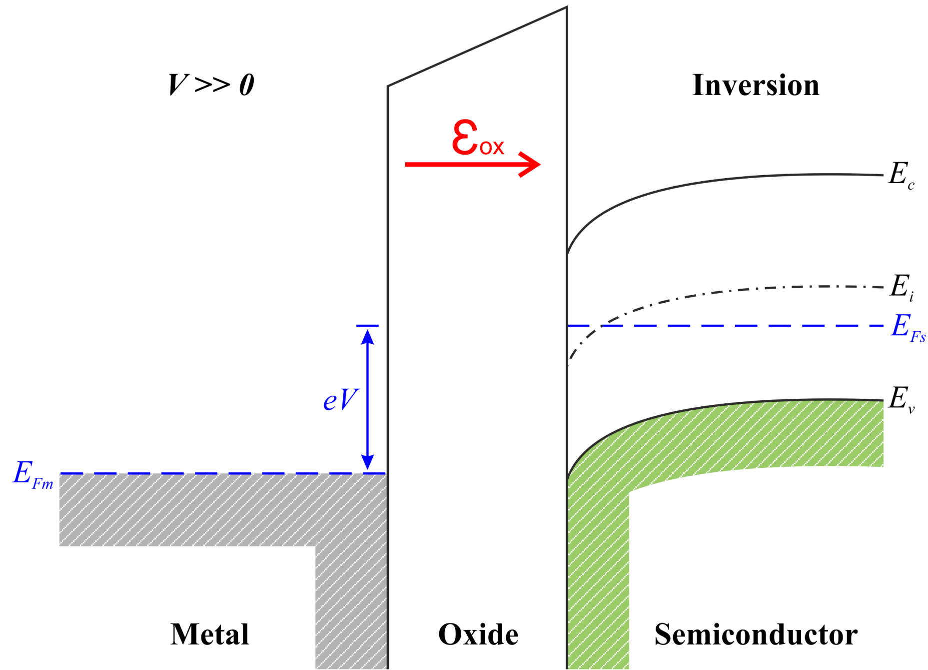

Figure 3.6. Energy band diagram of MOS capacitor in inversion. After [82].

An n-channel MOSFET has n-diffusion source and drain regions, and works in inversion mode because an n-type channel region is required between source and drain for current to pass through. On the other hand, WG-FET has no diffusion regions. Source and drain electrodes are patterned from Al in contact with ultra thin Si layer; therefore, an inverted channel is not required. It works in accumulation mode. Charge carrier density is modulated with the application of negative voltage between gate and source electrodes. Working principle of the WG-FET device is simply shown in Figure 3.7 for both probe- and planar-gate setups.

To derive current-voltage relations, it is convenient to start with classical MOSFET. In Figure 3.8, a simplified cross-section of p-channel MOSFET is given.

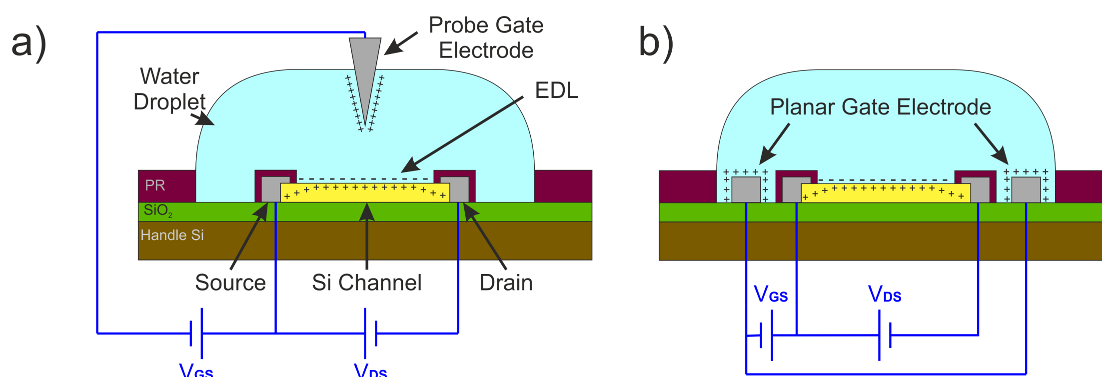

Figure 3.7. Working principle of WG-FET devices with a) probe- and b) planar-gate topologies.

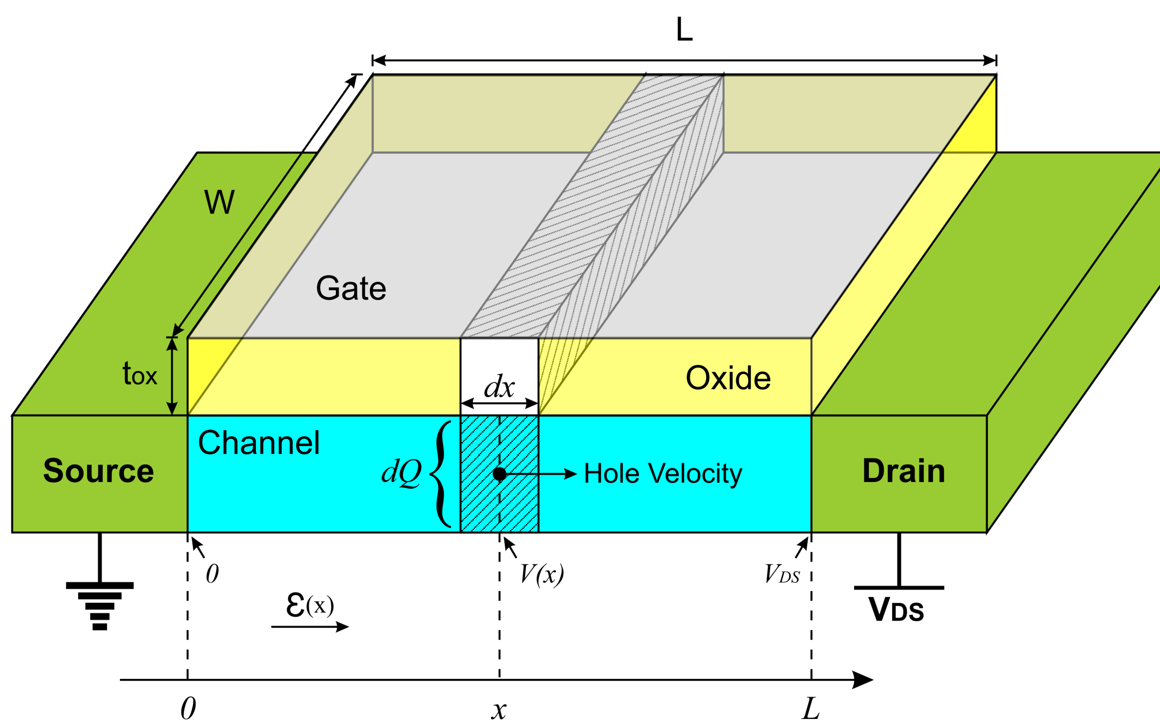

Figure 3.8. A simplified cross-secton of a p-channel MOSFET. After [84].

Capacitance of the strip of the oxide layer at channel position x shown in Figure 3.8 can be calculated as

$$C_{Strip} = WC_{OX}dx \tag{3.9}$$

where C_{OX} is oxide capacitance per unit area, W is the channel width, and dx is the length of the strip. With application of gate voltage, hole charge stored in the channel region under the strip, dQ, can be found by multiplying C_{Strip} with the effective voltage at point x as

$$dQ = WC_{OX}dx \left[V_{GS} - V(x) - V_{th}\right]. \tag{3.10}$$

$V(x)$ stands for the voltage in channel region at point x. V_{th} is the voltage required to form a channel in strong inversion for a classical MOSFET. However, our device works in accumulation mode, and it is enough to ensure flatband condition instead of strong inversion as minimum channel requirement. Therefore, Equation 3.10 should be re-written as

$$dQ = WC_{OX}dx \left[V_{GS} - V(x) - V_{FB}\right] \tag{3.11}$$

where V_{FB} is the required voltage for flatband condition. [85]

Electric field in the channel region at point x can be expressed in terms of channel potential as

$$\mathcal{E}(x) = \frac{dV(x)}{dx}. \tag{3.12}$$

Drift velocity of holes in the channel region due to electric field can be calculated as

$$Velocity = \frac{dx}{dt} = \mu_p \mathcal{E}(x) \tag{3.13}$$

where μ_p is the hole mobility in the channel. By combining Equation 3.12 and 3.13, it can be written that

$$\frac{dx}{dt} = \mu_p \frac{dV(x)}{dx}. \tag{3.14}$$

The channel current at point x can be expressed as

$$I = \frac{dQ}{dt} \tag{3.15}$$

and since the current should be equal throughout the channel, we can use the same equation to find the drain current, I_D. dQ/dt part can be rearranged as the multiplication of two derivatives as

$$\frac{dQ}{dt} = \frac{dQ}{dx}\frac{dx}{dt}. \tag{3.16}$$

dQ/dx can be found from Equation 3.11, and dx/dt is found from Equation 3.14. By plugging them into Equation 3.15, it can be obtained that

$$I_D = W\mu_p C_{OX}\left[V_{GS} - V(x) - V_{FB}\right]\frac{dV(x)}{dx} \tag{3.17}$$

which can be rearranged as

$$I_D dx = W\mu_p C_{OX}\left[V_{GS} - V(x) - V_{FB}\right]dV(x). \tag{3.18}$$

By using gradual channel model, [86] voltage at point x can be expressed as

$$V(x) = \frac{V_{DS}}{L} x \tag{3.19}$$

and its derivative becomes

$$dV(x) = \frac{V_{DS}}{L} dx. \tag{3.20}$$

If we replace $V(x)$ and $dV(x)$ with their equivalents as in Equation 3.19 and 3.20, and integrate along the channel length, we obtain

$$I_D \int_0^L dx = W \mu_p C_{OX} \left[V_{GS} - V_{FB} - \frac{V_{DS}}{L} x \right] \frac{V_{DS}}{L} dx. \tag{3.21}$$

Equation 3.21 gives the drain current of an accumulation mode p-channel MOSFET as

$$I_{D,res} = \frac{W}{L} \mu_p C_{OX} \left[(V_{GS} - V_{FB}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{3.22}$$

in linear region where $V_{DS} > V_{GS} - V_{FB}$. For $V_{DS} \leq V_{GS} - V_{FB}$, MOSFET goes into saturation region and the channel current becomes

$$I_{D,sat} = \frac{1}{2} \mu_p C_{OX} \frac{W}{L} (V_{GS} - V_{FB})^2 . \tag{3.23}$$

In classical MOSFET device, gate electrode covers the thin oxide layer. Therefore, voltage on the oxide is uniform throughout the channel length, and equals to V_{GS} as in Equation 3.21. In WG-FET device, effective V_{GS} is the voltage on the EDL which is formed on top of the Si channel area as given in Figure 3.9.

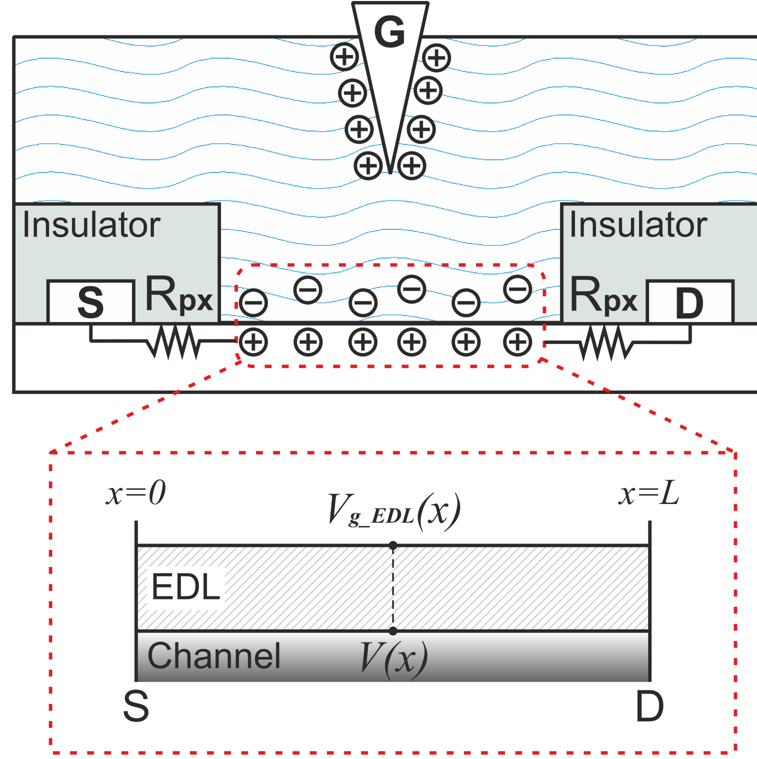

Figure 3.9. A simplified cross-secton of a WG-FET.

The value of this potential on any arbitrary point along the length of the device, $V_{g_EDL}(x)$, is a result of combined effects of source, drain and gate electrodes due to their contributions on EDL. Insulation on source and drain electrodes greatly reduces their effects on V_{g_EDL} by introducing extra serial capacitances with low values. However, their effects should be taken into account in calculating the channel current to obtain a more realistic model. Therefore, if the channel length is L, voltage of a point on EDL insulation layer can be written in most general form as

$$V_{g_EDL}(x) = k_1 V_{GS} + k_2 V_{DS} + (k_3 V_{DS} + k_4 V_{GS}) \frac{x}{L} \tag{3.24}$$

where x goes from 0 to L. Geometry of the gate electrode can be designed in a way that it produces approximately uniform potential distribution throughout the channel, so the contribution of V_{GS} in V_{g_EDL} does not depend on x, which makes $k_4 = 0$. Potential

distribution on the insulation layer then becomes

$$V_{g_EDL}(x) = k_1 V_{GS} + k_2 V_{DS} + k_3 V_{DS} \frac{x}{L} \tag{3.25}$$

where k_1, k_2 and k_3 are topology specific parameters. Then, we can rearrange Equation 3.21 to represent WG-FET as

$$I_D \int_0^L dx = W \mu_p C_{EDL} \left[V_{g_EDL}(x) - V_{thc} - \frac{V_{DS}}{L} x \right] \frac{V_{DS}}{L} dx \tag{3.26}$$

where C_{EDL} is the capacitance of EDL formed on the Si channel region. V_{thc} stands for a threshold constant. It represents the cumulative effects of trapped charges at the Si/water interface with the flatband voltage needed to form the channel in accumulation mode. By combining Equation 3.25 and 3.26, and integrating throughout the channel length, channel current can be calculated as

$$I_{D,res} = \frac{W}{L} \mu_p C_{EDL} \left[\left(k_1 V_{GS} + k_2 V_{DS} - V_{thc} \right) V_{DS} - \frac{1 - k_3}{2} V_{DS}^2 \right] \tag{3.27}$$

in linear region, and in saturation region it becomes

$$I_{D,sat} = \frac{\left(k_3 + 1 \right) W}{2L} \mu_p C_{EDL} \left(k_1 V_{GS} + k_2 V_{DS} - V_{thc} \right)^2 . \tag{3.28}$$

In $I_{D,sat}$ expression of Equation 3.28, k_1 represents the gating capability of the applied V_{GS}. k_2 models the effect of drain electrode voltage on gating. When a negative V_{DS} is applied, it affects the transistor as a competing gate electrode. Therefore, it is desirable to have higher k_1 and lower k_2 values. k_3 depends on both the effect of drain electrode and channel length. It acts as a common multiplier.

3.3. Preliminary Tests

In preliminary studies, WG-FET devices were fabricated with crude methods as a proof of concept. No lithographic steps were used.

3.3.1. Fabrication

Fabrication steps are summarized in Figure 3.10. For all samples, SOI wafers with 16-nm-thick sc-Si layer were used. Thin Si layer at the edge of sample piece was etched to prevent unwanted contacts with handle Si layer due to cleaving defects (Figure 3.10a). Then, electrodes were evaporated on thin Si layer with a small gap between them (Figure 3.10b). Source and drain electrodes were covered with photoresist for insulation purposes (Figure 3.10c). After getting electrical contacts, WG-FET was completed by placing a de-ionized water droplet on the active area (Figure 3.10d), and a probe was immersed into the droplet as gate electrode.

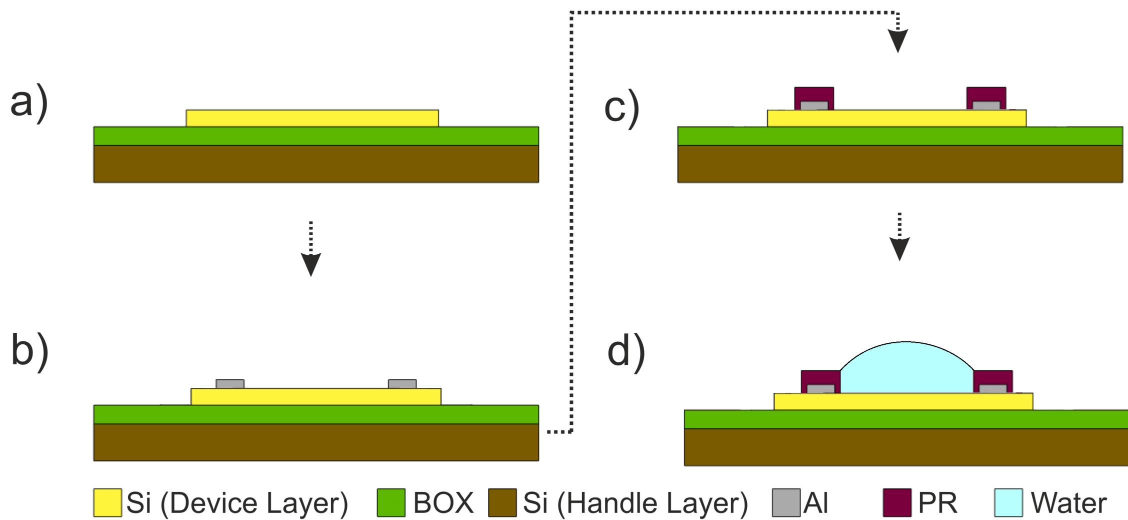

Figure 3.10. WG-FET fabrication steps for preliminary studies. a) Si is patterned on SOI wafer. b) Al source-drain electrodes are evaporated. c) Source-drain electrodes are insulated with PR. d) De-ionized water droplet is placed on top.

An important point is that when a metal and a semiconductor are brought together, the contact is not always ohmic, but depends on the work function difference of metal and semiconductor. Electron work function of Al is around 4.06-4.26 eV, whereas it is approximately 4.91 eV for a p-type Si with (100) surface. [87]

When a low work function metal is in contact with a higher work function semiconductor, their band diagram takes the form given in Figure 3.11. Energy bands of the semiconductor bend to make Fermi levels equal. Therefore, a depletion region is formed in the semiconductor surface which results in a rectifying contact. [88]

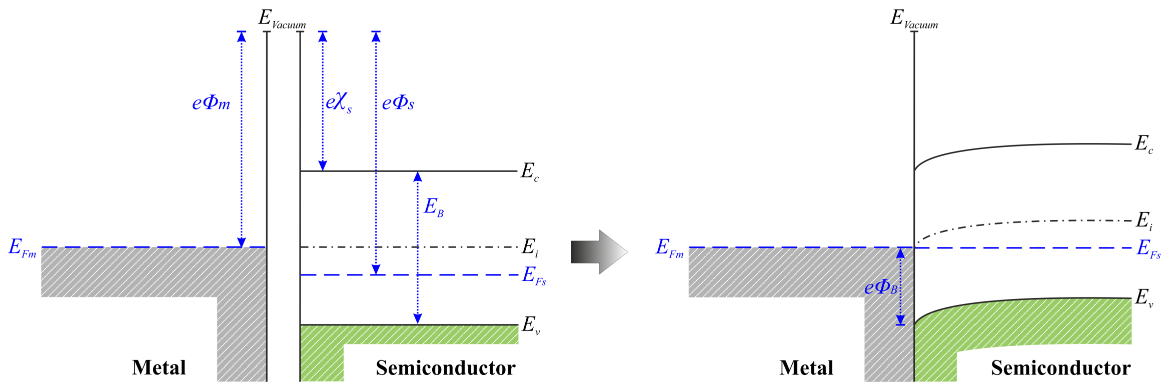

Figure 3.11. Energy band diagram of a low work function metal with a higher work function p-type semiconductor when they are in contact.

This phenomenon is called as Schottky-Mott rule. An energy barrier which is also known as Schottky barrier, $e\Phi_B$, occurs to prevent hole injection from metal to semiconductor. According to Schottky-Mott rule, height of Schottky barrier can be calculated as

$$e\Phi_B = e\chi_s + E_B - e\Phi_m \tag{3.29}$$

where E_B is band gap, and χ_s is the electron affinity of the semiconductor. Although Schottky-Mott rule explains energy band behavior well, it is based on an ideal junction with abrupt termination of semiconductor crystal. However, in practice, that kind of

termination creates surface states in the band gap due to dangling bonds and other discontinuities. Existence of these surface states results in pinning of Fermi level to a fixed point in band gap. This phenomenon is called Fermi level pinning, and it predicts the energy barrier height as

$$e\Phi_B \approx \frac{1}{2}E_B \tag{3.30}$$

regardless of the type of metal. [89] Either way, this energy barrier problem should be handled to obtain proper source-drain contacts.

One way of obtaining ohmic contact in such a situation is annealing. When the metal/semiconductor contact is annealed, metal atoms diffuse into the p-type semiconductor and create a highly-doped p^{++} region in the vicinity of metal surface. This region narrows down the depletion region formed due to band bending, and allows charge carriers to tunnel through. [90] Therefore, annealing of source-drain contacts is a crucial step for WG-FET fabrication. [91]

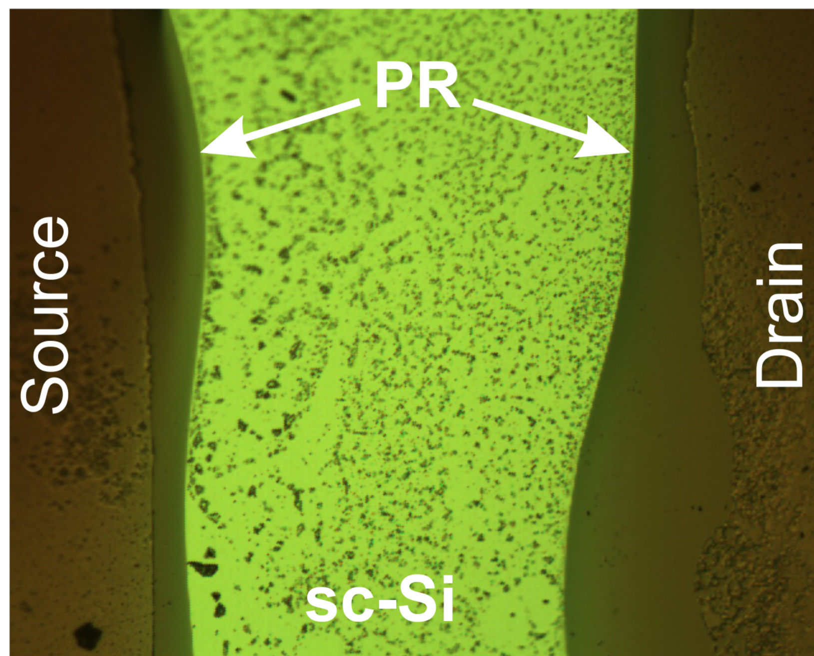

Figure 3.12. A micrograph of a fabricated sample for preliminary studies.

A micrograph of a fabricated sample is given in Figure 3.12. Fabricated transistor had approximately a width of 3,85 mm and a length of 0,6 mm. PR overlapped Si area was not uniform due to manual processing, but it was around 50-100 μm.

3.3.2. Experimental Results

<u>3.3.2.1. Transistor Characterization.</u> Current-voltage characteristic measurements of fabricated samples were performed with Keithley 4200SCS semiconductor parameter analyzer system. A picture of test setup is given in Figure 3.13.

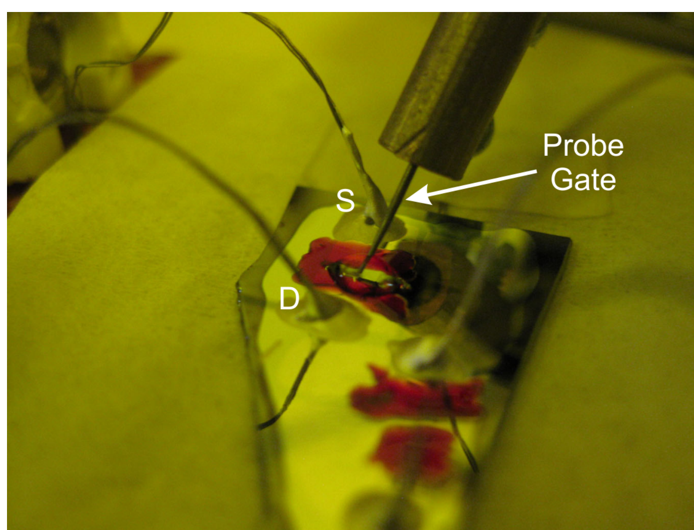

Figure 3.13. Experimental setup of preliminary studies.

Obtained $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$ graphs are given in Figure 3.14 and 3.15, respectively. Applied voltage values were limited to 1.0 V to ensure staying in non-Faradaic region.

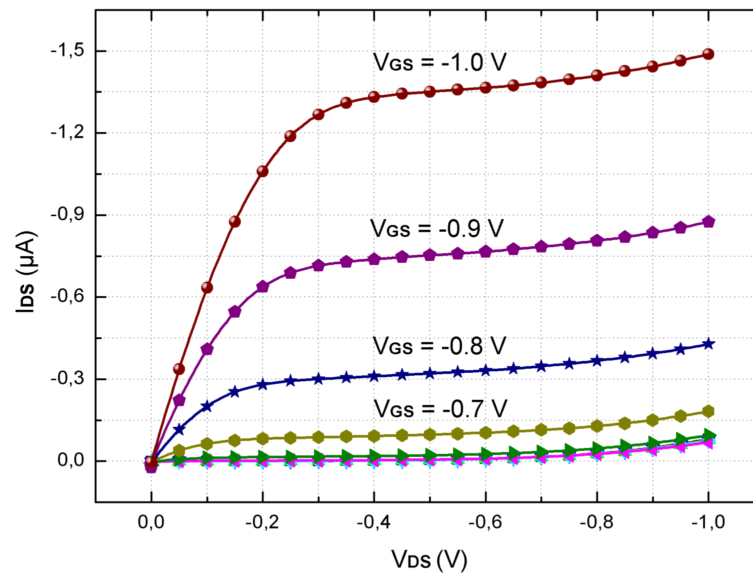

Figure 3.14. $I_{DS} - V_{DS}$ graph for fabricated WG-FET device.

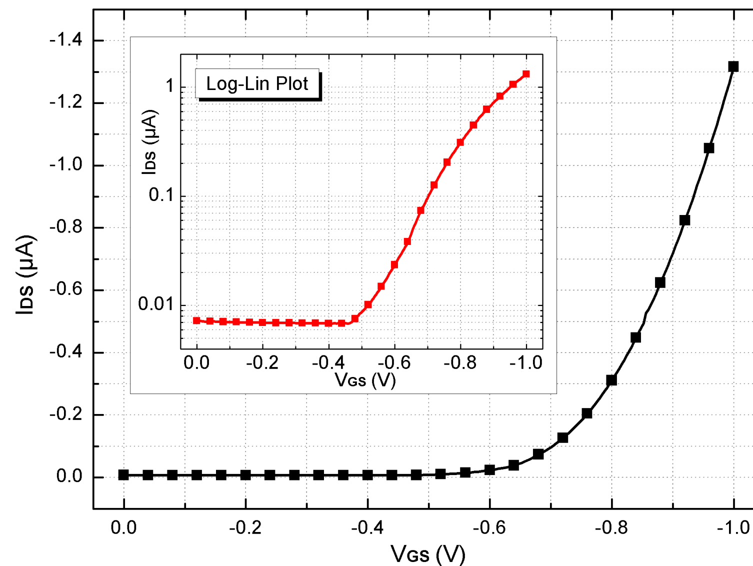

Figure 3.15. $I_{DS} - V_{GS}$ graph for fabricated WG-FET device. Subgraph is the same data in logarithmic scale. Measurement was performed for $V_{DS} = -0.5$ V.

From $I_{DS}-V_{DS}$ measurements, on- and off-currents, I_{ON} and I_{OFF}, were obtained as 1.49 μA and 80.85 nA, respectively, which gave an ON/OFF ratio of approximately 18 A/A for $V_{DS} = -1.0$ V. For $V_{DS} = -0.5$ V, I_{ON} decreased to 1.35 μA whereas I_{OFF}

became 4.5 nA which corresponds to an ON/OFF ratio of 300 A/A. For threshold voltage, V_{th}, $\sqrt{I_{DS}} - V_{DS}$ graph was used as in Figure 3.16. V_{th} was calculated as -0.61 V.

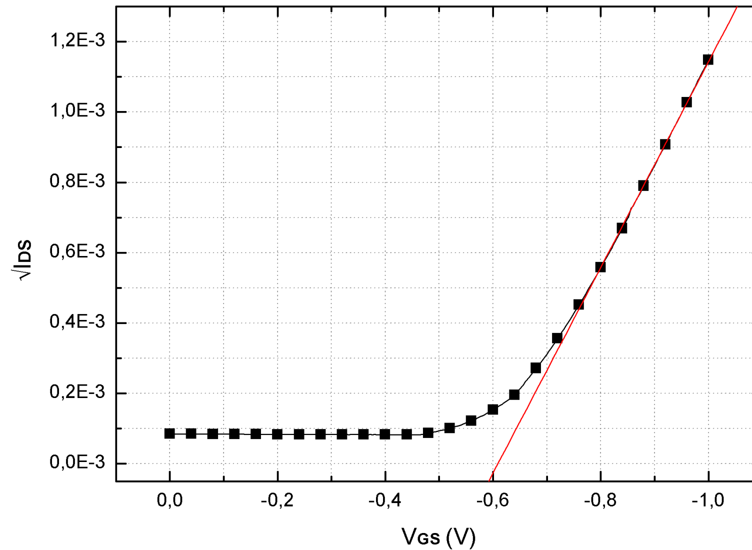

Figure 3.16. $\sqrt{I_{DS}} - V_{GS}$ graph for fabricated WG-FET device.

3.3.2.2. Remarks. Preliminary tests were done with only probe-gate setup. Despite poor device performance, first experiments were successful as a proof of concept.

3.4. First Generation WG-FET Devices

After preliminary hand-made sample experiments, a photolithographic fabrication process was designed to produce more reliable samples. Transistors were designed with separate active areas to prevent possible fringing fields or cross-talk.

3.4.1. Fabrication

A three-mask process was designed for WG-FET fabrication. First mask was used to pattern Si to form separate active areas. Second mask was used to pattern Al layer to form drain, source and planar-gate electrodes. Third mask was used for

insulating source and drain electrodes from water and also for forming a hydrophobic ring to hold water droplet on the active area of transistor. Layout of first generation WG-FET device is given in Figure 3.17.

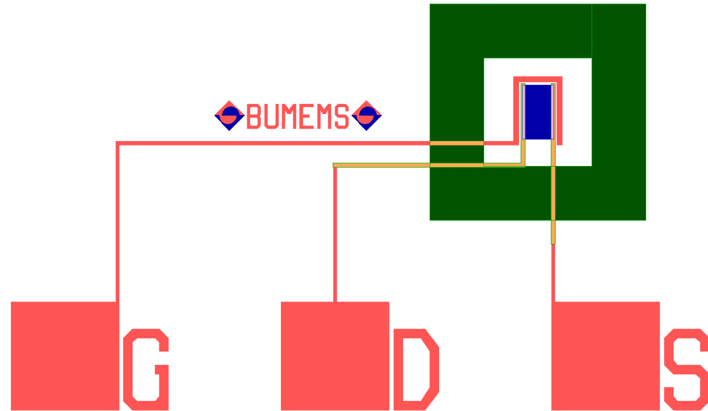

Figure 3.17. Layout of first generation WG-FET device.

First, Si was patterned with Trilogy etch ($126HNO_3$: $60H_2O$: $5NH_4F$). It was prepared with 126 ml of HNO_3, 65 ml of H_2O and 5.5 g of NH_4F. It did not attack the oxide much and gave clean and uniform etch results. Active Si areas were 1 mm x 500 μm rectangular shapes, so they had W/L ratio of 2. Then, Al layer was evaporated on the surface with approximately 200 nm thickness. Source and drain electrodes were 60 μm-thick whereas gate electrode had thickness of 100 μm. Planar gate distance to the active area was 40 μm due to mask resolution concerns.

After patterning of Al layer, samples were annealed to obtain ohmic contacts. Annealing was done in the vacuum chamber under continuous argon blow to prevent possible contamination. It started at 20 °C and ramped up to 450 °C in 15 min. Then the heater was turned off and samples were left to cooling. In 30-45 min time, temperature went down to around 100 °C and samples were left to cool down to room temperature.

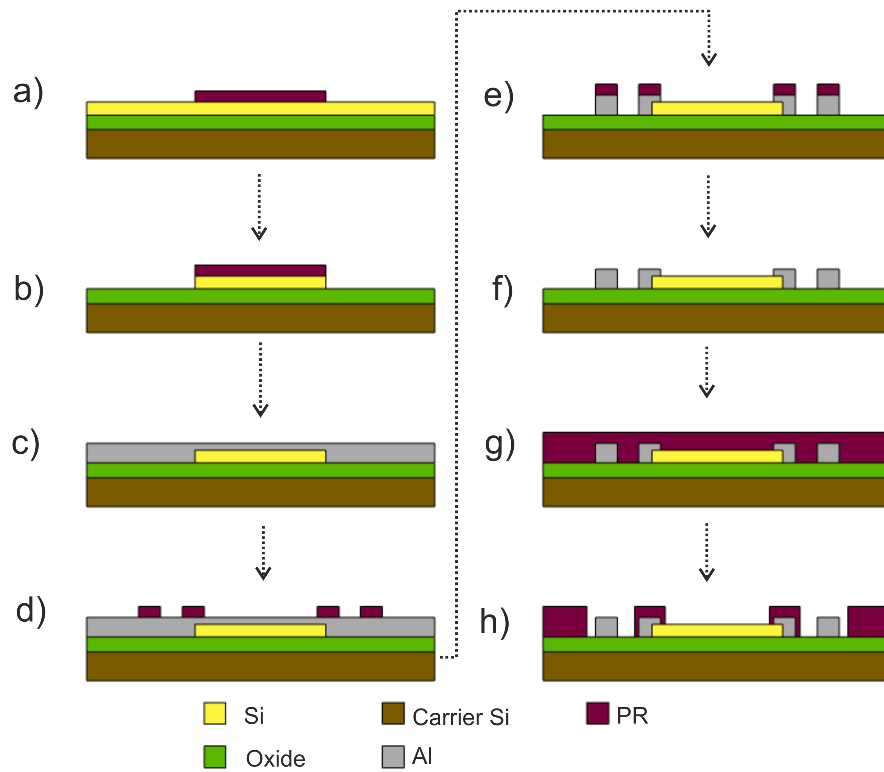

Figure 3.18. WG-FET fabrication. a) PR mask for Si etch. b) Patterning of Si. c) Al deposition. d) PR mask for Al etch. e) Patterning of source, drain and planar-gate electrodes. f) Annealing. g) PR deposition. h) Source-drain insulation.

Annealed samples were coated with PR1828 photoresist with approximately 4 μm thickness. Alignment of insulation layer was a problem because overlapping of photoresist layer with the active Si area narrowed the gate controlled region, which in turn introduced parasitic series resistances to the channel. For insulation of 60 μm-wide source and drain electrodes, 80 μm-wide insulation patterns were used. Fabrication steps are summarized in Figure 3.18, and a micrograph of a fabricated WG-FET device can be seen in Figure 3.19.

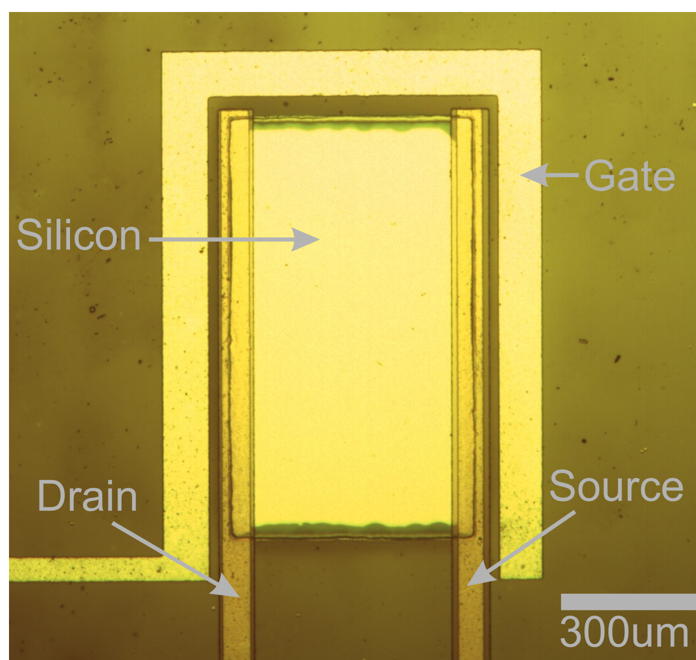

Figure 3.19. A micrograph of a fabricated first generation WG-FET device.

3.4.2. Experimental Results

After forming insulation layer and droplet holder ring, electrical contacts were made with silver epoxy. A de-ionized water droplet was placed on top of the active Si area and electrical measurements were performed with both probe- and planar-gate setups. However, results were not satisfactory. Neither probe- nor planar-gate setups gave reasonable transistor characteristics. Obtained channel current values were so small that they were indistinguishable from noise.

3.5. Second Generation WG-FET Devices

Second generation WG-FET devices were designed with a W/L ratio to 20. The idea was increasing the current to obtain more stable results on characteristic measurements.

3.5.1. Fabrication

Fabrication steps were similar with the first generation, except the width of the transistor was increased to 10 mm without changing the length. Active Si area was divided into four segments to preserve square shape for water droplet placement. Layout of second generation WG-FET device is given in Figure 3.20.

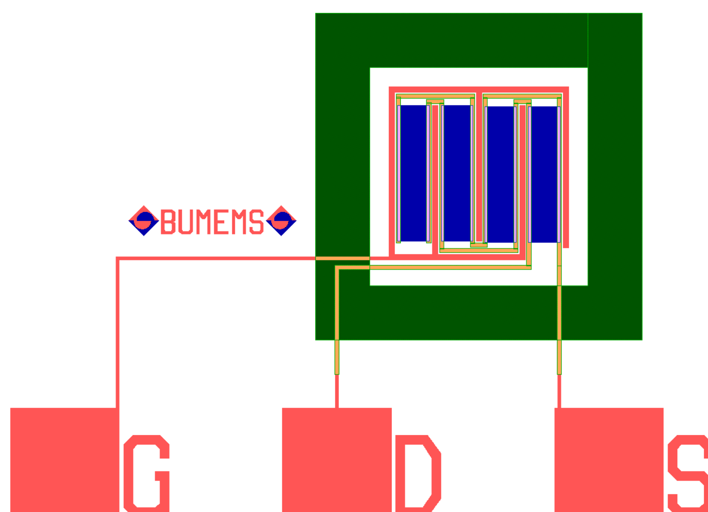

Figure 3.20. Layout of second generation WG-FET device.

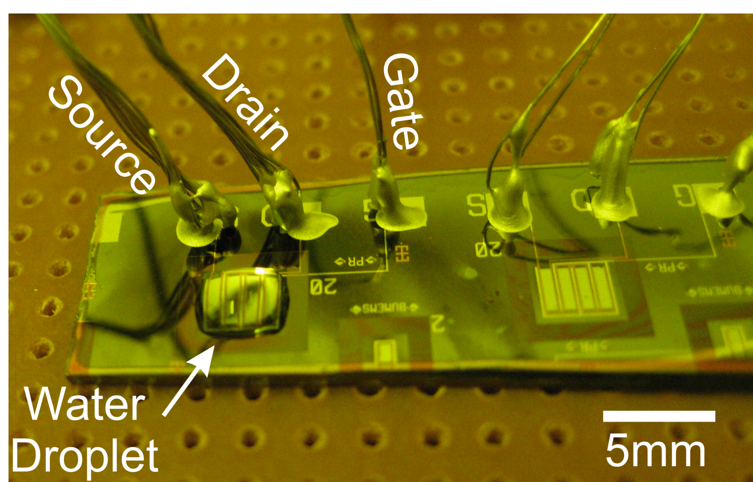

Figure 3.21. Test setup for a second generation WG-FET device.

3.5.2. Experimental Results

3.5.2.1. Transistor Characterization. A picture of a test setup for a second generation WG-FET device is given in Figure 3.21. First, probe-gate tests were performed. Applied voltages were limited with 0.7 V. Obtained $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$ graphs are given in Figure 3.22 and 3.23, respectively.

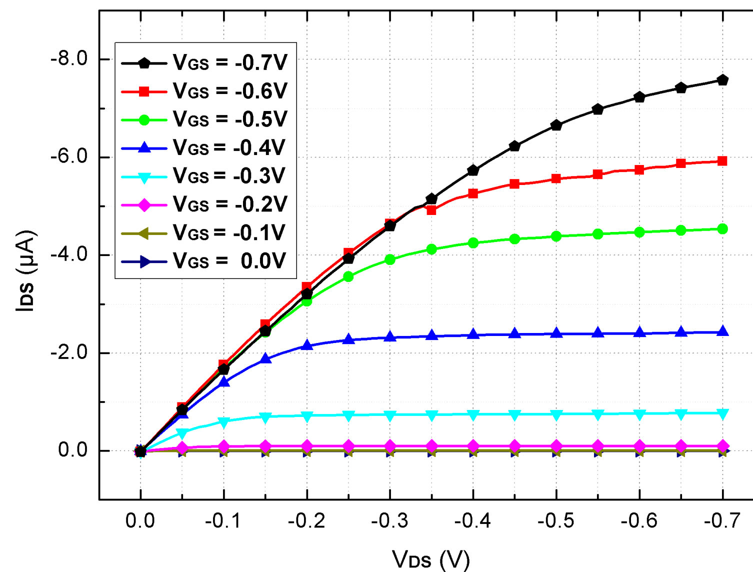

Figure 3.22. $I_{DS} - V_{DS}$ graph for second generation WG-FET device with probe-gate setup.

From $I_{DS} - V_{DS}$ measurements, on- and off-currents, I_{ON} and I_{OFF}, were obtained as 7.57 μA and 0.55 nA, respectively, which gave an ON/OFF ratio of approximately 14,000 A/A for $V_{DS} = -0.7$ V. Results were considerably better with respect to the preliminary hand-made samples. However, there were some difficulties during $I_{DS} - V_{GS}$ measurements. Device characteristics showed a deterioration with consecutive measurements, and obtained I_{DS} values were not consistent with $I_{DS} - V_{DS}$ measurements. Therefore, $I_{DS} - V_{GS}$ relationship was extracted from $I_{DS} - V_{DS}$ data.

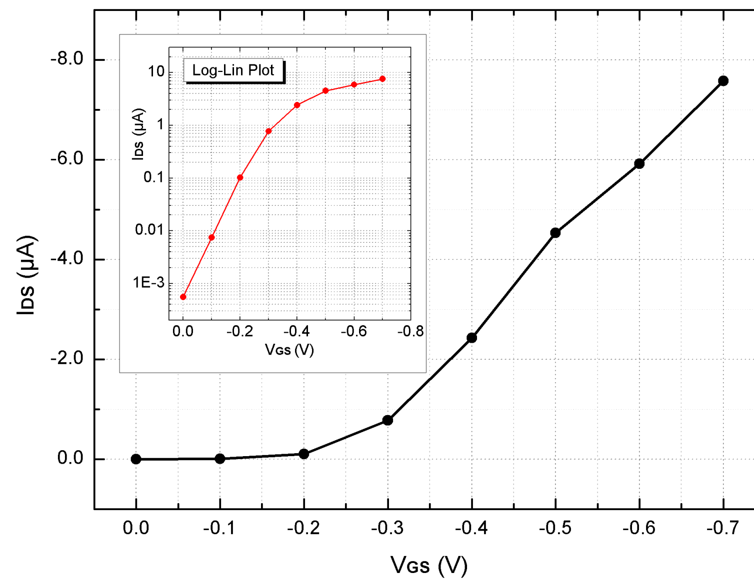

Figure 3.23. $I_{DS} - V_{GS}$ graph for second generation WG-FET device with probe-gate setup. Subgraph is the same data in logarithmic scale. For $V_{DS} = -0.7$ V.

For threshold voltage, V_{th}, $\sqrt{I_{DS}} - V_{DS}$ graph was used as in Figure 3.24. V_{th} was calculated as -0.16 V.

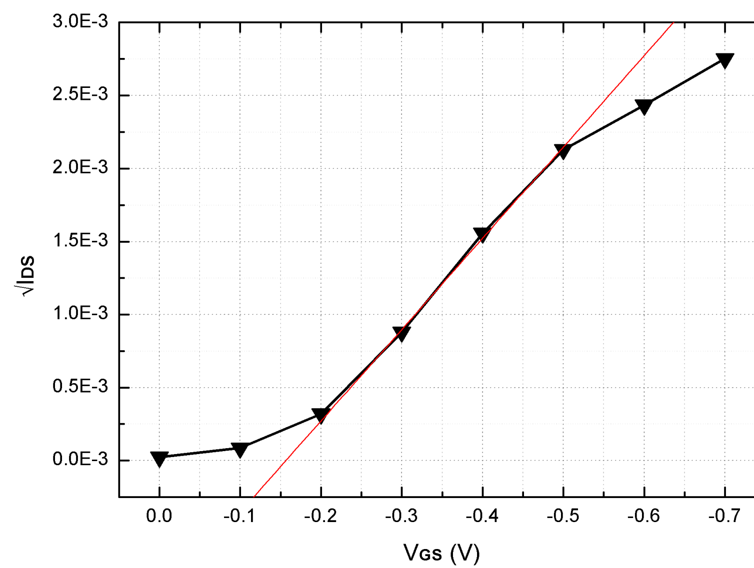

Figure 3.24. $\sqrt{I_{DS}} - V_{GS}$ graph for second generation WG-FET device with probe-gate setup.

After probe-gate setup measurements, planar-gate setup was tested. Same test conditions with probe-gate setup were applied for comparison. Obtained $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$ curves are given in Figure 3.25 and 3.26, respectively.

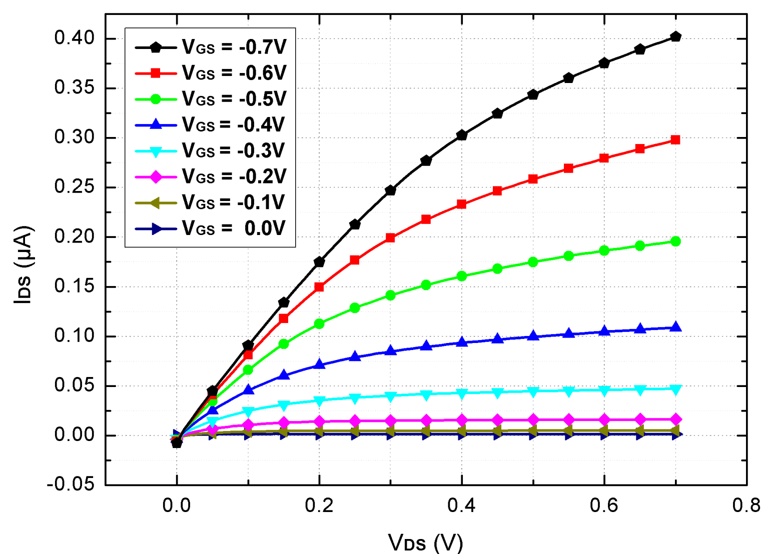

Figure 3.25. $I_{DS} - V_{DS}$ graph for second generation WG-FET device with planar-gate setup.

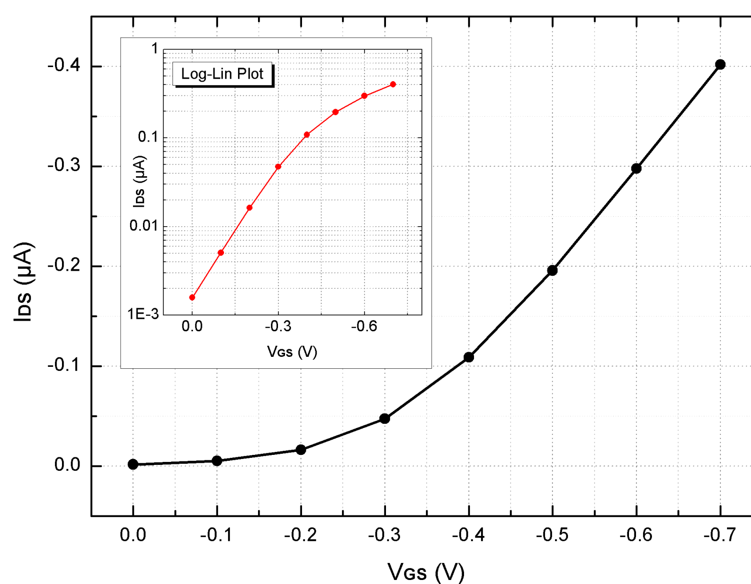

Figure 3.26. $I_{DS} - V_{GS}$ graph for second generation WG-FET device with planar-gate setup. Subgraph is the same data in logarithmic scale. For $V_{DS} = -0.7$ V.

From I_{DS}−V_{DS} measurements, on- and off-currents, I_{ON} and I_{OFF}, were obtained as 0.4 μA and 1.58 nA, respectively, which gave an ON/OFF ratio of approximately 250 A/A for $V_{DS} = -0.7$ V. Although it was inferior to probe-gate ON/OFF ratio, it demonstrated that WG-FET device could work with planar-gate topology. Difficulties experienced during $I_{DS} - V_{GS}$ measurements with probe-gate setup were also encountered with planar-gate. Device characteristics deteriorated even more severely with consecutive measurements. Again, $I_{DS} - V_{GS}$ relationship was extracted from $I_{DS} - V_{DS}$ data.

For threshold voltage, V_{th}, $\sqrt{I_{DS}} - V_{GS}$ graph was used as in Figure 3.27. V_{th} was calculated as −0.14 V.

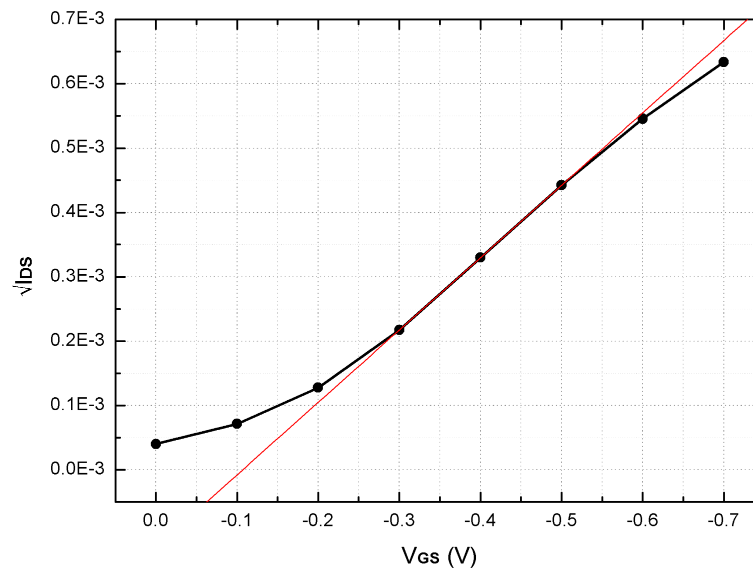

Figure 3.27. $\sqrt{I_{DS}} - V_{GS}$ graph for second generation WG-FET device with planar-gate setup.

3.5.2.2. Remarks. Experiments demonstrated that WG-FET device with probe-gate setup fabricated with photolithographic process showed better transistor characteristics with respect to preliminary hand-made samples. It had a significantly lower threshold voltage (−0.16 V vs. −0.61 V) and a better ON/OFF ratio (14,000 A/A vs. 300 V/V). Planar-gate setup had an ON/OFF ratio of 250 A/A which was inferior

compared to its probe-gate counterpart, but comparable with the preliminary sample results. It also had a similar V_{th} of -0.14 V with probe-gate setup.

$I_{DS} - V_{GS}$ measurements were problematic with both probe- and planar-gate setups in second generation WG-FETs. In probe-gate setup, device characteristics were deteriorating with consecutive measurements, therefore current levels in $I_{DS} - V_{GS}$ measurements were considerably lower than the data of $I_{DS} - V_{DS}$ measurements. In planar-gate setup, the situation was more drastic that current levels dropped to noise levels in experiments which prevented to obtain proper $I_{DS} - V_{GS}$ data. Yet, second generation WG-FET devices were important for showing a performance boost in probe-gate setup with photolithographic fabrication process, and demonstrating that they could also work with planar-gate electrodes. [92]

3.6. Third Generation WG-FET Devices

Improving the planar-gate setup to achieve better performance characteristics was the focus of third generation WG-FET devices.

3.6.1. Fabrication

Several transistor layouts were designed to examine effects of variables such as gate distance, gate shape and bulk contact on the transistor performance. Corresponding layouts are given in Figure 3.28.

Layout G stood for the design of second generation WG-FET device. W/L ratio was kept as 20 with length of 500 μm and width of 10 mm. Fingered structure was also kept for compactness. Only difference was the distance between gate electrode and source-drain electrodes which was increased to 150 μm. In *Layout H* and *I*, gate distances were increased to 300 μm and 600 μm, respectively, where other variables were kept unchanged.

In *Layout D*, gate electrode area was extended to cover all interior of droplet holder ring with a gate distance of 150 μm. In *Layout E* and *F*, gate distances were increased to 300 μm and 600 μm, respectively.

In *Layout A*, gate electrode did not circle around the active area. Only parts, which were perpendicular to current flow direction, were left open to liquid contact whereas other parts were insulated. Purpose of that layout was to test any possible effect of gate electrode geometry on device performance. Again, in *Layout B* and *C*, gate distances were increased to 300 μm and 600 μm, respectively.

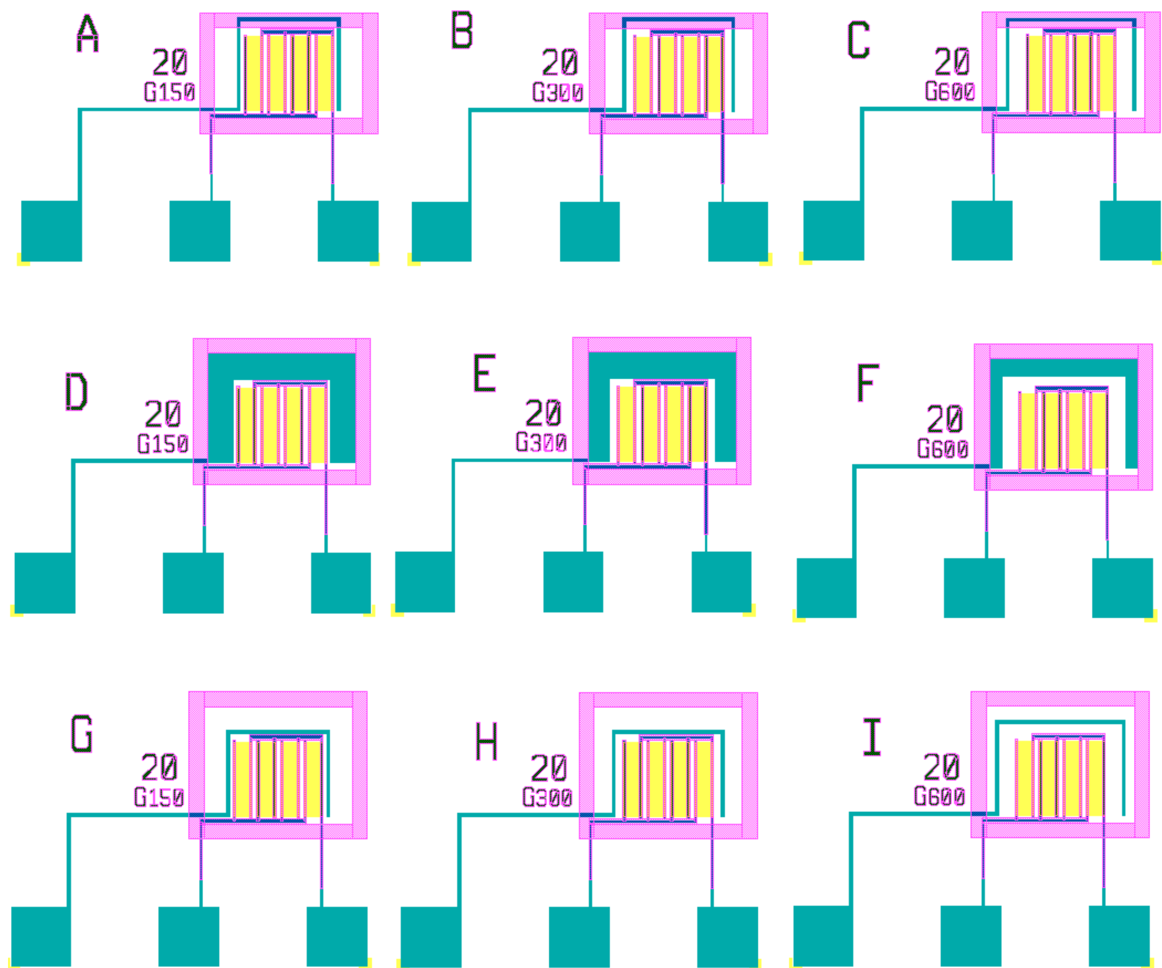

Figure 3.28. Layouts of third generation WG-FET devices.

Using those designs, samples were fabricated and tested. Bulk contacts were also added to fabricated devices.

3.6.2. Experimental Results

A more elaborate test setup as seen in Figure 3.29 was used for experiments of third generation WG-FET devices. In every test sample, there were two transistors of the same design.

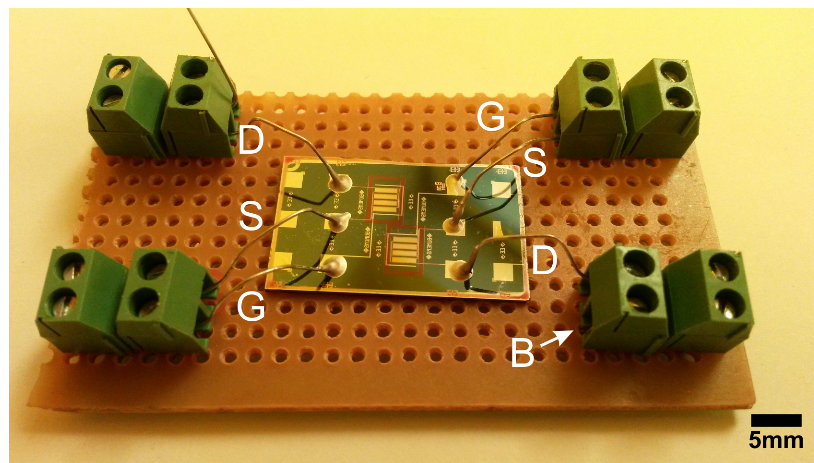

Figure 3.29. Test setup for third generation WG-FET devices.

3.6.2.1. Bulk Contact. First, bulk contact was tested. Back sides of samples were scratched to pass the oxide layer, and an electrical contact was established with handle silicon by using silver epoxy. A sample was prepared with two bottom contacts with separation of approximately 1 cm and current-voltage measurements were performed. Although contacts were not completely ohmic due to low doping of silicon and absence of annealing, handle silicon was not left floating for transistor characterization tests. Results were given in Figure 3.30.

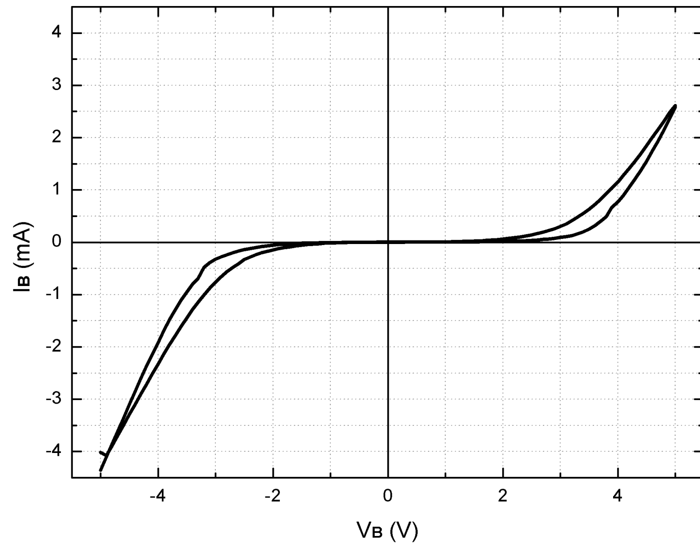

Figure 3.30. $I - V$ measurement of bulk contacts.

3.6.2.2. Resistance Without Water. Active Si area of the transistor was a 16-nm-thick single crystalline silicon with Boron doping of approximately 10^{15} cm^{-3}. With W/L ratio of 20, resistance between source and drain contacts without the water droplet was calculated as approximately 400 kΩ. However, different samples under test showed resistance values varying in a wide range between 15 kΩ to 750 kΩ. That kind of variation with a smaller range was observed in the same sample when the measurements were done in different days. An interesting note was that samples with best transistor performance showed resistance values between 30 kΩ to 60 kΩ. Those observations suggested that Si surface was affected by environment even without the water droplet.

3.6.2.3. Effect Of Gate On Channel Resistance. Effects of planar-gate electrode on the dry channel resistance was also tested. First, resistance measurement were performed without applying any voltage on planar-gate. V_{DS} was varied from 0 V to -0.7 V whereas source electrode and bulk were grounded. Similar current-voltage curves were obtained from consecutive measurements. Results were given in Figure 3.31.

Then, a constant -0.7 V was applied on planar-gate electrode, and the experiment was repeated. Obtained I-V curves showed that, after application of gate potential, channel resistance was considerably lower with respect to the floating gate case, and it continued to decrease slightly with each consecutive measurement. Results are given in Figure 3.32.

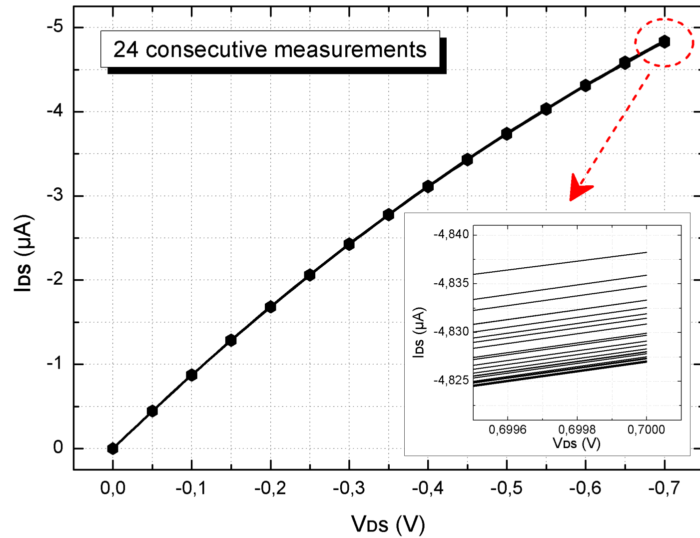

Figure 3.31. Dry measurement of $I_{DS} - V_{DS}$ without applying any voltage on planar-gate.

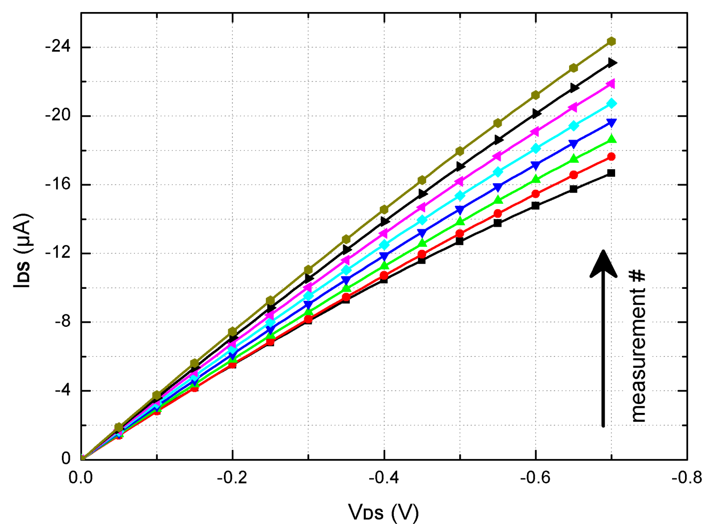

Figure 3.32. Dry measurement of $I_{DS} - V_{DS}$ with applying -0.7 V on planar-gate.

The experiment continued for 100 consecutive measurements, and channel resistance value was nearly halved at the end. Observed resistance trend is shown in Figure 3.33.

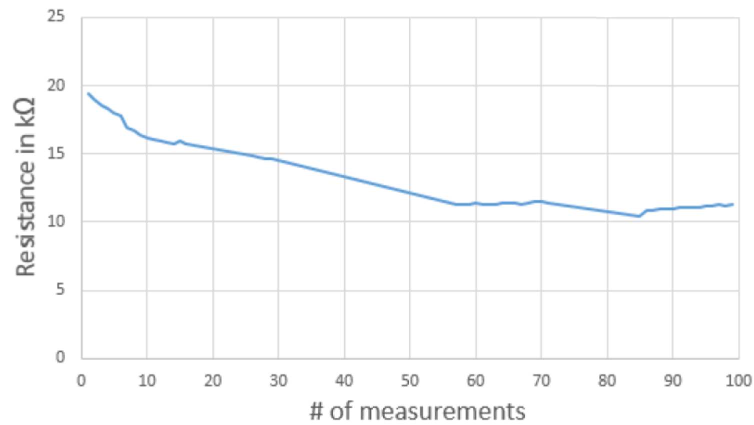

Figure 3.33. Channel resistance trend with planar-gate setup.

Those results suggested a possible charge trapping at thin Si/buried oxide interface. Planar-gate could be acting as a back-gate in spite of the oxide layer. We tried to ground all electrodes before each measurement to bleed out possible charge accumulation but it had no effect on the results.

Table 3.1. Effect of bulk potential on channel resistance.

Bulk Voltage (V_{BS})	**Resistance**
+7.0 V	1 MΩ
+2.5 V	40 kΩ
+0.7 V	20 kΩ
0 V	14 kΩ
−0.7 V	10 kΩ
−2.5 V	7.5 kΩ
−7.0 V	3 kΩ

<u>3.6.2.4. Effect Of Bulk On Channel Resistance.</u> Effects of bulk contact were also investigated. When voltage values higher than 7 V were applied to bulk contact, it resulted in electrolysis in the water droplet. Bubbles were observed and aluminium contacts were etched. Therefore, bulk contact voltages were limited with 7 V. In Table 3.1, applied bulk voltages (V_{BS}) and corresponding channel resistances are given. All measurements were performed without the water droplet. Although there was a thick (140 nm) buried oxide layer, bulk contact was effective on channel resistance with reasonable voltage values.

<u>3.6.2.5. Environmental Effects.</u> After bulk contact tests, vacuum chamber experiments were performed to test environmental effects. First measurements were performed in argon environment under 3 Torr pressure. V_{DS} was swept from 0 V to -0.7 V, while a constant -0.7 V was applied to planar-gate electrode. All measurements were performed without the water droplet. Maximum I_{DS} value increased around 300 nA in 48 consecutive measurements. Results are given in Figure 3.34.

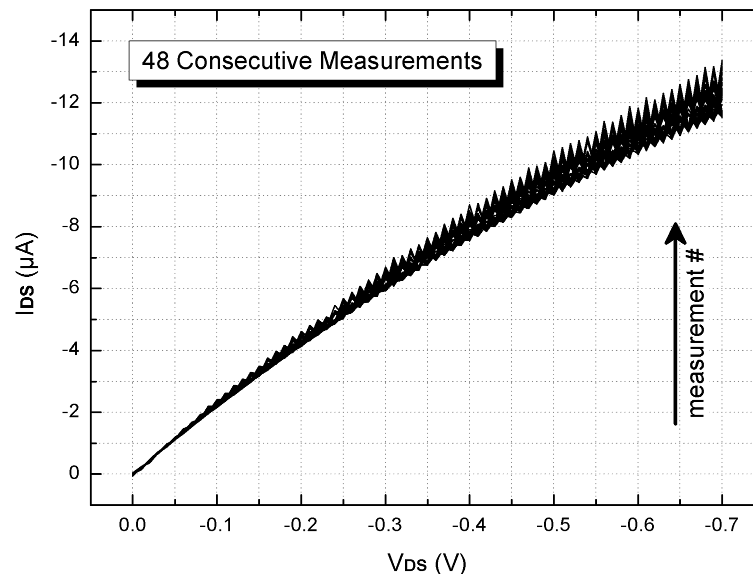

Figure 3.34. Dry measurement of $I_{DS} - V_{DS}$ in vacuum with applying -0.7 V on planar-gate.

Then, vacuum was broken and the seal was opened. The experiment was repeated. That time, maximum I_{DS} value increased around 4 μA in 48 consecutive measurements. Results are given in Figure 3.35.

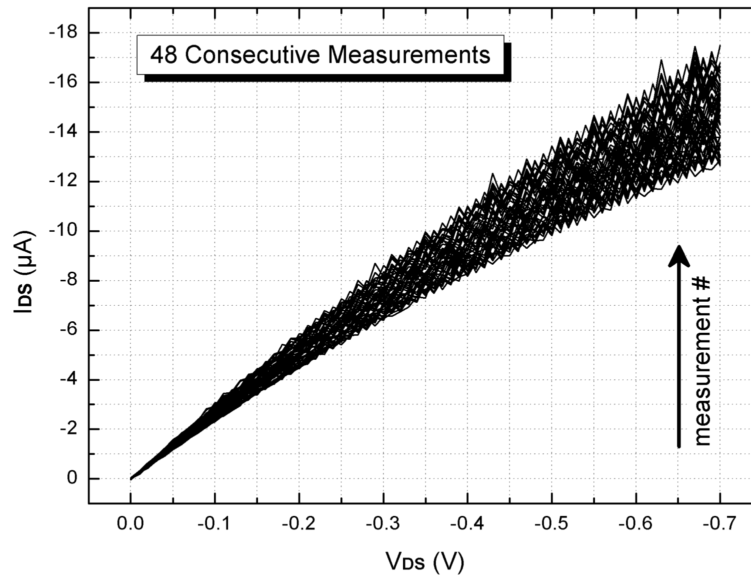

Figure 3.35. Dry measurement of $I_{DS} - V_{DS}$ after vacuum was broken. -0.7 V was applied on planar-gate.

Results showed that when no water droplet was applied on active area, variation in maximum I_{DS} current was an order of magnitude higher in open environment with respect to the situation under vacuum.

For further investigation of environmental effects, an experimental setup was prepared in open environment. First, sample was slightly covered with an aluminium foil and resistance measurements were performed. Then, cover was removed and measurements were continued in open environment. After the open environment measurement, a moderate cover was applied and the process was repeated. Following another open environment measurement, a tight cover was applied and reinforced with weight on it. With that firmly covered sample, resistance measurements were repeated and results of the whole experiment are given in Figure 3.36. For each region except the tightly covered one, same number of measurements were performed in equal amounts of time.

For tightly covered setup, measurements were continued for an additional 60 minutes.

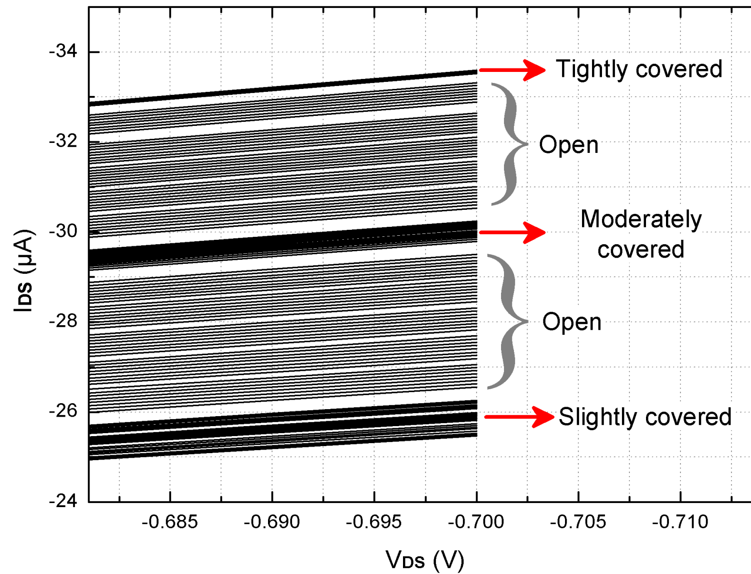

Figure 3.36. $I_{DS} - V_{DS}$ curves obtained from covered sample test.

$I_{DS} - V_{DS}$ curves in first region were obtained with slightly covered setup and they were followed by the open environment measurements. -0.7 V was applied to planar-gate electrode during the whole experiment. Second region corresponds to moderately covered setup and the third region corresponds to tightly covered setup. In slightly covered setup, increase in maximum I_{DS} value was 1.19 μA whereas it increased 2.9 μA in the following open environment part. In moderately covered setup, increase in the maximum I_{DS} value was 0.44 μA which was smaller than slightly covered setup. Second open environment part gave a maximum I_{DS} increase of 2.78 μA which was comparable with the first open environment results. However, in tightly covered setup, maximum I_{DS} value decreased for 0.07 μA and when the experiment was continued in that setup, maximum I_{DS} almost stood stable for another one hour of measurements.

Those findings were supporting the vacuum chamber results. Closed environment significantly reduced planar-gate induced resistance variations in test samples.

<u>3.6.2.6. Mixed Tests And Effect Of Time.</u> Cycles of application and removal of water droplet were further investigated. An experimental setup was used where $V_{DS} = V_{GS} = -0.7$ V and I_{DS} was measured with time intervals of 5 ms. Each data set included 21 data points and when a data set was completed, new measurement was started manually. First, experiment was performed with a dry sample in open environment. In Figure 3.37, obtained results are given.

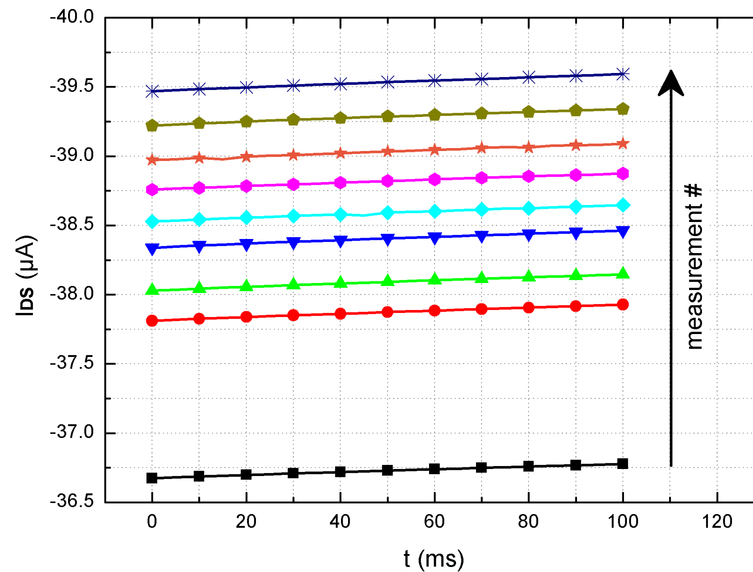

Figure 3.37. Dry sample open environment stress test.

Current value was increasing in consecutive measurements. An important observation was that the increase between the first and the second measurements was far greater than the other ones. The reason was that there was a 2-minute delay between the first and second measurement whereas other measurements were done one after another without any waiting period. In delay period, no voltage was applied to the sample, therefore we could conclude that degradation process was a function of time even in dry setup. Once a potential was applied to setup while planar-gate was active, the channel resistance started to change even in absence of potential stress.

Then, the sample under test was covered and the experiment continued. The behavior was similar but increase in current value was smaller as expected from previous experiments. Results are given in Figure 3.38.

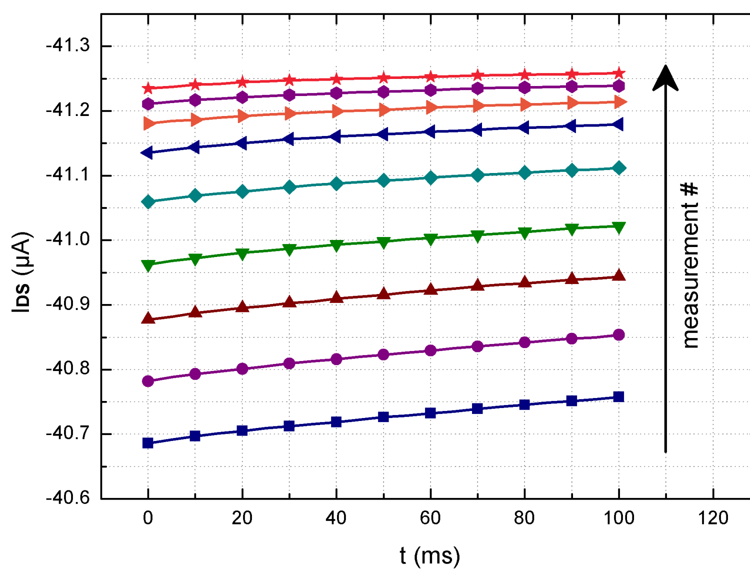

Figure 3.38. Dry sample with cover stress test.

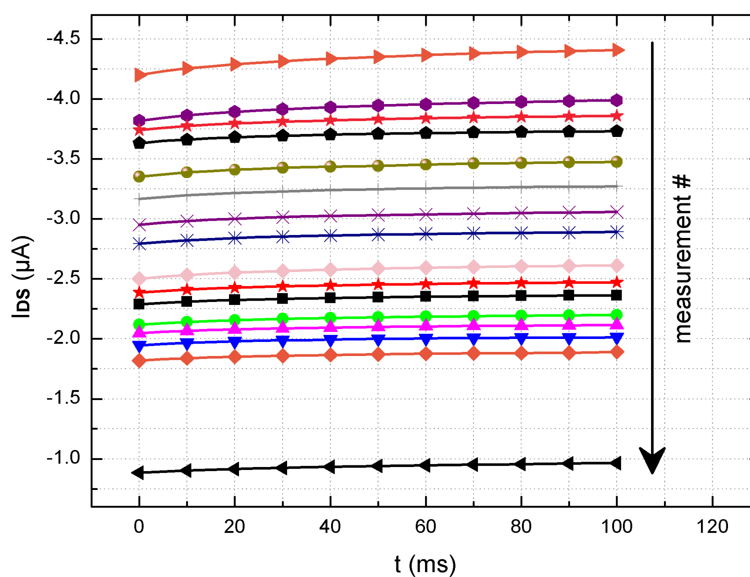

Figure 3.39. Sample with water droplet stress test.

Next, cover was removed and a de-ionized water droplet was placed on the Si active area. Existence of water droplet reverted the behavior. Current value started to decrease in consecutive measurements. Effect of time could also be seen in that setup. Before the last measurements, a 1-minute delay was applied and a greater difference was observed again. Results are given in Figure 3.39.

Although water droplet measurement started immediately after the dry measurement, starting current was -4.2 μA instead of the last I_{DS} value of previous measurements which was -41.3 μA. Application of water droplet decreased the current an order of magnitude. Then, water droplet was blown away and experiment continued with dry setup. I_{DS} started to increase again from the value which it had at the last measurement with water droplet. Same dry sample behavior was observed, but the current levels were similar with the water droplet test measurements. Results are given in Figure 3.40.

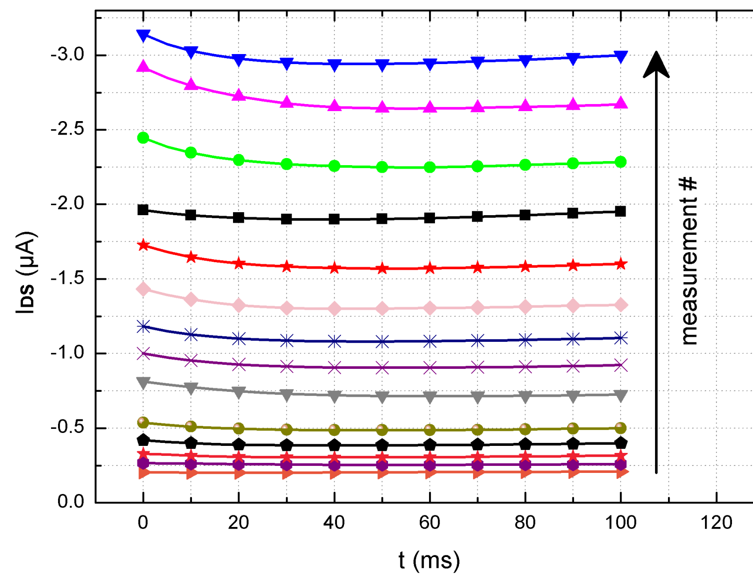

Figure 3.40. Stress test of the sample after water droplet was removed.

Experimental data showed that when the water droplet was blown away, dry sample behavior was observed in resistance characteristics. However, effect of water on the surface of Si active area could not be removed immediately, which was the

reason of obtaining I_{DS} levels of a sample with water droplet.

Another experiment was performed to test if water droplet itself was enough to start degradation without application of gate potential. First, a resistance test was done on sample without using the gate electrode. I_{DS} was measured approximately as -17 μA before placing the water droplet. Sample was left for 40 minutes with a droplet on it and then measurement was repeated. Results are shown in Figure 3.41.

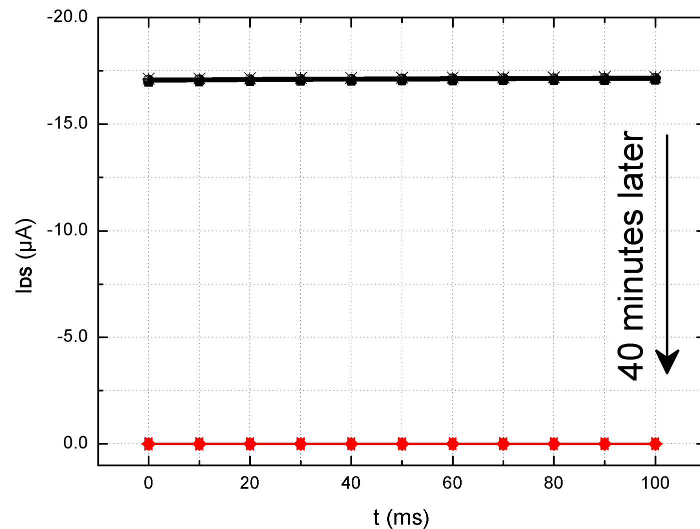

Figure 3.41. Degradation in I_{DS} with time in the presence of water droplet on the Si active area.

It could be seen that current went down almost to zero after 40 minutes even without application of potential to the planar-gate electrode. Therefore, contact with water droplet was enough to start degradation even without electrical operation.

3.6.2.7. Transistor Characterization. After dry tests, WG-FET devices were fabricated with layouts demonstrated in Figure 3.28 for transistor characterization. Best results were obtained with *Layout C*, *F*, and *I* with comparable performance characteristics. Yield of devices which fabricated with other layouts was low and testable ones showed poor performance except *Layout G*. Obtained $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$

graphs are given in Figure 3.42 and 3.43, respectively.

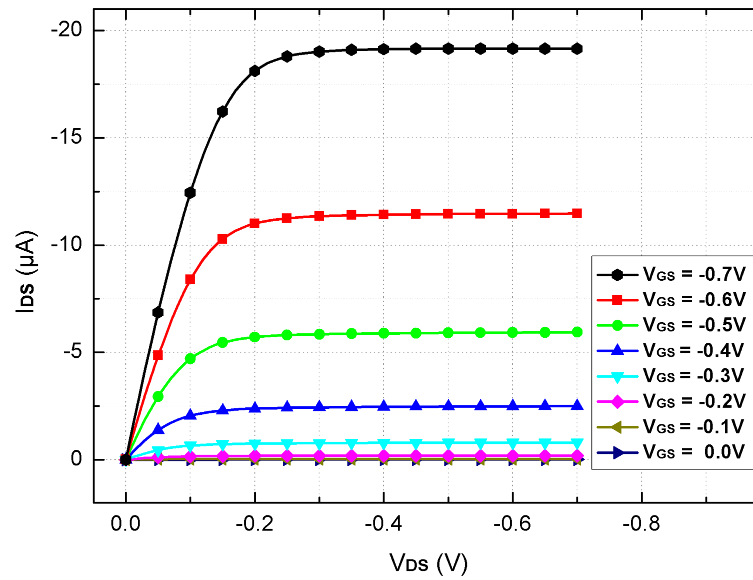

Figure 3.42. $I_{DS} - V_{DS}$ graph for third generation planar-gate WG-FET device fabricated with *Layout G*.

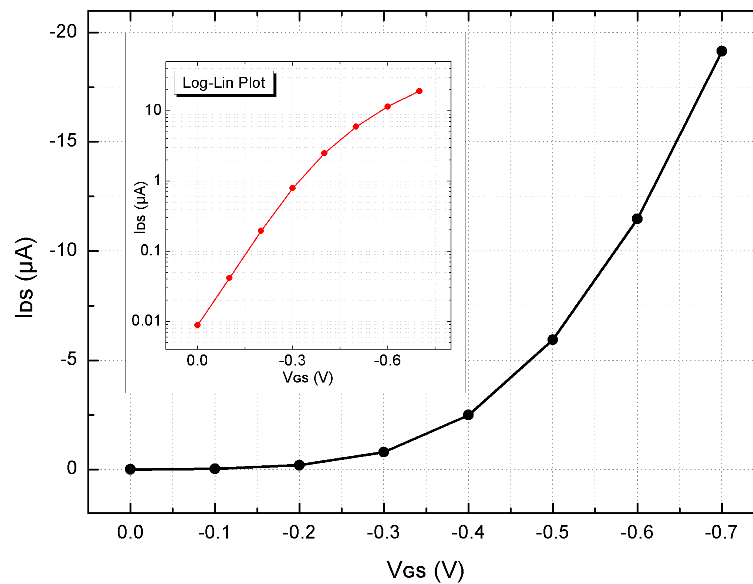

Figure 3.43. $I_{DS} - V_{GS}$ graph for third generation planar-gate WG-FET device fabricated with *Layout G*. Subgraph is the same data in logarithmic scale. For $V_{DS} = -0.7$ V.

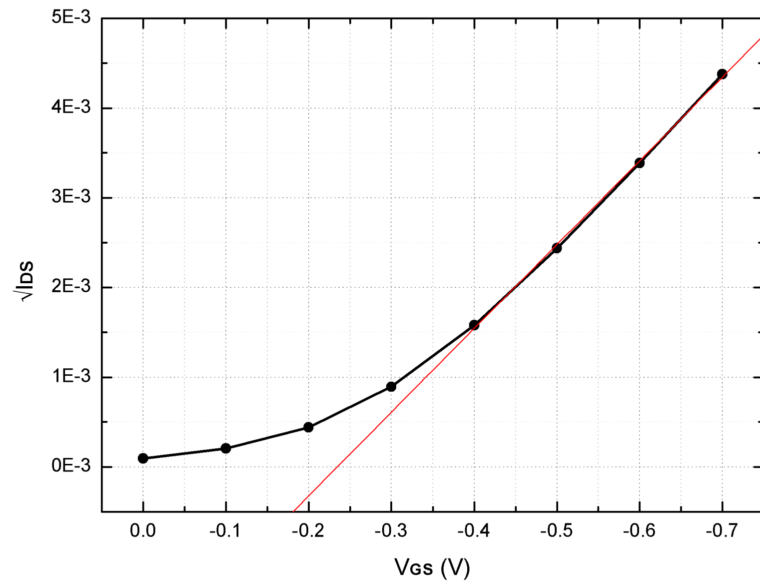

Figure 3.44. $\sqrt{I_{DS}} - V_{GS}$ graph for third generation planar-gate WG-FET device fabricated with *Layout G*.

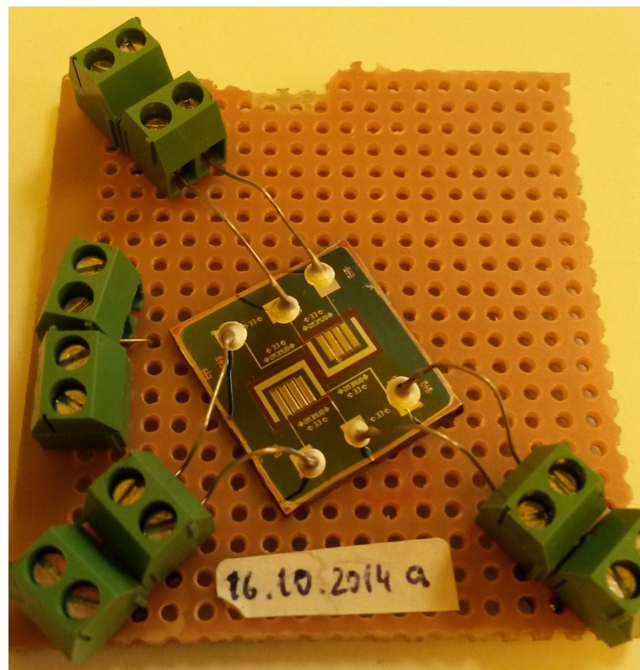

Figure 3.45. Experimental setup of third generation planar-gate WG-FET device fabricated with *Layout F*.

From $I_{DS} - V_{DS}$ measurements, I_{ON} and I_{OFF} were obtained as 19.15 μA and 8.91 nA, respectively, which gave an ON/OFF ratio of approximately 2,150 A/A for $V_{DS} = -0.7$ V. It was nearly ten-fold with respect to ON/OFF ratio of second generation planar-gate WG-FET. Device degradation based difficulties during $I_{DS} - V_{GS}$ measurements continued, so $I_{DS} - V_{GS}$ relationship was extracted from $I_{DS} - V_{DS}$ data. For threshold voltage, V_{th}, $\sqrt{I_{DS}} - V_{GS}$ graph was used as in Figure 3.44. V_{th} was calculated as -0.25 V.

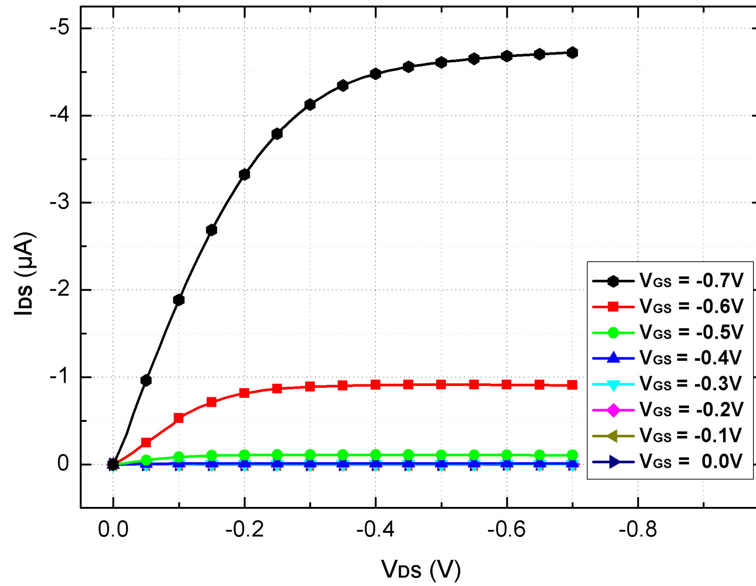

Figure 3.46. $I_{DS} - V_{DS}$ graph for third generation planar-gate WG-FET device fabricated with *Layout F*.

For comparison, $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$ graphs are given in Figure 3.46 and 3.47, respectively, for a third generation WG-FET device fabricated with *Layout F* as demonstrated in Figure 3.45.

From $I_{DS} - V_{DS}$ measurements, I_{ON} and I_{OFF} were obtained as 4.72 μA and 0.58 nA, respectively, which gave an ON/OFF ratio of approximately 8,140 A/A for $V_{DS} = -0.7$ V. Although it had a lower I_{ON}, ON/OFF ratio was better due to very low I_{OFF}. Again, $I_{DS} - V_{GS}$ relationship was extracted from $I_{DS} - V_{DS}$ data.

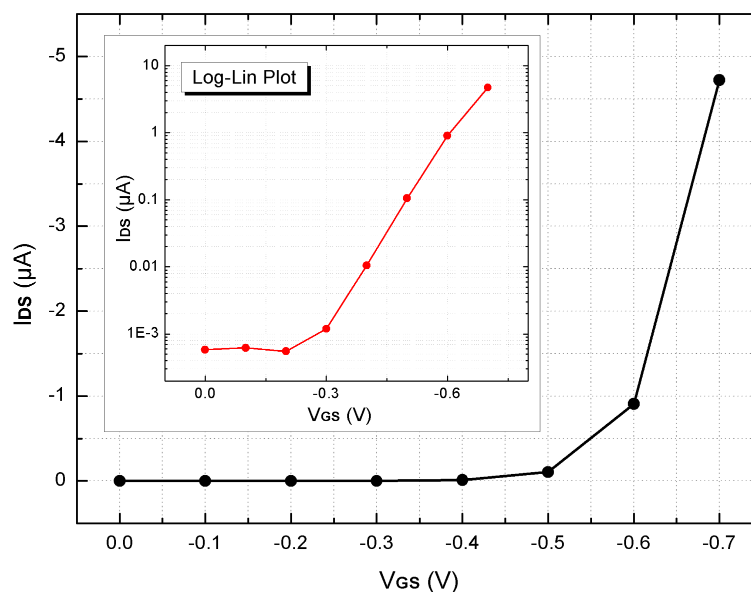

Figure 3.47. $I_{DS} - V_{GS}$ graph for third generation planar-gate WG-FET device fabricated with *Layout F*. Subgraph is the same data in logarithmic scale. For $V_{DS} = -0.7$ V.

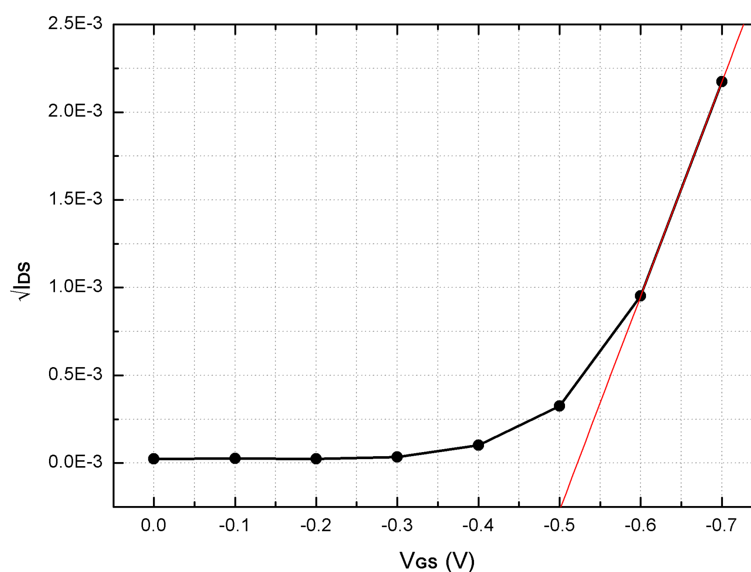

Figure 3.48. $\sqrt{I_{DS}} - V_{GS}$ graph for third generation planar-gate WG-FET device fabricated with *Layout F*.

For threshold voltage, V_{th}, $\sqrt{I_{DS}} - V_{GS}$ graph was used as in Figure 3.48. V_{th} was calculated as -0.52 V.

Table 3.2. Comparison of second and third generation planar-gate WG-FET devices.

	ON/OFF Ratio	$\mathbf{I_{D,max}}$	$\mathbf{V_{th}}$
2nd gen WG-FET	250 A/A	-0.4 μA	-0.14 V
3rd gen WG-FET (Layout G)	2,150 A/A	-19.15 μA	-0.25 V
3rd gen WG-FET (Layout F)	8,140 A/A	-4.72 μA	-0.52 V

In Table 3.2, a comparison of second and third generation planar-gate WG-FET devices is given.

<u>3.6.2.8. Gate Position Experiments.</u> Gate position and distance were examined. At first, probe gate setup was used for examination.

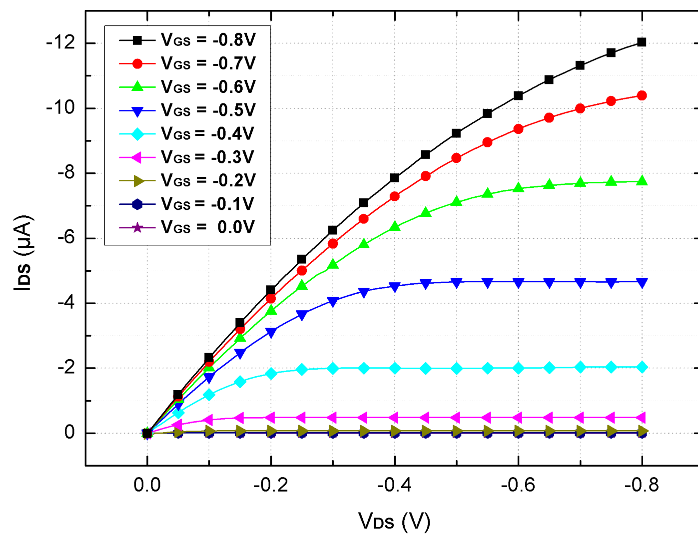

Figure 3.49. $I_{DS} - V_{DS}$ graph when the probe-gate was at the center.

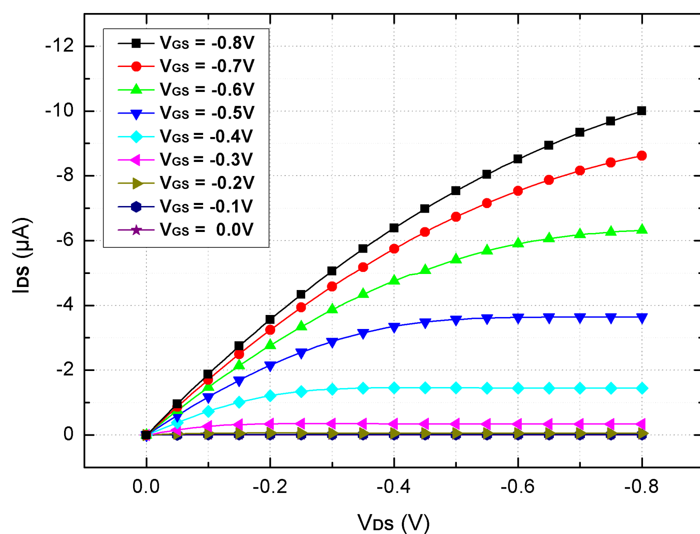

Figure 3.50. $I_{DS} - V_{DS}$ graph when the probe-gate was moved slightly to the side.

Probe was immersed into de-ionized water droplet and positioned at the center of the Si active area. $I_{DS} - V_{DS}$ measurements were performed with that configuration. Then, probe was moved approximately 2-3 mm to the side of droplet and measurements were repeated. After that, probe was relocated to the first position and measurements were performed. Results are given in Figure 3.49, 3.50, and 3.51, respectively.

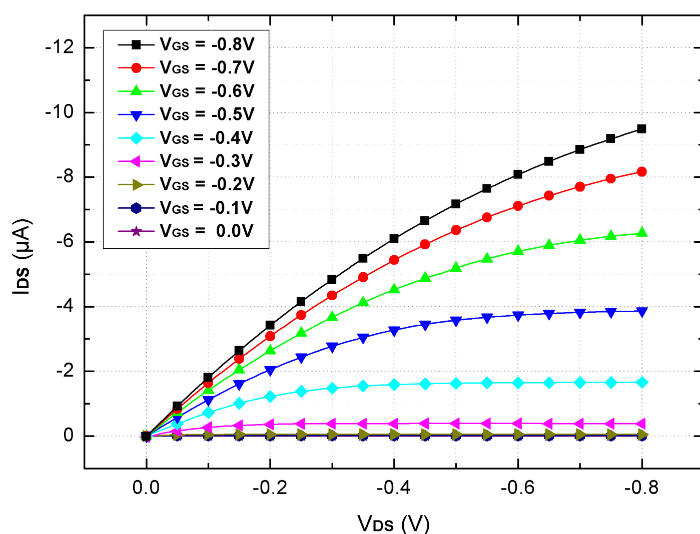

Figure 3.51. $I_{DS} - V_{DS}$ graph when the probe-gate returned to the center.

After a few minutes, probe was positioned further from the active area (around 5-6 mm) and $I_{DS} - V_{DS}$ measurements were repeated. Then, probe was returned to the central position again and measurements were completed. Results are given in Figure 3.52 and 3.53, respectively.

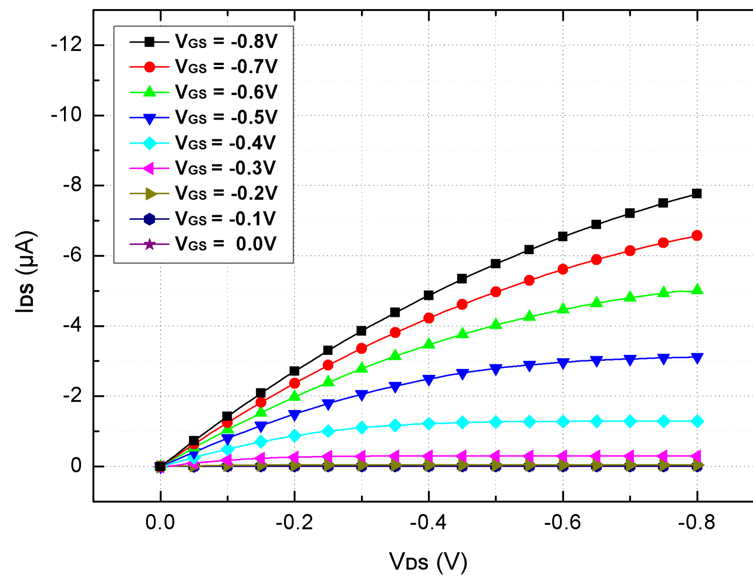

Figure 3.52. $I_{DS} - V_{DS}$ graph when the probe-gate was moved further away.

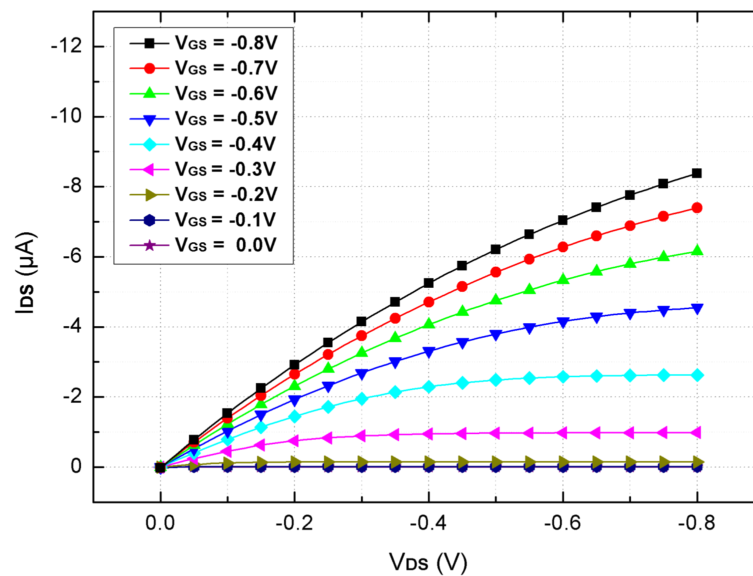

Figure 3.53. $I_{DS} - V_{DS}$ graph when the probe-gate returned to the center again.

From the $I_{DS} - V_{DS}$ graphs, it could be seen that there were not much difference between the measurement results of first three setups. Last two setups gave degraded results but it was due to a several minutes delay between measurements. Since last two measurements were also gave similar results, it can be concluded that gate distance did not affect the performance much in probe-gate setup.

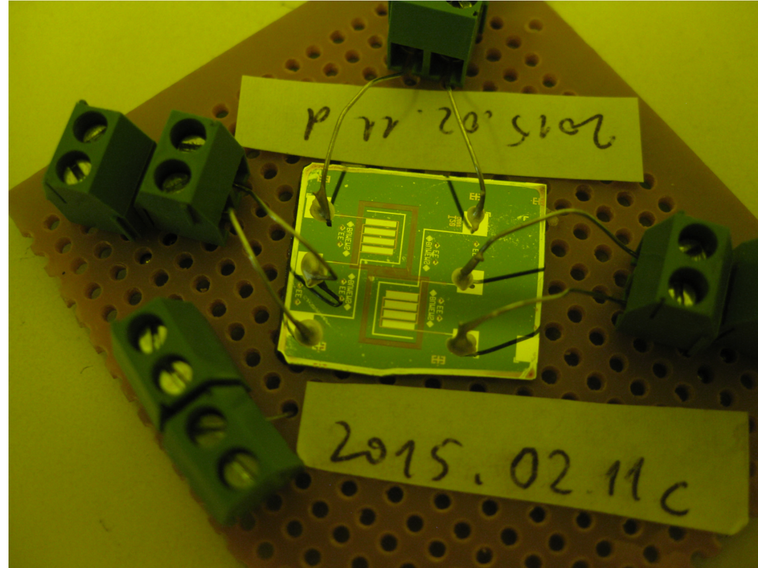

Figure 3.54. Planar gate position test setup. WG-FET used here was fabricated with *Layout I*.

Gate position experiments were also performed with planar-gate setup. Layouts of third generation WG-FET devices were designed for that purpose with three different gate distances as 150 μm, 300 μm, and 600 μm. Yet, measurement results of the ones with 150 μm and 300 μm gate distances were generally poor, which prevented a proper comparison. Therefore, gate of the second WG-FET was used as the far-planar-gate for the experiment (which corresponds to a gate distance around 2-3 mm). The test sample can be seen in Figure 3.54.

First, $I_{DS} - V_{DS}$ measurements were performed for normal operation. After that, de-ionized water droplet was broadened and second transistor's gate electrode was used as gate. $I_{DS} - V_{DS}$ measurements were repeated with that far-gate setup.

Then, original setup was measured again to eliminate time-based degradation effects. Results are given in Figure 3.55, 3.56, and 3.57, respectively.

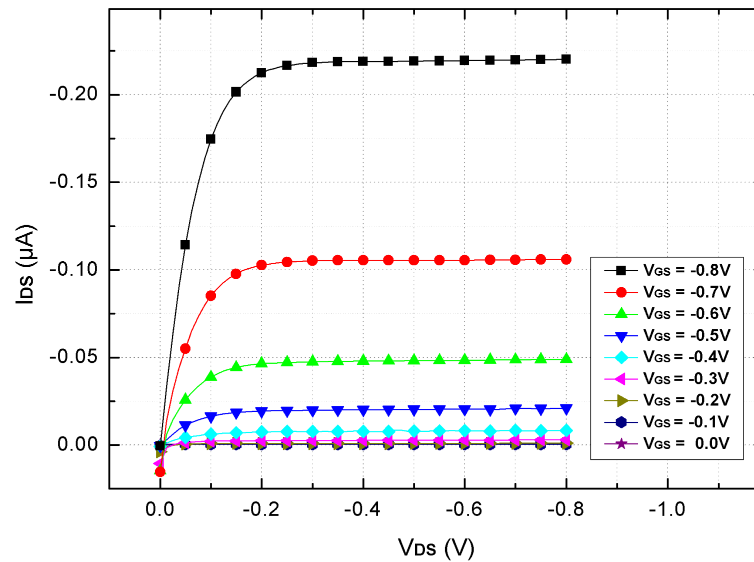

Figure 3.55. $I_{DS} - V_{DS}$ graph for the normal planar-gate operation.

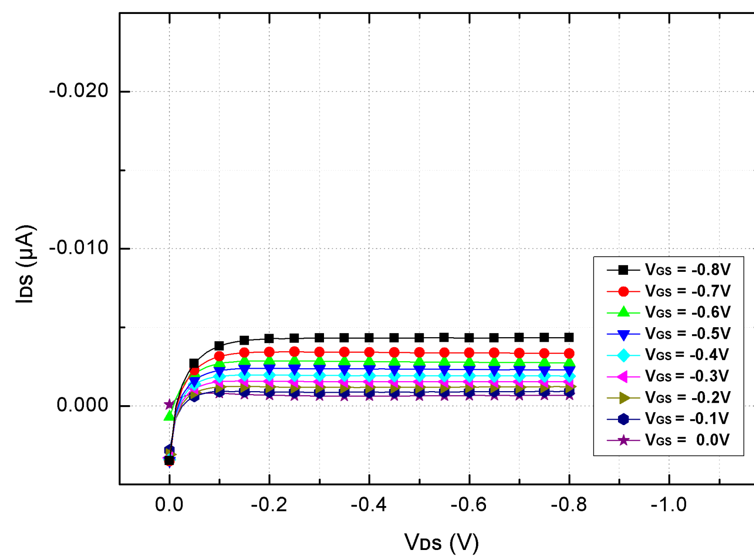

Figure 3.56. $I_{DS} - V_{DS}$ graph for the far planar-gate operation.

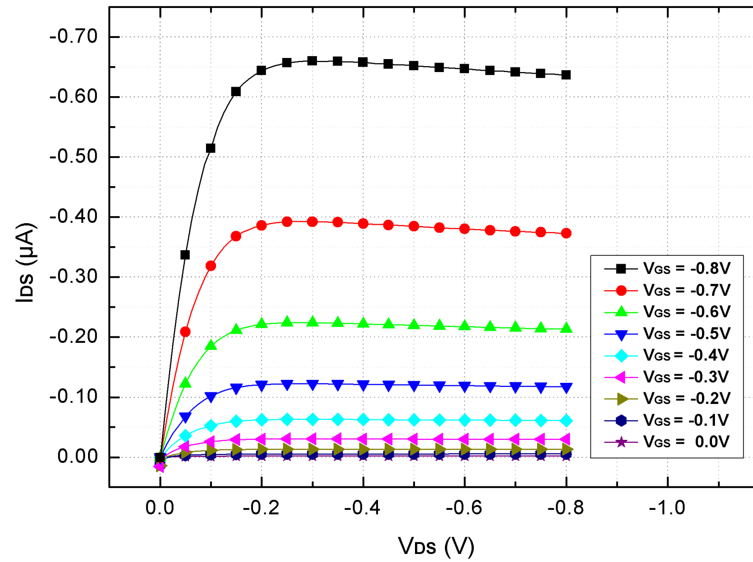

Figure 3.57. $I_{DS} - V_{DS}$ graph for the normal planar-gate operation, again.

Results showed that gate distance made a huge difference on $I_{DS} - V_{DS}$ curves in planar-gate setup. When far-gate was used, transistor performance was degraded considerably relative to the normal gate operation. After far-gate measurements, normal setup was tested again and gave even better results. If poor far-gate performance was originated from time-based degradation, second normal setup test should have given worse results compared to first test. Therefore, it could be concluded that gate distance was very effective on transistor performance for planar-gate topology.

3.6.2.9. Transistor Degradation. The biggest problem about tested devices was performance degradation with consecutive measurements, which made consistent data extraction harder from obtained current-voltage graphs. In Figure 3.58, two consecutive $I_{DS} - V_{DS}$ measurements of a third generation WG-FET (*Layout F*) with planar- and probe-gate setups are given.

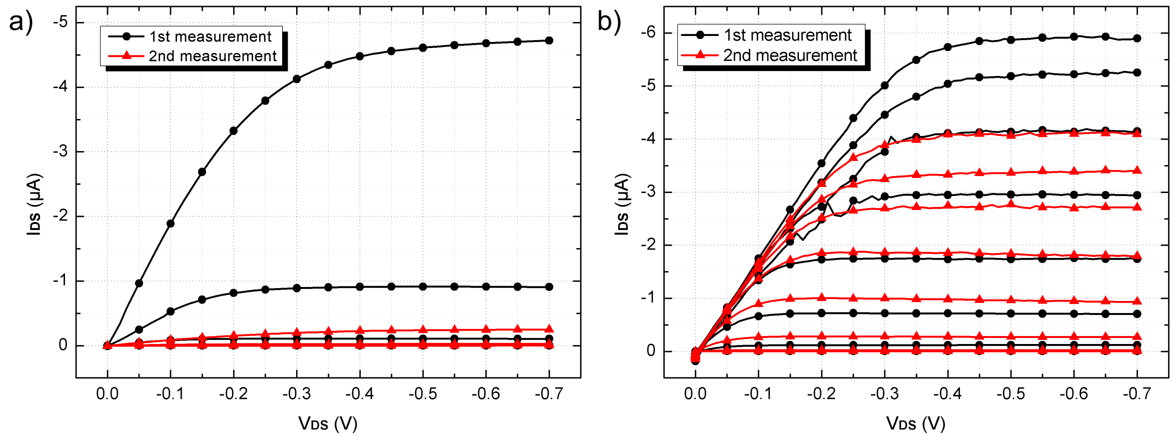

Figure 3.58. Two consecutive $I_{DS} - V_{DS}$ measurements of a third generation WG-FET (*Layout F*) with a) planar-gate, and b) probe-gate setups.

In planar-gate setup, degradation was considerably worse. After four consecutive measurements, $I_{D,max}$ decreased 3 orders of magnitude in planar-gate setup, whereas it was almost halved in probe-gate as shown in Table 3.3. Those measurements suggested that back-gate effect of planar-gate could accelerate degradation.

Table 3.3. Degradation of $I_{D,max}$ in four consecutive measurements.

Measurement #	**$I_{D,max}$ (planar-gate)**	**$I_{D,max}$ (probe-gate)**
1	-4.7 μA	-5.9 μA
2	-248.8 nA	-4.1 μA
3	-31.8 nA	-3.4 μA
4	-4.6 nA	-2.9 μA

An experiment was done to check whether the situation could be fixed. Water droplet on the Si active area was removed with nitrogen blow and 7 V was applied to test setup as $V_{DS} = V_{GS} = -7$ V. After a while, channel resistance value came back to the value which it had before experiment started. Therefore, resistance value could be

reverted to pre-experiment state by stressing a relatively high voltage to the channel in the absence of water droplet. However, when water droplet was placed on the Si active area again, no transistor characteristics could be obtained.

Voltage stress on channel was not an option due to electrolysis when there was a water droplet on the setup, so bulk voltage, V_{BS}, was varied from -7 V to 7 V to see whether it had any effect on the channel. No change was observed in transistor performance due to bulk voltage variation. It was concluded that electrical manipulations did not help on fixing the transistor which was degraded in existence of water droplet on the Si active area.

In dry resistance tests, sealed environment provided more stable measurement results. Therefore, a similar experimental setup was applied to a WG-FET device to test if better stability could be obtained. De-ionized water droplet was confined in an o-ring and sealed with a cover glass. Experimental setup is shown in Figure 3.59.

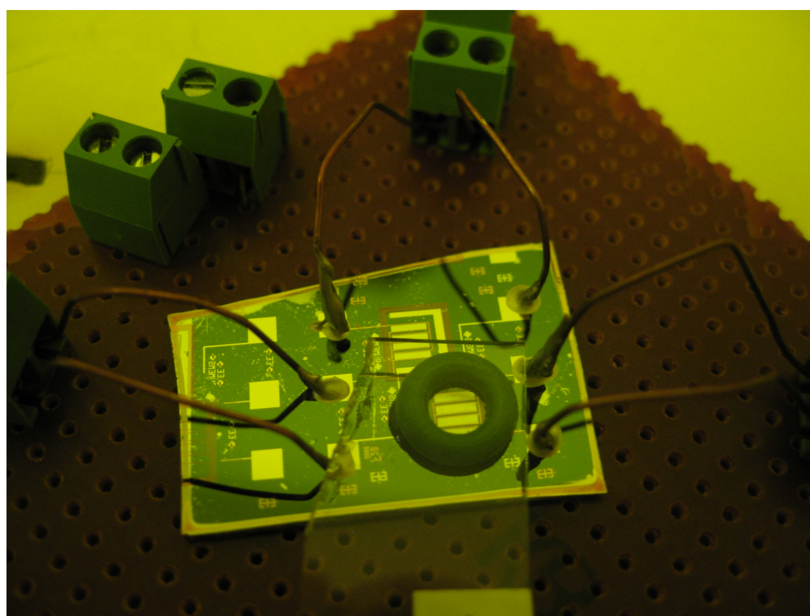

Figure 3.59. Experimental setup of a WG-FET with sealed environment.

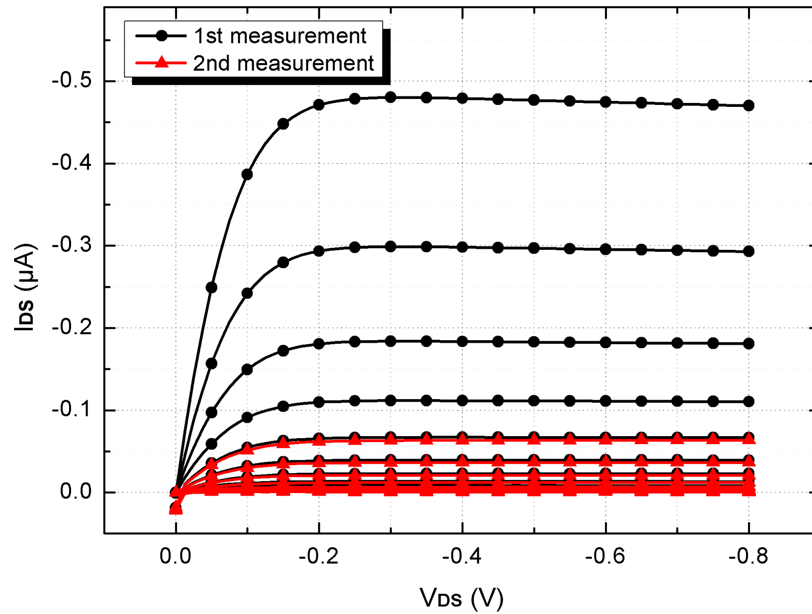

Figure 3.60. Two consecutive $I_{DS} - V_{DS}$ measurements of a third generation WG-FET (*Layout E*) with planar-gate setup in sealed environment.

With that setup, only planar-gate measurements could be performed. A third generation WG-FET device fabricated with *Layout E* was used in the experiments. Two consequent measurement results are shown in Figure 3.60. It could be seen that sealed environment did not make much difference on transistor performance degradation in planar-gate topology.

3.6.2.10. Remarks. In third generation WG-FET devices, main focus was improving the planar-gate transistor setup and investigating effects of several variables on transistor performance characteristics. New transistor layouts with different gate electrode patterns were designed to examine gate-based effects on transistor performance. Third generation WG-FET devices demonstrated better performance characteristics with respect to second generation devices. Best performance was obtained WG-FETs fabricated with *Layout C*, *F*, and *I*. No particular difference was noted between their transistor characteristics.

Gate position experiments were performed. It was seen that gate electrode distance did not affect the transistor performance much in probe-gate setup, whereas it was very effective in planar-gate measurement results.

Resistance measurements were done with both dry and water droplet setups. It was seen that planar-gate setup presented higher degradation than probe-gate setup even in the absence of water droplet. It suggested a back-gate effect which was related with a possible charge build up in thin Si/burried oxide interface. That degradation could be reverted in dry samples with application of relatively large V_{DS} values, however samples with water droplet could not be fixed.

Another observation was the positive effect of closed environments in dry resistance tests. Devices which were insulated from the environment showed less I_{DS} variation compared to the ones tested in open environment. However, same effect could not be observed in transistor performance tests. Severe performance degradation with consecutive measurements was noted in planar-gate WG-FET device with sealed setup.

An important observation was that performance degradation depended on not only the electrical bias, but also the time elapsed. Once a measurement was performed, device degradation continued with time even when the electrical bias was removed and all electrodes were grounded.

3.7. Fourth Generation WG-FET Devices

Solving stability issues was aimed in the design of fourth generation WG-FET devices.

3.7.1. Fabrication

In experiments with third generation WG-FETs, best results were obtained from the ones with gate distance of 600 μm for planar-gate topology. Other layouts with

smaller gate distances generally showed poor performance and exhibited degradation even before first measurements were completed. Therefore, layouts of fourth generation WG-FETs were designed with larger gate distances.

Basic model had a gate electrode thickness of 200 μm and distance of 2 mm. Previous tests did not show any prominent benefit of encircling gate geometry, so it was abandoned. All aluminium parts had Si separation layers under them to insulate metal parts from oxide layer. Bulk contact pads were added for ohmic bulk contacts. Every transistor had two of them, therefore quality of annealing step could be tested for every individual sample by using them.

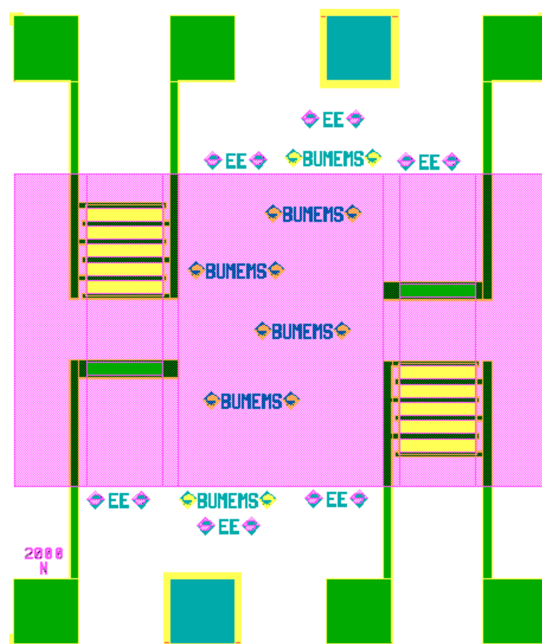

Figure 3.61. Layout of fourth generation WG-FET device.

Also, PR insulation layer area was extended to cover oxide areas exposed to environment. Silanol groups on thermal SiO_2 surfaces were known to be charge traps in existence of water molecules in contact with them. [93–95] Therefore, field insulation was applied for minimizing oxide surface charging which could be the underlying mechanism for performance degradation in samples after placing the water droplet.

Designed layout is shown in Figure 3.61. Samples with gate distances of 2 mm, 3 mm and 5 mm were designed. Si active area had a length of 500 μm and width of 12.5 mm which gave a W/L ratio of 25.

3.7.2. Experimental Results

<u>3.7.2.1. Stability Experiments.</u> With PR field insulation, stability experiments were performed as in Figure 3.62.

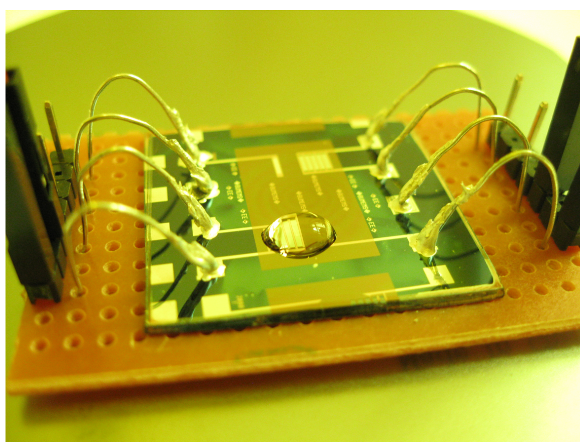

Figure 3.62. Experimental setup for a fourth generation planar-gate WG-FET device.

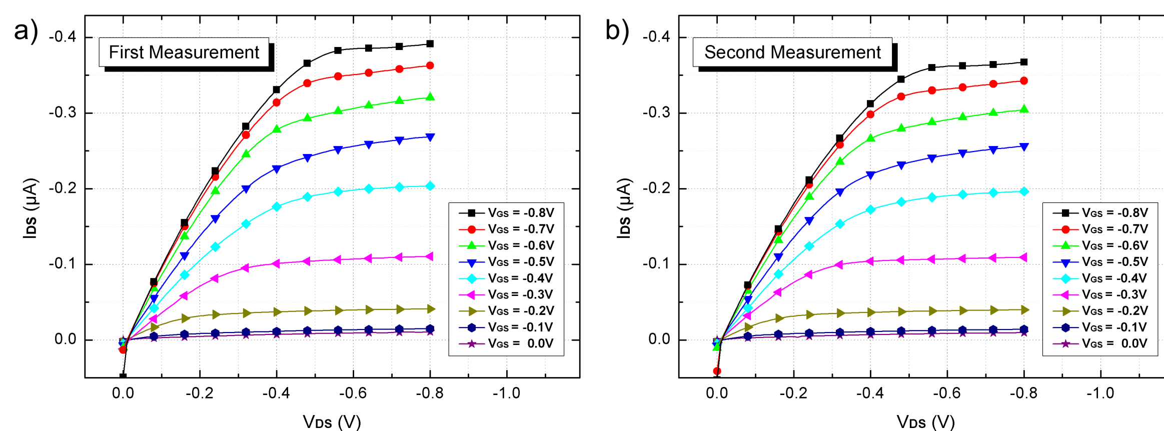

Figure 3.63. $I_{DS} - V_{DS}$ data of a) first and b) second measurements of a fourth generation planar-gate WG-FET device.

Experimental results showed that a relatively stable transistor operation was obtained. Although it had an unsatisfactory ON/OFF ratio of 40, deviation in $I_{DS} - V_{DS}$ curves between consecutive measurements was very low. In Figure 3.63, $I_{DS} - V_{DS}$ data of two consecutive measurements are given.

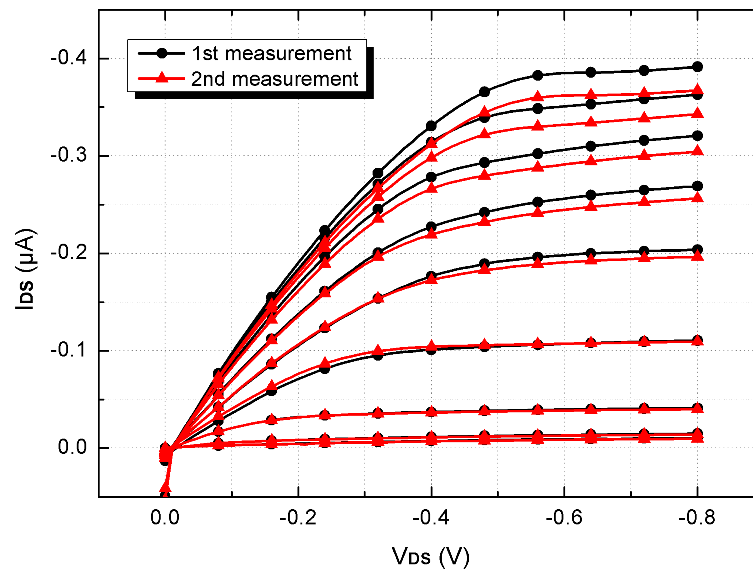

Figure 3.64. Comparison of two consecutive $I_{DS} - V_{DS}$ measurements.

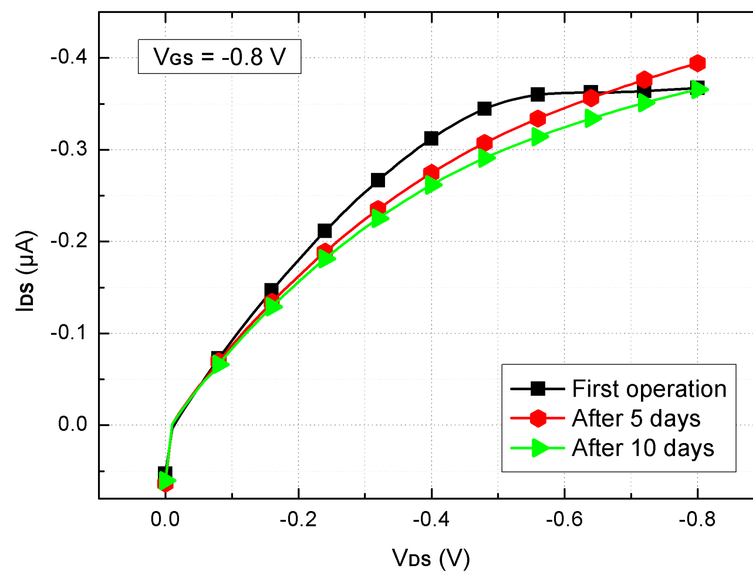

Figure 3.65. Performance degradation after ten days.

It can be seen that two graphs were almost identical as in Figure 3.64. For further examination, same measurements were repeated for the same device with five-day intervals. $I_{DS} - V_{DS}$ curves were compared for the same V_{GS} value to investigate variations in transistor performance. Results are given in Figure 3.65. It can be seen that performance degradation was minimal even after ten days. [96]

Further stability experiments were performed with both planar- and probe-gate setups for comparison. In Figure 3.66 and 3.67, $I_{DS} - V_{DS}$ measurement results of planar- and probe-gate setups are given, respectively.

For both setups, three $I_{DS} - V_{DS}$ measurements were performed with 10 minute intervals. Although variation was smaller with probe-gate, both setups gave similar curves even after 20 minutes from the first measurement.

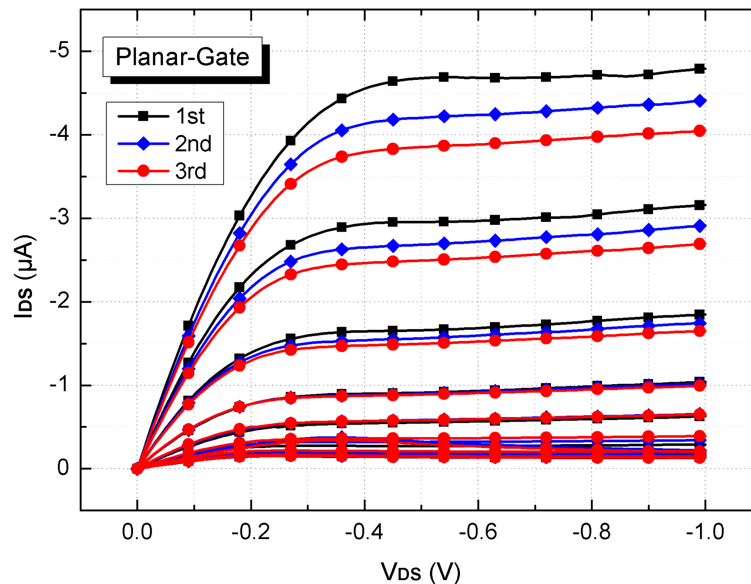

Figure 3.66. $I_{DS} - V_{DS}$ curves of planar-gate setup. Measurements were performed with 10 minute intervals.

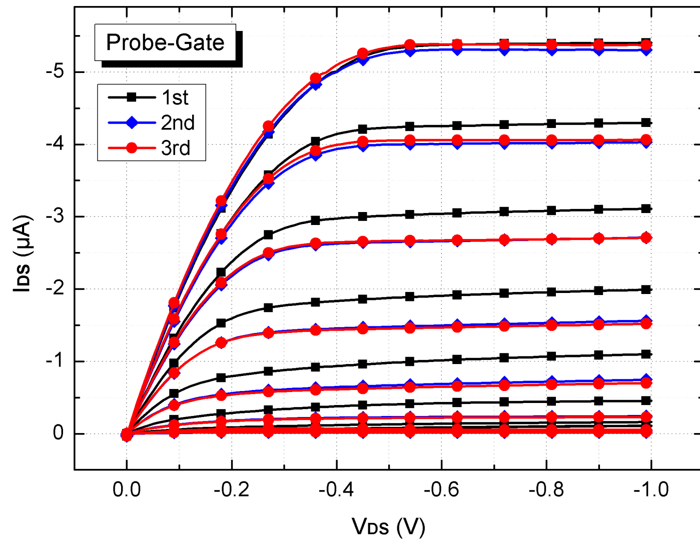

Figure 3.67. $I_{DS} - V_{DS}$ curves of probe-gate setup. Measurements were performed with 10 minute intervals.

3.7.2.2. Effect of Probe Distance. Measurements were repeated for probe-gate setup with the probe-gate electrode horizontally displaced for 2 mm to test its effect on stability. In consecutive measurements, no prominent effect due to vertical distance of probe-gate electrode was noted. However, hysteresis in cyclic measurements was slightly increased for displaced probe as demonstrated in Figure 3.68.

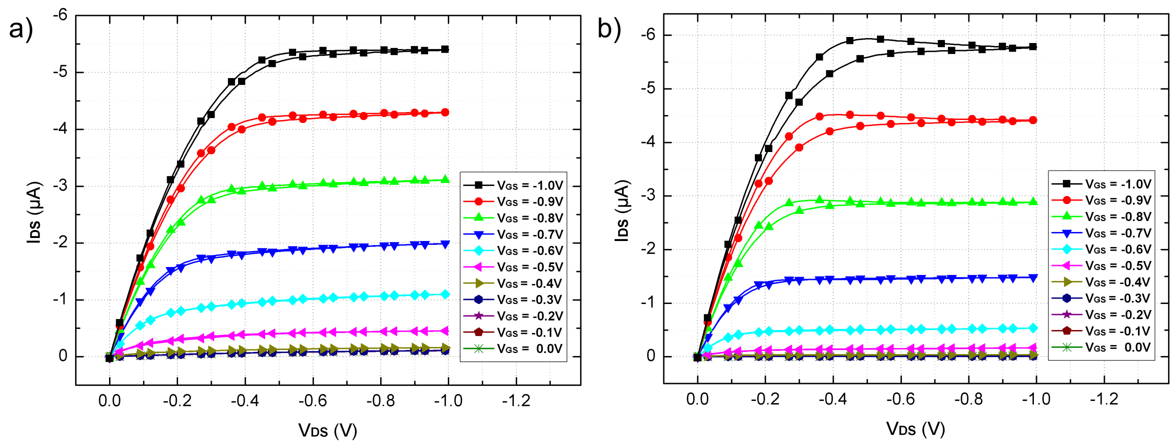

Figure 3.68. $I_{DS} - V_{DS}$ data of a) normal and b) 2 mm displaced probe-gate electrode.

<u>3.7.2.3. Effect of Probe Material.</u> Effect of probe material was also tested. Aluminium and tungsten probes were used as gate electrodes with the same fourth generation WG-FET device. Again, no particular effect on stability or transistor performance was noted. Results are given in Figure 3.69.

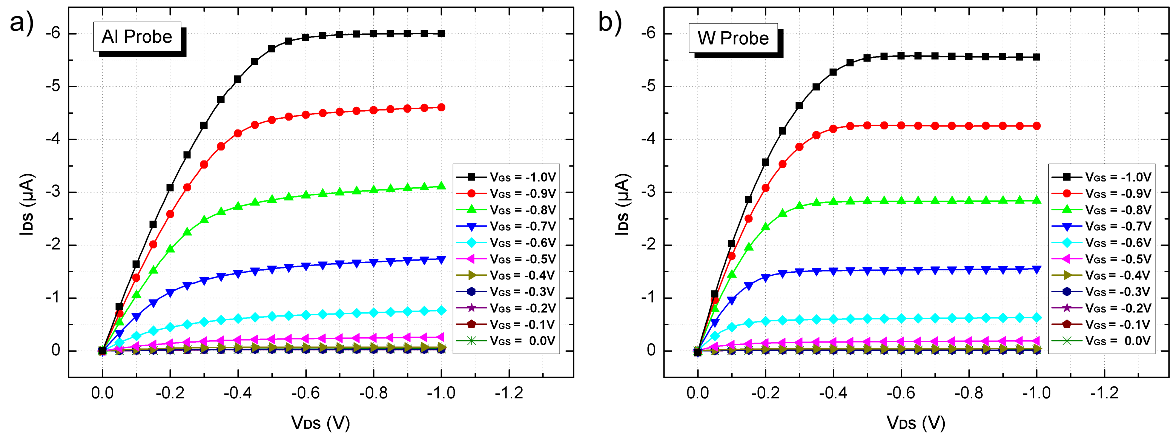

Figure 3.69. $I_{DS} - V_{DS}$ data of a probe-gate WG-FET with a) Al and b) W probes.

<u>3.7.2.4. Field Insulation on a Previous Design.</u> Insulation of oxide regions with PR was used on a third generation WG-FET device to see if it could help on degradation. A planar-gate device fabricated with *Layout F* was used for the experiment. All area except Si active region and the gate-electrode was insulated with PR. Again, three $I_{DS} - V_{DS}$ measurements were performed with 10 minute intervals. Obtained results are given in Figure 3.70.

Measurement results showed that field insulation could be used with previous designs to decrease degradation. Although, transistor characteristics of the planar-gate WG-FET device were not optimal, degradation in the repeated measurements was negligible. Same transistor was tested with probe-gate setup, as well. Results are given in Figure 3.71. With probe-gate setup, considerably better transistor characteristics were obtained in addition to stable results.

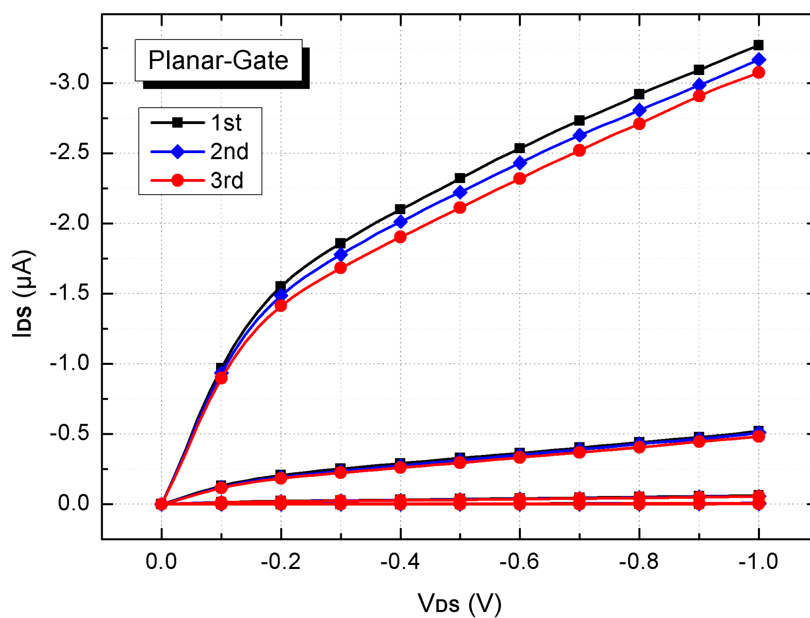

Figure 3.70. $I_{DS} - V_{DS}$ curves of planar-gate setup. Measurements were performed with 10 minute intervals.

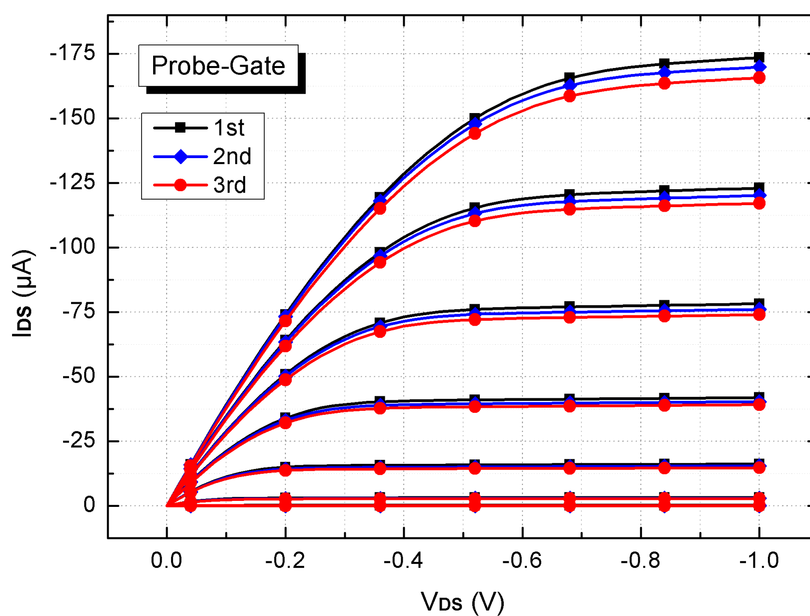

Figure 3.71. $I_{DS} - V_{DS}$ curves of probe-gate setup. Measurements were performed with 10 minute intervals.

<u>3.7.2.5. Effect of Source/Drain Insulation.</u> In original WG-FET design, source and drain electrodes were covered with PR layer to minimize their gating effect on transistor operation. To test extreme conditions, a device without source/drain insulation was fabricated. Transistor measurements were done with probe-gate setup. Results are given in Figure 3.72.

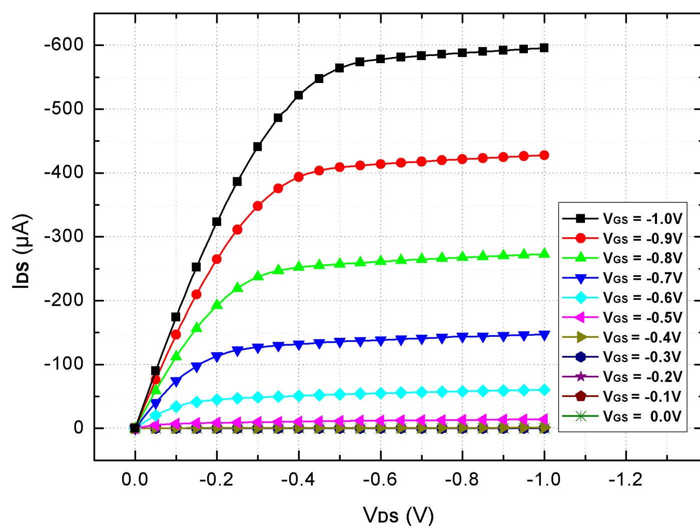

Figure 3.72. $I_{DS} - V_{DS}$ measurement results of a probe-gate WG-FET device without source/drain insulation.

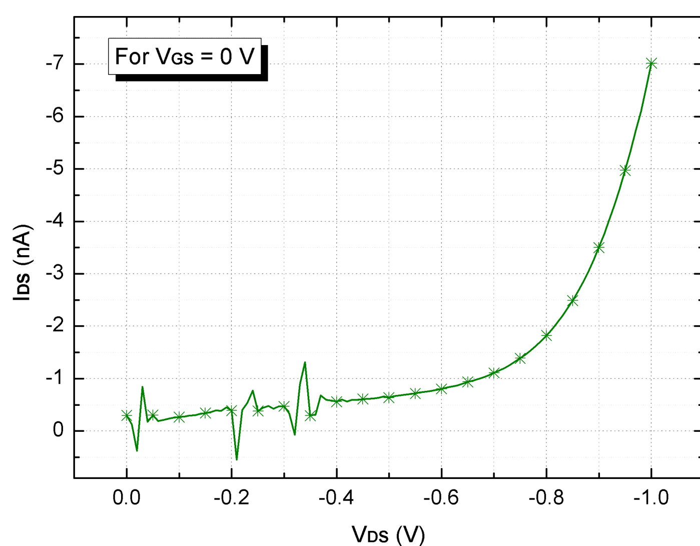

Figure 3.73. $I_{DS} - V_{DS}$ measurement for $V_{GS} = 0$ V.

From $I_{DS} - V_{DS}$ measurements, ON/OFF ratio was calculated as 85,000 A/A with approximately −0.6 mA on-current. Such high current was attributed to absence of PR overlap areas on Si active region. They introduced extra series resistance to device and could not be manipulated by gate electrode. Gating effect of exposed drain electrode could be seen when probe-gate was grounded as in Figure 3.73.

For $V_{DS} = -0.5$ V, ON/OFF ratio was nearly 900,000 A/A. Gating effect of the exposed drain electrode caused an increase in the off-current which in turn resulted in an order of magnitude decrease in ON/OFF ratio. However, obtained transistor performance was still better than previous designs.

Same device was also tested with planar-gate setup. A fourth generation planar-gate WG-FET with gate distance of 2 mm was used in the experiment. Results are given in Figure 3.74. $I_{DS} - V_{DS}$ measurements showed considerable deviations from proper transistor operation. Planar gate electrode was too far to dominate on Si active area against drain electrode. Similar results were obtained when probe-gate was placed at the same distance with planar gate. Therefore, it was concluded that source/drain insulation was crucial for planar-gate operation.

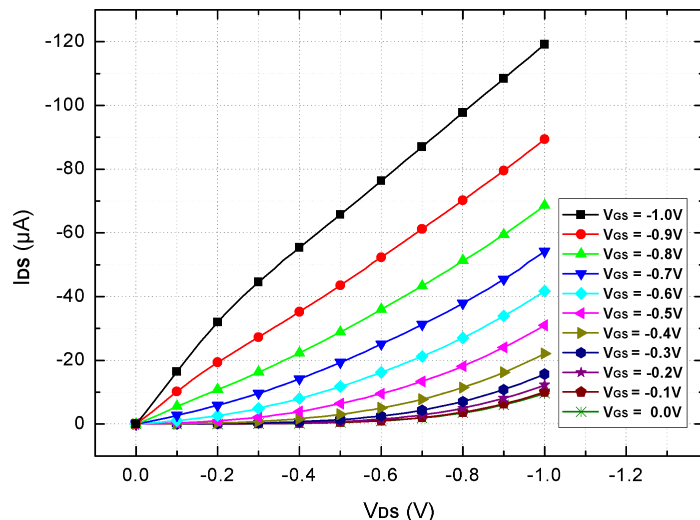

Figure 3.74. $I_{DS} - V_{DS}$ measurement results of a planar-gate WG-FET device without source/drain insulation.

Anodization of source/drain electrodes was tested as an alternative to PR insulation. A thin Al_2O_3 layer was used to insulate source/drain electrodes. With that technique, overlapping areas could be minimized while providing insulation to minimize gating effect of drain. $I_{DS} - V_{DS}$ measurements were performed with both probe- and planar-gate setups after source/drain anodization. Results are given in Figure 3.75.

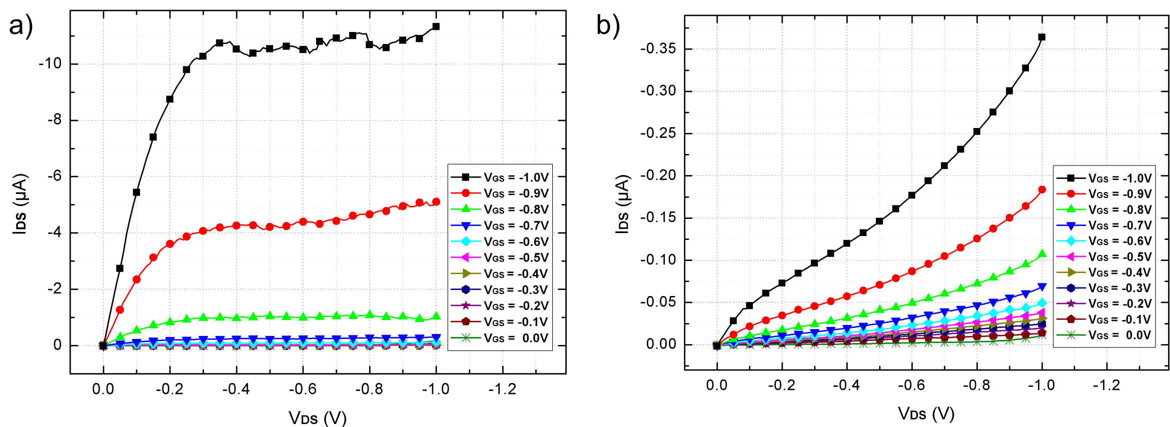

Figure 3.75. $I_{DS} - V_{DS}$ measurement results of a) probe- and b) planar-gate WG-FET devices with anodized source/drain electrodes.

Although, anodization slightly reduced the gating effect of drain electrode, obtained results with planar-gate setup were still far from proper transistor operation. Also, current levels remarkably reduced after anodization process which negated all advantages of PR-less design.

<u>3.7.2.6. Remarks.</u> Stability issues were targeted with fourth generation WG-FET devices. Better repeatability was achieved for both probe- and planar-gate setups with field insulation. Planar- and probe-gate WG-FET devices with field insulation were tested in consecutive measurements and exhibited minimal degradation after 20-minutes of operation. Similar current levels were obtained even after 10 days.

Effect of probe distance on stability was tested. No significant difference was noted due to horizontal probe-gate distance on stability for devices with field insulation. Also, different probe-gate materials were tested. Obtained transistor characteristics were almost similar.

WG-FET devices with uninsulated source/drain electrodes were tested. Although the gating effect of drain electrode was considerably higher with respect to previous WG-FETs, probe-gate was still dominant in transistor operation and ON/OFF ratio of 85,000 A/A was obtained. However, planar-gate setup did not exhibit proper transistor operation without source/drain insulation.

3.8. Analysis and Comparison

In experiments, WG-FET devices with various designs were tested for both probe- and planar-gate setups. Best transistor characteristics were obtained with probe-gate setups. For planar-gate devices, a deterioration in transistor performance was observed with increasing gate distance. Field insulation provided more repeatable results for both setups. Absence of source/drain insulation removed overlapping regions on Si active area, which were beyond gate control and acted like series parasitic resistances, at the expense of increased gating effect of drain electrode. For probe-gate setup, gate electrode was dominant on transistor operation, and adequate transistor characteristics were obtained despite the effect of drain electrode on off-current. Same situation was not observed with planar-gate setup. In that case, gate and drain electrodes had comparable gating effects which led to deviant current-voltage relations. A proper transistor operation could not be obtained with planar-gate WG-FET device which had uninsulated source/drain electrodes.

For comparison with the theoretical model stated in Section 3.2, WG-FETs with probe- and planar-gate setup were used. Planar-gate WG-FETs were fabricated with two different gate distances as 600 μm and 3 mm. Both setups also had their versions without source/drain insulation. All devices had proper field insulation with PR and W/L ratio of 20.

WG-FET model required the potential distribution function on EDL, $V_{g_EDL}(x)$, for each device topology to extract transistor performance parameters. To verify $V_{g_EDL}(x)$ function, electric field and voltage distribution simulations were performed with COMSOL Multiphysics 5.2 for probe- and planar-gate setups. Results for WG-FETs with insulated source/drain electrodes are given in Figure 3.76.

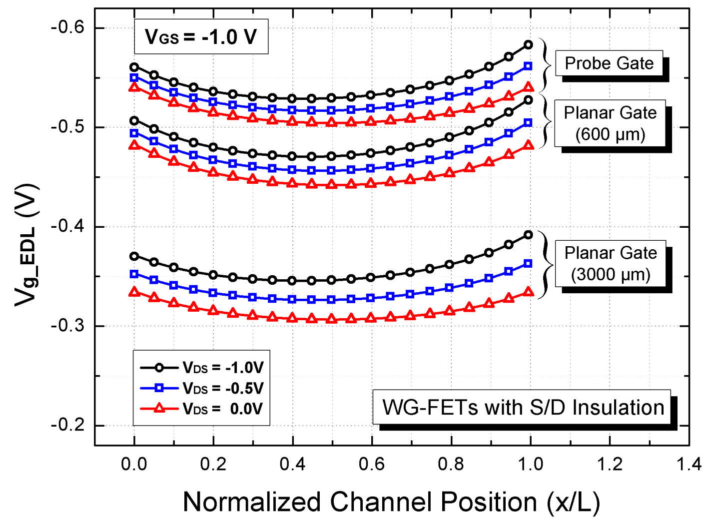

Figure 3.76. $V_{g_EDL}(x)$ vs. normalized channel position graphs for probe- and planar-gate setups with source/drain insulation.

In simulations, voltage distribution on EDL was analyzed for different V_{GS} and V_{DS} values. In Figure 3.76, it can be seen that combined effects of drain and gate electrodes resulted in an uneven voltage distribution on EDL throughout the channel. In planar-gate setup with the closer gate electrode layout, effect of gate electrode on voltage distribution was lower compared to the probe-gate setup and it decreased further when the planar gate electrode is placed in 3000 μm distance.

For WG-FETs with uninsulated source/drain electrodes, simulation results are given in Figure 3.77. Since results for two planar-gate setups were similar, only the one with 3000 μm gate distance was demonstrated.

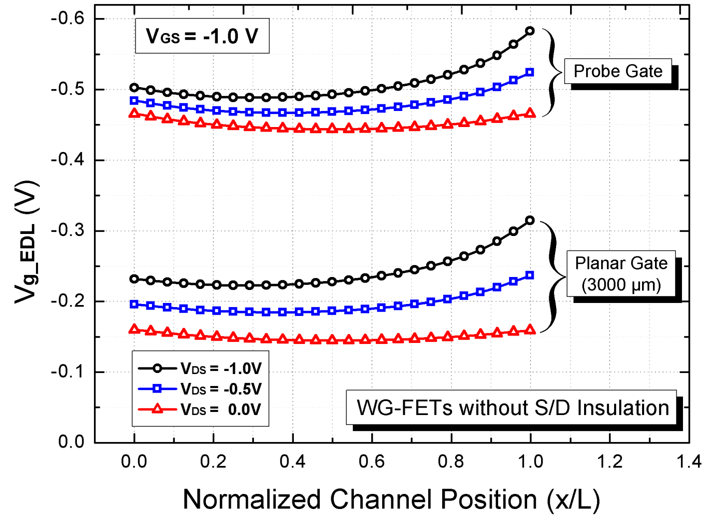

Figure 3.77. $V_{g_EDL}(x)$ vs. normalized channel position graphs for probe- and planar-gate setups without source/drain insulation.

In devices without source/drain insulation, source and drain electrodes were directly in contact with the water droplet like the gate electrode. Due to absence of insulator overlap with channel area, series parasitic resistance R_{px} did not exist, which was desirable for proper transistor operation. For those devices, difference between simulation results of probe- and planar-gate setups was more significant. In planar-gate setups, effect of gate electrode on voltage distribution was drastically lower and V_{g_EDL} curves dissociated more for different V_{DS} values, compared to probe-gate setup.

Simulations confirmed that the effective voltage on the EDL insulation layer for a WG-FET device was not uniform throughout the channel when V_{DS} was not equal to 0 V. Instead, it was a function of the channel position as indicated in Equation 3.25. By making linear approximations in simulation results, parameters k_1, k_2, and k_3 were calculated for all WG-FET topologies as given in Table 3.4.

Table 3.4. Topology specific parameters.

WG-FET Topology	$\mathbf{k_1}$	$\mathbf{k_2}$	$\mathbf{k_3}$
Probe Gate with S/D insulation	0.515	0.017	0.021
Planar Gate with S/D insulation (600 μm)	0.454	0.021	0.019
Planar Gate with S/D insulation (3000 μm)	0.315	0.032	0.020
Probe Gate without S/D insulation	0.450	0.026	0.063
Planar Gate without S/D insulation (600 μm)	0.198	0.050	0.071
Planar Gate without S/D insulation (3000 μm)	0.150	0.056	0.073

In probe-gate setup with source/drain insulation, approximately 51.5% of the applied V_{GS} and 1.7% of the applied V_{DS} were transferred as effective gate voltage. Planar-gate setup with 600 μm gate distance and source/drain insulation, had slightly inferior k_1 and k_2 values relative to probe-gate setup. When the gate electrode distance was increased to 3000 μm for the same setup, k_1 decreased to 0.315 while k_2 increased to 0.032, which showed that the effect of gate electrode was weakening with increasing planar gate electrode distance.

For devices without source/drain insulation, probe-gate setup had a comparable k_1 value with a slightly elevated k_2 value with respect to devices with source/drain insulation. On the other hand, planar-gate setups had considerably poor k_1 and k_2 values. For planar-gate setup with 600 μm gate distance, k_1 value was halved whereas k_2 value was doubled compared to probe-gate setup. When the gate distance was increased to 3000 μm, they deteriorated further. For planar-gate setups without source/drain insulation, k_1 and k_2 values were comparable as shown in Table 3.4, which implied that the effect of gate electrode voltage was no longer dominant on V_{g_EDL} and the effect of drain electrode became significant which was not desired for a proper transistor operation. Those results supported the significance of source/drain electrode insulation for planar-gate devices.

Experimental results were compared with theoretical calculations for all WG-FET topologies given in Table 3.4. Theoretical current-voltage relations were obtained with SPICE simulations using Equation 3.27 and 3.28 with corresponding k_1, k_2, and k_3 values. For devices with source/drain insulation, series parasitic resistances due to insulator overlapping, R_{px}, were added in SPICE models. V_{thc} values were extracted from equations using measurement data.

To determine C_{EDL} value, an experimental setup was designed. A sample was fabricated with 1 mm^2 of Si active area. Electrical contacts to active Si and bulk were patterned from Al and annealed. Both contacts were grounded to prevent parasitic effects. All area except the patterned Si region was coated with PR to define the capacitor surface area and to provide field insulation. Layout of the sample is given in Figure 3.78.

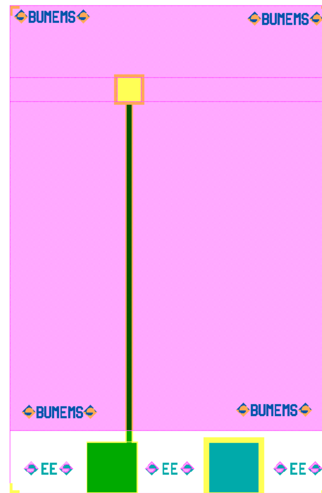

Figure 3.78. Layout of samples used in capacitance measurement setup.

An Al layer was patterned on a glass substrate as gate electrode. A de-ionized water droplet was placed on the active Si area. Then it was encapsulated with the gate electrode. PR layer also ensured a constant separation between Si and Al surfaces. With that setup, an EDL capacitor system was obtained with equal areas of Si and Al layers. Capacitance-voltage measurements were done with Keithley 4200SCS. Bias

voltage applied on gate electrode was swept from -0.8 V to $+0.8$ V with a 10 mV AC signal at 1 kHz added on it. Although capacitance values near 1 μF/cm^2 were reported [97] for similar EDL-based systems, C_{EDL} was measured approximately as 90 nF/cm^2.

In Figure 3.79a and 3.79b, $I_{DS}-V_{DS}$ and $I_{DS}-V_{GS}$ measurements and simulation results are given for probe-gate setup with source/drain insulation.

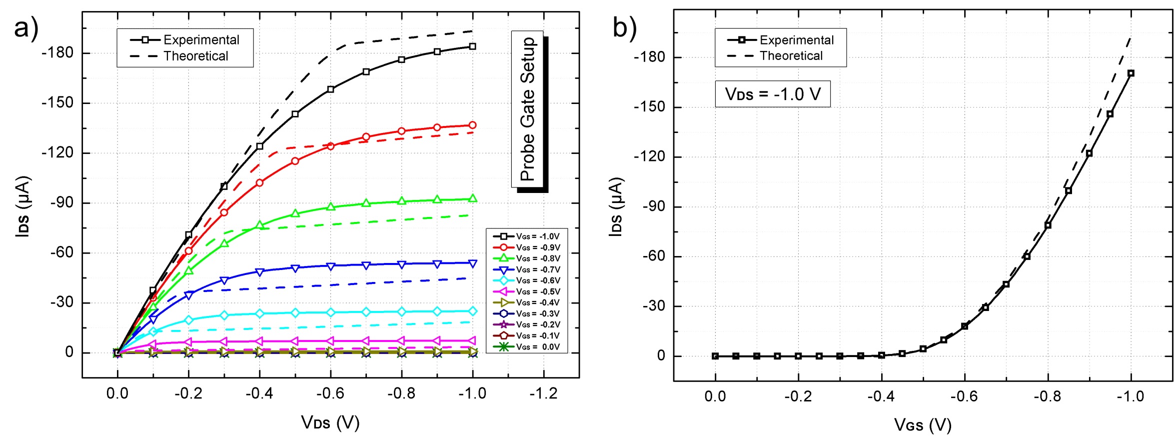

Figure 3.79. Measurement (solid lines) and simulation (dashed lines) results for probe-gate WG-FET device with source/drain insulation. a) $I_{DS} - V_{DS}$ curves for V_{GS} values swept from 0 V to -1 V. b) $I_{DS} - V_{GS}$ curve for $V_{DS} = -1$ V.

I_{ON} and I_{OFF} currents were measured as -184 μA and -8 nA, respectively, which gave an ON/OFF ratio of 23,000 A/A. Transfer curve measurements for $V_{DS} = -1$ V pointed to an effective threshold voltage of -0.46 V which corresponds to a V_{thc} value of -0.26 V. Both $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$ measurement results were parallel with SPICE simulations.

In Figure 3.80a and 3.80b, $I_{DS} - V_{DS}$ measurements and simulation results are given for planar-gate setups with gate distances of 600 μm and 3 mm, respectively.

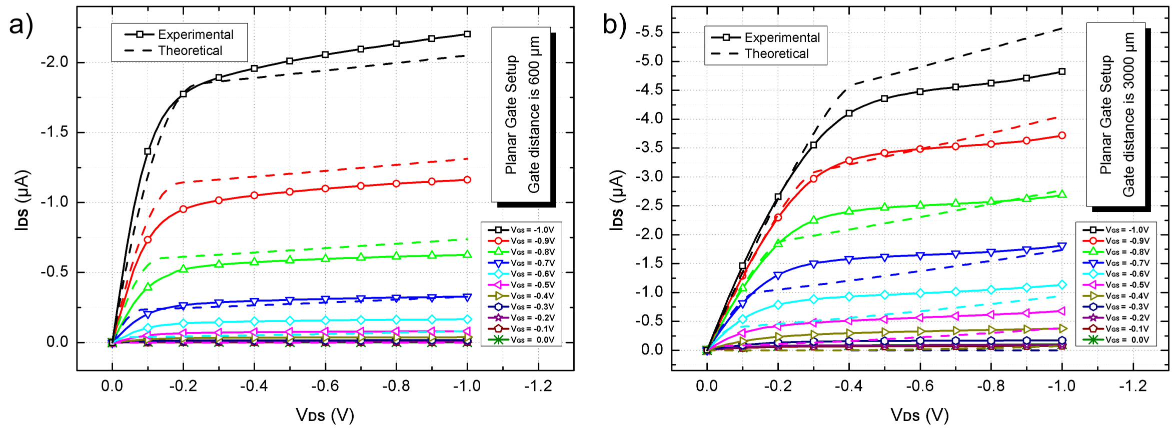

Figure 3.80. $I_{DS} - V_{DS}$ measurements (solid lines) and simulation (dashed lines) results for planar-gate WG-FET devices with gate distances of a) 600 μm and b) 3 mm. Both devices had source/drain insulation.

For planar-gate setup with 600 μm gate distance and source/drain insulation, ON/OFF ratio was found as 1,100 A/A. The effective threshold voltage was calculated as -0.56 V, which resulted in V_{thc} value of -0.27 V. Decrease in ON/OFF ratio was expected due to inferior k_1 and k_2 values. Simulations were in agreement with measurement results as seen in Figure 3.80a.

Similarly, for planar-gate setup with 3000 μm gate distance and source/drain insulation, ON/OFF ratio was found as 45 A/A and effective threshold voltage was calculated as -0.63 V. For that measurement, V_{thc} was found as -0.13 V. Increasing gate electrode distance from 600 μm to 3000 μm, decreased ON/OFF ratio further. Theoretical and experimental results are given in Figure 3.80b.

In Figure 3.81a, $I_{DS} - V_{DS}$ measurements and simulation results are given for probe-gate setup without source/drain insulation. Inferior k_1 and k_2 values compared to its counterpart with source/drain insulation suggested worse transistor performance. However, I_{ON} and I_{OFF} currents for that setup were measured as -596 μA and -7 nA, respectively, which gave ON/OFF ratio of 85,000 A/A. That could be explained with the absence of R_{px}. When there were no series parasitic resistances due to insula-

tor overlapping, I_{ON} was boosted which significantly increased the ON/OFF ratio. The effective threshold voltage was calculated as -0.51 V, which gave a V_{thc} value of -0.26 V. Simulation results were also in agreement with measurements as in Figure 3.81a.

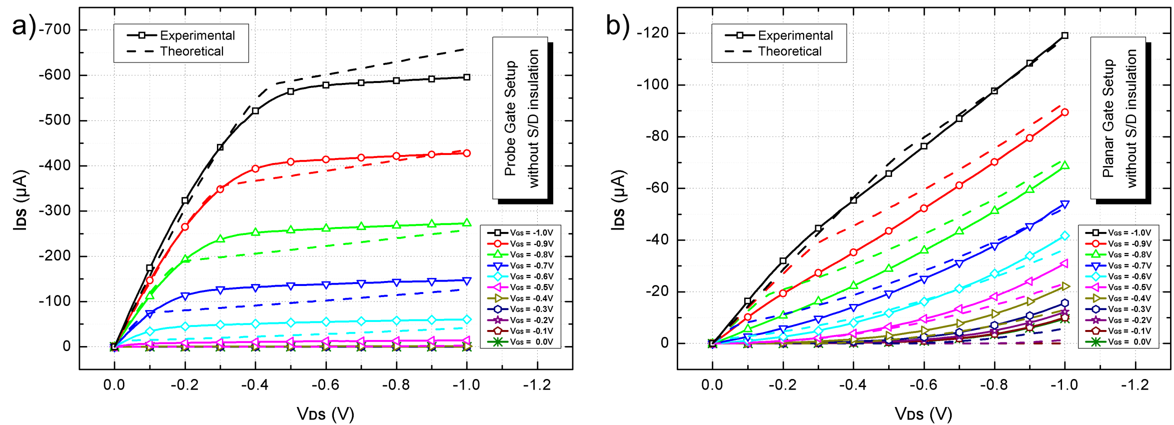

Figure 3.81. $I_{DS} - V_{DS}$ measurements (solid lines) and simulation (dashed lines) results for a) probe- and b) planar-gate WG-FET devices without source/drain insulation.

For planar-gate setup without source/drain insulation, $I_{DS} - V_{DS}$ measurements and simulation results are given in Figure 3.81b. Gate electrode distance was 3000 μm in that layout. Again, absence of R_{px} manifested itself with high current levels like in the probe-gate setup. However, deteriorated transistor operation could be seen in the results as expected from the comparable k_1 and k_2 values. It was hard to mention about a proper threshold voltage or ON/OFF ratio about the planar-gate setup without source/drain insulation. Theoretical simulations demonstrated similar behavior and supported the measurement results as seen in Figure 3.81b.

Those results showed that the best ON/OFF ratio was obtained with probe-gate setup for devices with both insulated and uninsulated source/drain as expected from V_{g_EDL} simulations. Higher k_1 value indicated that higher effective gate voltage could be obtained on the device. In combination with low k_2, a high ON/OFF ratio was expected. For planar-gate topology, the setup with smaller gate distance gave a higher

ON/OFF ratio relative to the one with further gate electrode. When the gate distance was increased from 600 μm to 3000 μm, ON/OFF ratio decreased drastically. These findings were in agreement with device parameters given in Table 3.4 and supported by the SPICE simulations.

Effects of source/drain insulation were also tested. For probe-gate setup, transistor operation was affected slightly due to uninsulated source/drain, since it resulted in a little lower k_1 and a little higher k_2 values as shown in Table 3.4. However, they exhibited higher ON/OFF ratio compared to the devices with insulated source/drain electrodes, because those devices did not have series parasitic resistances, R_{px}. On the other hand, for planar-gate setup without source/drain insulation, $I_{DS} - V_{DS}$ measurement results showed considerable deviations from proper transistor operation due to increasing effect of drain voltage on V_{g_EDL}. Therefore, insulation of source/drain regions was crucial for WG-FET devices with planar-gate topology. [98]

4. CIRCUIT APPLICATIONS OF WG-FET

WG-FET is a promising device structure for microfluidic applications. By exploiting its fluidic interface, sensory function can be infused into read-out circuit parts in transistor level. Therefore, implementation of WG-FET based circuit applications is essential for future all-in-one systems. In this chapter, some examples of WG-FET based circuit applications are demonstrated.

4.1. WG-FET Inverter

Inverter circuits were implemented using both planar- and probe-gate WG-FET devices. Fabricated devices for this purpose are shown in Figure 4.1.

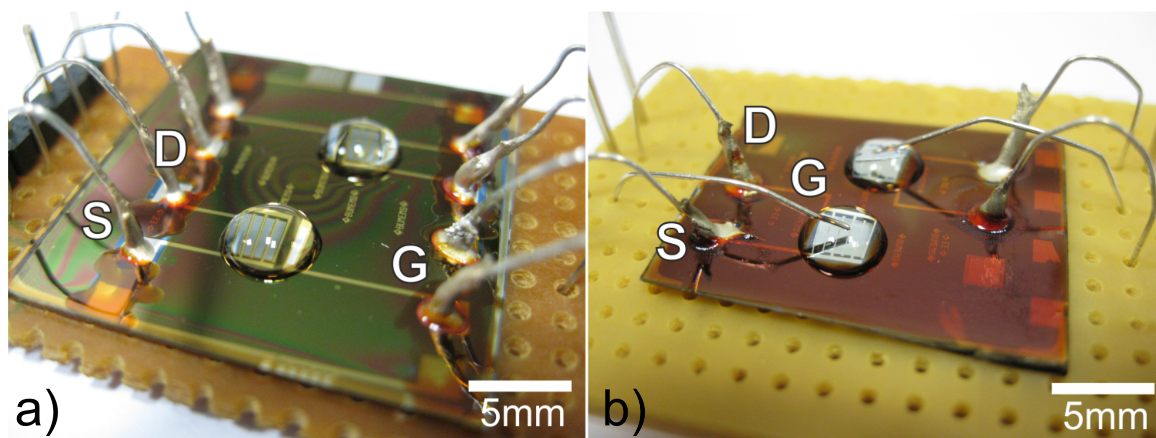

Figure 4.1. a) Planar- and b) probe-gate WG-FET devices fabricated for implementation of inverter circuits.

Since fabricated WG-FETs were all p-channel devices, a complementary circuit design was not applicable. Therefore, pseudo-pMOS designs were inherited. Resistive load and zero drive load [99–101] structures were implemented for inverter circuits as shown in Figure 4.2. Resistive load designs involved one WG-FET device and a proper pull-down resistor. Zero drive load design was preferred because WG-FETs are

accumulation-mode devices and they could imitate the operation of depletion-mode pull-down transistor.

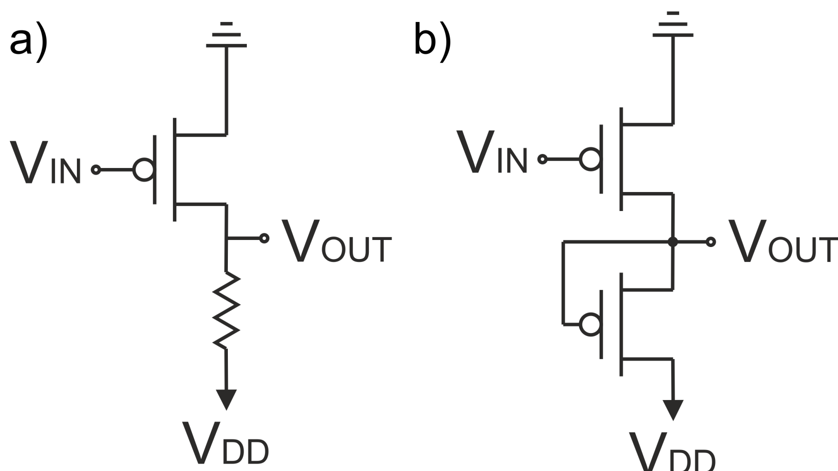

Figure 4.2. a) Resistive load and b) zero drive load inverter structures.

To compare performances of planar- and probe-gate WG-FETs in inverter circuit, same sample was used with both setups in a resistive load inverter structure. Voltage transfer curve of the inverter implemented with planar-gate WG-FET device was given in Figure 4.3. Measurement results showed that inverter circuit implemented with planar-gate WG-FET device exhibited a considerable hysteresis in cyclic operation.

Experiment was repeated with the probe-gate setup of the same WG-FET device. Voltage transfer curve of the inverter implemented with probe-gate device is given in Figure 4.4. It can be seen that hysteresis was almost negligible when the inverter was implemented with probe-gate device.

Then, zero drive load configuration was tested. Probe-gate devices were used in the circuit due to their low hysteresis. Voltage transfer curve of the inverter implemented with two WG-FET devices is given in Figure 4.5

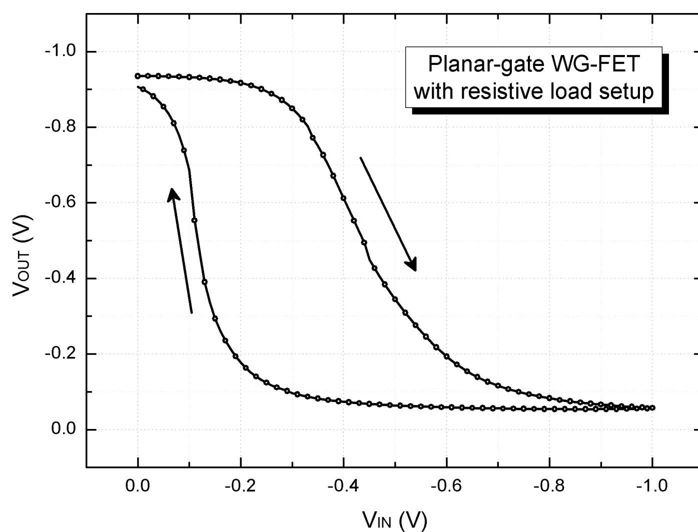

Figure 4.3. Voltage transfer curve of the inverter implemented with planar-gate WG-FET device.

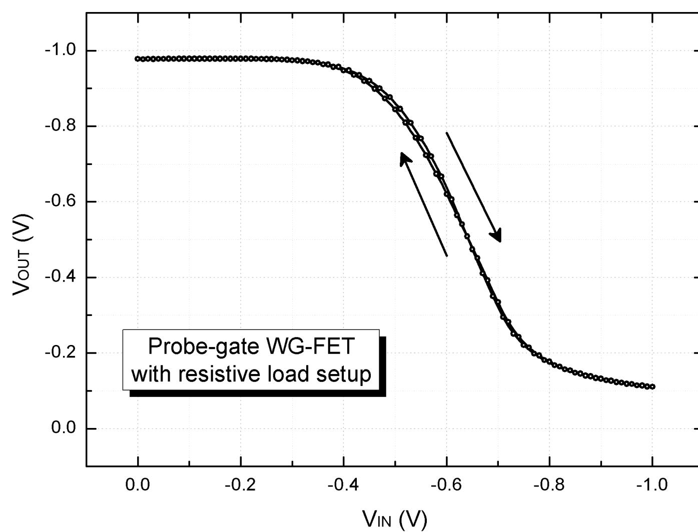

Figure 4.4. Voltage transfer curve of the inverter implemented with probe-gate WG-FET device.

Measurements showed that the inverter implemented with zero drive load structure had an output swing between 0 V and -0.2 V which was an indication of a weak load transistor. The situation could be improved with proper scaling of transistors,

however it would require new mask sets and extensive fabrication of new samples. Therefore, resistive load structure with probe-gate WG-FETs was used for further inverter experiments for the sake of simplicity and versatility.

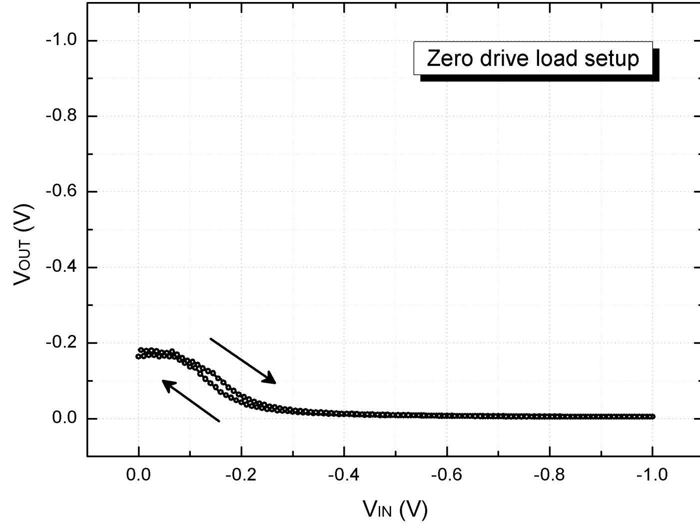

Figure 4.5. Voltage transfer curve of the inverter implemented with two WG-FET devices.

In experiments, inverter circuits with approximately -11 V/V gain and rail-to-rail output swing were fabricated with resistive load structure. $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$ graphs of the probe-gate WG-FET device used in the inverter setup are given in Figure 4.6.

WG-FET device had a W/L ratio of 20. From $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$ measurements, I_{ON} and I_{OFF} were found as -219 μA and -5.4 nA, respectively, which gave an ON/OFF ratio of approximately 40,000 A/A. V_{th} was also found as -0.4 V.

Voltage transfer curve of the inverter circuit implemented with given WG-FET device is shown in Figure 4.7. A 87 kΩ resistor was used as load in the circuit.

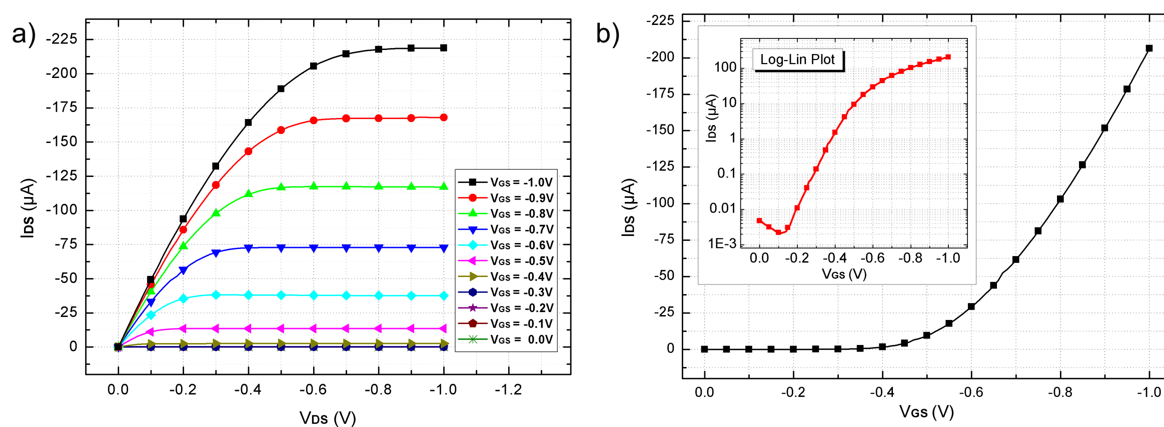

Figure 4.6. a) $I_{DS} - V_{DS}$ and b) $I_{DS} - V_{GS}$ measurements of the probe-gate WG-FET device used in inverter circuit.

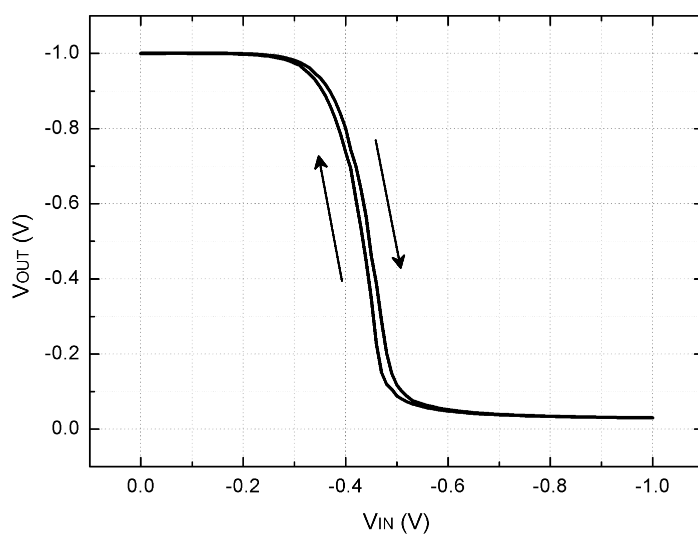

Figure 4.7. Voltage transfer curve of the inverter circuit.

From Figure 4.7, input high and input low voltages, V_{IH} and V_{IL}, were found as -0.34 V and -0.53 V, respectively. Switching threshold, V_M, was calculated as -0.44 V. Voltage gain at V_M was approximately -11 V/V. Almost rail-to-rail output performance was observed. Output high and output low voltages, V_{OH} and V_{OL}, were found as -0.03 V and -1.00 V, respectively. Voltage noise margins were calculated as 0.31 V for input high (VNM_H) and 0.47 V for input low (VNM_L).

In Figure 4.8, output of the inverter circuit is given for a 1 Hz square wave input signal. From the data, rise time, t_r, and fall time, t_f, were calculated as 37 ms and 50 ms, respectively. Propagation delay was found as 41 ms.

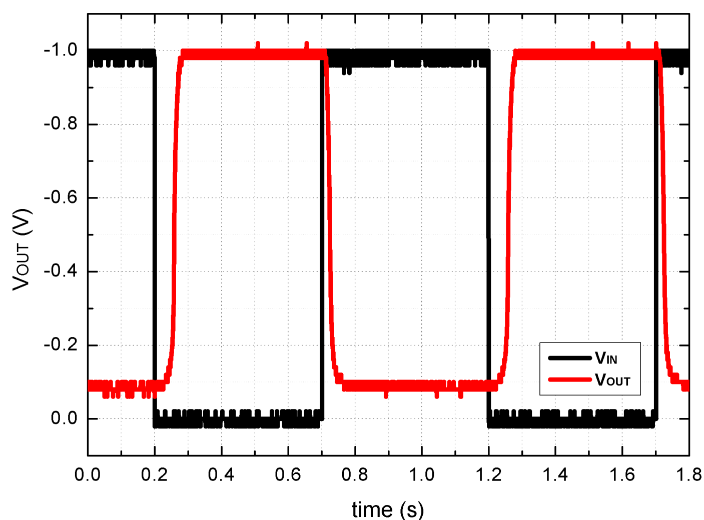

Figure 4.8. Input and output waveforms for the inverter circuit.

4.2. WG-FET Ring Oscillator

Ring oscillator circuits were realized with inverters shown in the previous section. First, three inverters were used as in Figure 4.9.

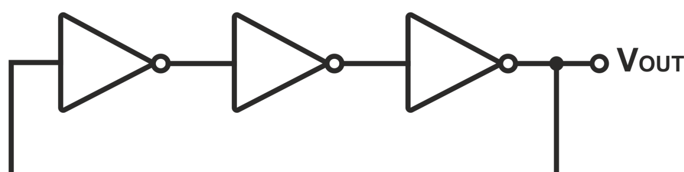

Figure 4.9. Ring oscillator circuit with three inverters.

In first tests, oscillation was not observed. Instead, output voltage was fixed to −0.54 V. When the input of first inverter was momentarily forced to ground and released, a decaying signal was observed at the output node as shown in Figure 4.10.

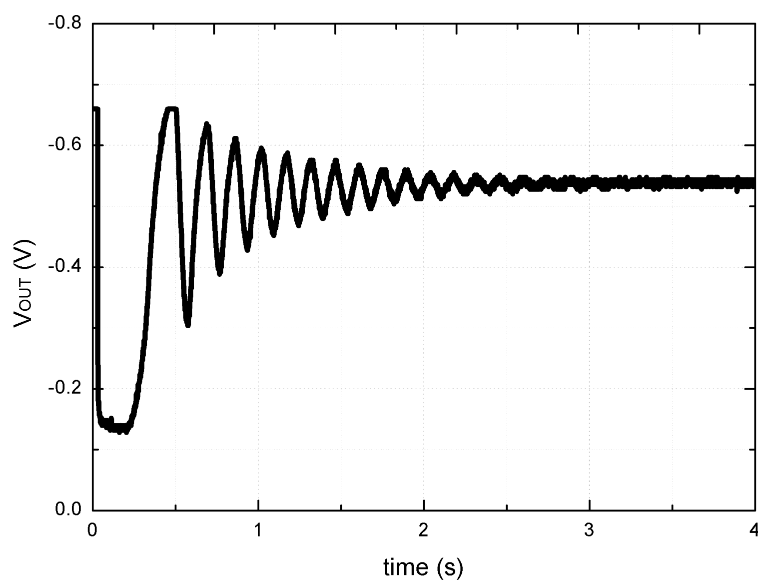

Figure 4.10. Decaying signal at the ring oscillator output.

Then, a 1 μF capacitor was connected to the output node to increase signal propagation delay. A sinusoidal signal with amplitude of 60 mV and frequency of 9 Hz was obtained at the output as given in Figure 4.11.

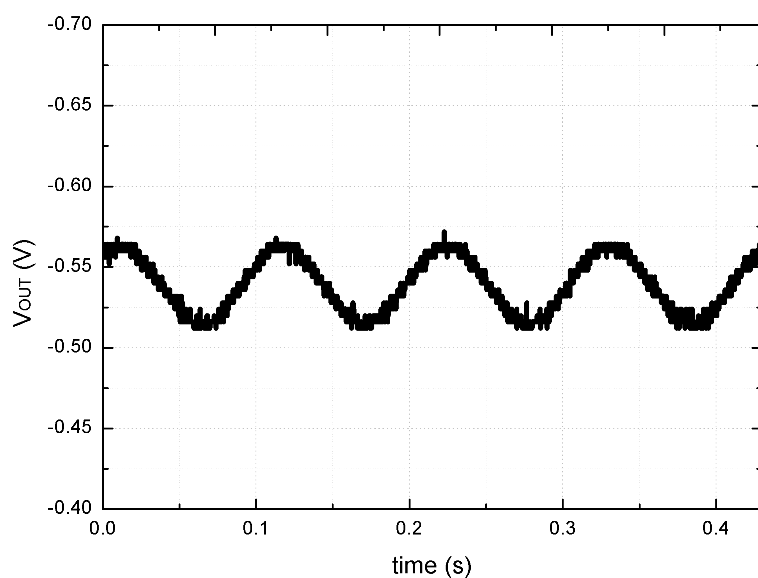

Figure 4.11. Output of the ring oscillator with a 1 μF capacitor.

Then, 1 μF capacitors were connected to input of each inverter to increase propagation delay further. Although oscillation frequency decreased to 1.9 Hz, signal amplitude increased to 580 mV. Obtained output signal is shown in Figure 4.12.

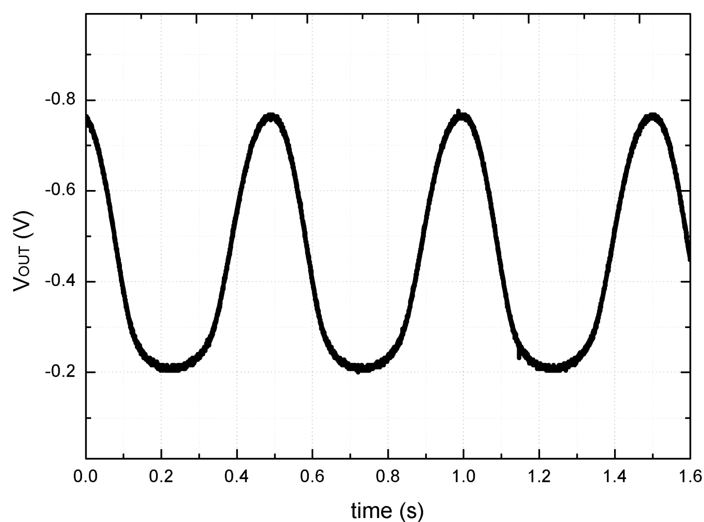

Figure 4.12. Output of the ring oscillator with three 1 μF capacitors.

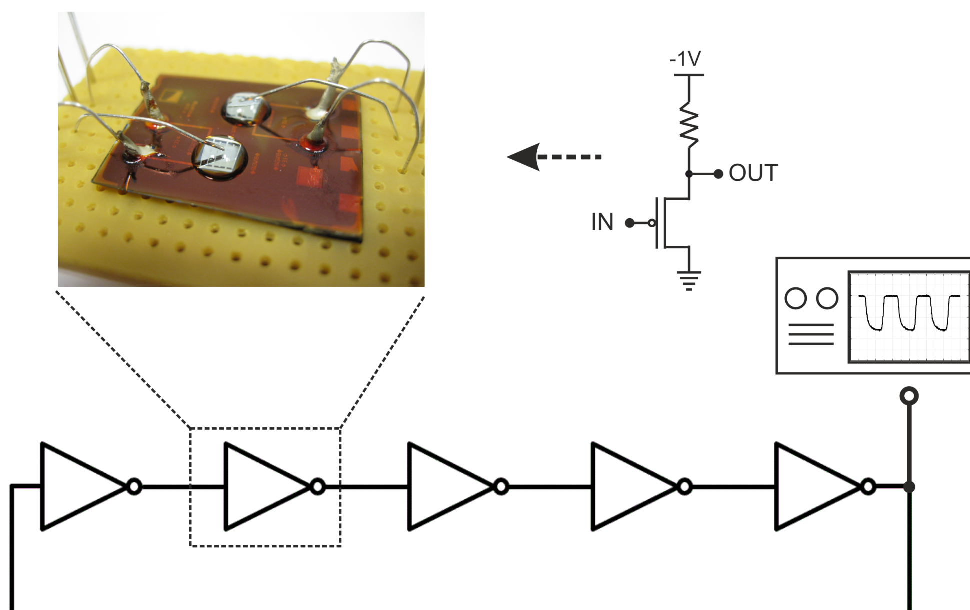

Figure 4.13. Ring oscillator circuit with five inverters.

To eliminate capacitors, a five-inverter ring oscillator was implemented as demonstrated in Figure 4.13. An output signal with amplitude of 840 mV and frequency of 2.6 Hz was obtained as shown in Figure 4.14.

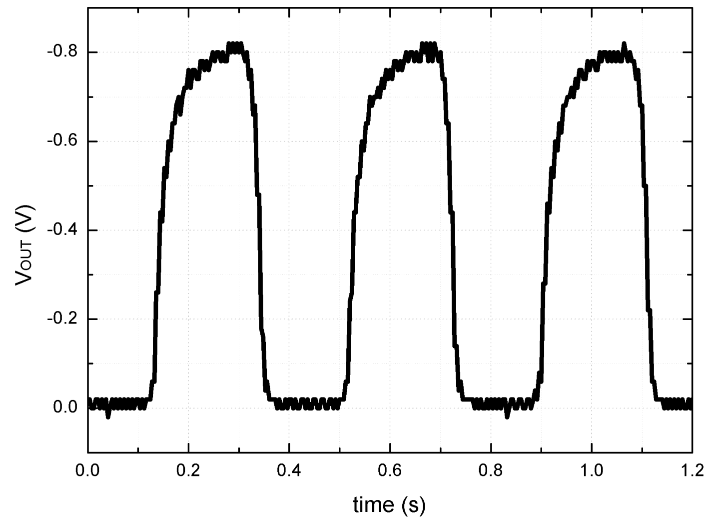

Figure 4.14. Output of the ring oscillator with five inverters.

5. CONCLUSION AND FUTURE WORK

5.1. Overview

Silicon-based MOSFET technology is the foundation for most of today's electronic devices. Since the first MOS circuits hit the market, device technology has been evolving to meet increasing demand for higher performance. Device features shrink to increase efficiency and speed, yet there are physical limits for this process. One of the main issues is the scaling of the gate oxide. As it gets thinner, gate leakage current increases due to quantum tunneling and devices become more vulnerable for dielectric breakdown. Under $1 - 1.5$ nm thickness, the natural oxide of silicon would not suffice and should be replaced with a high-κ material. Having a natural oxide makes the fabrication process easier for silicon-based devices compared to other semiconductors, which was one of the main reasons that made them market leader at the first place. Using high-κ materials require more complex fabrication and, thus, increase costs.

At that point, other device structures emerged which have alternative solutions for oxide scaling problem. One of them was EDLT structure. As the name suggests, EDLTs use electric double layer as insulator instead of gate oxide. EDL is formed at the interface when a solid is in touch with an electrolyte. It behaves like a parallel plate capacitor as explained by the Gouy-Chapman-Stern model. Very high electric fields can be obtained at EDL without the risk of dielectric breakdown. Also, using electrolyte for EDL makes EDLTs naturally compatible with fluidic systems which remarkably broadens their application area.

In this thesis, an EDLT device named as water-gated field effect transistor is introduced. It uses 16-nm-thick sc-Si as active layer, therefore it has the superior charge mobility of sc-Si and 2DEG feature of the ultra thin active layer. It is an SOI-based device, therefore it is compatible with existing MOSFET fabrication process.

De-ionized water is used as electrolyte in WG-FET to obtain an EDL layer as a pinhole-free, ultra thin, high-κ gate insulator. No ionic compounds are necessary which makes the device more robust. WG-FET is a promising device for microfluidic applications due to its inherent fluidic interface. EDL characteristics are sensitive to the properties of the Si surface and electrolyte. Therefore, it can also be manipulated for sensor operation. These features present WG-FET as a platform where sensors and read-out circuits can be combined at transistor level.

Here, WG-FET devices with both probe- and planar-gate structures are investigated. Mathematical models are proposed for transistor operation and compared to the experimental data. Fabrication details and layouts for different WG-FET topologies are explained. Effects of gate electrode position, bulk contact, source/drain insulation on transistor performance are tested. Improvements in fabrication process about device performance and repeatability are explained for each device generation.

Various WG-FET devices are tested in experiments. Best performance is obtained with probe-gate setups as expected from theoretical simulations. Planar-gate setup has inferior but plausible results when gate electrode is placed near to the channel. Transistor performance deteriorates with increasing planar-gate distance. When insulation of source and drain electrodes is removed, transistor performance is increased for probe-gate setup. Better ON/OFF ratios are obtained due to absence of parasitic resistances. However, a proper transistor operation is not achieved with planar-gate setup without source/drain electrode insulation. Unlike probe-gate, gating effect of drain electrode is comparable with planar-gate and it manifests itself at even higher V_{GS} values. Topology specific parameters, which are extracted from theoretical simulations for corresponding WG-FET devices, are in agreement with experimental measurements.

As a circuit application of WG-FET, inverter circuits are implemented. Near rail-to-rail operation and acceptable noise margins are achieved. By using these inverters, ring oscillator circuits, which consist of three and five sequential inverters, are realized.

5.2. Future Work

WG-FET devices have a wide application area. Their inherent fluidic interface make them valuable elements for biomedical applications. Therefore, integration of WG-FET devices with microfluidic channels can be useful. Since WG-FET has a flexible design, they can be fabricated as they extend throughout the fluidic channel. Planar-gate topology can make the integration process easier due to whole planar device layout.

WG-FETs used in this work are all p-type devices. Fabrication of n-type devices would make implementation of complementary circuits possible. Thus, more complex and efficient circuits can be realized by using only WG-FETs.

Si/electrolyte fluidic interface can be exploited further for sensor applications. pH and ion concentration dependence of EDL can be used for this purpose. [102] WG-FETs are also good candidates for components of label-free detection systems. With integration of microfluidic channels, WG-FET-based sensor arrays can be implemented. Active Si surface can be functionalized for specific biomolecule detection.

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APPENDIX A: PHOTOLITHOGRAPHIC MASKS

A.1. First Generation WG-FET Masks

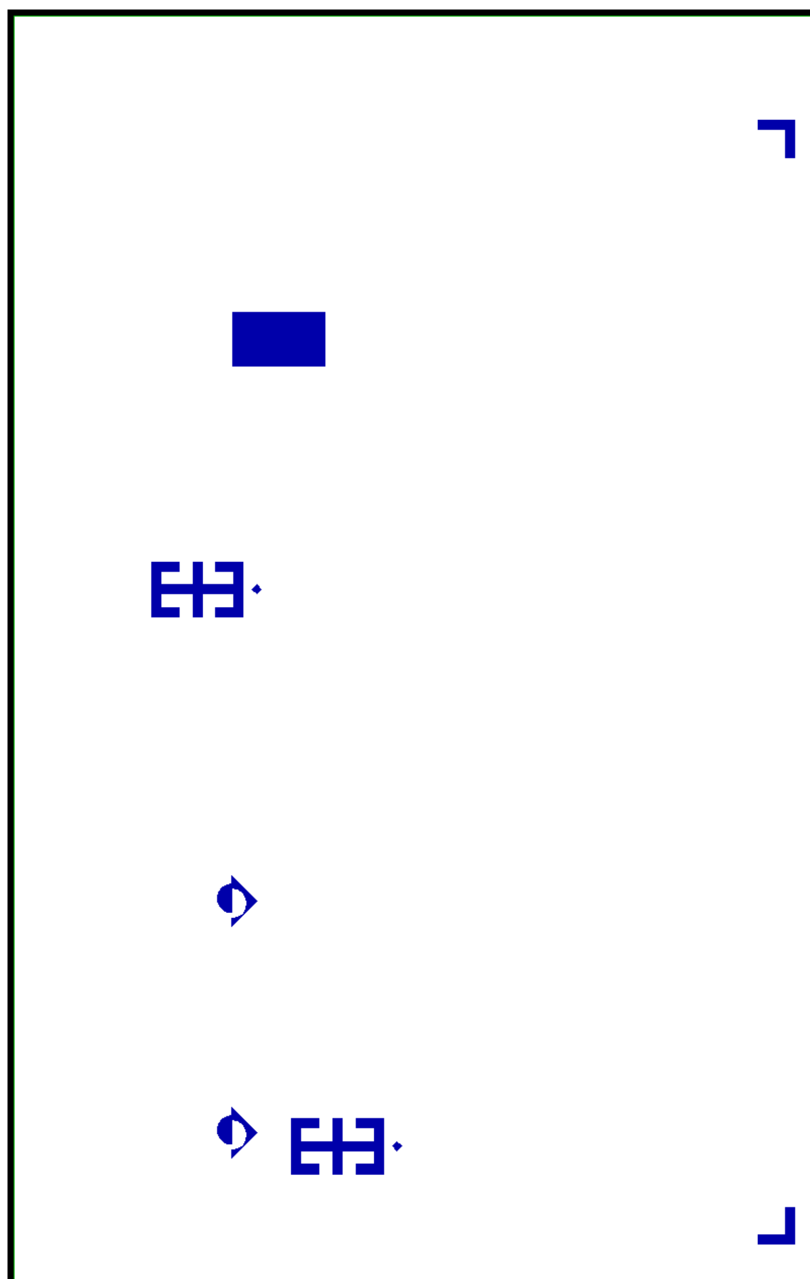

Figure A.1. Si mask for first generation WG-FETs.

Figure A.2. Al mask for first generation WG-FETs.

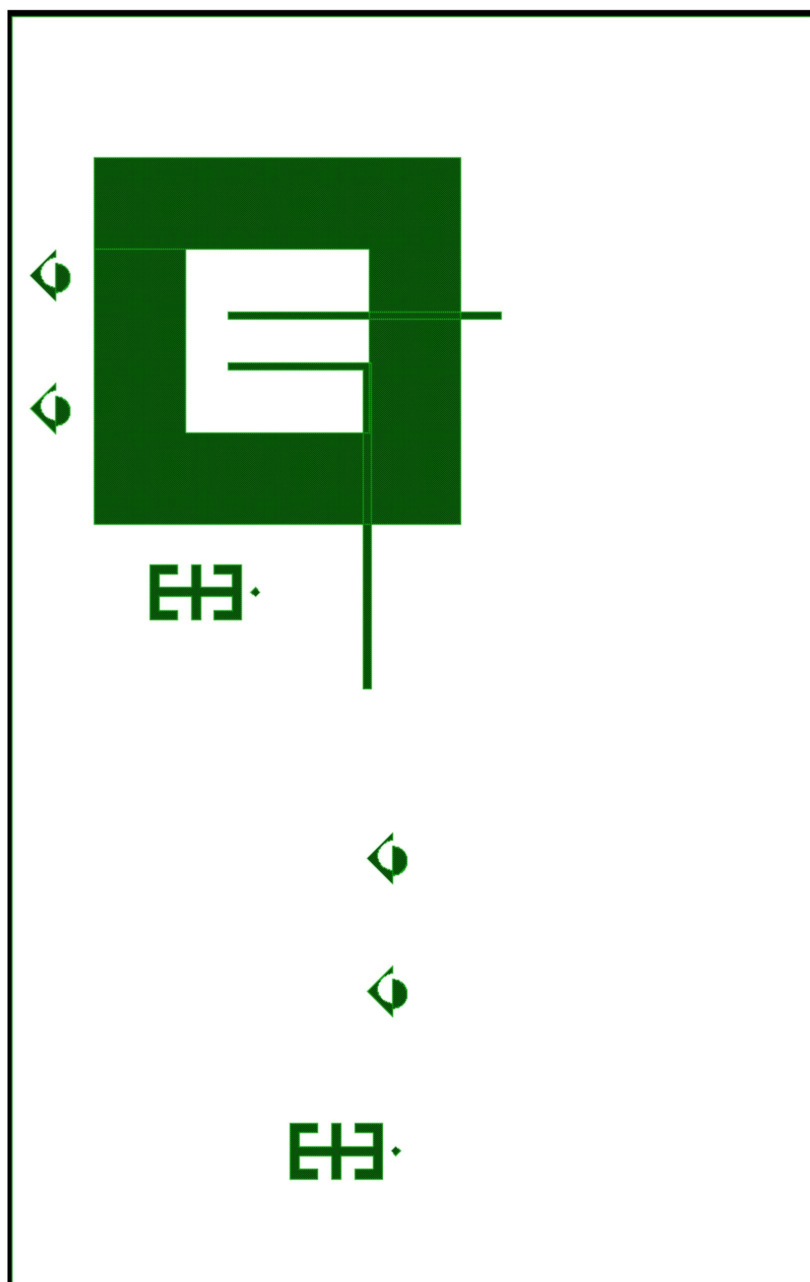

Figure A.3. Photoresist mask for first generation WG-FETs.

A.2. Second Generation WG-FET Masks

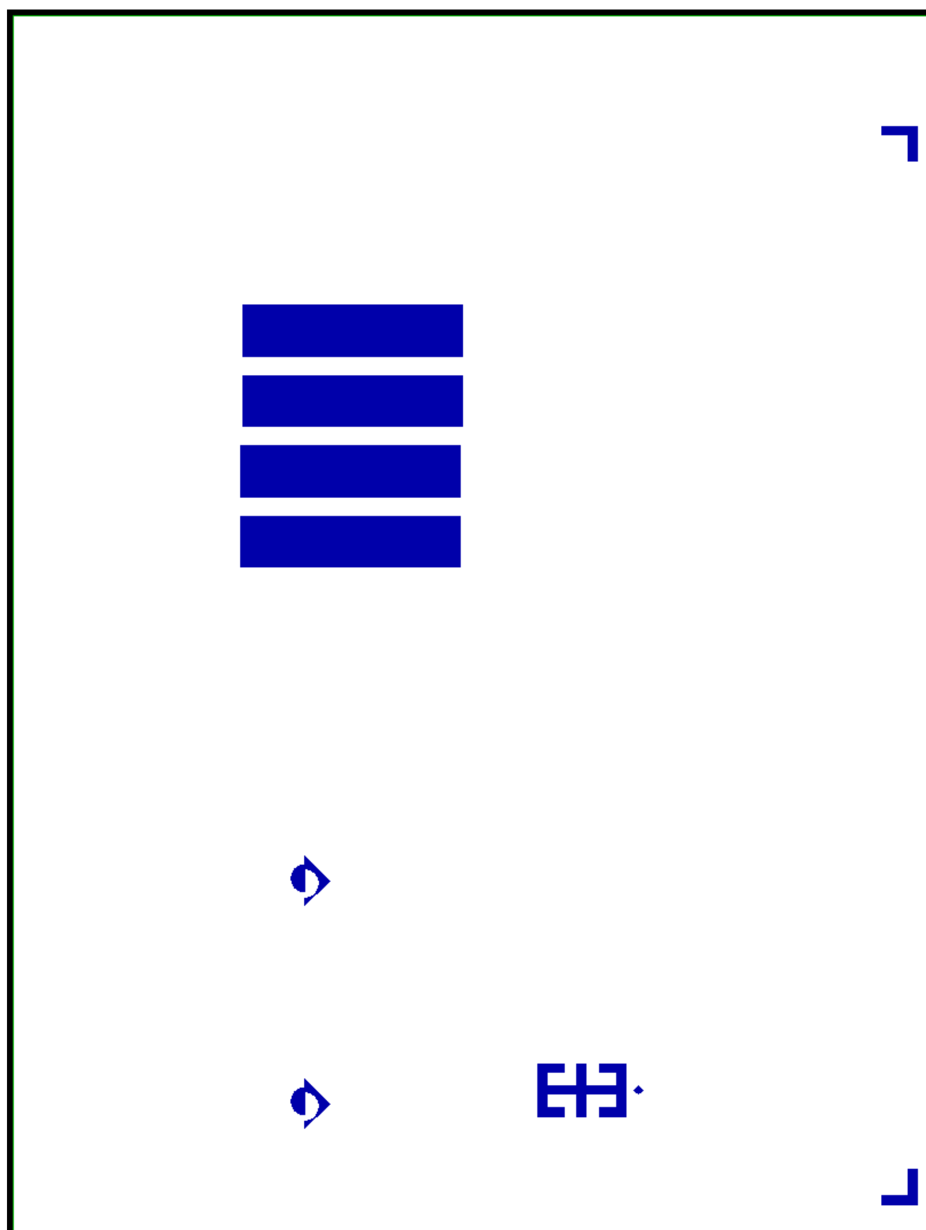

Figure A.4. Si mask for second generation WG-FETs.

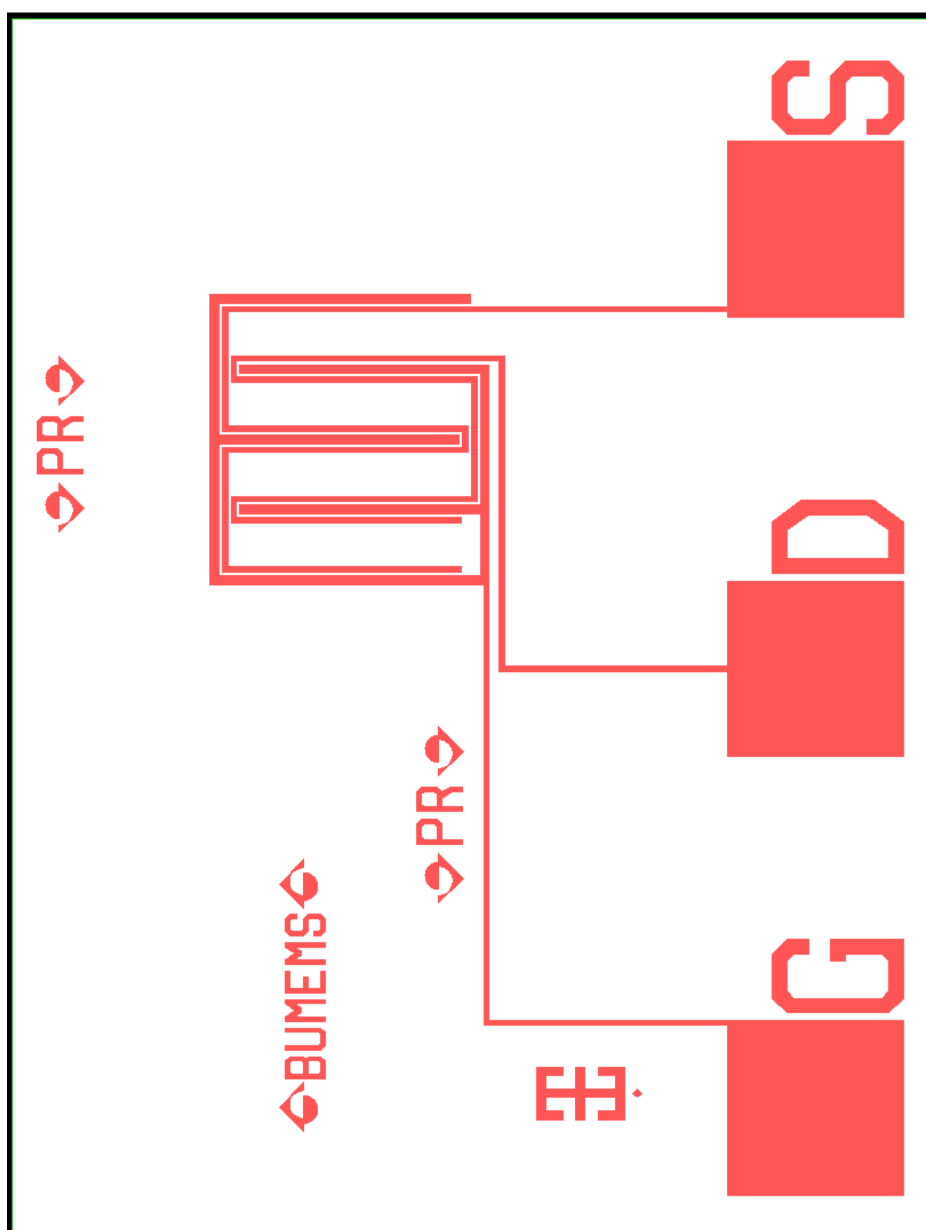

Figure A.5. Al mask for second generation WG-FETs.

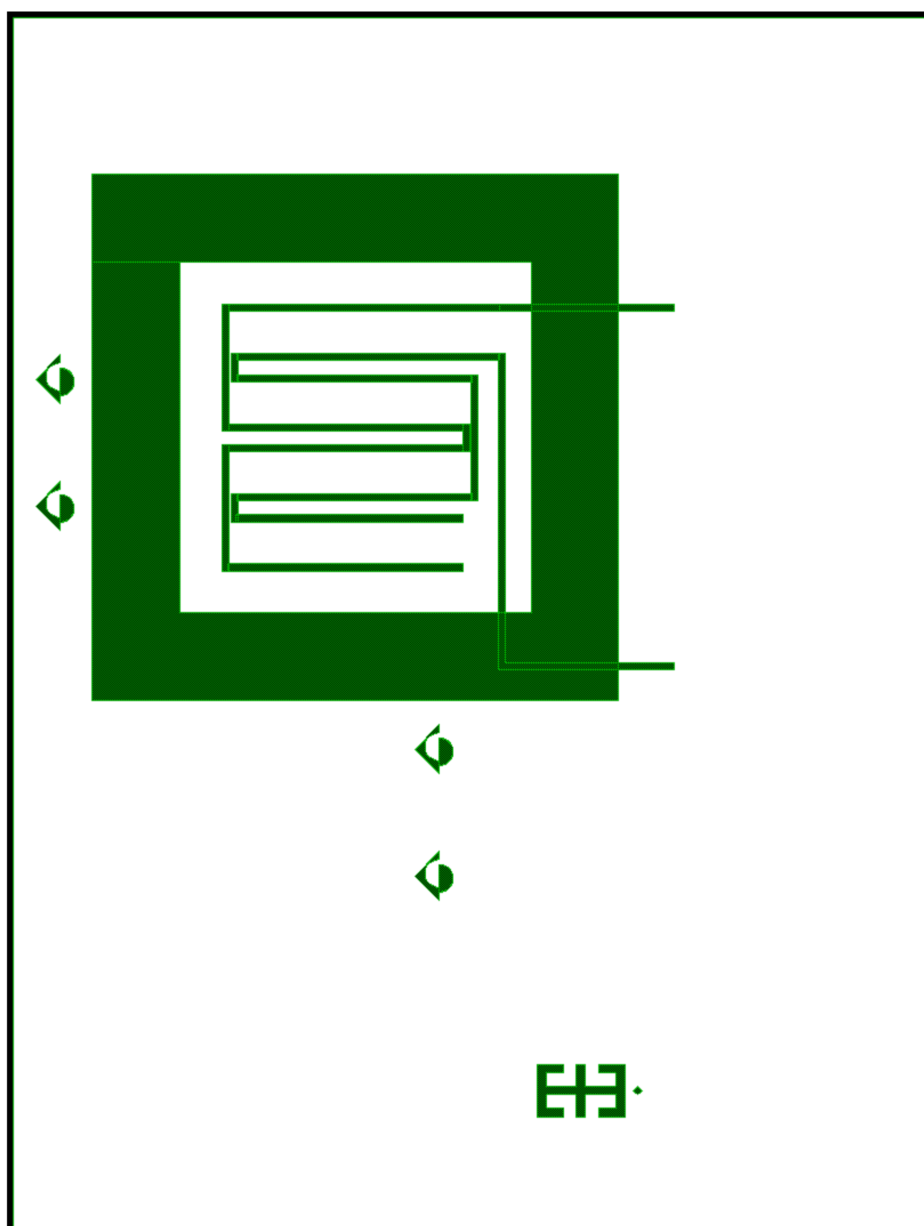

Figure A.6. Photoresist mask for second generation WG-FETs.

A.3. Third Generation WG-FET Masks

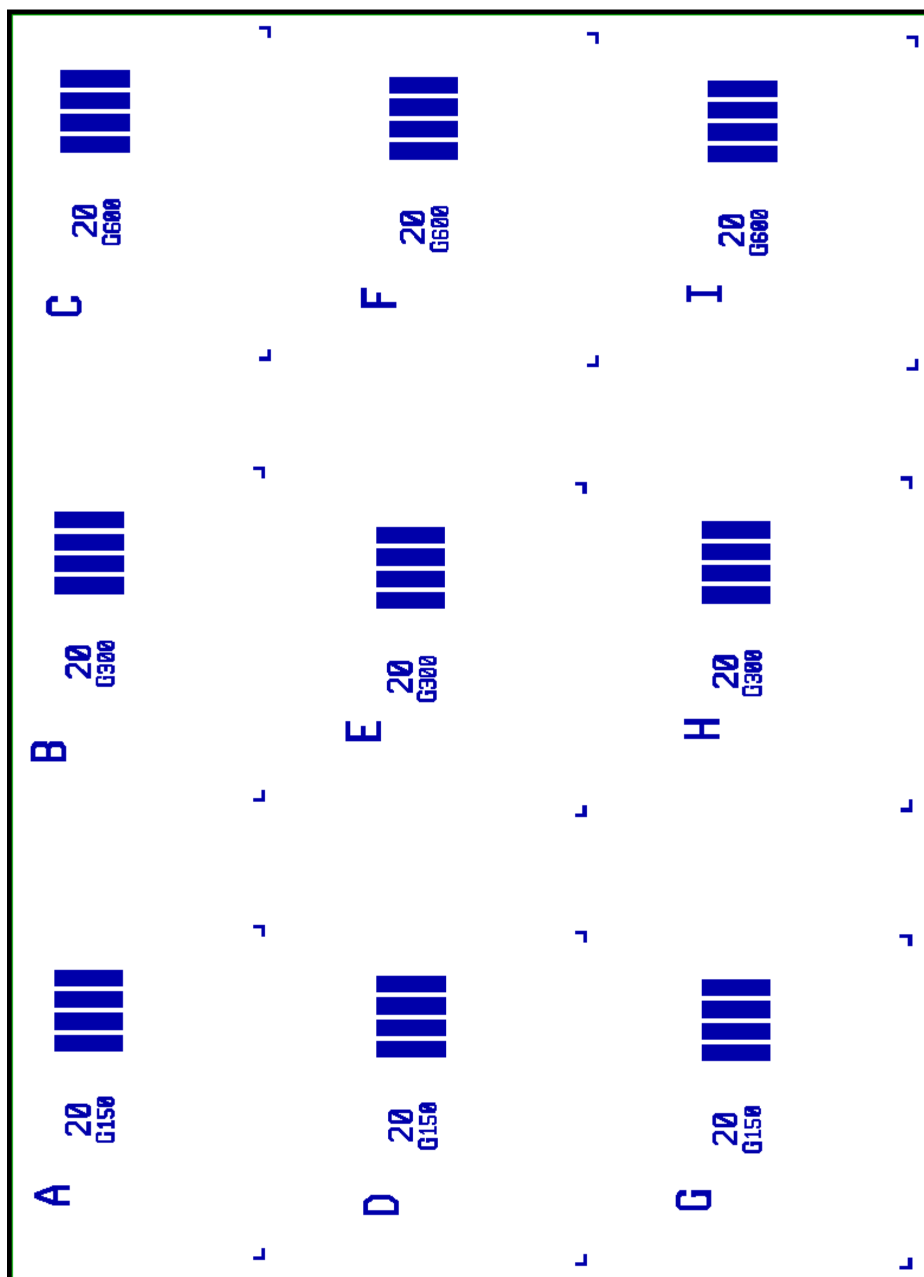

Figure A.7. Si mask for third generation WG-FETs.

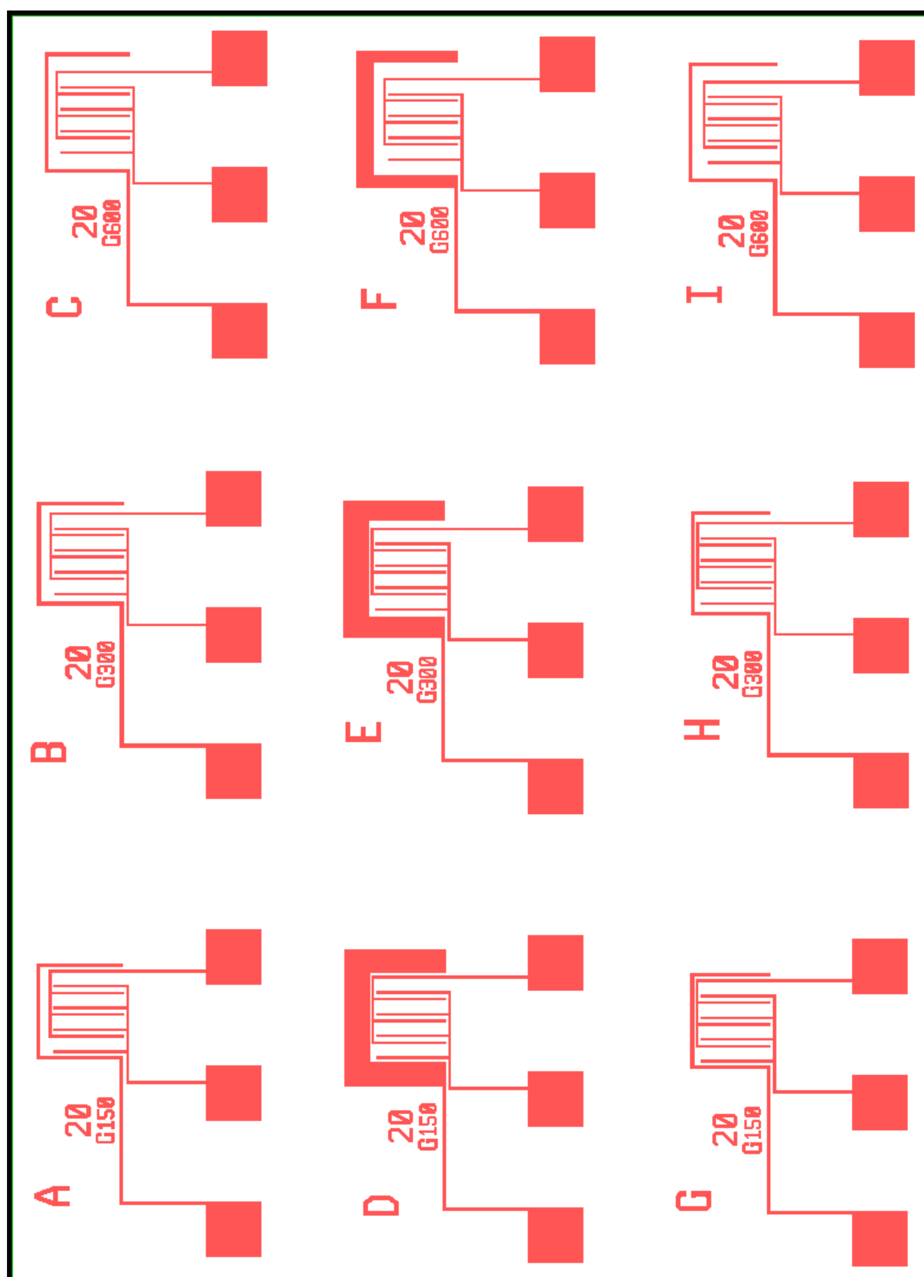

Figure A.8. Al mask for third generation WG-FETs.

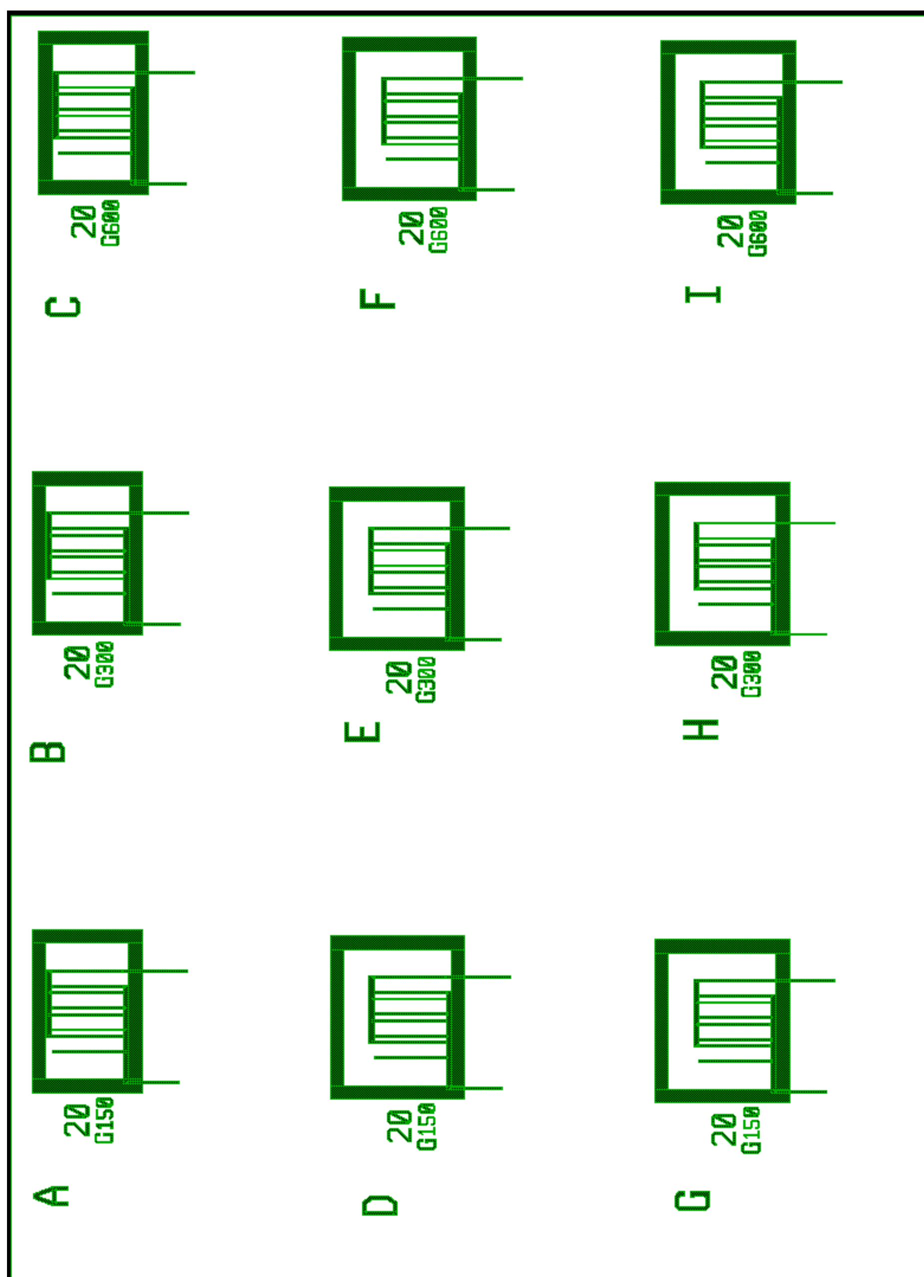

Figure A.9. Photoresist mask for third generation WG-FETs.

A.4. Fourth Generation WG-FET Masks

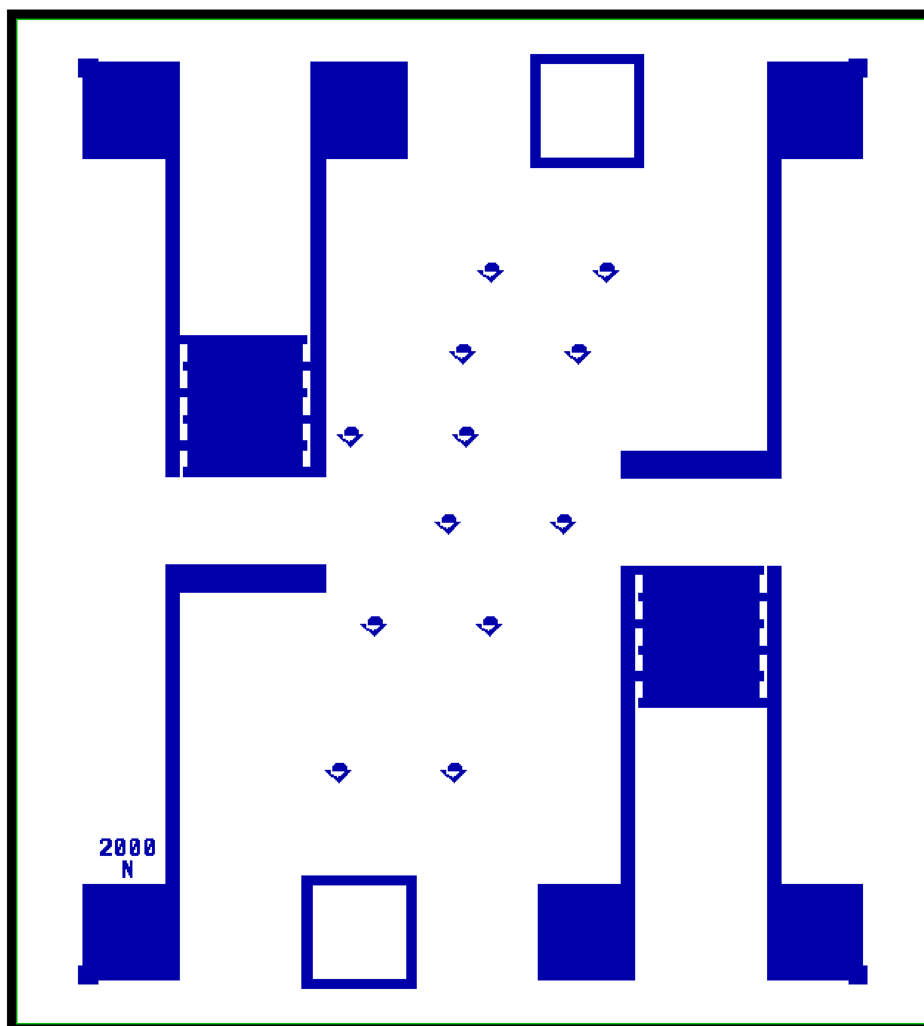

Figure A.10. Si mask for fourth generation WG-FETs.

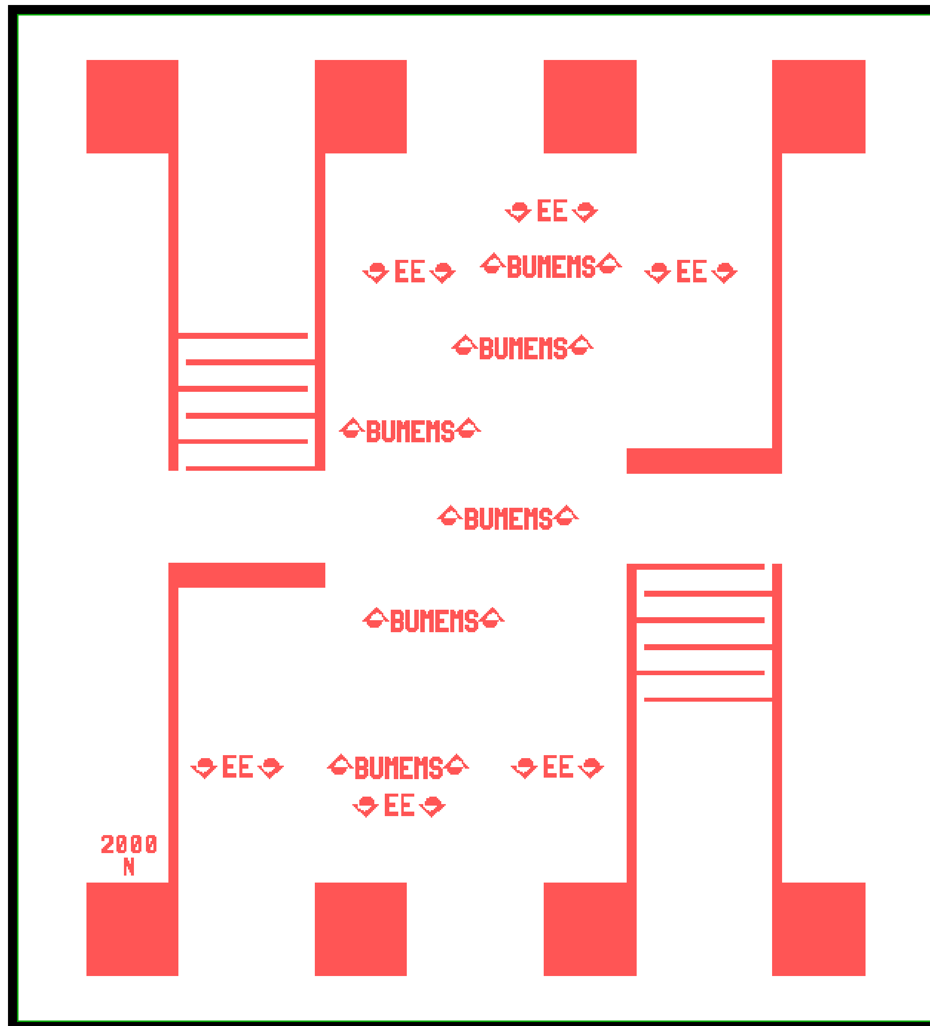

Figure A.11. Al mask for fourth generation WG-FETs.

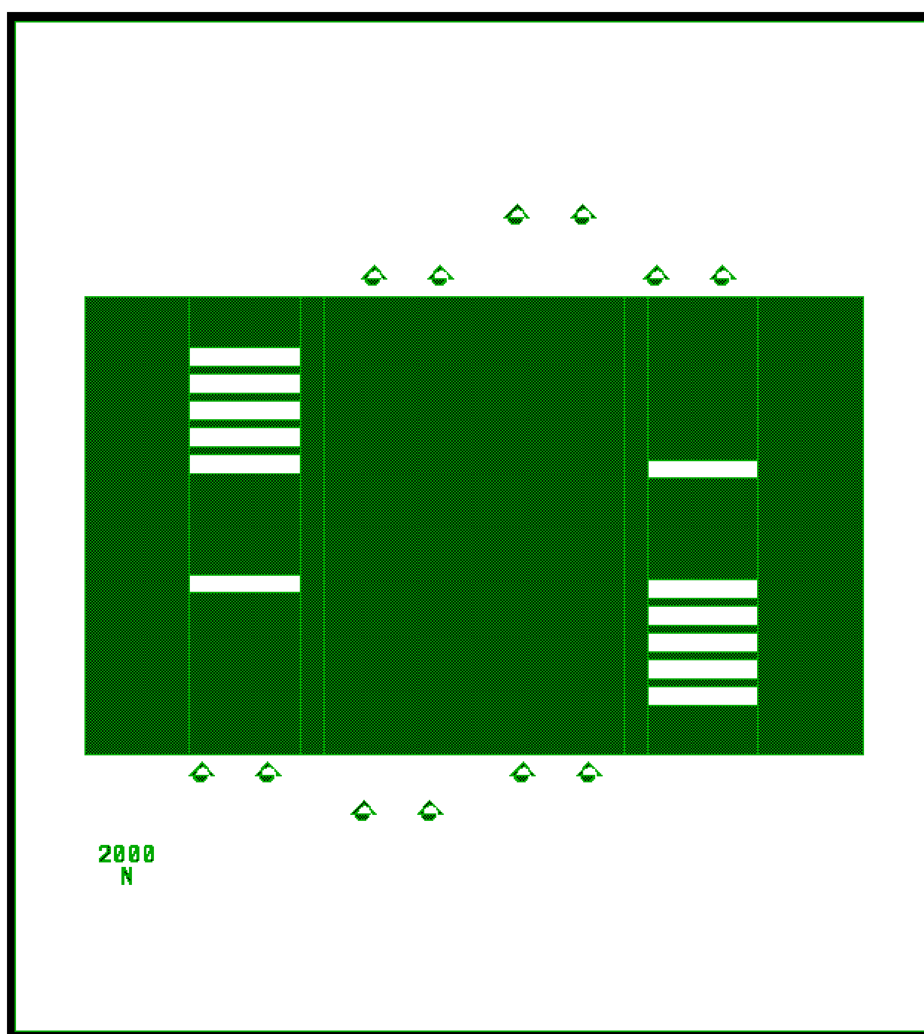

Figure A.12. Photoresist mask for fourth generation WG-FETs.

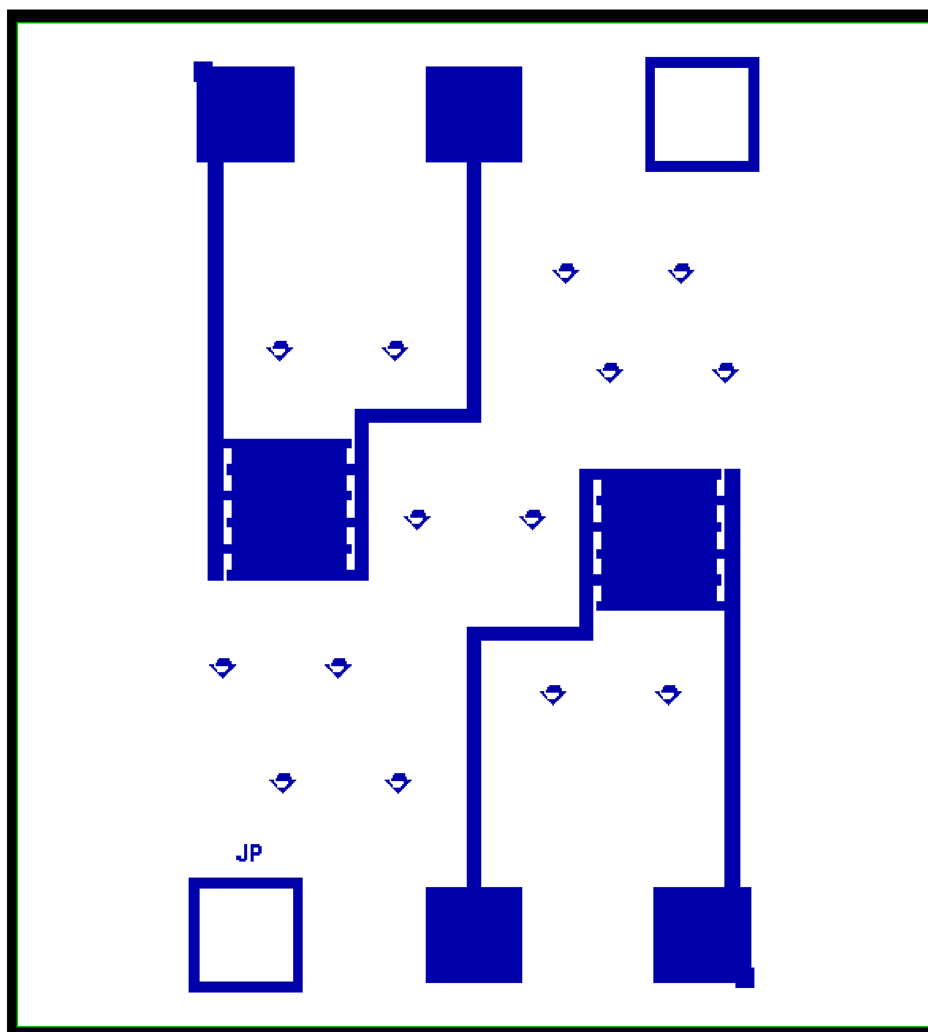

Figure A.13. Si mask for fourth generation WG-FETs without planar-gate electrode.

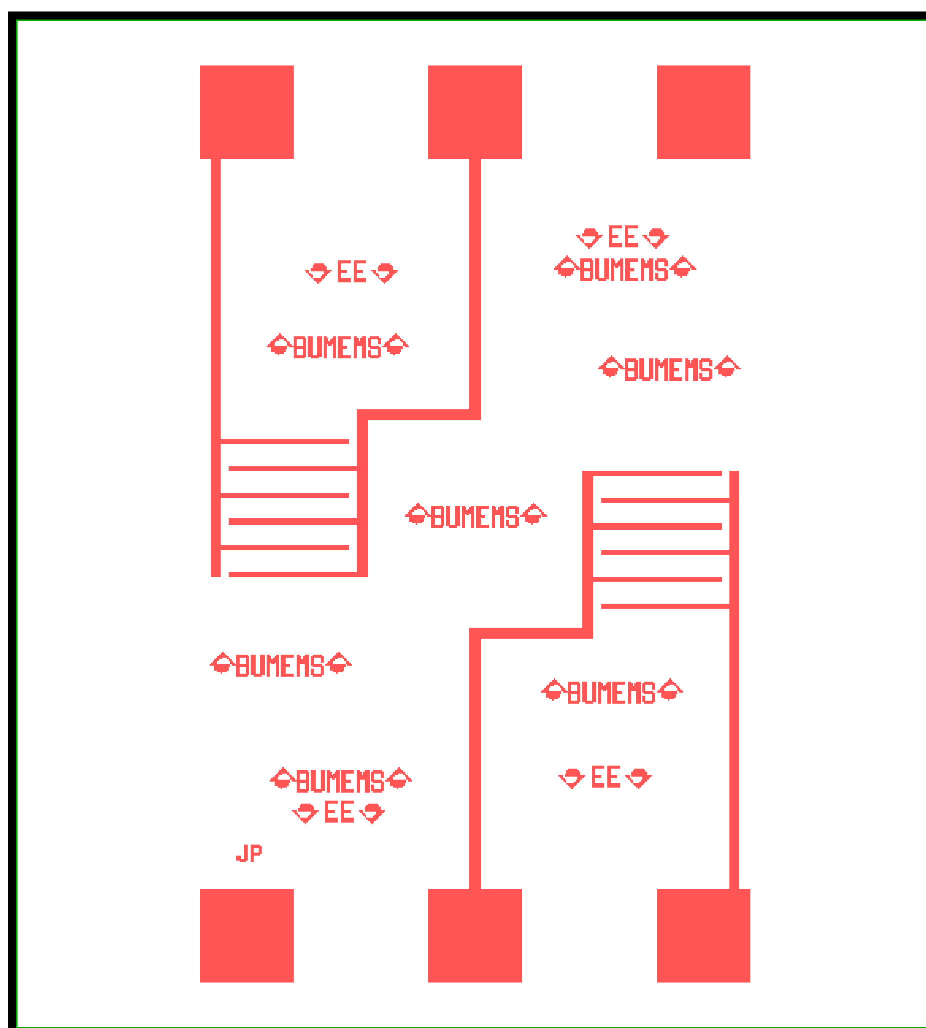

Figure A.14. Al mask for fourth generation WG-FETs without planar-gate electrode.

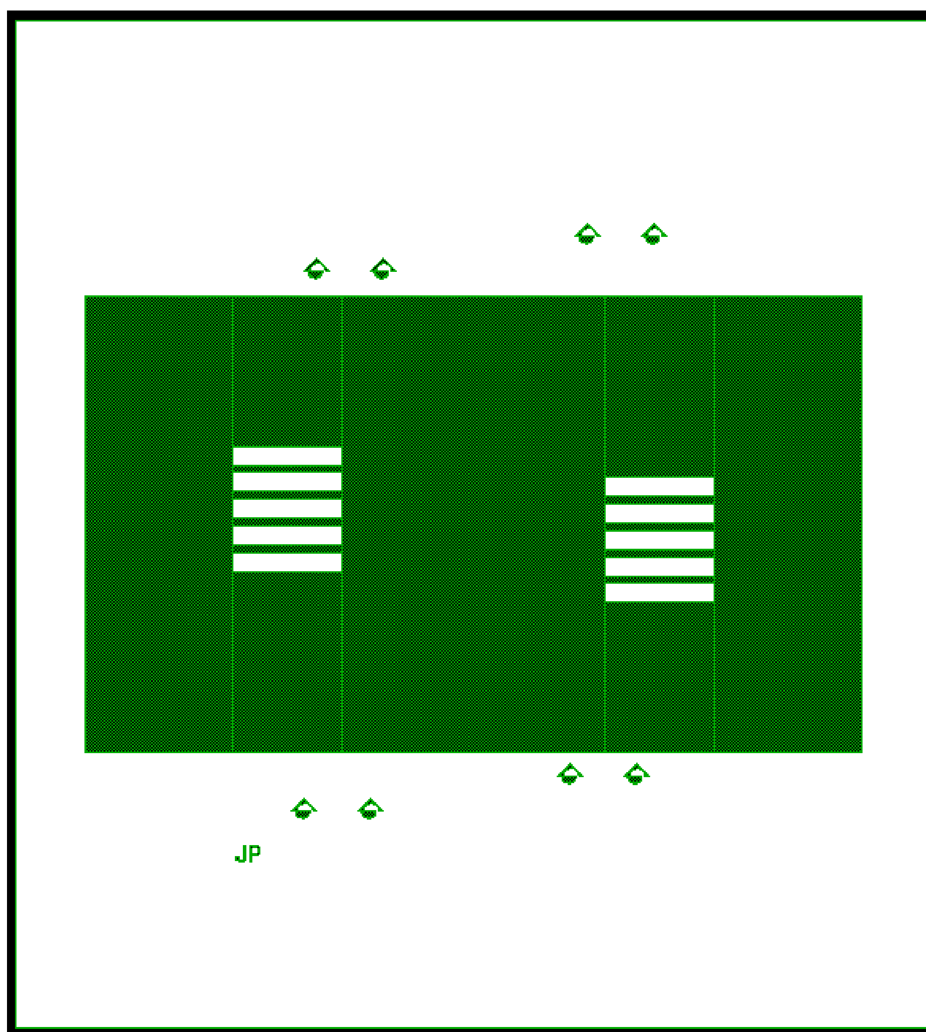

Figure A.15. Photoresist mask for fourth generation WG-FETs without planar-gate electrode.

A.5. Capacitance Measurement Sample Masks

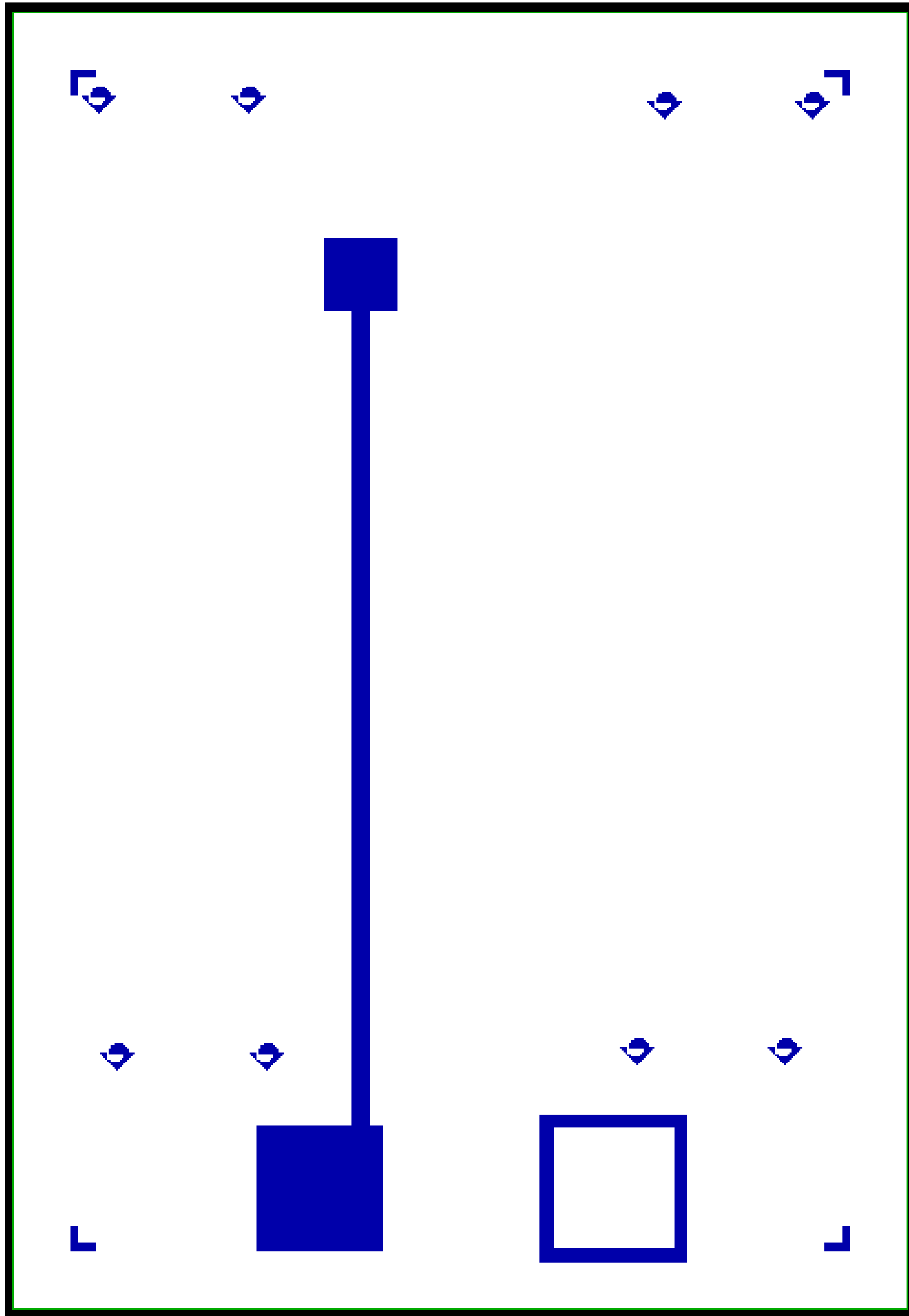

Figure A.16. Si mask for capacitance measurement sample.

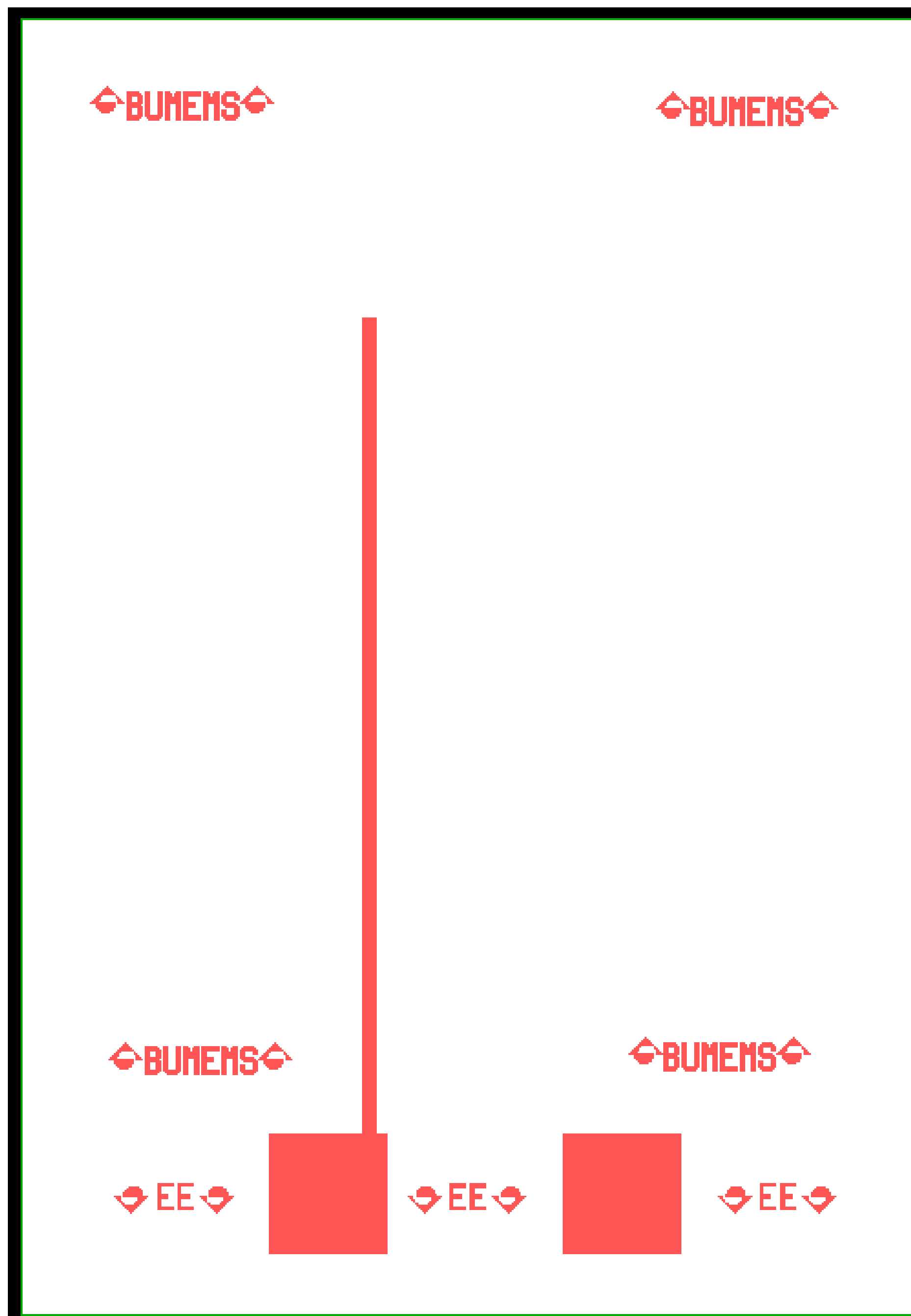

Figure A.17. Al mask for capacitance measurement sample.

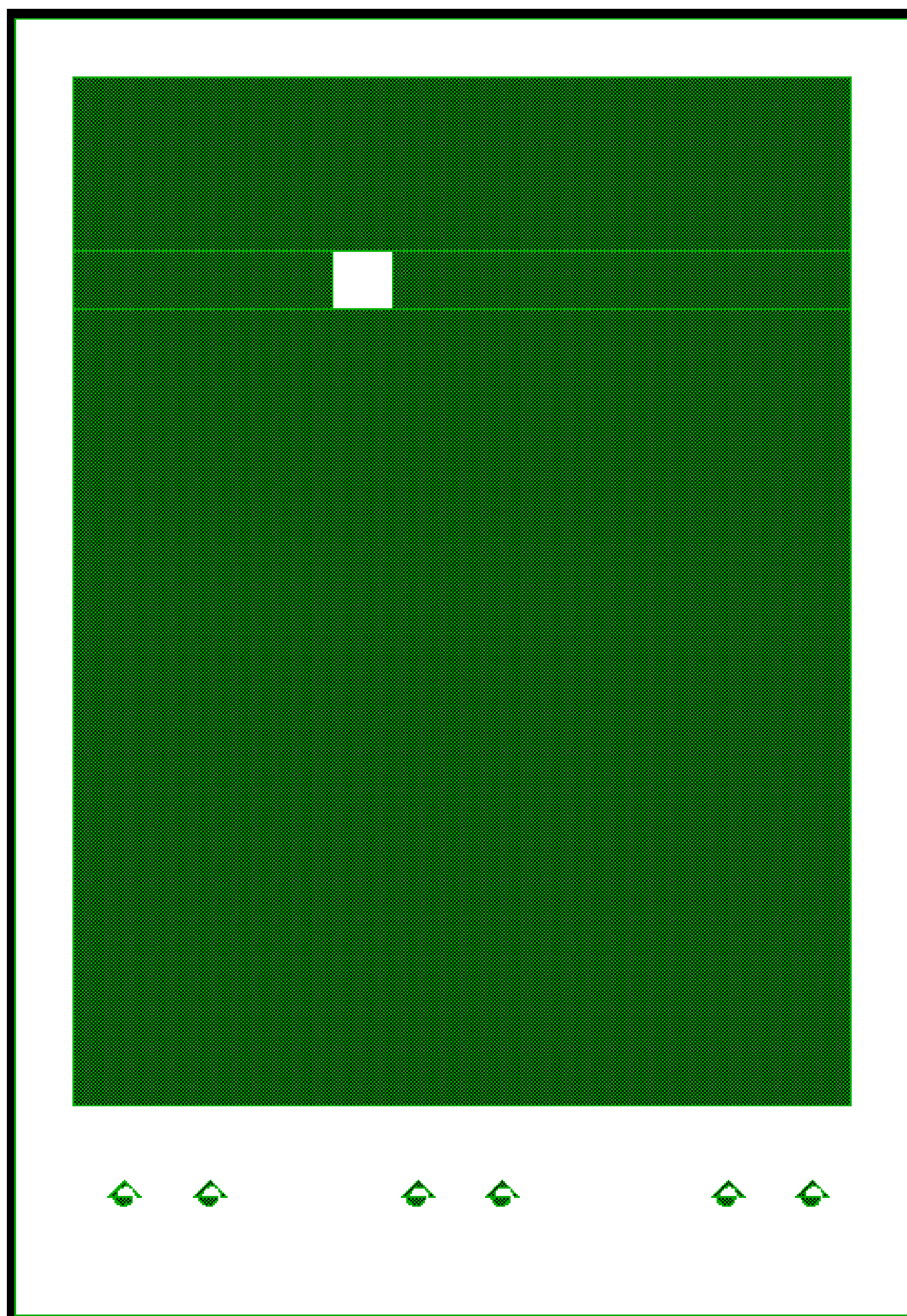

Figure A.18. Photoresist mask for capacitance measurement sample.