

TEMPERATURE INSENSITIVE ULTRA LOW POWER 0.7 V SUPPLY INPUT
AND REFERENCE DRIVER FOR 8 BIT ADC IN 65 NM CMOS TECHNOLOGY

by

Berk As

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ABSTRACT

TEMPERATURE INSENSITIVE ULTRA LOW POWER 0.7 V SUPPLY INPUT AND REFERENCE DRIVER FOR 8 BIT ADC IN 65 NM CMOS TECHNOLOGY

With CMOS technology scaling down, performance of ADCs has been improving in terms of area, low supply voltage and especially ultra-low power consumption. However, analog performance has not been advancing compared to progress of the digital performance as CMOS technology is scaling down. This causes the design of ultra-low power ADC input driver still challenging due to its analog architecture. Settling time requirements, ADC input capacitance, low noise and THD requirements limits performance of ADC input driver for ultra-low power operation. On the other hand, off-chip drivers lead to usage of larger area unnecessarily. This thesis offers the design of an on-chip temperature insensitive, ultra-low power input and reference driver for 8 bit ADC with 0.7 V supply. Temperature insensitivity is an essential feature for temperature measurement to avoid the degradation of ADC performance as the temperature varies. The proposed design is able to drive 8 bit ADC along operating temperature range (from -40°C to 125°C). The proposed ADC input driver performs single ended to differential signal conversion, buffering, amplitude scaling, output common-mode adjustment and filtering. In the thesis, an ultra-low power 0.7 V supply temperature sensor operating from -40°C and 125°C and 100 kSPS differential input SAR ADC with 1V full scale input range is used. ADC reference driver is configured as current controlled non-inverting unity gain buffer between bandgap reference circuit and ADC reference voltage pin. According to the post-layout simulation results, average power consumption over operating temperature range is $111.53\ \mu\text{W}$. As a worst case scenario, total output noise voltage is 1.418 mV at -40°C . The input driver has a THD of -72.51 dB at 244 Hz and -70.88 dB at 976 Hz.

ÖZET

65 NM CMOS TEKNOLOJİSİNDE 8 BIT ADC İÇİN SICAKLIĞA DUYARSIZ ULTRA DÜŞÜK GÜÇ 0.7 V BESLEMELİ GİRİŞ VE REFERANS SÜRÜCÜSÜ

CMOS teknolojisinin küçülmesiyle birlikte, ADC'lerin performansı alan, düşük besleme voltajı ve özellikle çok düşük güç tüketimi açısından iyileşmektedir. Bununla birlikte, CMOS teknolojisi küçülürken, teknolojinin analog performansındaki ilerleme, sayısal performansına kıyasla daha azdır. Bu durum, analog mimarisi nedeniyle ultra düşük güçlü ADC giriş sürücüsünün tasarımını zorlaştırmaktadır. Yerleşme süresi gereksinimleri, ADC giriş kapasitansı, düşük gürültü ve THD gereksinimleri, ADC giriş sürücüsünün ultra düşük güçte çalışması için performansını sınırlar. Öte yandan, çipsiz sürücüler gereksiz yere daha büyük alan kullanımına yol açmaktadır. Bu tez, 0,7 V beslemeli 8 bit ADC için çip üzerinde sıcaklığa duyarlı, ultra düşük güçte çalışan giriş ve referans sürücüsünün tasarımını sunar. Sıcaklık duyarlılığı, sıcaklık değişikçe ADC performansının düşmesini önlediğinden dolayı sıcaklık ölçümleri için önemli bir özelliktir. Önerilen tasarım, çalışma sıcaklığı aralığı boyunca (-40°C ile 125°C) 8 bit ADC'yi sürebilir. Önerilen ADC giriş sürücüsü, tek uçlu-diferansiyel sinyal dönüşümü, tamponlama, genlik ölçeklendirme, çıkış ortak mod ayarı ve filtrelemeyi gerçekleştirir. Tez çalışmasında, -40°C ile 125°C arasında çalışan ultra düşük güçte 0.7 V beslemeli sıcaklık sensörü ve 1V tam ölçekli giriş aralığına sahip 100 kSPS diferansiyel giriş SAR ADC kullanılmıştır. ADC referans sürücüsü, bant aralığı referans devresi ile ADC referans voltajı pini arasında akım kontrollü, ters çevrilmemiş birlik kazanç tamponu olarak yapılandırılmıştır. Serim sonrası simülasyon sonuçlarına göre, çalışma sıcaklığı aralığında ortalama güç tüketimi $111,53\ \mu\text{W}$ 'dır. En kötü senaryo olarak, toplam çıkış gürültüsü gerilimi -40°C 'de $1.418\ \text{mV}$ 'tur. Giriş sürücüsü $244\ \text{Hz}$ 'de $-72.51\ \text{dB}$ 'lik ve $976\ \text{Hz}$ 'de $-70.88\ \text{dB}$ 'lik bir THD performansına sahiptir.

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LIST OF SYMBOLS

A	Amper
$^{\circ}C$	Celcius
C	Capacitance
F	Farad
k	Boltzman constant
k_f	Flicker noise coefficient
g_m	Transconductance
I	Current
q	Electric charge
R	Resistance
V	Voltage
β	Feedback factor
γ	Thermal noise coefficient
Ω	Ohm

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
MOS-FET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	Negative-Channel Metal Oxide Semiconductor
OTA	Operational Transconductance Amplifier
PMOS	Positive-Channel Metal Oxide Semiconductor
RMS	Root Mean Square
SAR	Successive Approximation Register
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion

1. INTRODUCTION

1.1. Background

SAR ADCs are highly demanded devices for medium to high resolution ADCs. In the market, they can be found with maximally 5 Msps sampling rate and varying resolutions from 8 to 18 bit. SAR ADCs provide low power consumption, great accuracy and high resolution. Due to all these features, SAR ADCs can be used in various applications such as battery powered instruments, industrial controls, communication and medical implementations [14]. While the internal clock of the SAR ADC operates at several Mhz, the sampling rate is a fraction of that due to the successive approximation algorithm. Low sampling rate is the main disadvantage of the SAR ADCs.

SAR ADCs can be classified into three according to their input types: single ended, pseudo differential and differential. Differential input SAR ADCs have superior attributes against other input types of ADCs. Differential input signal offers two times dynamic range with same supply-reference voltage and power consumption compared to the single ended and pseudo differential inputs. Figure 1.1 illustrates that input characteristics of a differential input SAR ADC. As shown in Figure 1.1, input differential signals are 180° out of phase with each other while the input common mode voltage equals to half of the full scale input voltage and is ideally constant through operation. With these input characteristics, noise immunity and THD performance are improved due to the fact that it offers a maximum noise rejection and cancels out even order harmonics [2]. These features become much more critical in low voltage and ultra-low power applications. In the thesis, a low supply voltage and ultra-low power ADC input driver is designed for a differential input SAR ADC.

ADC input driver is an interface circuit between an analog input signal and an ADC. For micro-powered sensors which generate an analog input signal, providing settling time requirement within an acquisition time of a SAR ADC may be challenging. Due to high output impedance of ultra-low power sensors, serious signal attenuation

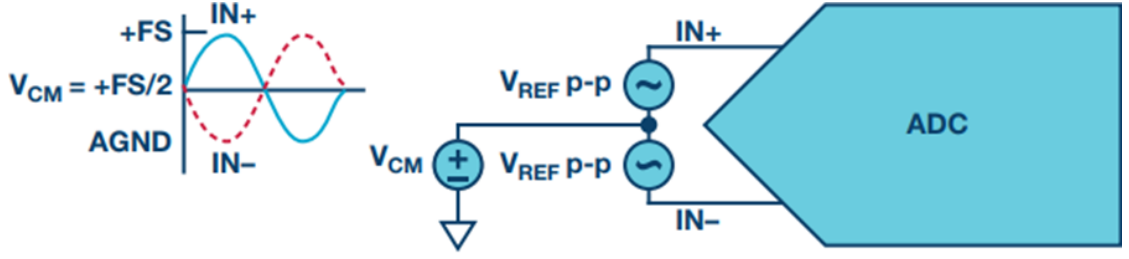


Figure 1.1. Input Characteristics of a Differential Input SAR ADC [1].

can occur. A buffer amplifier driver generally is required at these situations. An ADC input driver functions as not only a buffer but it also scales the analog input signal. Full scale of analog input signal may be a fraction of full scale of ADC input. To take advantage of full scale voltage range of ADC, an input driver is able to multiply the peak-to-peak signal of the analog input by a desired gain. A sensor often produces a single ended output signal. ADC input driver converts the single ended to differential signal for differential input ADCs. As discussed before, common mode input level of a differential input SAR ADCs should be constant for proper operation. ADC input driver operates the input common mode adjustment for SAR ADCs. As a last function, an input driver performs filtering to noise reduction to avoid performance degradation of ADCs. All these features are also valid for reference driver which is a front-end circuit between reference voltage source and ADC reference input pin.

In this thesis, an ADC input and reference driver design are proposed to drive a specific ultra-low power temperature sensor for an ultra-low power differential input SAR ADC. The design motivations of the input and reference driver are low power consumption, simplicity and on-chip design. Generally, the power consumption of the ADC driver is higher than that of the ADC. This results from analog structure of the driver and using external amplifiers. The analog performance is related to the technology model. However, using external amplifiers is a designer choice. On-chip input driver design provides the optimization for specific load and timings of the ADC. In addition, application specific design offers power efficiency in contrary to external drivers since a design procedure is determined according to needs of a sensor and ADC.

1.2. Approach

Selection of right ADC driver configuration depends on the specifications of ADC. Each ADC feature should be examined carefully to obtain the best performance of the driver. It may cause the degradation of the ADC performance unless the driver is designed according to its specifications.

In this thesis, a temperature sensor which has a temperature range from -40°C to 125°C is used. Its output voltage varies from 488.24 mV to 629.67 mV. Input common mode of the temperature sensor is calculated by equation (1.1).

$$\begin{aligned} V_{incm} &= \frac{V_{max} + V_{min}}{2} \\ &= 558.96mV \end{aligned} \tag{1.1}$$

On the other hand, differential input SAR ADC with full scale of 1 V and 0.35 V input common mode is used. Different input common mode values of the temperature sensor and the ADC requires level shifting for the input driver design.

Full scale input range of the temperature sensor is calculated by subtracting the output voltage of the temperature sensor at operating maximum temperature (125°C) from that at operating minimum temperature (-40°C) as below.

$$\begin{aligned} FS_{sensor} &= V_{sensor_{125^{\circ}\text{C}}} - V_{sensor_{-40^{\circ}\text{C}}} \\ &= 143.52mV \end{aligned} \tag{1.2}$$

Due to the different full scale values of the temperature sensor and ADC, the input driver should perform amplitude scaling to benefit full scale input range of ADC.

Another purpose of the input driver is the conversion of the single ended to differential signal. Temperature sensor generates single-ended output voltage while the ADC has differential inputs. Therefore, the circuit topology performing this conversion is needed to digitize the analog output of the temperature sensor properly.

Many ADCs, as the differential input SAR ADC used in this thesis, have switched capacitor inputs which produce charge spikes should be prevented [15]. Buffering provides electrically isolation between a sensor signal and an input of ADC and this isolation blocks the incoming and outgoing charge spikes. Figure 1.2 shows that a single-ended amplifier driver for differential input ADC. The amplifier is used as a unity gain buffer by connecting the output terminal to the negative terminal of the amplifier. In addition to the buffering function of the driver, R_S and C_f perform filtering to reduce the total output noise of the driver. Bandwidth requirement should be taken into consideration to determine the resistor and capacitor values as well. R_S also decouples the driver from ADC input capacitance [2].

While the problem of the switching transient current can be solved with this configuration, it shows poor AC performance compared to a fully differential driver. In addition, input-output common mode voltage values cannot be set with this architecture. Hence, this circuit topology is not suitable for our case.

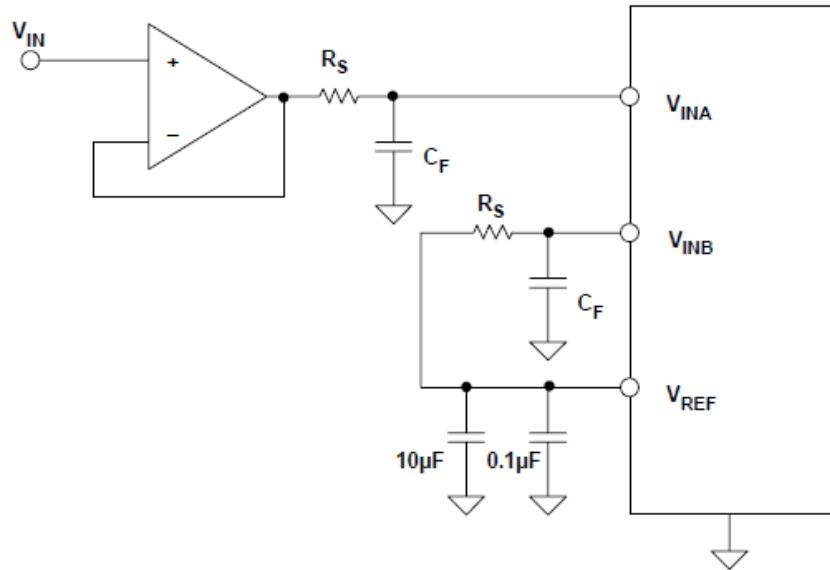


Figure 1.2. A Single Ended Switched Capacitor ADC Input Driver [2].

The input driver must perform level shifting if input common mode level of a signal source is different from that of ADC, at the same time the output of the input driver. Level shifting means moving input common level of a signal source to desired output common mode level. Level shifting implementation is shown in Figure 1.3. ADR431 as shown in Figure 1.3, is a voltage reference with low supply current and low noise by using reference generation technique known as XFET [16]. Unlike the input driver in Figure 1.2, ADR431 is used to shift the input common mode to the average value of the ADC input range from 1.25 V to 2.5 V numerically. Another function of the voltage reference circuit is to provide constant voltage for the other differential ADC input (V_{INB}). Although this circuit structure enables level shifting, buffering and filtering, it is still not sufficient to meet the requirements mentioned at the beginning of the section.

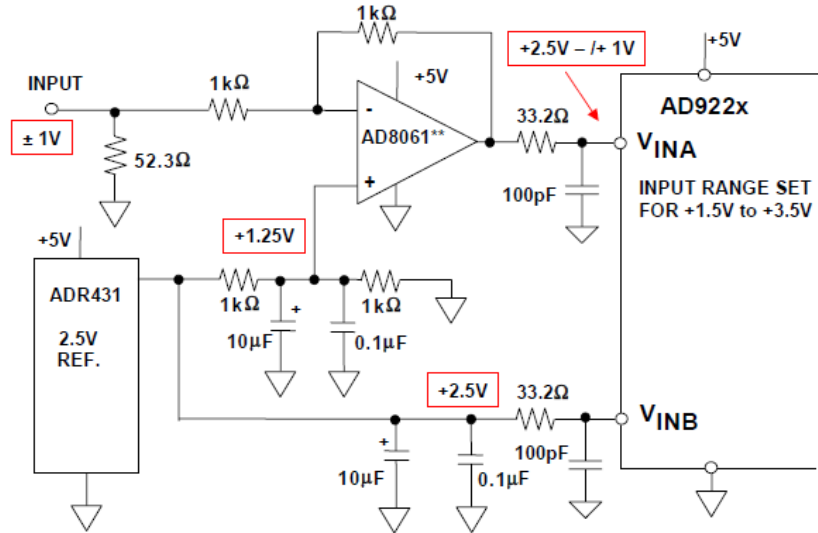
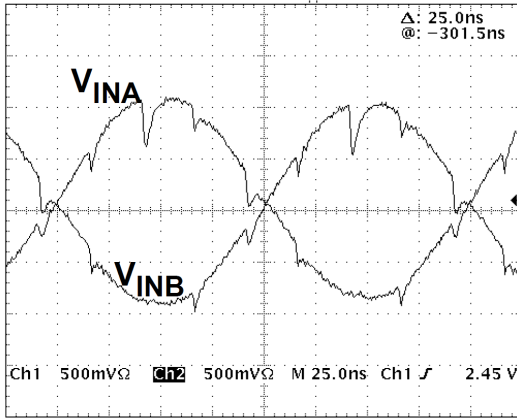


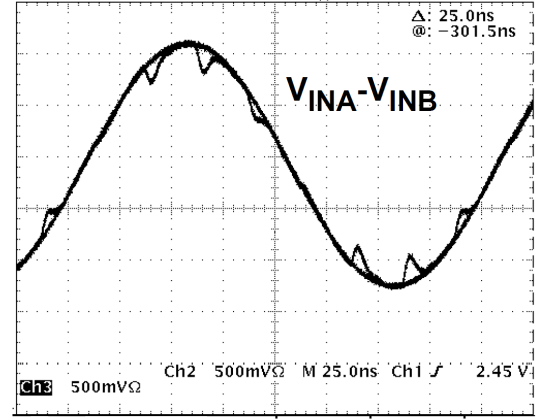
Figure 1.3. Level Shifter Single Ended Amplifier Driver [2].

Two circuit topologies discussed are the single-ended drivers. Instead of the single ended drivers, differential drivers generate a balanced differential output which means nominally equal in amplitude and 180° out of phase with respect to a common-mode level [17]. In the case of the single-ended driver as shown in Figure 1.2 and 1.3, V_{INB}

has a constant voltage value produced by the voltage reference, V_{INA} varies with input signal source. Compared to the single-ended drivers, differential input drivers provide better common-mode rejection and eliminating even order harmonic distortion. Figure 1.4, compares the effects of switching glitches on single-ended and differential drivers. Differential charge spikes are symmetrical about mid-scale. This shows that there is a distinct linear component which results in reduction in the common-mode transients and better total harmonic distortion performance [2].



(a) Single Ended.



(b) Differential Drivers.

Figure 1.4. Single Ended vs Differential Drivers Output Characteristics as Driving CMOS Switched Capacitor ADC [2].

Amplifier based differential drivers for DC coupled drive circuitry can be separated into two categories: dual amplifier drivers and fully integrated differential drivers. A typical implementation of dual amplifier drivers are shown in Figure 1.5. Even if this implementation has excellent matching performance, SNR degradation can be inevitable due to noise gain. Another disadvantage is that there is no internal feedback to stabilize the common-mode output voltage. With resistor mismatches, this causes a large differential-mode output offset voltage, hence unbalanced output voltage which degrades the overall performance of ADCs. On the other hand, fully integrated differential amplifiers offer common-mode feedback (CMFB) circuit to balance the output signal. Unlike the single ended amplifiers, common-mode output voltage can be set by extra input pin (V_{OCM}) as shown in Figure 1.6. Ratio of R_F to R_1 controls the

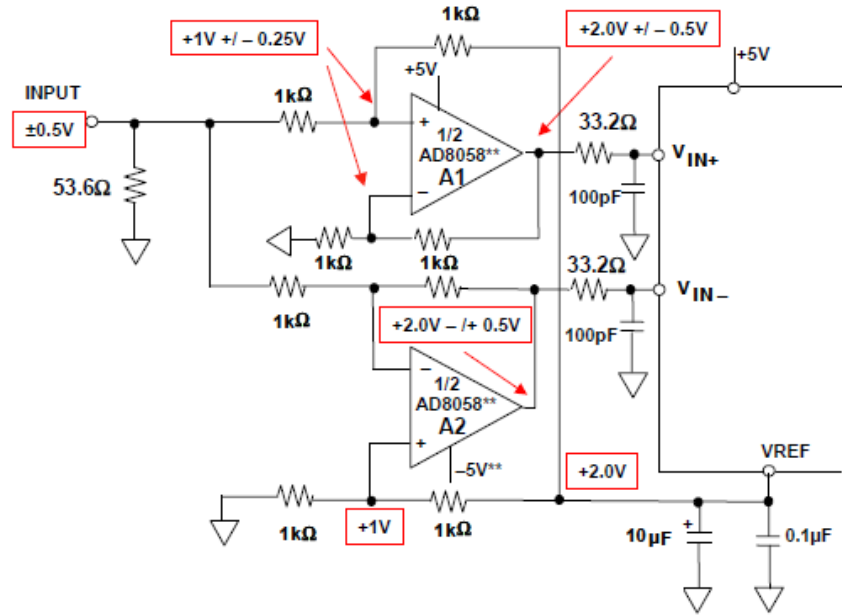


Figure 1.5. A Dual Amplifier Driver [2].

differential output voltage by adjusting the voltage gain. Since the differential and common-mode output voltage are regulated by different feedback mechanisms, mismatches of resistors in feedback system does not have an effect on common-mode output voltage. This is also valid for the CMFB circuit that does not affect the differential output voltage. Besides having two different feedback system to obtain perfectly balanced output signal, a fully integrated differential amplifier has distinct advantages such as high immunity to noise, high output voltage swing, compatible with low voltage systems, reduced even order harmonics [18].

Figure 1.6 illustrates that DC coupled fully integrated differential amplifier driver performing single-ended to differential signal conversion and level shifting. Single-ended input signal (V_{IN}) can be turned into a differential signal centered on the output common mode voltage by equating V_{REF} to V_{INCM} which is the average of the minimum and maximum value of V_{IN} in a measurement range. In this configuration, the values of the input resistors (R_1) must be greater than source resistance of the input signal. R_T and R_2 are utilized for impedance matching and differential balance, respectively [3].

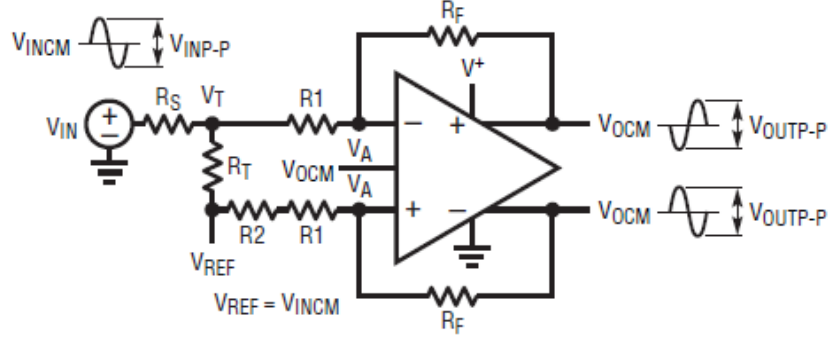


Figure 1.6. A Fully Integrated Differential Amplifier Driver [3].

Among all circuit architecture discussed so far, the fully integrated differential amplifier is the most suitable topology for our purpose. However, the circuit in Figure 1.6 must be modified to drive the differential input ADC properly along temperature range specified with ultra-low power design. In the proposed design, V_{REF} ($=V_{INCM}$) signal is as shown in Figure 1.8, generated by 1.2 V supply ultra-low power bandgap reference circuit in 65 nm CMOS technology designed in [19]. V_{IN} is replaced with 0.7 V supply ultra-low power temperature sensor designed in [19]. The temperature sensor and bandgap reference circuit consumes a few μA which is not sufficient to drive the resistive and capacitive load for proper operation of the input driver and the ADC. Therefore, two single ended op-amps are placed to buffer the output signal of the temperature sensor and V_{INCM} signal produced by the bandgap reference circuit. Both op-amps are configured as non-inverting unity gain buffer. Top level of the proposed input driver as shown in Figure 1.8.

Reference driver is designed to buffer the signal generated by the bandgap reference which provides a reference voltage for the ADC. The need of buffering comes from the insufficient drive capability of the ultra-low power reference circuit which has higher output impedance that increase significantly with frequency [20]. As shown in Figure 1.7, “b” and “c” input pins are the control bits to regulate the current consumption and value of the compensation capacitor, respectively. Control of the Compensation capacitor is the important issue due to keeping the phase margin constant with varying current controlled by “b” pin. Details about designing input and reference driver will

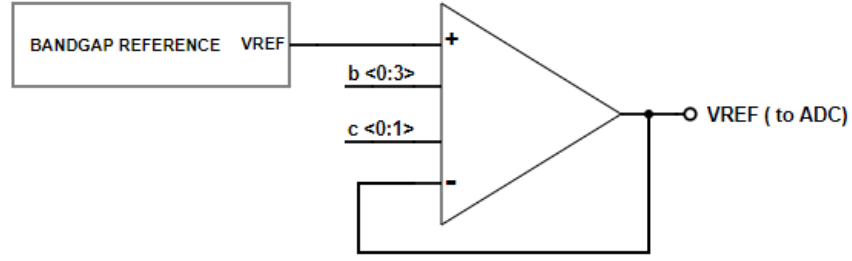


Figure 1.7. Top Level of the Proposed Reference Driver.

be explained in the next chapter.

1.3. Thesis Organization

Chapter one provides a background and an approach on top level architecture of input and reference driver. In chapter two, the metrics affect the performance of the input driver, is explained in the section of system design theory. Subsequent sections describe sub-blocks of the input driver which include a rail-to-rail input-output fully differential amplifier and voltage buffers for input common mode and temperature sensor. The design of the reference driver is explained in chapter three. Post-layout simulation results and performance of input and reference driver are discussed in chapter four.

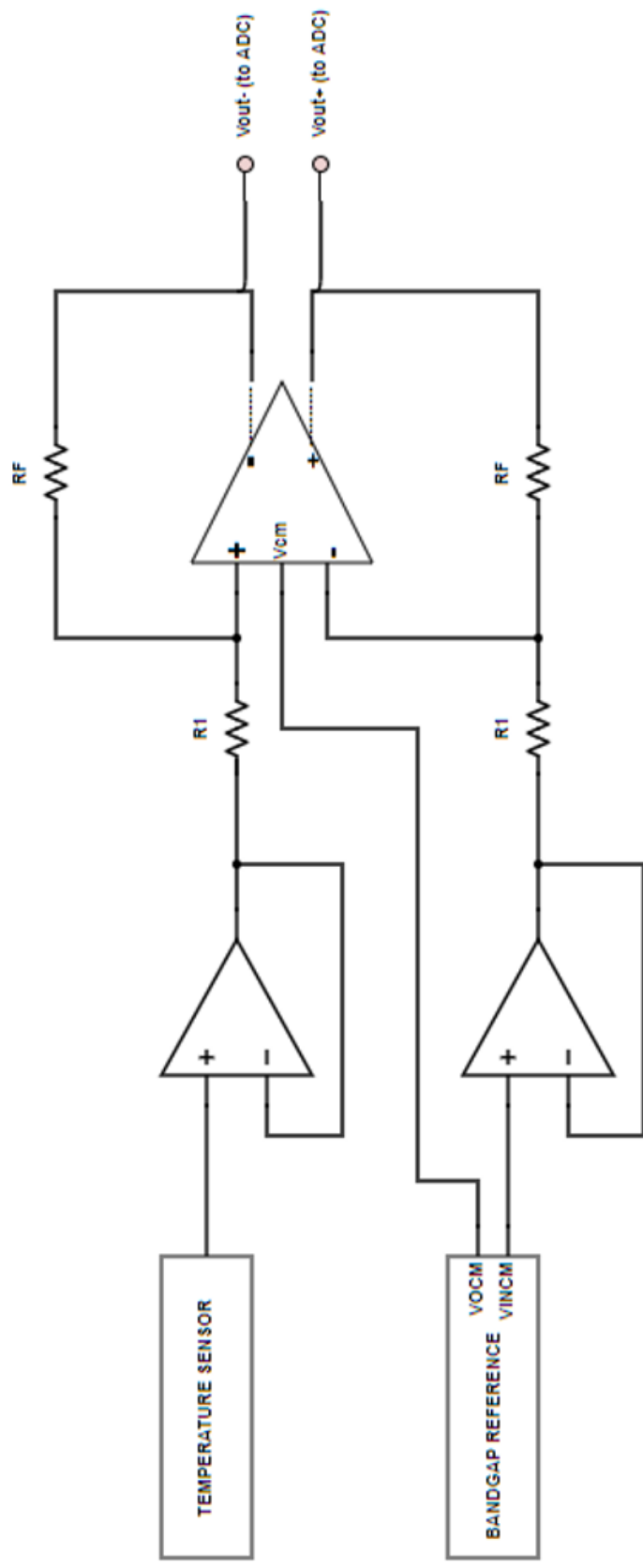


Figure 1.8. Top Level of the Proposed Input Driver (Excluding Filters).

2. INPUT DRIVER CIRCUIT DESIGN

2.1. System Design Theory

Total output noise and THD primarily determines the performance of the input driver design. These two metrics directly affects the ADC resolution. Since there is a trade-off between noise and power consumption, noise calculation is a critical point especially for ultra-low power applications. In addition, accuracy and settling time are the other specifications have an impact on the performance of the ADC. After determining the right input driver topology, component values must be selected according to the metrics mentioned above.

Noise is an inevitable phenomenon in all electronic circuits and occurs due to random motion of electrons in a resistive material (thermal noise), random recombination of carriers in a semiconductor (flicker noise) and when holes and electrons diffuse through a potential barrier (shot noise) [21]. Noise is a random process, therefore it cannot be determined instantaneously. Instead of it, average power of noise can be calculated as below [22].

$$P_n = \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T n^2(t) dt \quad (2.1)$$

Where “n” represents noise quantity. In noise analysis, working in frequency domain is much more useful to have the deeper insight. Power spectral density (PSD) of the noise gives us information how each frequency contributes the average power of it. Like in time domain, integration of all frequencies from zero to infinity equals the average power of the noise as shown in equation (2.2).

$$\int_0^\infty S_n(f) df = \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T n^2(t) dt \quad (2.2)$$

PSD of a resistor of value R producing a noise voltage is represented in equation (2.3)

$$\overline{V_n^2} = 4kTR \quad (2.3)$$

where V_n^2 refers the average power of V_n in 1 Hz, k is the Boltzmann constant and T is the temperature in Kelvin [23]. Equation (2.3) shows that the thermal noise is positively proportional to temperature and independent from the frequency. Independent of the frequency is valid for up to 1 THz [24]. The input driver circuit is designed to drive 100 kHz temperature sensor signal maximally. Low-pass RC filters are used to filter out the frequency components beyond 100 kHz. Therefore, thermal noise contribution of the resistors used in the proposed design can be considered as a constant value over the frequency range. According to the equation of the thermal noise in equation (2.3), R_1 and R_F values in Figure 1.8, should be selected as low as possible to reduce the contribution to total output noise. However, there are tradeoffs to determine the minimum value of the resistors. In our system, the input common-mode voltage of the input driver is calculated as 558.96 mV in equation (1.1). On the other hand, the output common-mode voltage of the input driver must be equal to input common-mode of the SAR ADC which is 350 mV. This common-mode voltage difference results in DC feedback current that is represented by equation (2.4).

$$I_n = \frac{V_{INCM} - V_{OUTCM}}{R_F} \quad (2.4)$$

As shown in equation (2.4), lowering R_F causes the larger feedback current to maintain input-output common mode voltages. Since the output stage of the fully differential amplifier have to sink much more amount of current from feedback network, this situation leads to a loading problem for the fully differential amplifier. Only solution is to strengthen the drive capability of the fully differential amplifier by increasing the current consumption. Therefore, excessive lowering the feedback resistance results in significantly high power consumption which is not desirable. Second tradeoff is that

usage of lower resistance value degrades THD performance due to increased loading of the amplifiers [25]. External loading of an amplifier must be greater than output resistance of an amplifier to avoid the degradation of THD.

Estimating total output noise of the input driver helps the designer to select appropriate parameter values of the components and circuit tuning. A driver noise analysis provides expected SNR performance of a driver, hence calculation of the output noise plays a key role to design a high performance driver. All components producing noise are uncorrelated and all of them is illustrated in the simplified schematic of a fully integrated differential driver as shown in Figure 2.1.

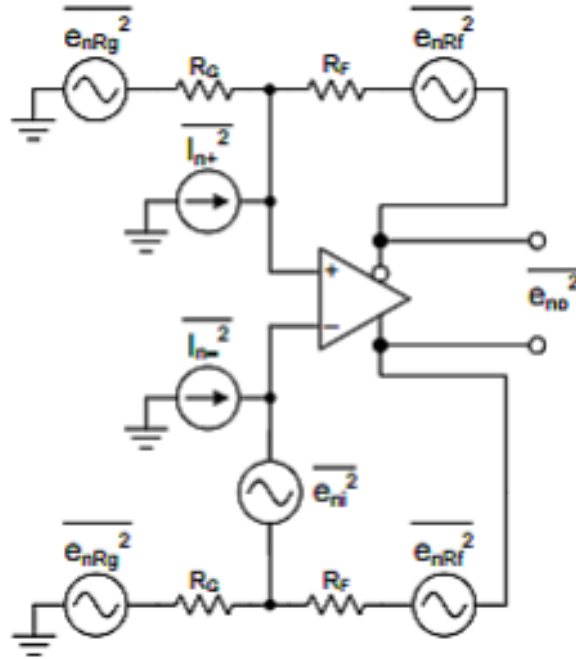


Figure 2.1. Noise Model of the Input Driver [4].

Each noise source contribution must be computed separately and added to the root-sum-squared values. Noise contribution of the resistor of R_G represented as R_1 in

the proposed input driver design in Figure 1.8 is computed as

$$\overline{e_{nRg}^2} = 4ktR_G\left(\frac{R_F}{R_G}\right)^2 \quad (2.5)$$

Equation (2.5) shows that average noise power of R_G multiplied by the square of the external gain set by the R_F/R_G . Noise contribution of the feedback resistor R_F is directly equal to the thermal noise of it [26].

$$\overline{e_{nRf}^2} = 4ktR_F \quad (2.6)$$

Input voltage noise spectral density and total current noise of each input contribution is calculated as following.

$$\overline{e_{ni}^2} = e_i^2\left(1 + \frac{R_F}{R_G}\right)^2 \quad (2.7)$$

Where $\overline{e_i^2}$ denotes the average power of the differential input voltage noise. In our setup, this noise contribution comes from the temperature sensor, bandgap reference circuit and voltage buffers. Differential input noise is multiplied by the square of the $(1+R_F/R_G)$ which is called “noise gain”.

$$\overline{e_c^2} = (i_{n+}R_F)^2 + (i_{n-}R_F)^2 \quad (2.8)$$

Where i_{n+} and i_{n-} denotes the input current noise of corresponding terminal. Since these two input currents are uncorrelated, input current noise must be calculated separately unlike the differential input voltage noise [26].

After all noise power contribution is found, total output noise can be computed by taking the square root of the sum of power of the noise sources.

$$e_{no} = \sqrt{2(e_{nRg}^2) + 2(e_{nRf}^2) + e_i^2(1 + \frac{R_F}{R_G})^2 + (i_{n+}R_F)^2 + (i_{n-}R_F)^2} \quad (2.9)$$

Where e_{no} is defined as differential output noise voltage. V_{OCM} input pin in Figure 1.8 produces the noise voltage as well. With proper bypassing, the effect of that pin on the noise can be minimized [4]. This contribution is neglected in equation (2.9).

Our target is to design an input driver whose total output noise is less than $\frac{1}{2}$ LSB value of the ADC is driven. In the thesis, 8 bit SAR ADC with 1 V full scale range is used. Maximum total output noise over the temperature range for proper operation of the SAR ADC is computed by

$$V_{maxnoise} = \frac{FS_{ADC}}{2(2^n)} \quad (2.10)$$

where FS_{ADC} represents full scale of an ADC, n is number of bit. According to the equation (2.10), total output noise can take the maximum value is 1.953 mV.

Internal noise contribution of the amplifiers should be taken into consideration. Transistor level noise analysis is required to minimize an amplifier noise contribution. The average power of the current noise at drain of MOSFET is given by [27]

$$\overline{i_o^2} = [4kT\gamma g_m + \frac{k_f g_m^2}{c_{ox} L W f}] * \Delta f \quad (2.11)$$

Where γ denote thermal noise coefficient, g_m is MOSFET transconductance at the operating point, C_{ox} is the oxide capacitance, L and W represent length and width of MOSFET. First term in equation (2.11) is corresponding to thermal noise, second one is flicker noise contribution. As shown in equation (2.11), increasing length of a transistor significantly reduces the flicker noise. This leads to lower current and transconductance. Keeping W/L ratio as L increases can be a compensation method

to maintain current and transconductance. However, excessive large width and length brings internal capacitance which results in phase margin degradation.

Total output noise voltage of folded cascode OTA with a single pole is given by

$$V_{noise,FC} = \sqrt{\frac{8kT}{g_{m1}} f_{BW}} * \sqrt{1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m3}}{g_{m1}}} \quad (2.12)$$

where f_{BW} is bandwidth of folded cascode OTA, g_{m1} is the transconductance of input pair, g_{m2} and g_{m3} are the transconductance of the cascode transistors. First term represents the differential input pair noise contribution and second term is associated with cascode transistors. Input pair W/L ratio can be increased to reduce the noise associated with input pair. Phase margin degradation can be a problematic issue while increasing (W/L) ratio due to large parasitic capacitance. Keeping the input pair in saturation region is another factor as increasing W/L ratio. Unlike the input pair case, transconductance of the cascode transistors is positively proportional to total output noise voltage. Minimized cascode transistor transconductance enables reduction of the total output noise. To keep the current constant flowing to cascode transistors, gate to source voltage of the cascode transistors can be increased. This leads to reduced output voltage swing and it can be compensated by increasing length of the transistors which provides lower flicker noise [28].

Total harmonic distortion is defined as the ratio of the root square of sum of the all harmonic powers to the amplitude of fundamental frequency [29]. THD in decibel is given by

$$THD = 20\log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots}}{V_1}\right) \quad (2.13)$$

where V_n^2 denotes the average power of the n^{th} harmonic and V_1 is the RMS amplitude of fundamental frequency. A sinusoidal signal is applied to the input of the circuit to test the THD performance of the system. FFT of the output signal is taken and THD of the system is calculated. THD performance of the input driver depends on

many parameters such as input and output amplitude, input frequency, load conditions and feedback configurations. In addition, choosing right operating point, the design of the output stage for the amplifiers which can handle the power to avoid clipping and perfect balanced output improve the THD of the input driver.

Heavy capacitive load degrades THD performance and phase margin. As shown in Figure 1.2, isolation resistors can be used to improve stability and form low pass filter to reduce total output noise. However, choosing the resistor value is another design challenge because the output signal is more distorted as the resistance becomes larger [30].

Accuracy is the another factor to affect the performance of the input driver. It measures how accurately output signal of the sensor reflects to output of the input driver at DC. Closed loop gain of the amplifiers used in the input driver is a major parameter to affect the accuracy. How it has an impact on the accuracy is shown by

$$\frac{V_{OUT,dm}}{V_{IN,dm}} = \left[\frac{R_F}{R_G} \right] \left[\frac{1}{1 + \frac{1}{A(s)(\beta)}} \right] \quad (2.14)$$

where $A(s)$ is frequency dependent open loop gain of an amplifier, β is the feedback factor equals to $R_G/(R_F + R_G)$, $V_{OUT,dm}$ and $V_{IN,dm}$ are differential output and input voltages, respectively. If $A(s)$ goes to infinity, closed loop gain reduces to R_F/R_G which is the ideal slope of the input driver characteristic [17]. The closed loop gain should be larger than the RMS signal-to-noise ratio for an ideal N-bit converter defined by the equation (2.15) to avoid any conversion error. According to the equation (2.15), the closed loop gain should be larger than 49.92 dB for 8-bit ADC driver.

$$SNR = 6.02N + 1.76dB \quad (2.15)$$

Settling time of the input driver is defined as the time passed from applying the ideal step input to response of the closed-loop amplifier settle within a specified error band which is considered acceptable under one fourth of LSB [31]. In addition, the

driver circuit must settle faster than acquisition time of the SAR ADC. If it exceeds the acquisition time, it means that the input driver cannot response the instantaneous input change, hence ADC evaluates the incorrect input.

Main purpose of the RC filters in the input driver design is noise and distortion attenuation. RC filter is placed between driver amplifier and SAR ADC blocks the charge injection from the switched capacitor circuit of the SAR ADC. As shown in Figure 2.2, R_{filt3} and C_{filt3} are used with this aim. Cut-off frequency $R_{filt1} - C_{filt1}$ and $R_{filt3} - C_{filt3}$ low pass filters are designed as 100 kHz in order to drive the input signal from zero frequency to 100 kHz. $R_{filt2} - C_{filt2}$ low pass filter is used to suppress excessive noise generated by bandgap reference circuit. Since this filter has no an effect on the driver bandwidth, there is no requirement about designing cut-off frequency of this filter as 100 kHz. However, there is a limit to decrease the cut-off frequency. R_{filt2} value must not be increased excessively because thermal noise becomes dominant and cannot perform noise attenuation. On the other hand, larger C_{filt2} from its optimum value cause the leakage current which leads to voltage drop between output of the bandgap reference and output of the filter, and larger deviated output voltage over temperature range, hence leakage current results in unbalanced output signal and affects the performance of the input driver adversely. The denser capacitor types can be used to solve the leakage problem at the expense of usage of larger area.

2.2. Fully Differential Rail-to-Rail Input-Output Amplifier

2.2.1. Literature Review

Low voltage single supply systems as the proposed input driver, generally suffer from reduced signal range. In contrast to high voltage systems, they cannot use wide voltage range for the proper operation. This limitation results in SNR and THD degradation which are very critical problems for the performance of the input driver [32]. A Rail-to-rail input-output amplifier offers the solution to overcome dynamic range issue. It provides constant specifications such as gain, gain-bandwidth product, phase margin and power consumption against input common mode variations [5].

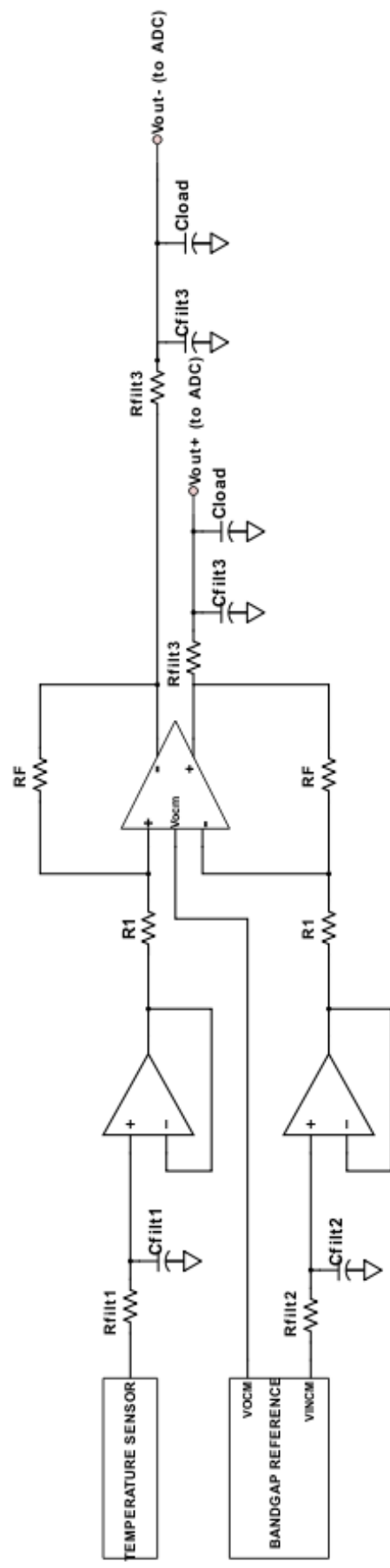


Figure 2.2. Top Level of the Proposed Input Driver.

The proposed input driver design is an interface circuit between temperature sensor and SAR ADC. Therefore, input signal of the driver varies with temperature. The rail-to-rail input-output amplifier design must be robust against temperature variations as well for our purpose. Constant operating point parameters are generally related to the input transconductance of the amplifier, hence keeping input transconductance constant over input common-mode range is a critical issue to obtain rail-to-rail input voltage. If input transconductance changes with the input common-mode voltage, THD performance of the amplifier can be degraded due to varied amplifier gain. This affects directly linearity of the system which is undesirable for the input driver design.

Rail-to-rail output stage is needed to obtain the output signal swings from ground to supply rail. In the proposed design, differential input SAR ADC accepts maximum 600 mV and minimum 100 mV voltage for each input pin. To avoid clipping and improve linearity, rail-to-rail output stage is required in the proposed amplifier design. Output stage also affects specifications such as open loop gain, slew rate and capability of sourcing and sinking currents which is directly related to the distortion and noise performance of the input driver.

Conventional technique to obtain rail-to-rail input signal is the complementary input stage which consists of n-type and p-type differential pair connected in parallel. With this input stage architecture, if common-mode input voltage varies from negative rail to threshold voltage of the NMOS, PMOS operates in saturation region while NMOS is cut-off. If common-mode input voltage varies from $V_{DD} - |V_{th,p}|$ to the positive rail (V_{DD}), NMOS operates in saturation region while PMOS is cut-off. There is a transition region where two types of the input pairs are active around middle of the input common mode range. As shown in Figure 2.3, total input transconductance equals the sum of the n-type and p-type transconductance values. This large transconductance variation results in varied operating point parameters and additional circuits are needed to maintain the input transconductance constant. In the literature, various techniques are implemented to control transconductance of the input stage, will be analyzed and compared how well these techniques meet our requirements.

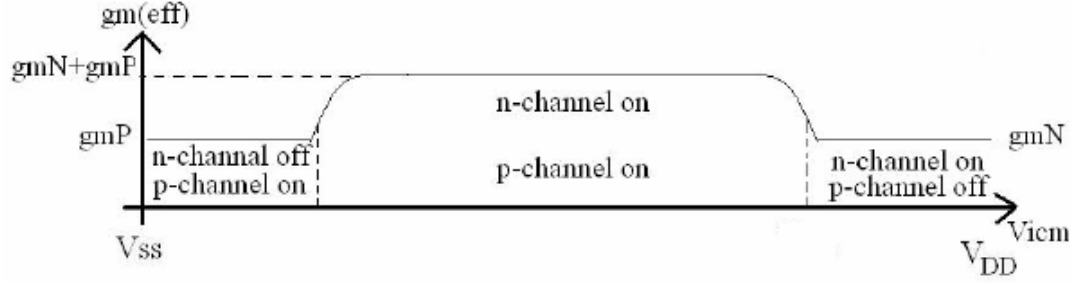


Figure 2.3. Complementary Input Stage Gm Characteristic [5].

2.2.1.1. Complementary Input Stage Operating in Weak Inversion Region. Working in weak inversion region is a suitable method to achieve ultra-low supply and power operation. Drain current and transconductance of MOSFET operating in weak inversion region is given by

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_{GS}}{nKT/q}} \quad (2.16)$$

$$g_m = \frac{W}{L} \frac{I_{D0}}{nKT/q} e^{\frac{V_{GS}}{nKT/q}} = \frac{I_D}{nKT/q} = kI_D \quad (2.17)$$

Total transconductance of the complementary input stage is calculated by

$$g_{m,tot} = g_{mN} + g_{mP} = k(I_N + I_P) \quad (2.18)$$

Equation (2.17) shows that transconductance of a transistor working in weak inversion region is proportional to the drain current of it. Therefore, total transconductance is the proportional to sum of the drain currents of the differential pairs. There is a need of the circuit to keep the total input pair current constant. Current switches and depletion mode transistors to buffer a bulk-driven complementary pair transistors

are implemented for this purpose. C.-W. Lu and C.-M. Hsiao [33] develops a technique by keeping the sum of currents in the complementary pairs constant to keep the input transconductance constant, unlike the current switch method by changing the tail current of complementary pairs. Independency of controlling tail current is achieved by negative feedback loop. Although this technique is superior to previous ones, it is not still sufficient to meet our requirements. Even if working in weak inversion region provides low supply and power operation, the current equation is strongly dependent on the temperature hence, it is not feasible design for temperature insensitive systems. Weak inversion operation significantly degrades the noise performance of the amplifier [34] and strict matching is required to avoid mismatch effects.

2.2.1.2. Complementary Input Stage Operating in Strong Inversion Region. Based on the square law model, drain current and transconductance of the MOSFET operating in strong inversion by neglecting channel length modulation is computed as

$$I_D = \frac{K}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (2.19)$$

$$g_m = \sqrt{2K \left(\frac{W}{L}\right) I_D} \quad (2.20)$$

Tail current of the input stage (I_{TAIL}) equals the sum of the currents of each input.

$$g_m = \sqrt{K \left(\frac{W}{L}\right) I_{TAIL}} \quad (2.21)$$

Total transconductance of the complementary input stage is calculated with assumption $K_N(W/L)_N = K_P(W/L)_P = K$ as following.

$$\begin{aligned} g_{m,tot} = g_{mN} + g_{mP} &= \sqrt{K_N\left(\frac{W}{L}\right)_N I_N} + \sqrt{K_P\left(\frac{W}{L}\right)_P I_P} \\ &= \sqrt{K}(\sqrt{I_N} + \sqrt{I_P}) \end{aligned} \quad (2.22)$$

As shown in equation (2.22), keeping the sum of the square root of the currents of the input transistors constant is sufficient to obtain constant input transconductance over rail-to-rail input common-mode voltage.

Square root biasing circuit is proposed in [6] based on complementary input stage operating in strong inversion region. The main idea of the square root current control is to keep the sum of gate to source voltages of the complementary input pairs constant. Translinear loop $M_{10} - M_{13}$ provides the constant g_m control as shown in Figure 2.4 by following equation.

$$V_{|GS|,M10} + V_{|GS|,M11} = V_{|GS|,M12} + V_{|GS|,M13} \quad (2.23)$$

which implies that

$$\sqrt{I_{D,M10}} + \sqrt{I_{D,M11}} = \sqrt{I_{D,M12}} + \sqrt{I_{D,M13}} \quad (2.24)$$

To achieve constant the sum of the square root of the tail currents of the complementary input pair, I_{REF} and tail current of the NMOS differential pair are measured and fed into M_{12} whose drain voltage changes against variation of the tail current and translinear loop circuitry forces the amount of current depends on the formula in equations (2.23) and (2.24) [6]. The circuit provides constant input g_m by square root

technologies.

Maximum-minimum current selection circuit [35] and [7] is proposed as a method independent from technology, transistor types and operating region to obtain constant input gm over rail-to-rail input range. As shown in Figure 2.5, traditional biasing technique is used as an indication of the process independent. Assuming that positive input terminal voltage is the greater than the negative one,

$$I_{n1} = \frac{I_N}{2} + g_{m,n} \frac{v_{id}}{2} \quad (2.26)$$

$$I_{n2} = \frac{I_N}{2} - g_{m,n} \frac{v_{id}}{2} \quad (2.27)$$

$$I_{p1} = \frac{I_P}{2} + g_{m,p} \frac{v_{id}}{2} \quad (2.28)$$

$$I_{p2} = \frac{I_P}{2} - g_{m,p} \frac{v_{id}}{2} \quad (2.29)$$

where I_{n1} , I_{n2} , I_{p1} and I_{p2} represent the drain current of corresponding to input transistors, I_N and I_P are the DC current of corresponding input pair, v_{id} is the differential input voltage, $g_{m,n}$ and $g_{m,p}$ are the transconductance of corresponding input pair. If common mode input voltage is close to negative rail, NMOS input pair cannot operate in saturation region and the tail current of the NMOS pair is smaller than I_B represented as a bias current in Figure 2.5. Therefore I_P becomes greater than I_N which leads to $g_{m,p}$ is larger than $g_{m,n}$. In that case, the maximum selection circuit selects the $g_{m,p}$ and conducts to the gain stage as shown in Figure 2.5. On the other hand, if common mode input voltage is close to supply voltage, PMOS input pair cannot operate in saturation region and the tail current of the PMOS pair is smaller than I_B which means that $g_{m,n}$ becomes larger than $g_{m,p}$. The maximum selection circuit selects the current, at the same time transconductance, of the NMOS pair and conducts to the

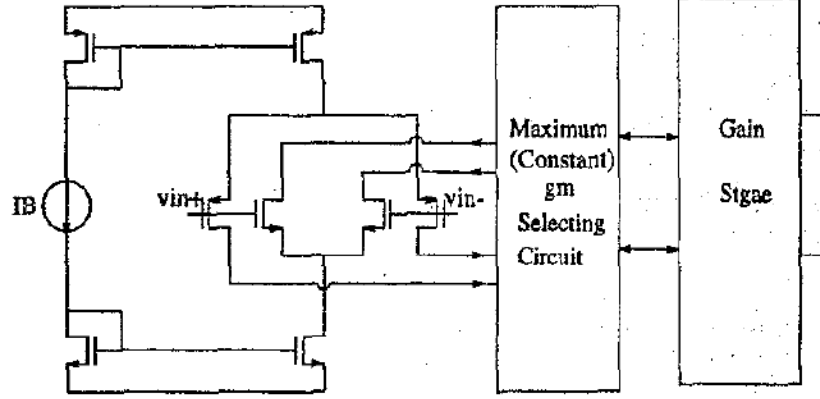


Figure 2.5. Circuit Diagram of the Maximum Current Selection Circuit [7].

output stage. At the gain stage, the larger currents of the differential pair, hence the larger transconductance are obtained [7].

Figure 2.6 shows that maximum current selection circuit. This circuit compares the I_{in1} and I_{in2} and gives the maximum current to the output. If I_{in2} is larger than I_{in1} , M_1 and M_3 try to replicate I_{in1} . However, M_3 cannot operate in saturation region due to insufficient current to sink and it enters the linear region which leads to small drain to source voltage. M_2 and M_5 operates in cut-off region. By neglecting the subthreshold current, $I_{out} = I_{in1}$. If I_{in1} is larger than I_{in2} , M_3 and M_5 mirror the current of I_{in2} . The drain current of M_2 equals the $I_{in1} - I_{in2}$ and M_1 replicates it. I_{out} equals the sum of the drain currents of M_1 and M_5 which equals the I_{in2} .

Minimum current selection circuit must be preferred if the gain stage topology is the folded cascode. If the maximum current of the input pair is selected and conducted to folded cascode stage, minimum output current is obtained which is undesirable. Minimum current selection circuit is required to folded cascode topology. Figure 2.7 shows the outgoing type minimum current selection circuit which sources the current of I_{out} . In the case of I_{in1} is larger than I_{in2} , M_6 and M_7 mirrors the current of I_{in2} . Due to the incapability of M_2 sinking the I_{in2} , it operates in linear region and M_3 and M_4 are in cut-off region. I_{out} equals the drain current of M_7 which replicates the I_{in2} .

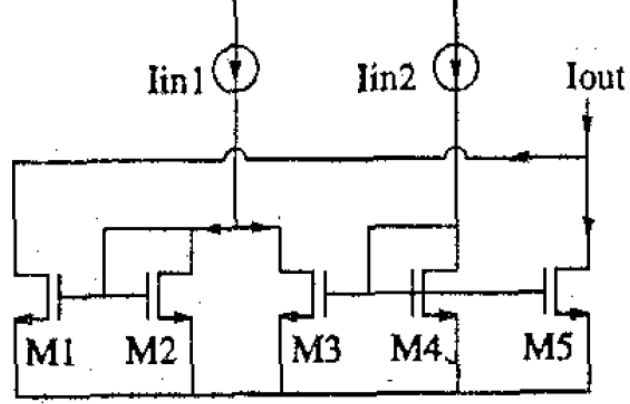


Figure 2.6. Maximum Current Selection Circuit [7].

If I_{in1} is larger than I_{in2} , M_6 and M_7 mirror the I_{in2} as the previous case while M_1 and M_2 mirror the I_{in1} . The drain current of the M_3 and M_4 equals the $I_{in2} - I_{in1}$. I_{out} is calculated by subtracting the drain current of the M_7 to that of the M_4 which equals to I_{in1} .

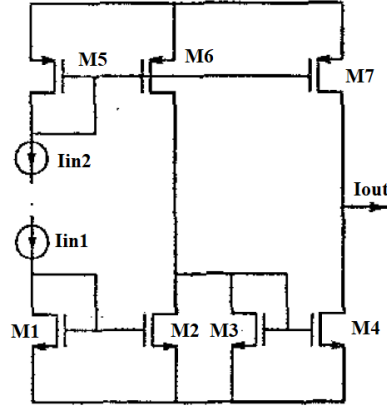


Figure 2.7. Minimum Current Selection Circuit [7].

Maximum-minimum current selection circuit has various advantages such as independency of the transistor type, model and operating region, low static power consumption and continuous operation mode against constant sum of the tail current technique, square root biasing circuit and current switches. However, higher power

consumption is inevitable as differential input voltage is presented. In addition, this technique may cause larger transconductance variation in transition region where both input pairs operate in saturation region, especially at the supply voltage which is less than $2V_{GS} + 2V_{DS,sat}$. Complementary input stage architecture is a problematic issue in terms of matching [33].

2.2.1.4. Complementary Input Stage with Overlapping Transition Region. All constant g_m techniques discussed so far try to change the tail currents of the complementary input stage or compare the input currents which need to additional circuits, area and power. Alternative method to keep the input transconductance constant is to overlap the transition region of PMOS and NMOS input pair.

Main problem of keeping the input transconductance constant arises at middle the input common mode voltage where doubles the transconductance value due to both active input pairs as shown in Figure 2.8. If one of transition regions of the complementary input pairs shifts until the transition regions overlap as shown in Figure 2.9, constant total input transconductance can be obtained over rail-to-rail input common mode range. Figure 2.9 shows that shifted n-pair transition region towards left to overlap with p-type transition region. M. Wang in [8] proposes overlapped transition region by using a pair of dc level shifters which are implemented as a source follower.

Main issue of the proposed complementary input stage with overlapped transition region is to find an optimal shift value which provides constant total input transconductance. If the level shifting exceeds the optimal value, total input transconductance drops below the nominal value. If the amount of the level shifting is not sufficient, it goes up the nominal value. The amount of the shifting can be adjusted by changing the bias current of the source follower [8]. An advantage of using the source follower is that it does not affect the slope of the transition region [5]. Therefore, it just shift the transconductance curve without distorting it as shown in Figure 2.9.

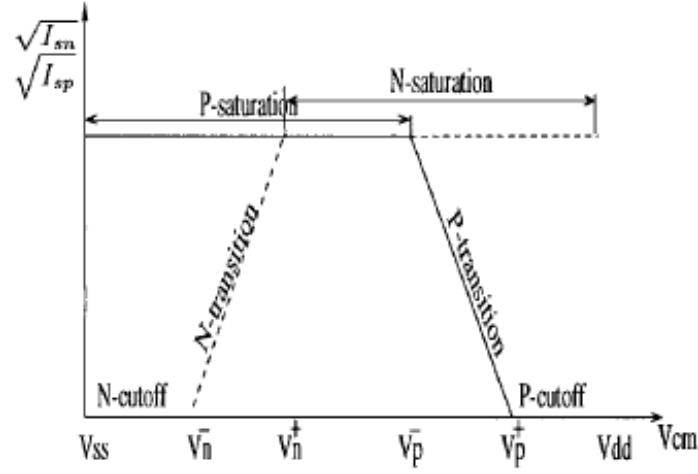


Figure 2.8. Transition Region of Complementary Input Pair [8].

Figure 2.10 shows that the implementation of the rail-to-rail op-amp with DC level shifters in complementary input stage. $M_{S1} - M_{S3}$ and $M_{S2} - M_{S4}$ transistor pairs function as a PMOS source follower. Optimal voltage shift is determined by biasing transistors which is M_{B1} and M_{B11} . The folded cascode topology and AB class output stage are used for high gain, input-output swing and rail-to-rail output voltage, respectively. Compared to other constant g_m architecture, this technique offers simple circuit with same performance. As discussed in [8], process variations and mismatches degrade the performance of the circuit and auto-bias circuit is required to minimize the g_m variation. String matching is needed to a consequence of complementary input stage as well.

2.2.1.5. Dual Channel Input Stage with Overlapping Transition Region. The techniques used in [9] and [10] overcome the issues encountered in [7]. Dual NMOS input pair [9] and PMOS input pair [10] are used to remedy the matching problem of the complementary input stage. J. M. Carrillo and J. F. Duque-Carrillo proposes the rail-to-rail input op-amp with constant small-signal and large-signal behavior over rail-to-rail input common mode voltage in [9] as a distinct advantage from the other techniques discussed. Dual channel input stage does not require compensation calculation for different mobility values with adjusting W/L ratios of input pair transistors. This

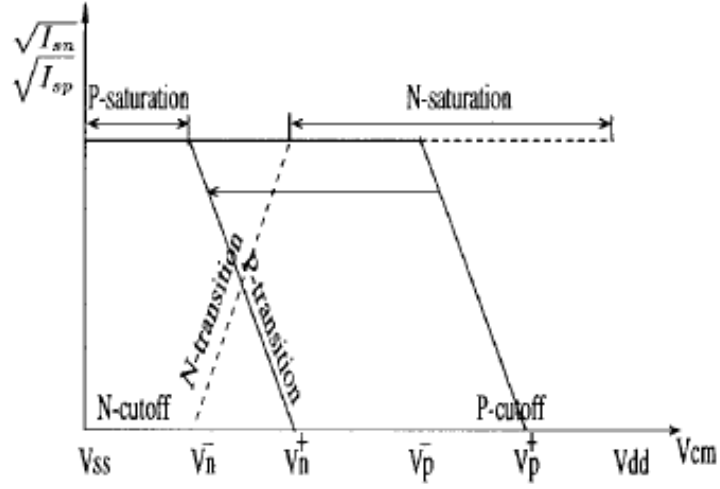


Figure 2.9. Shifted Transition Region of Complementary Input Pair [8].

is the important feature in terms of the temperature insensitivity due to the mobility factor is dependent on process and temperature. Figure 2.11 shows the implementation of rail-to-rail dual channel input stage with overlapping transition region. As in [8], DC level shifting is realized by the PMOS source follower. In contrast to the previous case, the output of the source follower is connected to gate of the shifted same type differential pair. The proposed circuit needs a mechanism to obtain constant small and large signal operating point because the PMOS level shifter enters the linear region as input common-mode voltage is close to the supply voltage and shifter NMOS differential pair lost the ability to amplify the signal differentially which leads to variations in small and large signal behavior. Feed-forward canceling stage is introduced to demonstrate the same variations of the circuit without cancelling stage and output current of the cancelling stage is subtracted from the output current of the dual channel input stage to remove the deviations in total input transconductance [9]. Figure 2.12 shows that the implementation of the feed-forward cancelling stage. M_{A1} and M_{A2} transistors sense the input common mode voltage to avoid the large variations when both dual channel input pairs operate in active region. Outputs of the feed-forward cancelling stage are connected to the drain nodes of the input pairs in reverse polarity to subtract the output current of the feed-forward cancelling stage from the drain current of the input pairs.

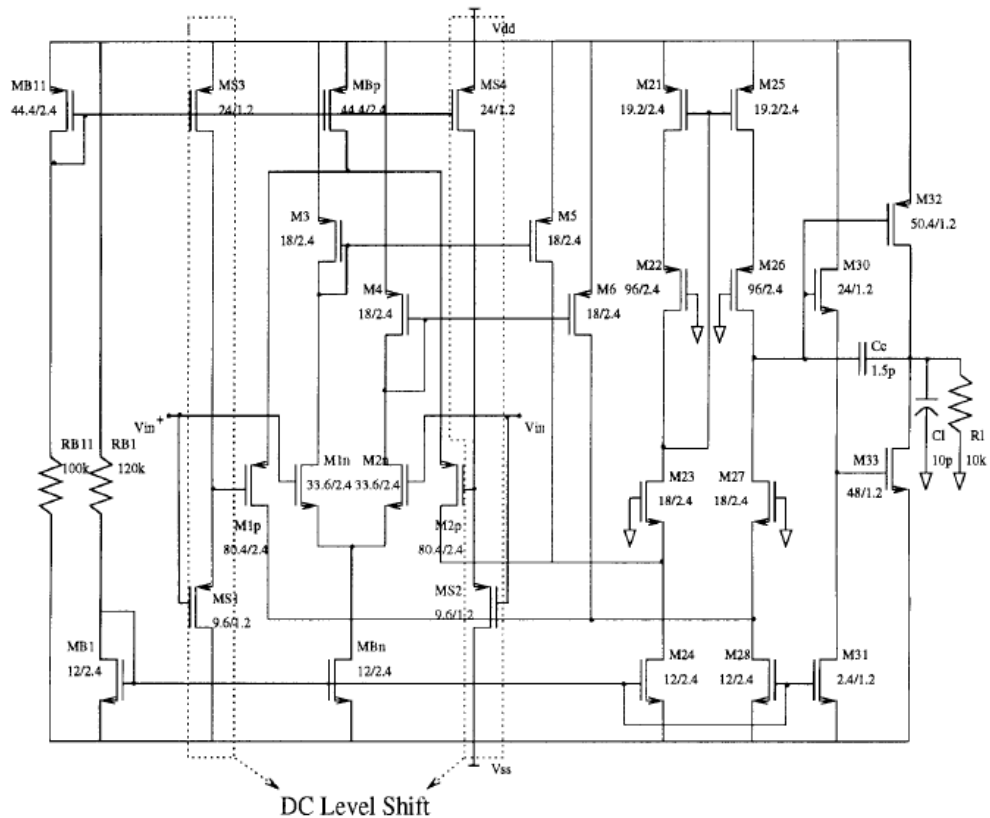


Figure 2.10. Rail to Rail Op-amp with DC Level Shifters in Complementary Input Stage [8].

Dual channel input pair implementation does not suffer from strict matching requirement. At the same time, temperature sensitivity is reduced by same channel input pairs which have same mobility values. Both input pairs can be easily matched by common centroid layout technique. Therefore, the circuit becomes more immune to process and temperature variations. However, feed-forward cancelling stage causes excessive current variation of the output stage of the amplifier which is undesirable for ultra-low power applications.

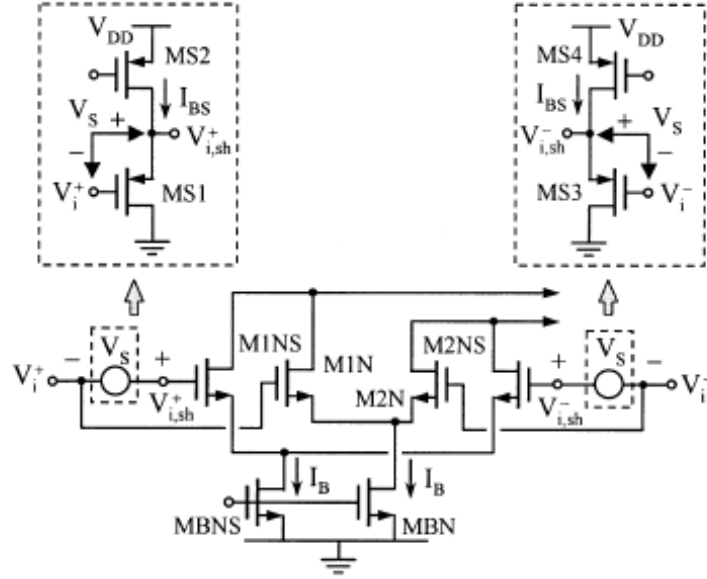


Figure 2.11. Rail-to-Rail Input Stage Based on Two NMOS Input Pairs [9].

W. Yan, R. Kolm and H. Zimmermann proposes the low voltage fully differential rail-to-rail input-output op-amp by a novel current-mode common-mode feedback technique in 65 nm CMOS technology [10]. Low voltage operation and using same CMOS technology are the compatible attributes for the fully differential rail-to-rail input-output amplifier will be used in the input driver design.

The input stage of the op-amp consists of the dual p-channel input pairs with complementary voltage level shifters and folded cascode circuit with gain boosting am-

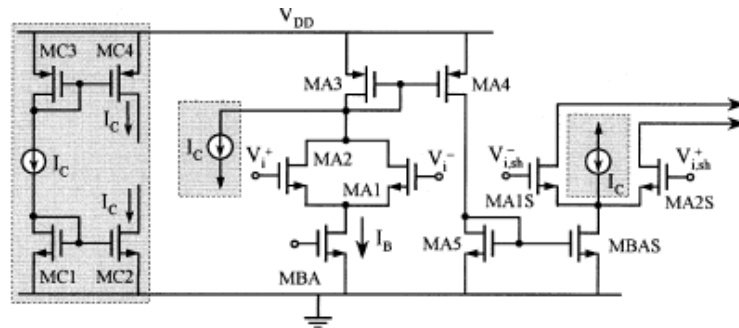


Figure 2.12. Feed-Forward Cancelling Stage [9].

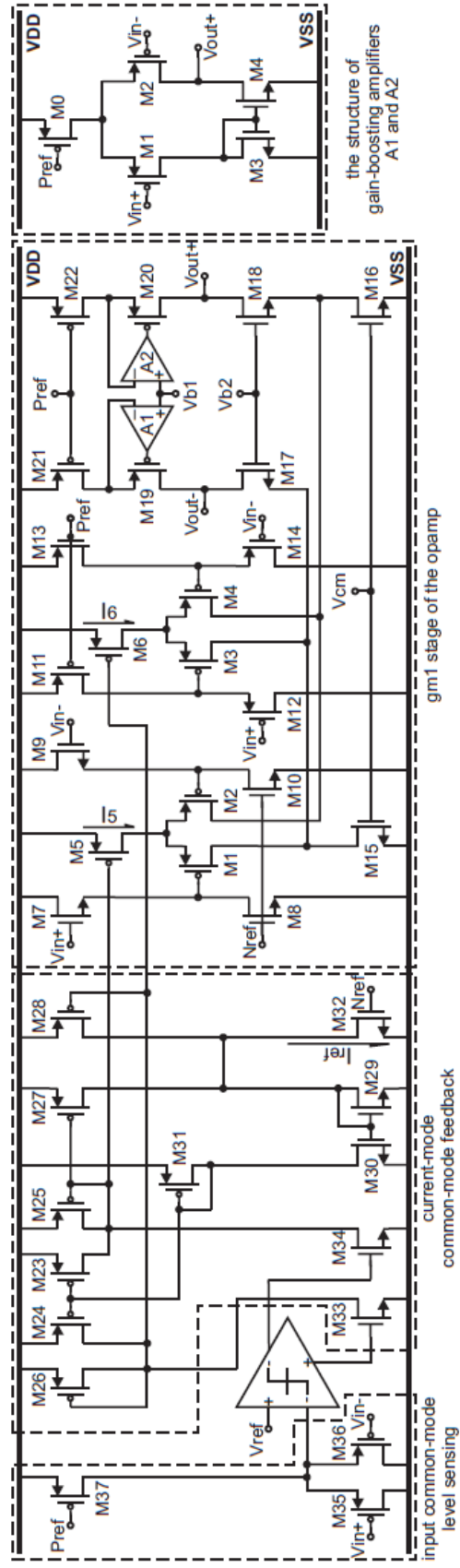


Figure 2.13. Fully Differential Rail to Rail Input-Output Op-amp with a Current-Mode Common-Mode Feedback Technique [10].

plifiers as shown in Figure 2.13. Folded cascode topology provides high DC gain and gain-boosting amplifiers can be needed to improve the gain due to lower output resistance of the transistors in 65 nm technology which causes lower DC gain compared to the older technologies. The output of the input common mode level sensing circuit is connected to the negative terminal of the fully differential comparator. The comparator block controls the tail currents of the dual channel input pairs by comparing sensed input common mode level with V_{ref} voltage. Performance of a conventional common mode sensing circuit is highly sensitive to the mismatch which causes large transconductance variation due to the overlapped transition regions cannot be achieved exactly. However, reference voltage of the comparator determines shifting amount of the transconductance curve. In that technique, mismatches does not have an impact on performance of the constant transconductance anymore. The constant signal characteristic is achieved by keeping total tail current of the input pair constant with current-mode common-mode feedback circuit. M_{27} and M_{28} replicate the tail currents. With this replication, these tail currents can be compared with reference current as the drain current of M_{32} . The current difference is flown into M_{29} which provides current subtraction from M_{33} and M_{34} to M_{23} and M_{24} .

Current-mode common-mode feedback circuit is a superior technique compared to feed-forward cancelation circuit in terms of the power efficiency. Dual channel input pair implementation and comparison technique with voltage reference remedy the strict matching problem. This technique is the most appropriate design for the amplifier used in the input driver in terms of low voltage operation, high power efficiency, compatibility with 65 nm CMOS technology and constant signal behavior compared to the other techniques discussed so far. However, circuit complexity is the main disadvantage of this technique.

2.2.2. Proposed Fully Differential Rail-to-Rail Input-Output Amplifier

2.2.2.1. Rail-to-Rail Input Stage. The proposed rail-to-rail input stage consists of a dual n-channel input pair with PMOS level shifter, a common mode sensing circuit, a gain boosting circuit and a common-mode feedback circuit. In ADC input driver

design, accuracy and speed are the essential parameters to process a source signal such as output voltage of a sensor properly. Accuracy is directly related to the DC gain of the driver amplifier as shown in equation (2.14). As the open loop gain increases, the error decreases and the accuracy is improved. Due to the poor DC properties of 65 nm CMOS technology, high gain amplifier design is challenging [10]. Multi-stage and cascode topologies are the main alternatives to obtain higher gain [36]. Design of the multi-stage structures increases the complexity to maintain the stability. However, cascode topologies such as folded cascode and telescopic cascode enable higher gain in a single stage. Although a folded cascode circuit consumes much more power rather than a telescopic circuit, it provides larger output swing and wider input common mode range. Therefore, folded-cascode topology is preferred in the proposed rail-to-rail input stage. Speed of an amplifier is determined by its unity gain frequency. As unity gain frequency increases, output signal of an amplifier settles within shorter time. NMOS input pairs offer higher unity gain frequency with low non-dominant pole while PMOS input pairs causes lower unity gain frequency with high non-dominant pole [37]. Wider PMOS input transistors and larger current consumption are needed to provide high speed amplifier. In terms of high speed and low power requirements, dual n-channel input pairs are preferred.

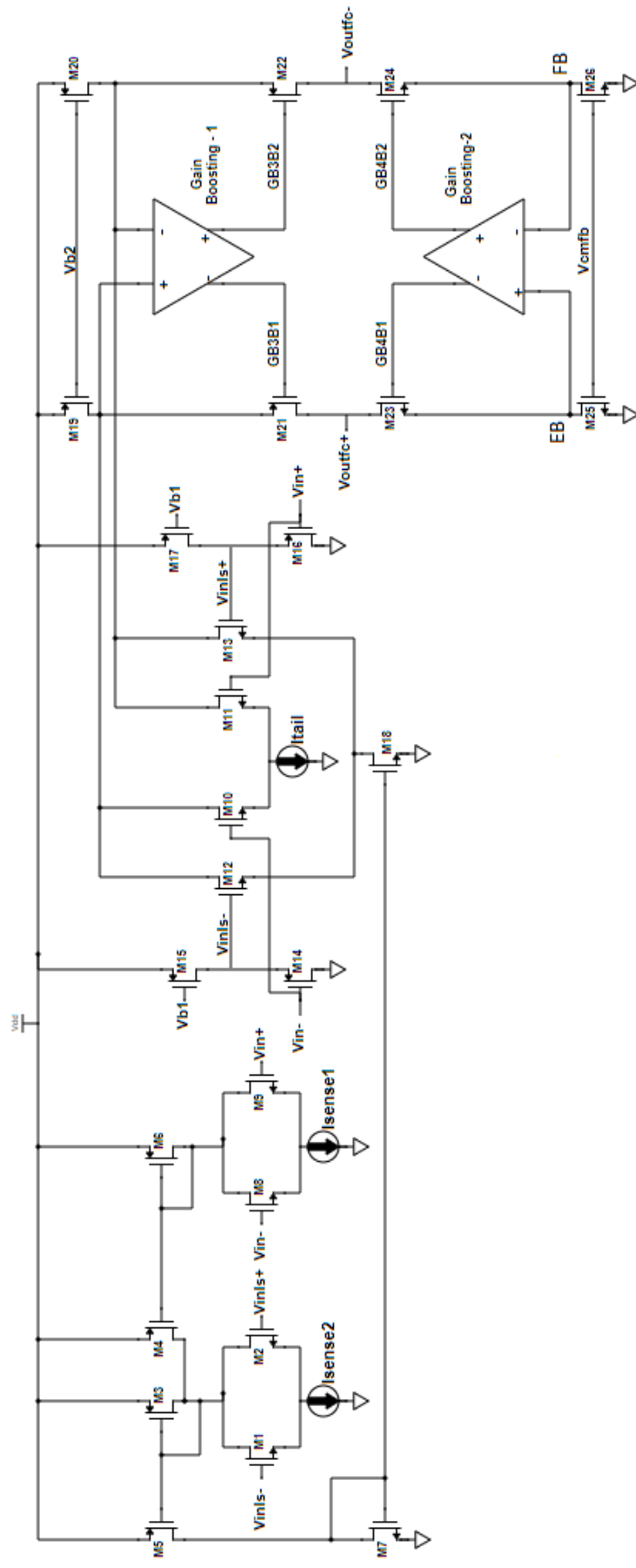


Figure 2.14. The Proposed Rail-to-Rail Input Stage (CMFB Circuit Excluded).

Input referred noise of the amplifier should be minimized to avoid the degradation of the input driver performance. According to the equation (2.12), the transconductance of the input transistors ($M_{10} - M_{13}$) should be maximized and the transconductance of the cascode transistors ($M_{19} - M_{20}, M_{25} - M_{26}$) should be minimized. In order to increase the transconductance of the input transistors, aspect ratio of them must be increased as much as possible. For the cascode transistors, gate to source voltages of them should be increased without causing reduced output swing while their aspect ratios are minimized. However, $M_{25} - M_{26}$ is driven by the output of the common-mode feedback circuit and there is a serious limitation to increase the gate voltage of them due to the proper operation of the common mode feedback circuit whose transistors must operate in saturation region. Minimum $V_{D,sat}$ value of the transistors in 65 nm technology does not allow to increase V_{CMFB} voltage excessively. Second term in the equation (2.11) shows that flicker noise is negatively proportional to transistor area. Therefore, minimum length of transistors in folded cascode topology is selected as 2 μm .

Input common mode range of the NMOS input pair folded cascode amplifier without implementing any rail-to-rail input technique can be computed by

$$V_{SS} + V_{D,sat(I_{tail})} + V_{D,sat10} + V_{TH,n} \leq V_{incm} \leq V_{DD} - V_{D,sat19} + V_{TH,n} \quad (2.30)$$

V_{SS} represents the lowest voltage level which equals zero voltage (ground) in our case. $V_{D,sat}$ denotes the minimum saturation voltage technology allows which is found as 0.075 V by referencing the bias transistor whose width and length are 4 μm and 3 μm , respectively and gate voltage is 0.35 V. $V_{TH,N}$ is the NMOS threshold voltage which is equal to 0.279 V that is valid for the transistors whose bulk is connected to source. Power supply voltage is 0.7 V. According to all known parameters, input common mode range is calculated between 0.429 V and 0.904 V. While the input common mode range exceeds the power supply value, the lowest limit cannot reach the ground value.

To obtain input common mode voltage range, level shifter technique [8] [9] [10] is implemented in the proposed design. The purpose of the level shifter is to remain in the saturation region for the input pair when input common mode voltage is applied under the lowest limit in equation (2.30). Amount of shifting voltage should be higher than 0.429 V. Level shifter implementation is realized as PMOS source follower and its output is connected to the additional n-channel input pair as shown in Figure 2.14. Additional n-channel input pair provides the robustness against process and temperature variations.

Only level shifter implementation is not sufficient to obtain rail-to-rail input stage. Without additional control circuitry, input stage cannot obtain constant total input transconductance over input common mode range. If input common mode voltage applied is higher than the lowest limit in equation (2.30), both input pairs work in saturation region. This situation leads to unnecessary current consumption and larger transconductance variation. In addition, the input pair connected to the output of the source follower cannot amplify the signal differentially because output voltage of the source follower hits the supply voltage value which means that source follower enters the linear region and cannot work properly. Although the main input pair $M_{10} - M_{11}$ is biased by constant I_{tail} , these input transistors enter the cut-off region and conduct the subthreshold current if input common mode voltage is close to ground. These tail current variation should be compensated to obtain constant signal behavior. Therefore, a control circuitry is required to maintain constant total input current. This achieves by a common mode sensing circuit which creates negative feedback loop and adjusts the tail current of the additional input pair.

2.2.2.2. Level Shifter Design. Figure 2.15 shows that dual channel input pair implementation with level shifters which are realized by source followers. A source follower is a type of common drain amplifier which offers a very high input resistance and lower output resistance compared to common source and common gate amplifier topologies. It is suitable for voltage buffer implementation with these features and functions as a level shifter as well. $M_{14} - M_{15}$ and $M_{17} - M_{18}$ form the PMOS source followers in the

proposed design as shown in Figure 2.15. $M_{14} - M_{16}$ are the input transistors to shift up the DC level of input voltage and $M_{15} - M_{17}$ act as a current source to flow the required current into the input transistor for proper operation.

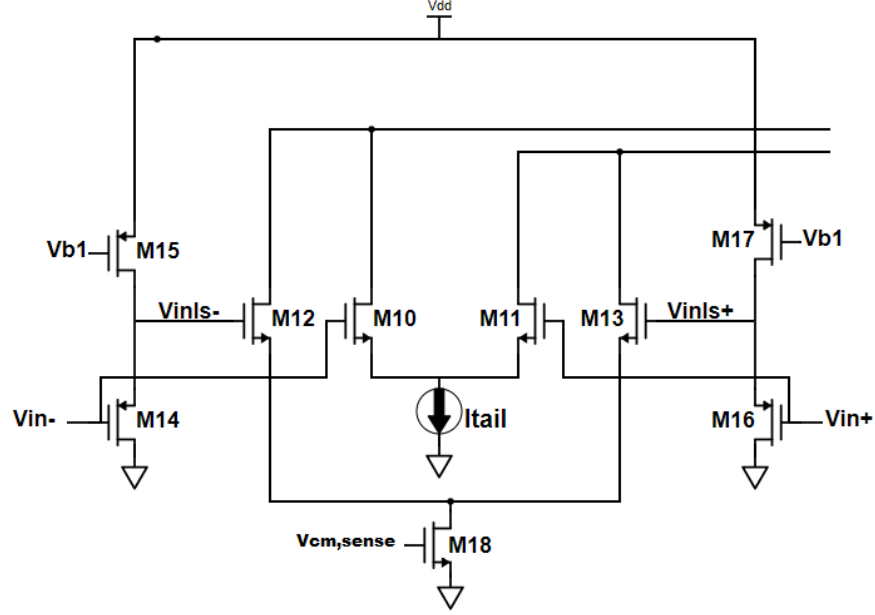


Figure 2.15. Dual Channel Input Pairs with Level Shifter.

Amount of shifting voltage (V_S) is a critical design parameter for source follower implementation. Aspect ratio of the biasing transistor ($M_{15} - M_{17}$) is positively proportional to the shifting voltage. If the current increases, gate to source voltage of the input pair increases, hence shifting voltage increases as well. Another way to increase the shifting voltage is to increase the overdrive voltage of the biasing transistor by reducing the bias voltage (V_{b1}). However, excessive reduction of the V_{b1} decreases the maximum limit of the output voltage of the source follower which is defined by $V_{DD} - V_{b1} + V_{TH,P}$. In conclusion, changing overdrive voltage is not efficient method to increase the current.

In order to understand the effect of the transistor length, DC gain formula should be derived. Figure 2.16a illustrates that source follower circuit and its equivalent small signal model. For DC gain analysis, all capacitances are open circuited in Figure 2.16b.

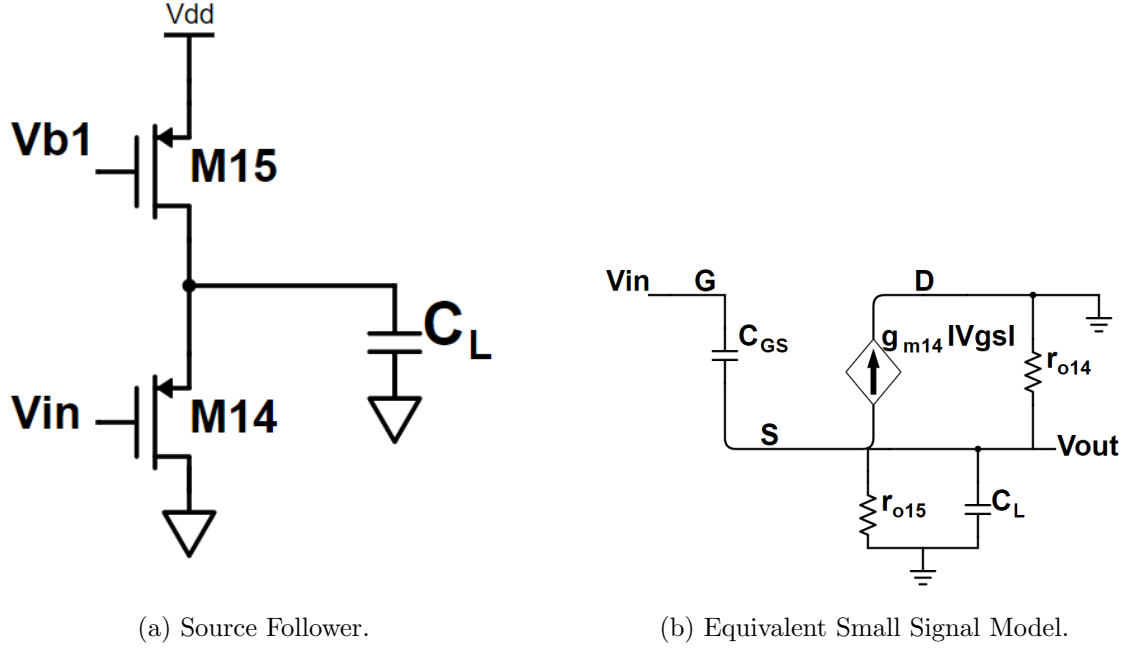


Figure 2.16. Source Follower and Equivalent Small Signal Model.

The formula is derived by

$$A_{V,DC} = \frac{g_{m14}}{g_{m14} + \frac{1}{r_{o14} \parallel r_{o15}}} \quad (2.31)$$

where g_{m14} refers to input transconductance of the source follower and $r_{o14} - r_{o15}$ denotes the output resistance of the corresponding transistors. As output resistances go to infinity, DC gain becomes ideally unity. Output resistance of a transistor changes with drain to source voltage of the transistor which directly affects the shifting voltage of the source follower. Therefore, larger output resistance improves the linearity. A transistor's length should be increased in order to obtain larger output resistance. Maximum length value the technology allows is used for the transistors in the source follower design to obtain ideal transfer function in expense of increasing parasitic capacitance.

Without level shifter implementation, input common mode range is computed between 0.429 V and 0.904 V. If input common mode range is applied under 0.429 V, $M_{10} - M_{11}$ cannot enter the saturation region and I_{tail} conducts just subthreshold

current. Source follower must shift up the DC level at least 0.429 V to obtain rail-to-rail common mode input range. At middle of the input common mode range, the source follower is forced to enter the linear region and its output is saturated at supply voltage. At that point, $M_{12} - M_{13}$ cannot amplify the input signal differentially.

The source follower brings additional pole to the system which is undesirable to limit the speed of the amplifier. Frequency response of the source follower should be derived to analyze the effect of the pole. According to the Figure 2.16b, its frequency response is given by

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_{m14} + sC_{GS}}{s(C_{GS} + C_L) + (\frac{1}{r_{o14} \parallel r_{o15}} + g_{m14})} \quad (2.32)$$

The system has one pole and one zero which is given by

$$p_1 = -\frac{g_{m14} + \frac{1}{r_{o14} \parallel r_{o15}}}{C_{GS} + C_L} \quad (2.33)$$

$$z_1 = -\frac{g_{m14}}{C_{GS}} \quad (2.34)$$

Firstly, the pole frequency must be higher than the unity gain bandwidth frequency of the amplifier to maintain stability and speed. If the pole is located at lower frequency than it, phase degradation occurs and unity gain bandwidth decreases. As shown in equation (2.33), increasing transconductance of the input transistor (M_{14}) move the pole to higher frequency. However, this leads to increase power consumption and it is not suited for ultra-low power operation. The second way is to minimize the output resistance. However, this option distorts the linearity and deviates the ideal performance of the source follower. Third alternative method is to reduce the gate to source capacitance (C_{GS}) and load capacitance (C_L) which represents the total capacitance at output node. Due to the fact that additional input pair and differential

pair in common mode sensing circuit connect to the output of the source follower, all connected transistors contribute the load capacitance. The transistor area can be minimized to reduce the load capacitance. In that case, amplifier gain and noise can be affected adversely. Another method is to locate the zero closer to the pole as much as possible. With this method, the zero removes the phase shift due to the pole. It is the most power efficient technique compared to previous ones. Aspect ratios of the transistors as shown in Table 2.1 are chosen by considering all design parameters and tuned by the simulation results.

Table 2.1. The transistor sizing of the source follower.

	TOTAL WIDTH	LENGTH
$M_{15} - M_{17}$	$2 \mu m$	$3 \mu m$
$M_{14} - M_{16}$	$1 \mu m$	$3 \mu m$

2.2.2.3. Common Mode Sensing Circuit Design. In level shifter technique, at least one input pair always works in active region and amplify the signal over rail-to-rail input common-mode range. However, this technique does not offer the constant transconductance for rail-to-rail operation. Common mode sensing circuit provides the constant total current flowing into the input pairs, hence constant operating point through rail-to-rail common mode input voltage.

Figure 2.17 shows the implementation of the common mode sensing circuit. $M_1 - M_2$ pair detects the common mode level of the input pair connected to the source follower while $M_8 - M_9$ detects that of the main input pair. I_{sense1} and I_{sense2} represent the tail current of corresponding input pair and both of them are biased with same amount of current equals to tail current of the main input pair. PMOS transistors are named from M_3 to M_6 function as an active load current mirror. M_7 and the biasing transistor of the additional input pair form current mirror as well. Node of the $V_{cm,sense}$ is the output of the circuit and the bias voltage for the biasing transistor of

the additional input pair.

At low common mode input level, $M_8 - M_9$ works in subthreshold region and I_{sense1} flows only subthreshold current. The drain voltage of M_6 approaches the supply voltage and it is in subthreshold region as well. M_4 replicates the current of M_6 and flows it into the level shifted differential pair. On the other hand, level shifted differential pair ($M_1 - M_2$) operates in saturation region due to shifting voltage of the source follower. The drain voltage of M_3 decreases at the level to supply the sufficient current which is equal to bias current of the I_{sense2} . M_5 mirrors the drain current of M_3 and it forms the bias voltage for the tail current of the additional input pair attached to the source follower. If input common mode voltage starts to rise, the current flowing into $M_8 - M_9$ increases. The drain current of M_4 also increases. Since I_{sense2} is constant as long as $M_{11} - M_{12}$ operating in saturation region, the drain current of M_3 decreases by the increased amount of the current of M_{14} . Therefore, current consumption for each input pair is sensed and total input stage current keeps constant.

All differential input pair in common mode sensing circuit has same dimension with those in rail-to-rail input stage for well matching in expense of the pole at lower frequency of the source follower. Because level shifted differential input pair ($M_1 - M_2$) is connected to output of the source follower and increases the load capacitance of it. Negative effect of the pole is eliminated by locate zero and pole close each other. Therefore, all input pair is designed with same aspect ratio without any stability and speed degradation.

Main advantage of this technique is not dependent on any technology and transistor model. The total current can be controlled effectively with symmetrical two differential pair and it is suited for low voltage, low power applications. However, the performance is still depend on the input pair matching. In the proposed design, the matching problem is solved by common centroid layout technique with dummy transistor implementation to obtain symmetric geometry.

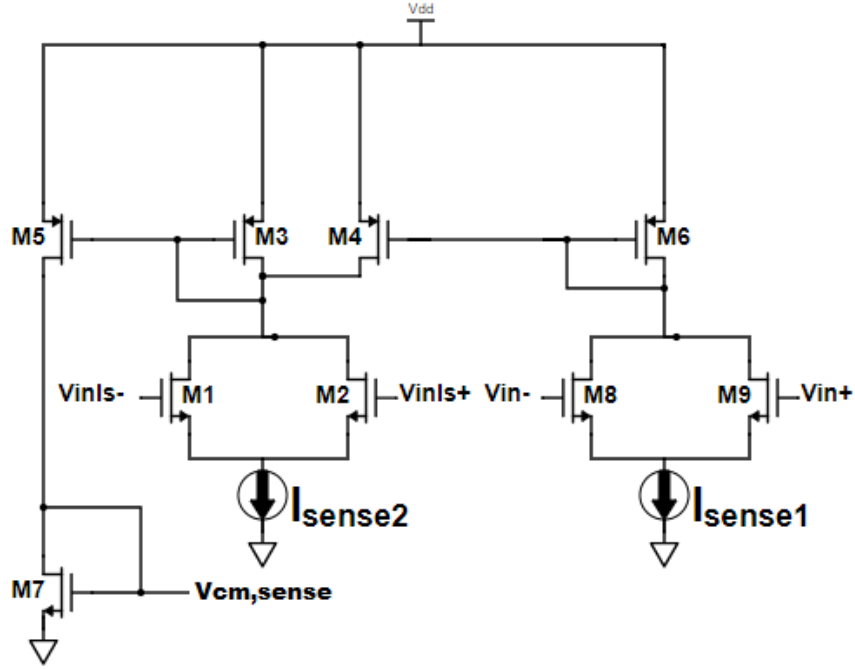


Figure 2.17. Common Mode Sensing Circuit.

2.2.2.4. Gain Boosting Circuit Design. Low intrinsic MOSFET gain in 65 nm technology is the main challenge to design a high gain amplifier. Even though folded cascode topology offers the high gain, required amplifier gain may not be achieved due to the technology related drawbacks such as low intrinsic gain. Multi stage amplifier topologies can be utilized to obtain desired gain. However, each stage brings an extra pole which requires complicated techniques to maintain the stability. In addition, a multi stage amplifier limits the speed of the amplifier due to the extra poles and the compensation techniques to remedy the stability problem. Triple cascode topology can

Table 2.2. The transistor sizing of the common mode sensing circuit.

	TOTAL WIDTH	LENGTH
$M_3 - M_4 - M_5 - M_6$	$40 \mu m$	$2 \mu m$
$M_1 - M_2 - M_8 - M_9$	$20 \mu m$	$2 \mu m$
M_7	$4 \mu m$	$3 \mu m$

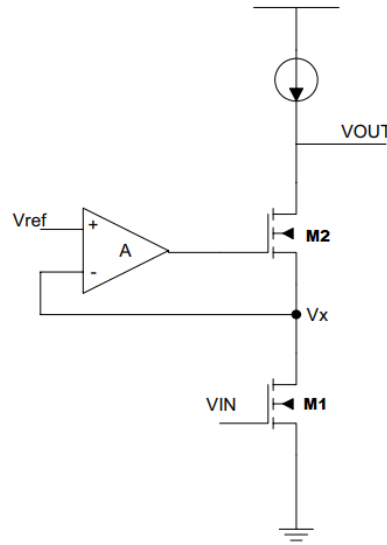


Figure 2.18. Schematic Diagram of Gain Boosting Circuit [11].

be considered as an alternative technique to enhance the gain. However, increasing stack of transistors makes the transistors remain in the saturation region impossible with 0.7 V supply voltage.

Gain boosting technique offers a relaxed trade-off among high DC gain, speed and power [38] since it increase the overall gain without extra amplifier stages or cascode devices. Figure 2.18 shows that the schematic diagram of the gain boosting circuit. Gain boosted amplifier which has a gain of A , creates a negative feedback loop and regulates the V_X against the variations at V_{OUT} [11]. M_1 converts the output current to a voltage across its output resistance. The input differential voltage of the gain boosted amplifier is multiplied by the gain of the amplifier and reflects the gate of the M_2 . The gain boosted amplifier forces the V_X equating to V_{REF} . This regulation mechanism increases the output resistance of the M_1 which makes the current less sensitive against any variation at V_{OUT} .

Small signal analysis shows that how much gain is increased by the gain boosting technique. Figure 2.19 shows that small signal model for the output resistance calculation. Test voltage is applied to the output node. Input voltage and all independent

voltage sources are killed. The gate voltage of M_2 equals $A(V_{REF} - V_X)$. Due to V_{REF} pulling down to ground, its small signal voltage appears as $-AV_X$. Small signal gate to source voltage of M_2 becomes $-V_X(A + 1)$ by subtracting V_X from $-AV_X$. The value of current source in Figure 2.19 is calculated by multiplying the transconductance value of M_2 by gate to source voltage of M_2 . As shown in Figure 2.19, M_1 is represented as only its output resistance in the small signal model. Because small signal current source of M_1 is zero due to V_{IN} pulling down to ground. Therefore, the small signal current flows across the output resistance of M_1 in small signal model.

Ratio of test voltage to test current gives the output resistance. Two equation can be derived to find the output resistance as following.

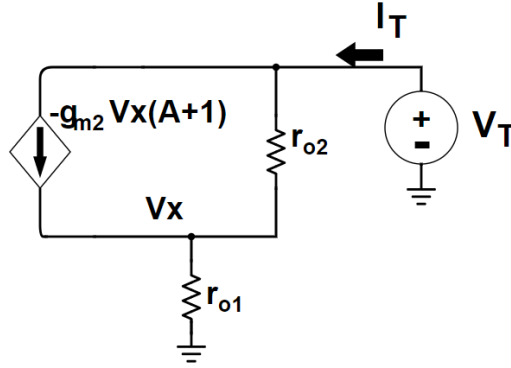


Figure 2.19. Small Signal Model of Gain Boosting Circuit for Output Resistance Calculation.

$$V_T = r_{o2}(I_T + (A + 1)V_X g_{m2}) + r_{o1}I_T \quad (2.35)$$

$$V_X = r_{o1}I_T \quad (2.36)$$

By plugging equation (2.36) into (2.35),

$$R_{OUT} = \frac{V_T}{I_T} = r_{o1} + r_{o2} + g_{m2}(A + 1)r_{o1}r_{o2} \quad (2.37)$$

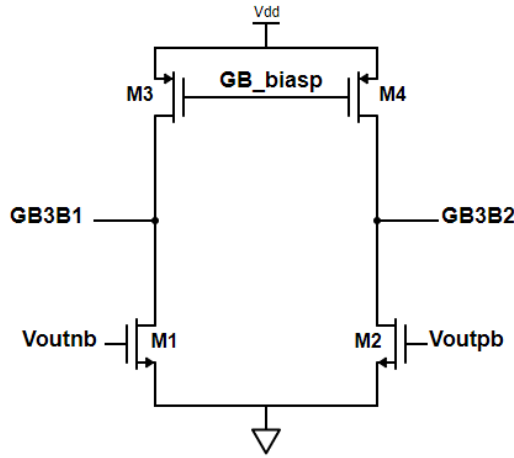
Due to $g_{m2}(A + 1)r_{o1}r_{o2} \gg r_{o1}, r_{o2}$, R_{OUT} can be reduced to

$$R_{OUT} \simeq (A + 1)g_{m2}r_{o1}r_{o2} \quad (2.38)$$

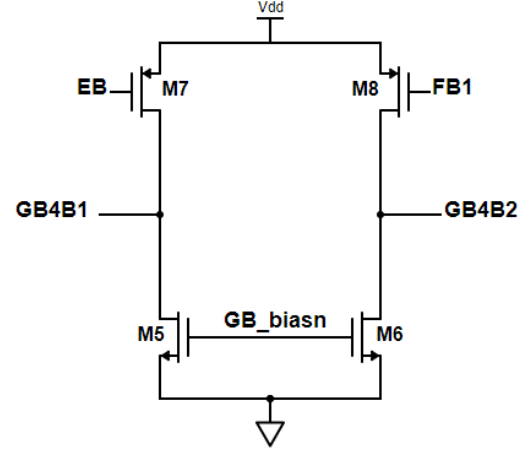
As shown in equation (2.38), the output resistance increases by $A+1$ compared to conventional cascode amplifier topology, thereby the DC gain increases by same factor.

As gain boosting amplifier improves main amplifier gain, it should not affect the performance of the frequency response of the main amplifier which is provided by faster settling time of gain boosting loop rather than settling time of the main amplifier. Unity gain bandwidth of the gain boosting amplifier should be larger than that of the main amplifier to meet this condition.

In the fully differential case, single ended gain boosting amplifier is replaced with fully differential counterpart as shown in Figure 2.14 which is labeled by “Gain Boosting-1” where is placed at upper part of the folded cascode amplifier and “Gain Boosting-2” where is placed at lower part of the folded cascode amplifier. NMOS differential input pair is used in “Gain Boosting-1” and PMOS differential input pair is used in “Gain Boosting-2”. This choice of input pair type is related to maximize the output swing. With these input pair types, minimum allowable input common mode voltage of “Gain Boosting-1” and maximum allowable input common mode voltage of “Gain Boosting-2” are independent from the gain boosting amplifiers. This results from PMOS input pair with zero voltage common mode level and NMOS input pair with 0.7 V common mode level which can operate in active region. Therefore, gain boosting circuit does not degrade the output swing of the main amplifier.



(a) NMOS Differential Input Gain Boosting Amplifier.



(b) PMOS Differential Input Gain Boosting Amplifier.

Figure 2.20. Differential Input Gain Boosting Amplifier.

Figure 2.20 shows that gain boosting amplifier design with PMOS and NMOS input pair. As shown in Figure 2.20, pseudo-differential amplifier topology is used. Both input common mode levels of gain boosting amplifiers cause large overdrive voltages which is greater than one third of supply voltage. This situation makes impossible to stack more than two transistors in the gain boosting amplifier design for the input transistors operating in active region.

Table 2.3. The transistor sizing of gain boosting amplifiers.

	TOTAL WIDTH	LENGTH
$M_1 - M_2$	$1 \mu m$	$3 \mu m$
$M_3 - M_4$	$6.1 \mu m$	$3 \mu m$
$M_5 - M_6$	$0.8 \mu m$	$3 \mu m$
$M_7 - M_8$	$1.6 \mu m$	$3 \mu m$

Transistor sizing is determined by the DC operating point and minimum current consumption to meet the unity gain bandwidth condition. Aspect ratio of transistors in gain boosting amplifiers is listed in Table 2.3.

2.2.2.5. Common-Mode Feedback Circuit Design. A folded cascode amplifier can be modeled as p-type and n-type current sources in series as shown in Figure 2.21. R_P and R_N represent corresponding output resistance of the amplifier. Ideally, I_P equals I_N and V_{OUT} becomes $V_{DD}/2$ which is desired output common mode voltage. However, any variation on the current sources deviates the output voltage by $|I_P - I_N|(R_P \parallel R_N)$ [11]. Due to the high value of the output resistances, very small variations lead to substantial deviation on the output voltage which avoids the transistors to work in active region. Therefore, a common mode feedback mechanism is required for a fully differential amplifier.

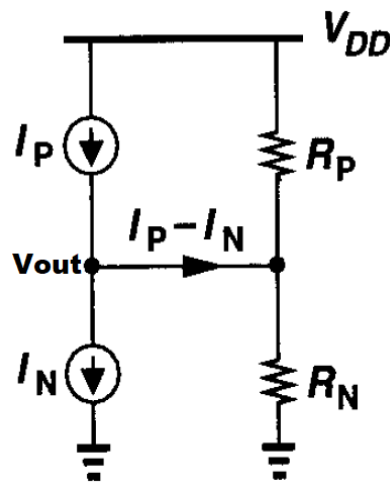


Figure 2.21. Folded Cascode Amplifier Model with Current Sources [12].

Simplest common mode feedback technique is to place two equal resistors between output nodes and biased with desired output common mode voltage between these two resistors as shown in Figure 2.22. Sensing transistors operate as a voltage average. Although simplicity is an advantage for a designer, this method introduces resistive loading problem. Sensing resistors lead to reduce the amplifier gain unless they have much higher value than the output resistance of the amplifier. A resistor of higher value results in usage of larger area and increasing parasitic capacitance which reduces the speed of the amplifier.

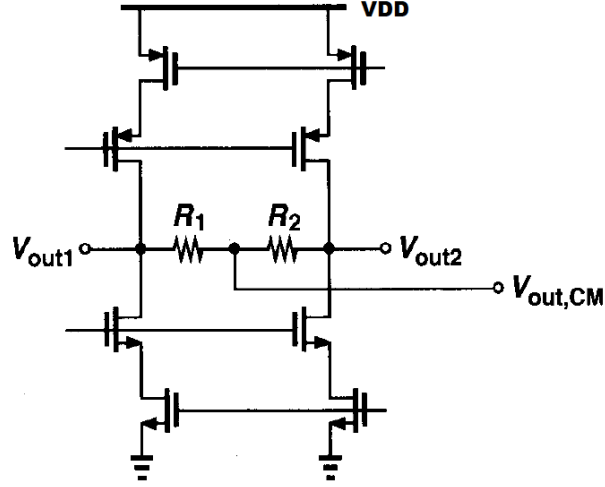


Figure 2.22. Resistive Divider Technique [12].

Sensing resistors can be isolated from the output node to remove the resistive loading effect by using a source follower as shown in Figure 2.23. However, it raises the minimum allowable output voltage, thereby it reduces the output swing. Without source follower technique, minimum allowable output voltage is determined as following according to Figure 2.23.

$$V_{OUT,min} = V_{OV3} + V_{OV5} \quad (2.39)$$

After source follower technique is implemented, new minimum allowable output voltage is computed as

$$V_{OUT,min} = V_{GS7} + V_{I1} = V_{OV7} + V_{OV,I1} + V_{TH} \quad (2.40)$$

As shown in equation (2.40), the source follower technique raises the minimum allowable output voltage by V_{TH} . This is a serious problem for low supply voltage operation. In 65 nm technology, V_{TH0} equals to 0.279 V which means reducing output voltage swing by more than one third of supply voltage. In addition, sensing resistors

value, I_1 and I_2 should be large enough in order to the fact that M_7 and M_8 can be driven properly if a large differential signal is presented at output node. Therefore, this technique is not suited for a low-power application.

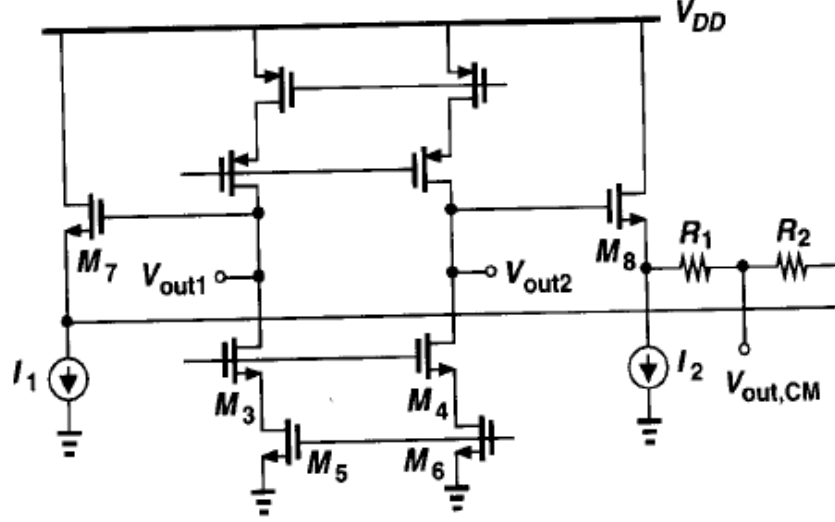


Figure 2.23. Source Follower Technique [12].

The proposed common mode feedback circuit is presented in Figure 2.24. This topology eliminates the resistive loading and does not affect the output voltage swing. The output nodes of the folded cascode amplifier which are labeled as " V_{outmfb} " and " V_{outpfb} ", are connected to the proposed CMFB circuit as shown in Figure 2.24. Parasitic capacitances of $M_3 - M_4$ may bring the extra capacitance to the output node of the main amplifier. However, this capacitance is too much small compared to the capacitance that is caused by the sensing resistors. Bandgap reference circuit generates 0.35 V which is the desired output common mode voltage and it is connected to " V_{outcm} " node in the CMFB circuit.

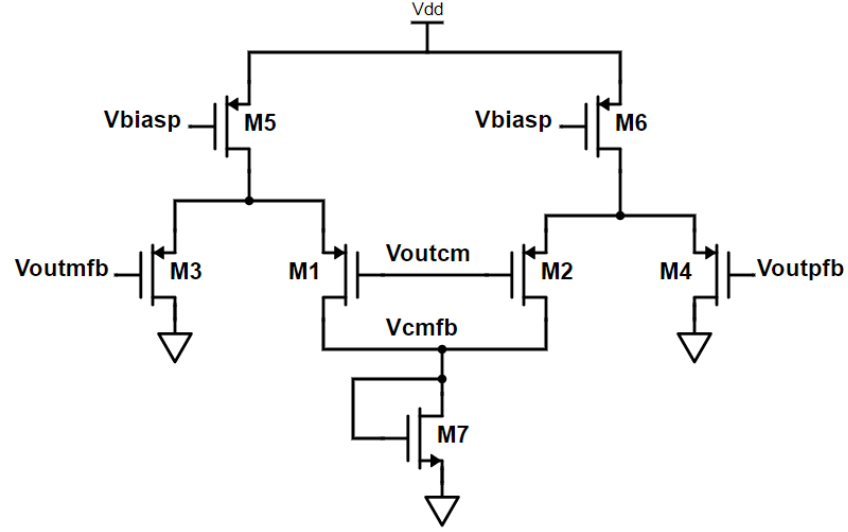


Figure 2.24. The Proposed CMFB Circuit.

Output common mode level is sensed by the transistor pair $M_3 - M_4$ and is compared with ideal output common mode voltage by $M_1 - M_2$. Increase in common mode output level causes reduced current flowing into $M_3 - M_4$, hence the drain current of $M_1 - M_2$ increases and this leads to increase the voltage at " V_{cmfb} " node which is connected to gate voltage of $M_{25} - M_{26}$ as shown in Figure 2.14. This increase in " V_{cmfb} " node drops the output common mode voltage to the desired level. Input transconductance of the CMFB circuit affects the linearity performance directly. Bias current or aspect ratio of the input pair should be increased to improve the linearity of the CMFB circuit. The transistor sizing of the proposed CMFB circuit is listed in Table 2.4.

Table 2.4. The transistor sizing of the proposed CMFB circuit.

	TOTAL WIDTH	LENGTH
$M_1 - M_2 - M_3 - M_4$	$20 \mu m$	$1 \mu m$
$M_5 - M_6$	$4.4 \mu m$	$1 \mu m$
M_7	$3 \mu m$	$2 \mu m$

2.2.2.6. Rail-to-Rail Output Stage. Rail-to-rail output swing is an essential feature for a low voltage system which reduces the dynamic range of the system. It improves the SNR and linearity by avoiding clipping output signal. In our design, each input of the differential input SAR ADC accepts the voltage level between 100 mV and 600 mV. Therefore, the output stage must drive the load resistance and capacitance with desired specifications at these extreme voltage values on the output node.

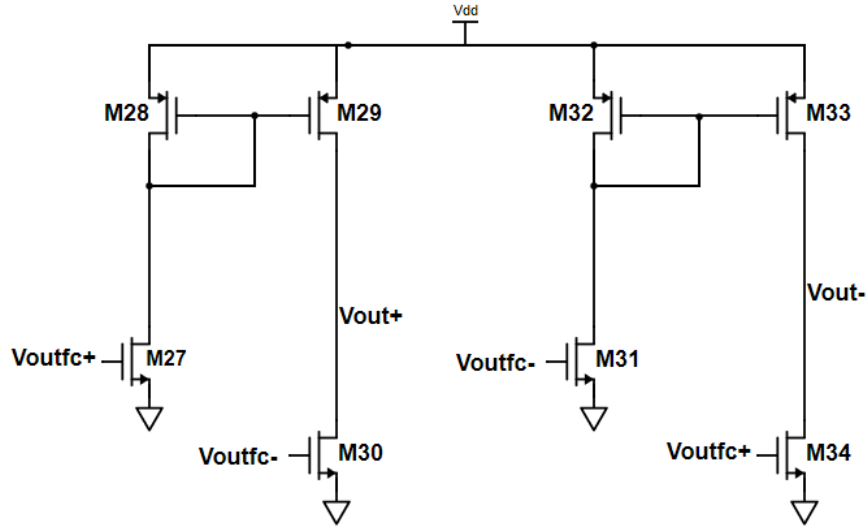


Figure 2.25. The Proposed Rail-to-Rail Output Stage.

Figure 2.25 shows that the proposed rail-to-rail output stage of the fully differential amplifier. Its working principle depends on a push-pull operation. " V_{outfc+} " and " V_{outfc-} " denote the positive and negative output nodes of the folded cascode stage and " V_{out+} " and " V_{out-} " represent the positive and negative output node of the fully differential amplifier, respectively. The performance of the CMFB circuit has an impact on the rail-to-rail output stage. If the positive output voltage of the folded cascode stage changes by ΔV , the negative output voltage of it changes by $-\Delta V$. Push-pull output stage takes advantage of it as one output node is pulled down to ground and the other is pushed up to supply voltage. Any voltage increase in " V_{outfc+} " node causes to flow more current through M_{28} . M_{29} mirrors the current of M_{28} and push a larger amount of current into the positive output node. Decreasing voltage on " V_{outfc-} " allows the

positive output voltage to hit the positive supply rail. On the other hand, M_{34} tries to pull down negative output voltage to ground due to the increase in current of M_{34} with the voltage increase in " V_{outfc+} ".

Figure 2.26 shows that the small signal equivalent circuit of the output stage for one output branch. According to Figure 2.26, the output resistance and the transconductance of the output stage is computed as

$$R_{OUT} = r_{o29} \parallel r_{o30} \quad (2.41)$$

$$G_m = \frac{1}{2} \left(\frac{g_{m27}g_{m29}}{g_{m28}} + g_{m30} \right) \quad (2.42)$$

The voltage gain of the output stage is given by

$$A_V = G_m R_{OUT} \quad (2.43)$$

$$A_V = \frac{1}{2} \left(\frac{g_{m27}g_{m29}}{g_{m28}} + g_{m30} \right) r_{o29} \parallel r_{o30} \quad (2.44)$$

$M_{28} - M_{29}$ and $M_{32} - M_{33}$ are the active loaded current mirrors. Current mirror gain is defined as

$$A_I = \frac{\left(\frac{W}{L}\right)M_{29}}{\left(\frac{W}{L}\right)M_{28}} = \frac{\left(\frac{W}{L}\right)M_{33}}{\left(\frac{W}{L}\right)M_{32}} \quad (2.45)$$

Higher current mirror gain reduces the drain current of M_{28} and M_{29} . From the ultra-low power design perspective, the active loaded current mirrors with high current

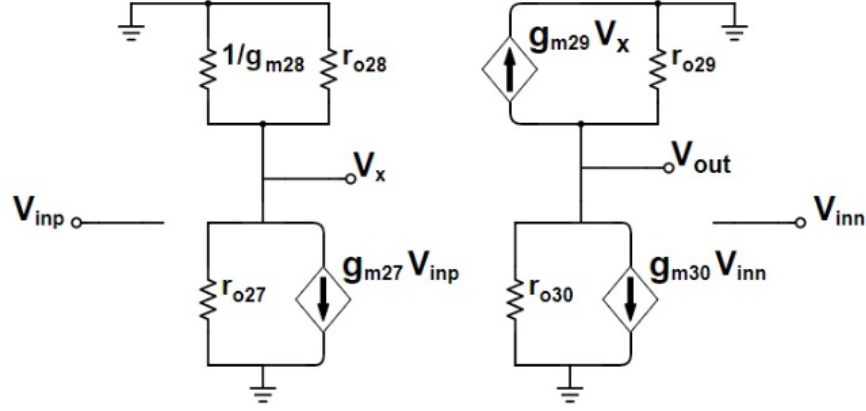


Figure 2.26. The Small Signal Equivalent Circuit of the Output Stage.

gain are utilized in the output stage design. Transistor sizing of the output stage is listed in Table 2.5.

Table 2.5. The transistor sizing of the rail-to-rail output stage.

	TOTAL WIDTH	LENGTH
$M_{27} - M_{31}$	$2 \mu m$	$3 \mu m$
$M_{28} - M_{32}$	$6.4 \mu m$	$3 \mu m$
$M_{29} - M_{33}$	$100 \mu m$	$1 \mu m$
$M_{30} - M_{34}$	$42.5 \mu m$	$1 \mu m$

2.2.2.7. Overall Design. Dual channel input pair offers the ease of matching, in contrary to complementary input pair, since same channel input pairs can be implemented in same well. With special layout techniques such as common centroid design with dummy transistors, these input pairs become more robust against PVT variations. P-type and N-type transistors have different mobility factors which depend on the temperature value. Therefore, complementary input pair is more sensitive to the temperature variations which is an undesirable feature especially for an ADC input driver circuit used in temperature measurement.

The working principle of the proposed input common mode sensing circuit is independent of the technology model and operation region. With this control mechanism, the total current flowing into input pairs remains constant through rail-to-rail input voltage range. The purpose is to provide constant signal behavior such as gain, GBW and phase margin because the current variation leads to change the signal characteristics.

Figure 2.28 shows that overall design and small signal model of the fully differential amplifier. Miller approximation method is utilized to obtain small signal equivalent circuit.

R_{out1} and G_{m1} are the small signal parameters of the folded cascode stage. R_{out2} and G_{m2} are related to the output stage which are calculated in the equation (2.41) and (2.42), respectively.

$$R_{out1} = R_u \parallel R_d \quad (2.46)$$

$$G_{m1} = g_{m11} \frac{R_u - r_{o22}}{R_u} \quad (2.47)$$

R_u and R_d represent upper and lower output resistance of the folded cascode stage, respectively.

$$R_u = R'_u(A + 1) \quad (2.48)$$

$$R_u = (g_{m22}r_{o22} + 1)(r_{o11} \parallel r_{o20}) + r_{o22} \quad (2.49)$$

$$R_d = R'_d(A + 1) \quad (2.50)$$

$$R_d = (g_{m24}r_{o24} + 1)r_{o26} + r_{o24} \quad (2.51)$$

Equation (2.52) shows the frequency dependent transfer function of the fully differential amplifier in s domain.

$$H(s) = G_{m1}G_{m2}R_{out1}(R_{out2}||R_L)K(s) \quad (2.52)$$

$$K(s) = \frac{1 - \frac{sC_c}{G_{m2}}}{sR_{out1}C_c(1 + G_{m2}R_{out2}R_L)(1 + s\frac{R_{out1}R_{out2}R_LC_L}{R_{out1}R_{out2} + R_{out1}R_L + R_{out2}R_L + G_{m2}R_{out1}R_{out2}R_L})} \quad (2.53)$$

The dominant and non-dominant poles of the fully differential amplifier are shown in the equation (2.54) and (2.55), respectively. The effect of the parasitic capacitances is neglected.

$$w_{p1} = -\frac{1}{R_{out1}C_c(1 + G_{m2}R_{out2})} \quad (2.54)$$

$$w_{p2} = -\frac{1}{(\frac{1}{G_{m2}} || R_{out1} || R_{out2} || R_L)C_L} \quad (2.55)$$

$$w_z = \frac{G_{m2}}{C_C} \quad (2.56)$$

The equation (2.58) shows the unity gain bandwidth frequency. Since the resistor of the low pass filter at the output of the input driver isolates the fully diff amplifier from the ADC input capacitance and the filter capacitance, the only parasitic capacitance contributes the load capacitance of the amplifier which is very small value compared to the ADC input capacitance of 5 pF. Therefore, the proposed design allows the smaller

value of the compensation capacitor and hence the speed of the amplifier improves significantly according to the equation (2.58).

$$w_u = |A_o|w_{p1} \quad (2.57)$$

For $|A_o| = G_{m1}G_{m2}R_{out1}(R_{out2}||R_L)$,

$$w_u \simeq \frac{G_{m1}}{C_C} \quad (2.58)$$

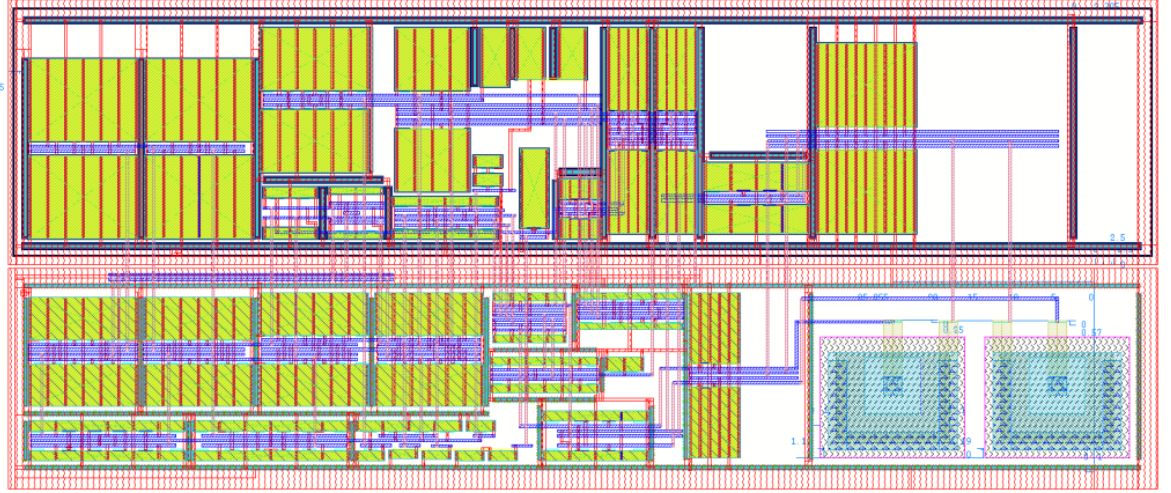
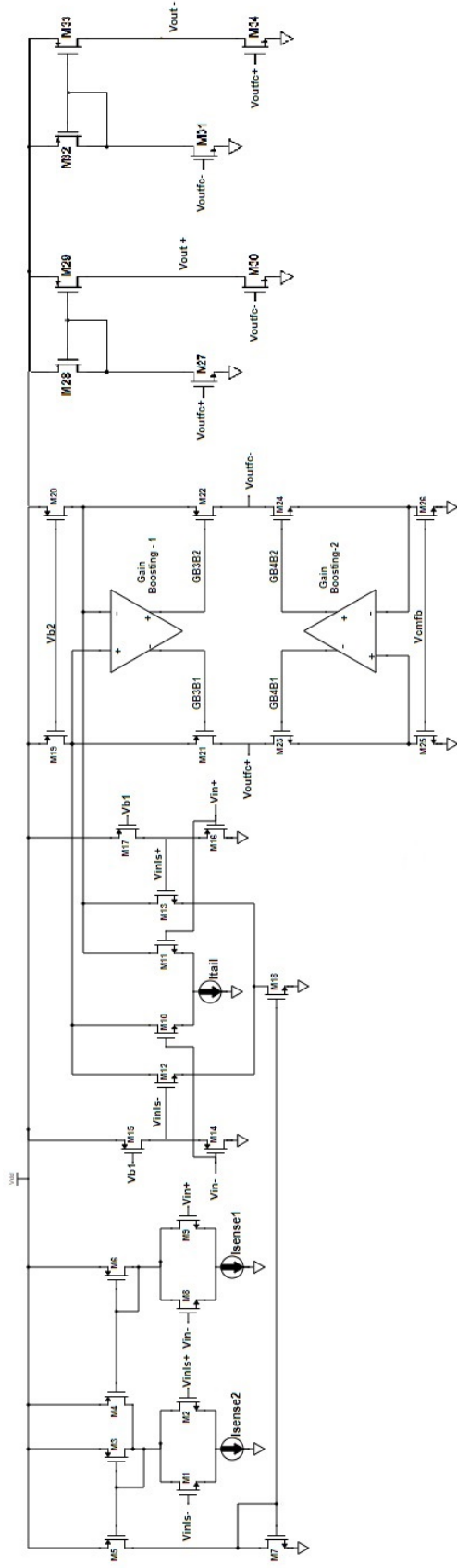
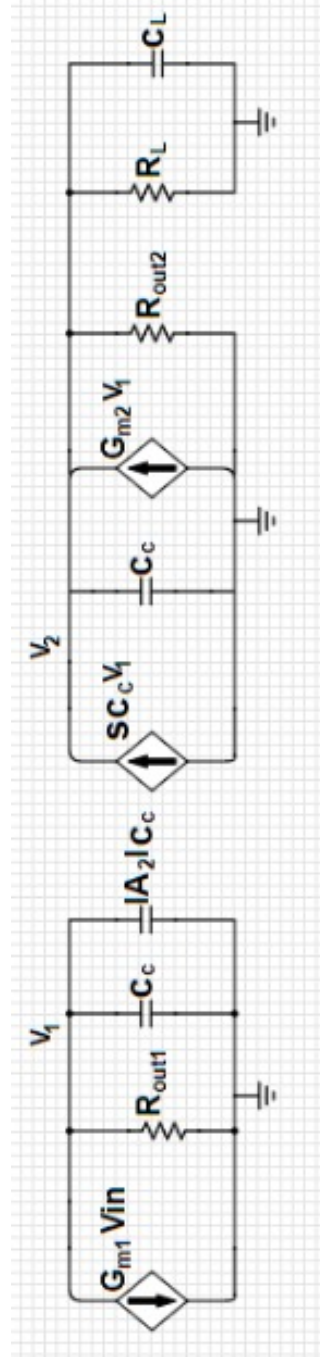


Figure 2.27. Layout of the Rail-to-Rail Input-Output Fully Differential Amplifier.



(a) Overall Design of the Fully Differential Amplifier.



(b) Small Signal Model of the Fully Differential Amplifier.

Figure 2.28. Overall Design and Small Signal Model of the Fully Differential Amplifier.

2.3. Voltage Buffer for the Input Common Mode Voltage

Voltage buffer for input common mode voltage consists of the bandgap reference circuit which generates the input common mode voltage that is calculated according to the equation (1.1), RC low-pass filter to reduce the noise caused by the bandgap reference and non-inverting unity gain buffer as shown in Figure 2.29. The output of the voltage buffer is connected to the resistor which determines the voltage gain of the input driver and is connected to the negative input terminal of the fully differential amplifier as shown in Figure 2.2. The purpose of generating input common mode voltage is to shift the input voltage centered input-common mode to obtain symmetry at the output of the input driver [17].

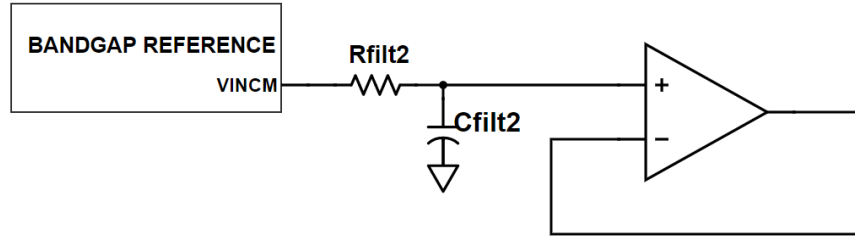


Figure 2.29. Top Level Architecture of the Voltage Buffer for Input Common Mode Voltage.

The ultra-low power bandgap reference circuit is lacking of the drive capability due to the very high output resistance. If the output of the bandgap circuit is directly connected to the rest of the circuit in Figure 2.2, this causes the signal attenuation which is given by

$$V_{OUT} = V_{INCM} \frac{R_L}{R_L + R_{BG}} \quad (2.59)$$

R_L and R_{BG} denote to the load resistance of the rest of the input driver and the output resistance of the bandgap reference circuit. Bandgap circuit can be considered

as a voltage source with source resistance in series. The load resistance should be much larger than the output impedance of the bandgap reference to avoid the signal attenuation. However, it is practically impossible since the resistors in the order of Mega-ohm are required.

A voltage buffer is required to drive the load resistance properly. A buffer amplifier is configured as a non-inverting unity gain which offers high input resistance and low output resistance. The macro model of the amplifier is used to calculate the output resistance of the voltage buffer as shown in Figure 2.30. The bandgap reference is modeled as a voltage source with source resistance (R_{BG}) in series. Due to the input terminals of the amplifier connected to the gate of the MOS-FET, the amplifier has very large input resistance (R_{in}). R'_{OUT} denotes the output resistance of the amplifier. To calculate the output resistance, V_{INCM} is pulled down to ground. Output resistance of the voltage buffer is computed as

$$\begin{aligned}
 R_{OUT} &= \frac{V_{OUT}}{I_{OUT}} \\
 &= \frac{V_{OUT}}{\frac{V_{OUT} - (-AV_{OUT})}{R'_{OUT}}} \\
 &= \frac{R'_{OUT}}{A + 1}
 \end{aligned} \tag{2.60}$$

“A” represents the open loop gain of the amplifier. As shown in equation (2.61), the higher open loop gain offers the lower output resistance. The calculated output resistance is much lower than the load resistance and it is suited for driving low resistive load.

RC low pass filter is placed between bandgap reference circuit and the buffer amplifier. Due to the output of the bandgap reference produces the constant DC voltage through the operating temperature range, the corner frequency of the low pass filter can be decreased as possible. It helps to reduce the total output noise of the

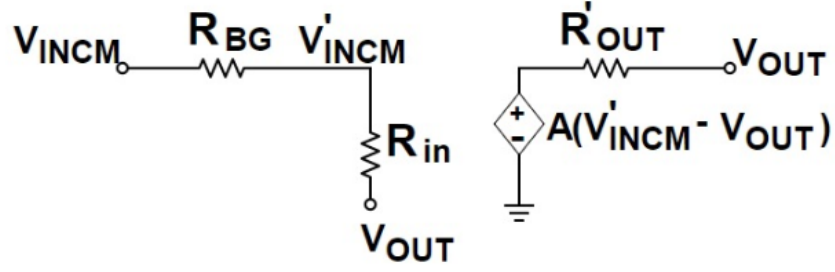


Figure 2.30. The Macro Model of the Buffer Amplifier.

input driver. The corner frequency of the RC low pass filter is defined as

$$f_c = \frac{1}{2\pi RC} \quad (2.61)$$

65 nm CMOS technology offers different types of capacitors: NCAP, PCAP, MOM and MIM. NCAP and PCAP utilize gate capacitance of NMOS and PMOS, respectively [39]. These devices suffer from nonlinearity and leakage. They occupy smaller area compared to other capacitor devices. MOMCAP consists of a multilayer metal wires which utilize parasitic capacitance of interconnects. It is very sensitive to process variations and switching noise. MIMCAP can be considered as an ideal parallel plate capacitor. It has the best linearity and leakage performance among the capacitor types in the technology. However, it has lowest unit capacitance so that it occupies the largest area in layout. Due to its improved performance, MIMCAP is used as a filter capacitor in voltage buffer for input common mode voltage at expense of larger area. It occupies $(75\mu m * 75\mu m)$ area with 11.27 pF value. As the capacitance is larger, leakage problem is the more serious so that MIMCAP is preferred. As shown in the equation (2.61) , as the resistance value increases, the corner frequency decreases and improves the noise performance. At some point, the noise reduction stops since thermal noise of the resistor dominates the system so that the resistance value should not be increased infinitely. $4.35M\Omega$ resistor is selected for the proposed design.

The proposed single ended amplifier for the input common mode voltage buffer is shown in Figure 2.31. Gain boosted folded cascode topology is used as in the fully differential amplifier design. For the voltage buffer, rail-to-rail output stage is not required since the output of the voltage buffer should follow the constant input common mode voltage through specified temperature range in contrary to the output of the fully differential amplifier must swing at least from 100 mV to 600 mV. Voltage buffers for the input common mode voltage and the temperature sensor have same design to obtain a balanced output signal. However, with same design, voltage buffer for the input common mode voltage starves the output current at the low temperature values and cannot source the current to the rest of the circuit. The output stage can be biased by the larger amount of the current as a solution. This leads to an excessive current increase over the temperature range. Therefore, it is not a power efficient solution. Instead of it, a different biasing scheme is proposed as shown in Figure 2.31. The current of the output stage varies with the output of the temperature sensor which is labeled as “VPTAT” in Figure 2.31. The output of the temperature sensor cannot be directly connected to the gate of the M_{12} since the sufficient current cannot be flown into the output branch with these bias voltage values. Therefore, the bias voltage must be shifted down to obtain a larger amount of output current. A source follower is utilized to shift the voltage down. The amount of the shifting voltage is determined by the total output current through temperature range should be less than the total output current without the temperature compensation. As the temperature decreases, the overdrive voltage of the M_{12} increases, hence the current increases at the output stage. As the temperature increases, the overdrive voltage of the M_{12} decreases and the current decreases at the output stage. The transistor sizing of the source follower is listed in Table 2.6.

Table 2.6. The transistor sizing of the source follower in the voltage buffer for input common mode voltage.

	TOTAL WIDTH	LENGTH
M_{14}	150 μm	0.5 μm
M_{13}	3 μm	3 μm

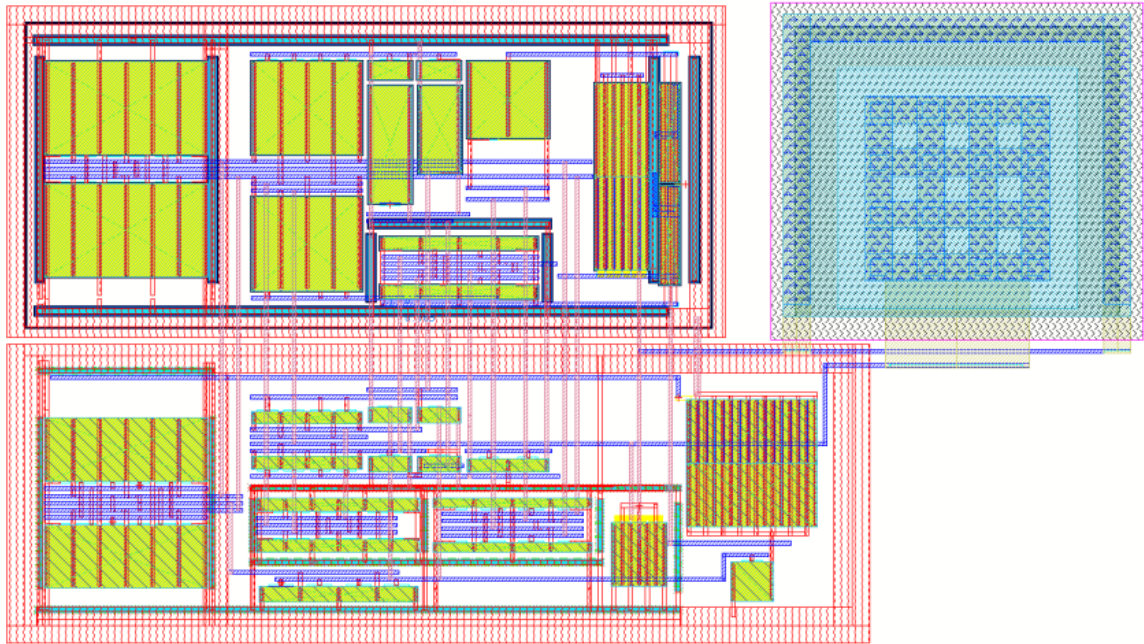


Figure 2.32. Layout of the Single Ended Amplifier for the Input Common Mode Voltage Buffer.

2.4. Voltage Buffer for the Temperature Sensor

Ultra-low power temperature sensor produces the output voltage which is proportional to the temperature value. Due to its ultra-low power nature, the output resistance of the temperature sensor is very large and not suited for direct connection to the rest of the circuit. Voltage buffer circuit is needed as in case of section 2.3. Voltage buffer for temperature sensor consists of temperature sensor, RC low pass filter and non-inverting unity gain amplifier as shown in Figure 2.33.

The corner frequency of the RC low pass filter must not be less than 100 kHz according to the design specifications since it directly affects the frequency response of the output of the input driver unlike the low pass filter in voltage buffer for input common mode voltage. In order not to affect the leakage problem, relatively small capacitance value is selected as 660 fF. NCAP device is used to occupy less area ($5 \mu\text{m} \times 5 \mu\text{m}$) in comparison to other types of capacitors. Resistance value is chosen as $400k\Omega$.

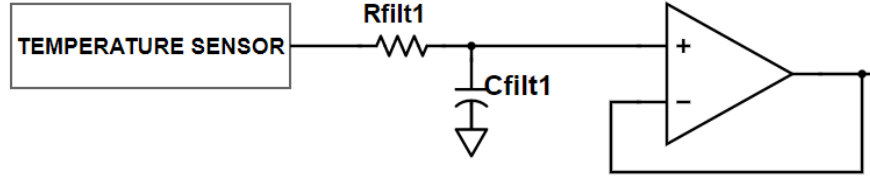


Figure 2.33. Top Level Architecture of the Voltage Buffer for the Temperature Sensor.

Figure 2.34 shows that the proposed single ended amplifier for temperature sensor voltage buffer. Gain boosted folded cascode input stage design is identical to the single ended amplifier for input common mode voltage buffer. As shown in Figure 2.34 , the gate of the $M_9 - M_{10}$ is connected to the drain of the $M_6 - M_7$ to form high swing cascode current mirror. " V_{bias} ", " $GB1B1$ " and " $GB2B1$ " represent the bias voltages which are produced by a bias generator for folded cascode topology.

Transistor sizing of the output stage is listed in Table 2.7. Smaller length is used compared to the gain boosted folded cascode circuit due to obtaining lower output resistance to drive load resistance properly.

Table 2.7. The transistor sizing of the output stage of temperature sensor buffer amplifier.

	TOTAL WIDTH	LENGTH
M_{12}	$90 \mu m$	$0.5 \mu m$
M_{11}	$30 \mu m$	$0.5 \mu m$

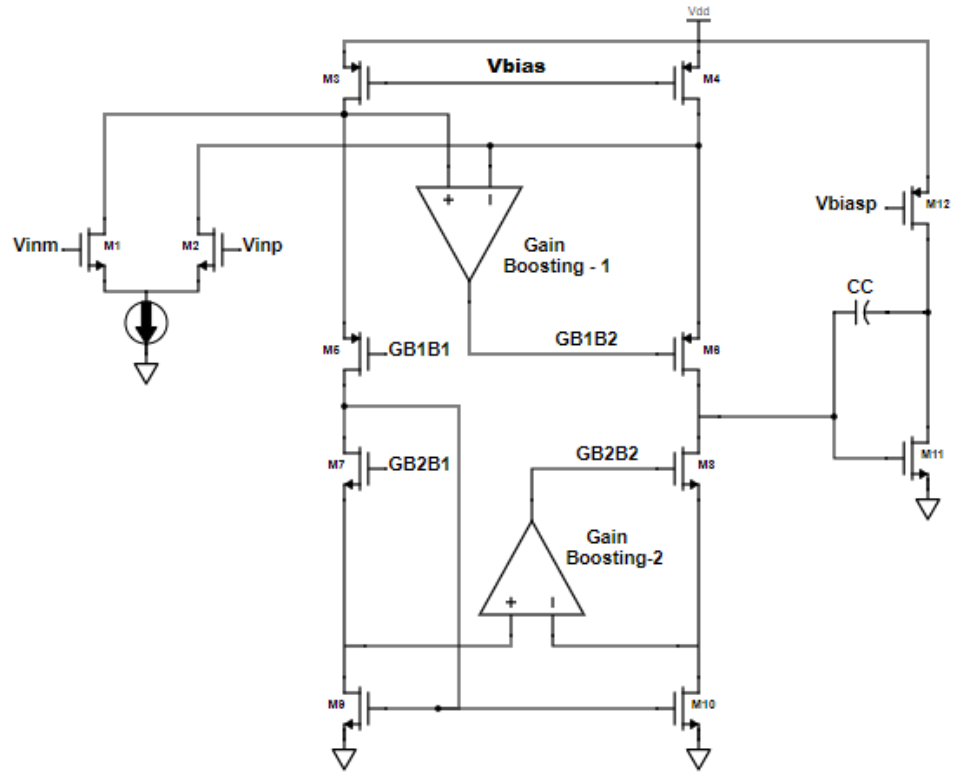


Figure 2.34. The Proposed Single Ended Amplifier for the Temperature Sensor Voltage Buffer.

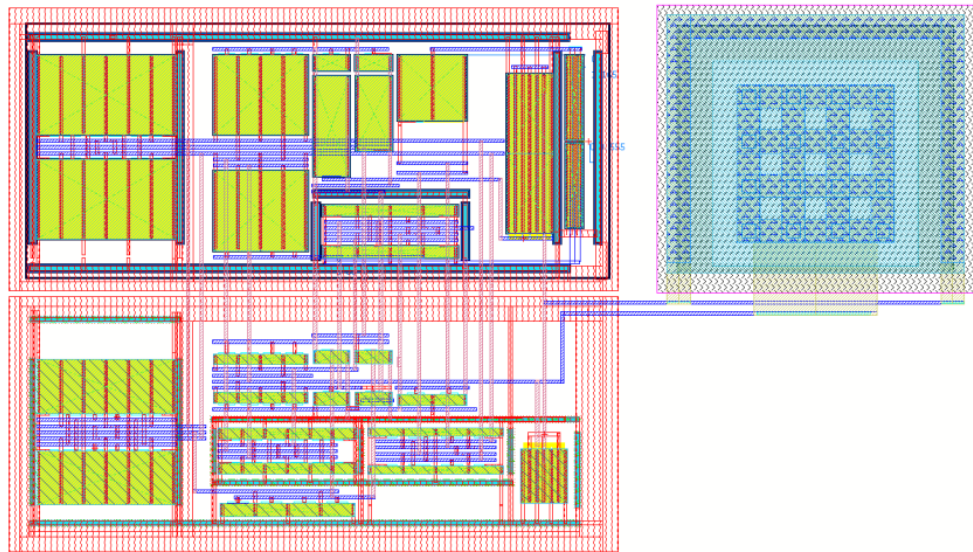


Figure 2.35. Layout of the Single Ended Amplifier for the Temperature Sensor Voltage Buffer.

3. REFERENCE DRIVER CIRCUIT DESIGN

3.1. System Design Theory

SAR ADCs operate conversions by comparing an input voltage with a reference voltage and produce a digital output according to the input voltage level. Any variation on reference voltage affects the performance of the SAR ADC adversely and it may cause wrong digital code. Reference driver circuit must be designed according to its some parameters such as settling time, drive capability, noise, accuracy and stability.

To provide a stable reference voltage for the SAR ADC, LDOs with low noise and fast settling time. Its equivalent series resistance must be low enough such that error of the steady state voltage value is less than $\frac{1}{2}$ LSB of the SAR ADC to avoid any conversion errors [40]. In our case, ultra-low power bandgap reference circuit is utilized to supply the reference pin of the SAR ADC. As discussed in previous chapter, the drive capability of the bandgap reference circuit is insufficient to meet the load conditions and the current demand of the SAR ADC. Due to its ultra-low power design, its high output impedance and insufficient bandwidth degrade the settling time performance and the signal strength. Therefore, it should not be connected to the reference pin of the SAR ADC directly. As shown in Figure 1.7, a buffer amplifier must be implemented in a unity gain configuration.

Settling time is defined as the time passed for an output voltage to reach its steady value within a specified error band. It depends on output load capacitance and reference voltage level. A reference driver circuit must settle faster than the acquisition time of the SAR ADC to obtain a stable reference for proper operation. Error band is determined as $\frac{1}{4}$ LSB of the SAR ADC.

Once the drive capability and settling time requirements have been met, total output noise at the reference input of the SAR ADC should not degrade the performance of the ADC. Therefore, the output noise voltage of the reference driver should

not exceed $\frac{1}{2}$ LSB of the ADC.

Ideally, closed loop gain of the reference buffer is unity as the open loop gain of the buffer goes to infinity. However, the open loop gain of the amplifier is finite and it introduces the error in the system. Therefore, the open loop gain of the reference buffer determines the accuracy of the reference driver. Closed loop gain of the voltage buffer in unity gain configuration can be computed as

$$\begin{aligned} A_{CL} &= \frac{A_{OL}}{A_{OL} + 1} \\ &= 1 - \frac{1}{A_{OL} + 1} \end{aligned} \quad (3.1)$$

A_{OL} denotes the open loop gain of the amplifier. Second term of the equation (3.1) represents the gain error. To improve the accuracy, open loop gain of the amplifier must be increased. Minimum open loop gain should be larger than the quantization noise of the ADC to avoid incorrect conversion bits. The equation (3.1) is derived from the formula for a linear system with feedback model as shown in the equation (3.2).

$$V_{out} = \frac{A}{1 + A\beta} V_{in} \quad (3.2)$$

β is the feedback factor which is one for the voltage follower topology. $A\beta$ represents the loop gain. Once the loop gain equals to -1, the system becomes unstable and oscillates.

If feedback loop is broken as shown in Figure 3.1, equation (3.3) gives the loop gain.

$$-\frac{V_r}{V_s} = A\beta \quad (3.3)$$

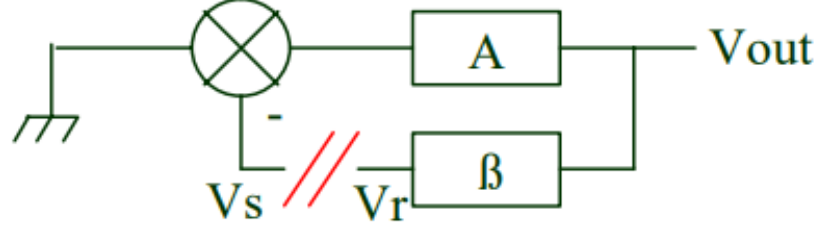


Figure 3.1. Broken Feedback Loop for Calculating Loop Gain [13].

For the reference buffer amplifier, the loop gain in s domain equals to

$$-\frac{V_r}{V_s}(s) = \frac{A(s)}{1 + sZ_O C_L} \quad (3.4)$$

As shown in equation (3.4), the load capacitance brings a pole to the loop gain. The stability improves as the pole frequency increases. If the pole frequency is lower than the unity gain bandwidth of the system, it affects the stability adversely and a stability compensation may be required in that case. Therefore, heavy capacitive load is a problematic issue to maintain the stability.

The proposed reference driver must drive the input capacitance ADC of 10 pF. Miller compensation method is utilized to obtain a stable system and phase margin of 55° is achieved. Out-of-loop compensation method by adding a resistor at outside of feedback loop to isolate the amplifier feedback network from the capacitive load is not needed. This method suffers from the accuracy of output voltage depends on a resistive load value [13].

3.2. Reference Buffer

The proposed reference buffer amplifier consists of a gain boosted folded cascode input stage and current and stability controlled output stage as shown in Figure 3.2. $M_{13}, M_{15}, M_{17} - M_{19}$ and M_{20}, M_{21} are the switching transistors to control the current of the output stage and the value of the compensation capacitor, respectively. They

add some ON-resistance to the signal path [41]. ON-resistance value can be found by the equation (3.5).

$$R_{ON} = \frac{1}{\mu_p C_{ox} \frac{W}{L} |V_{GS} - V_{TH}|} \quad (3.5)$$

There is a trade-off between ON-resistance value and parasitic capacitance to design an optimized switch. As shown in equation (3.5), increasing aspect ratio of the switching transistor reduces its ON-resistance. However, it increases the parasitic capacitance and leads to lower bandwidth. On the other hand, excessive ON-resistance value causes high power loss and large voltage drops [41]. For low voltage operation, voltage drops can become serious problem, since it leads to avoid the transistors of the output stage remain in active region. Therefore, the aspect ratio of the switching transistors should be large enough so that the amplifier operates properly. In the proposed design, minimum channel length that the technology allows is used to minimize the effect of the parasitic capacitance. The purpose of the switching transistors controlling the compensation capacitor value is to keep the phase margin 55° against varying output current.

$M_{12}, M_{14}, M_{16}, M_{18}$ are the biasing transistors to source the current into the output stage. The aspect ratios of the biasing transistors are set as binary weighted. With that configuration, 2^N-1 current level can be obtained by using N transistors. Transistor sizing of the output stage of the reference buffer is listed in Table 3.1.

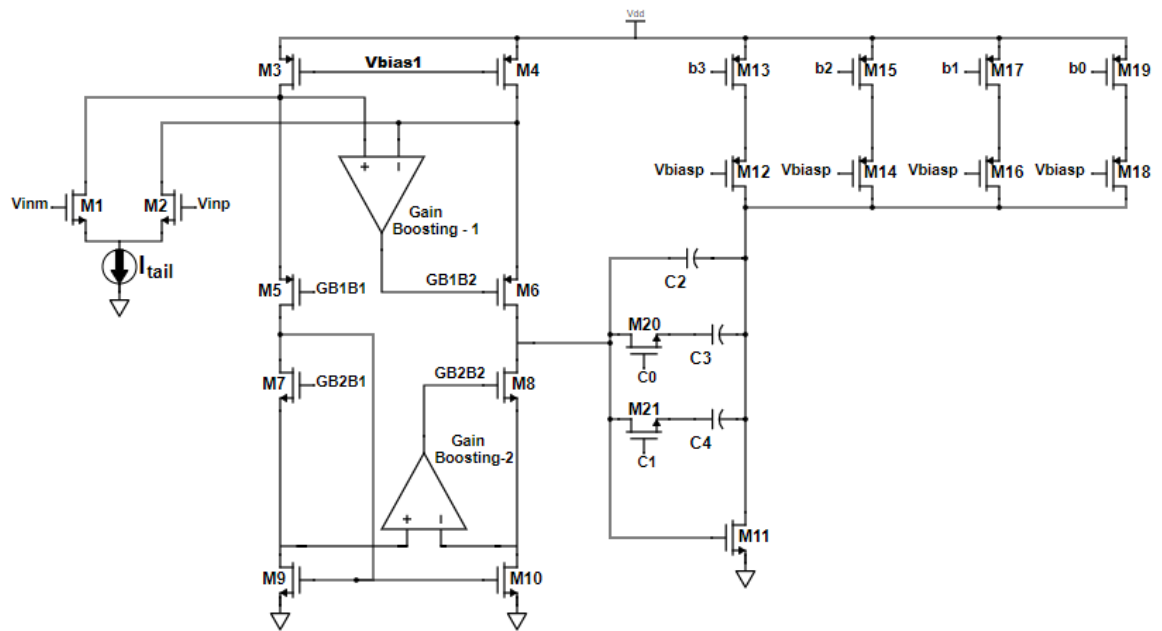


Figure 3.2. Reference Buffer Amplifier.

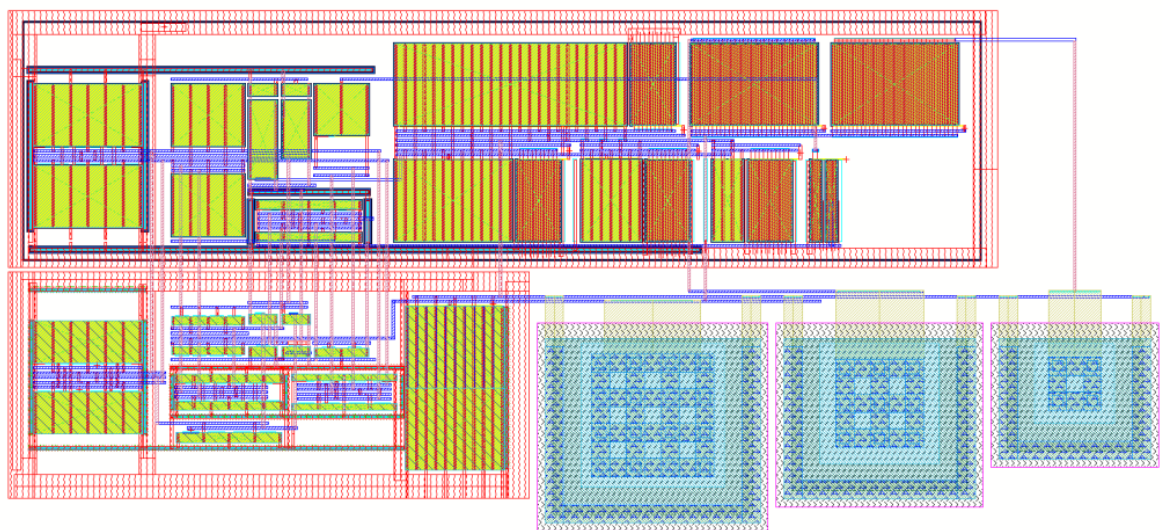


Figure 3.3. Layout of the Reference Buffer.

Table 3.1. Transistor sizing of the output stage of the reference buffer.

	TOTAL WIDTH	LENGTH
$M_{13}, M_{15}, M_{17}, M_{19}$	$200 \mu m$	$0.06 \mu m$
M_{20}, M_{21}	$600 \mu m$	$0.06 \mu m$
M_{11}	$200 \mu m$	$1 \mu m$
M_{12}	$240 \mu m$	$1 \mu m$
M_{14}	$120 \mu m$	$1 \mu m$
M_{16}	$60 \mu m$	$1 \mu m$
M_{18}	$30 \mu m$	$1 \mu m$

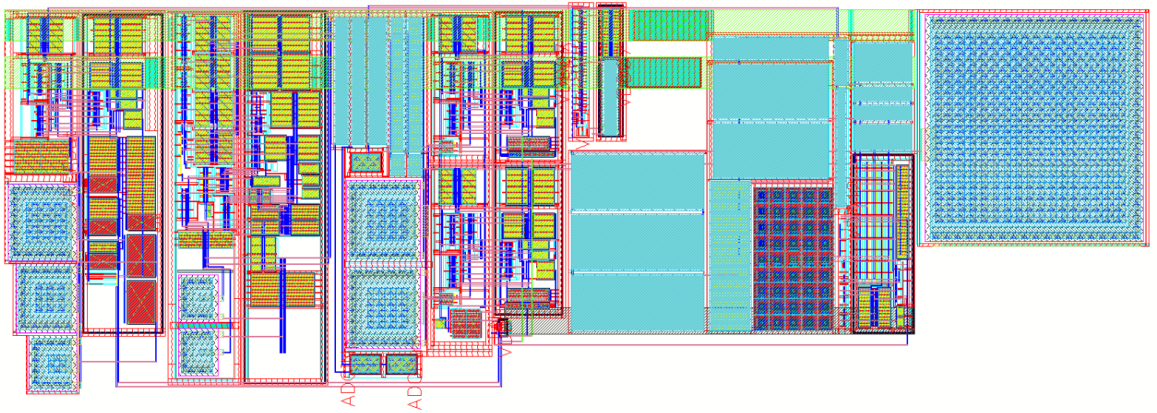


Figure 3.4. Layout of the Input and Reference Driver.

4. SIMULATION RESULTS

4.1. Post Layout Simulation Results of the Input Driver

Figure 4.1 shows that the output voltage of the temperature sensor as the temperature sweeps from -40°C to 125°C . As shown in Figure 4.1, the output voltage varies between 488.24 mV to 629.67 mV. The purpose of the input driver is to obtain the differential output voltage by scaling the full scale range of the temperature sensor with desired output common mode voltage.

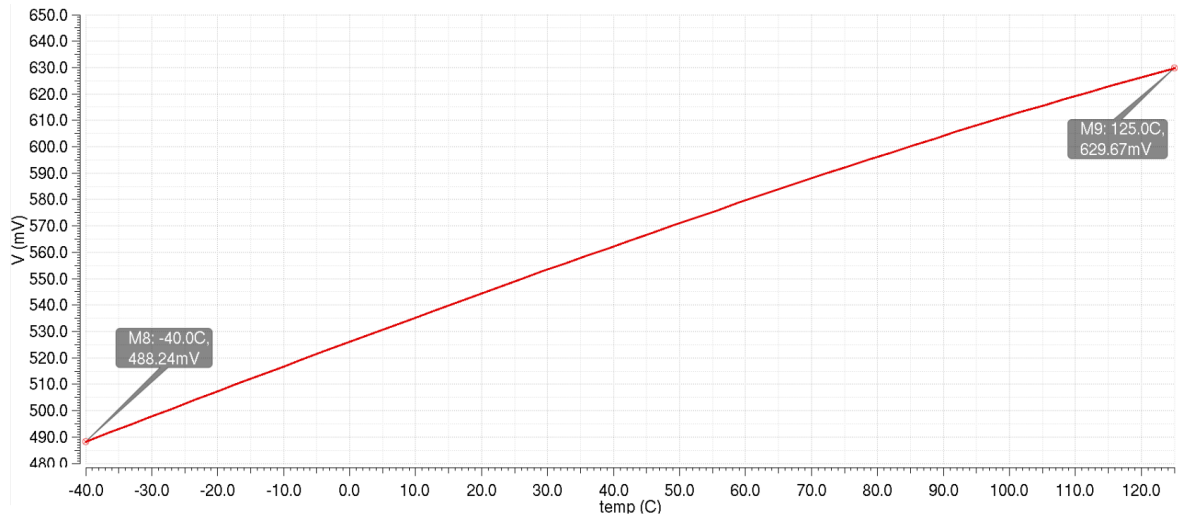


Figure 4.1. Output Voltage Characteristic of the Temperature Sensor.

Figure 4.2 shows that positive and negative output terminal voltage of the input driver through the specified temperature range. At the same time, these voltage values are the input voltages of the SAR ADC. Each input of the SAR ADC operates between 100 mV and 600 mV. As shown in Figure 4.2, the each output voltage of the input driver is within the specified input range of the SAR ADC.

Differential output voltage of the input driver is calculated by subtracting the positive output node voltage from the negative output node voltage. The differential

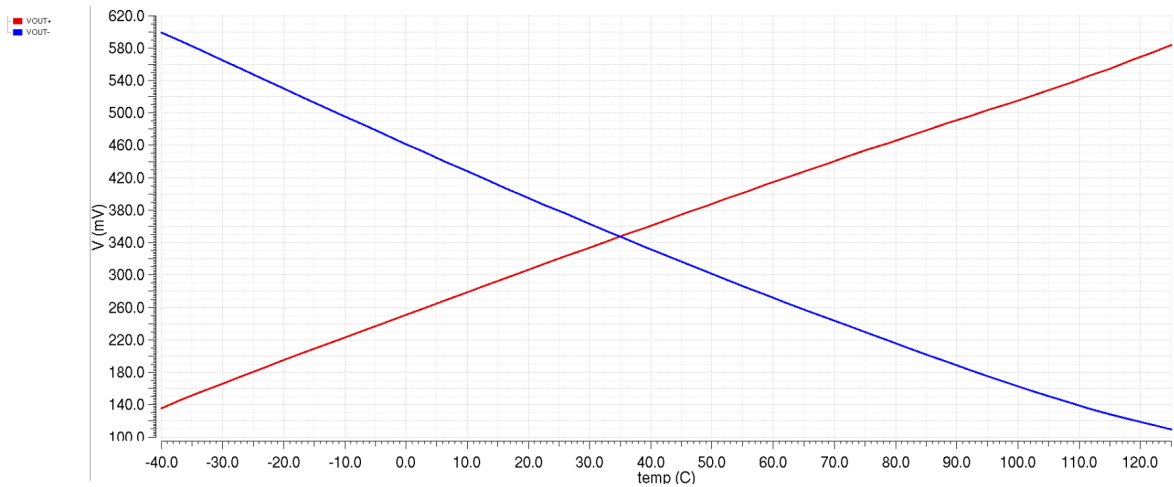
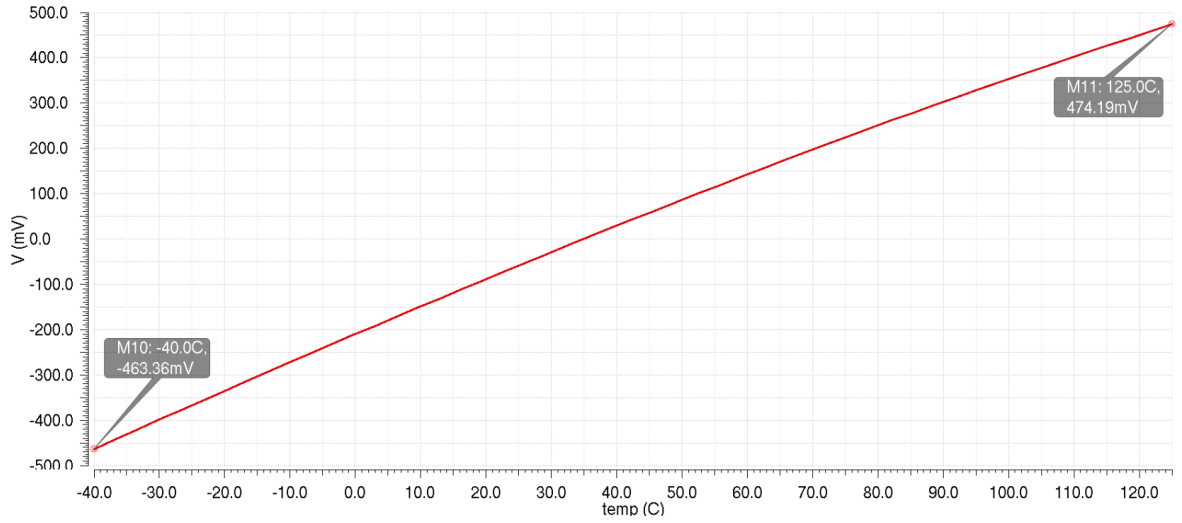


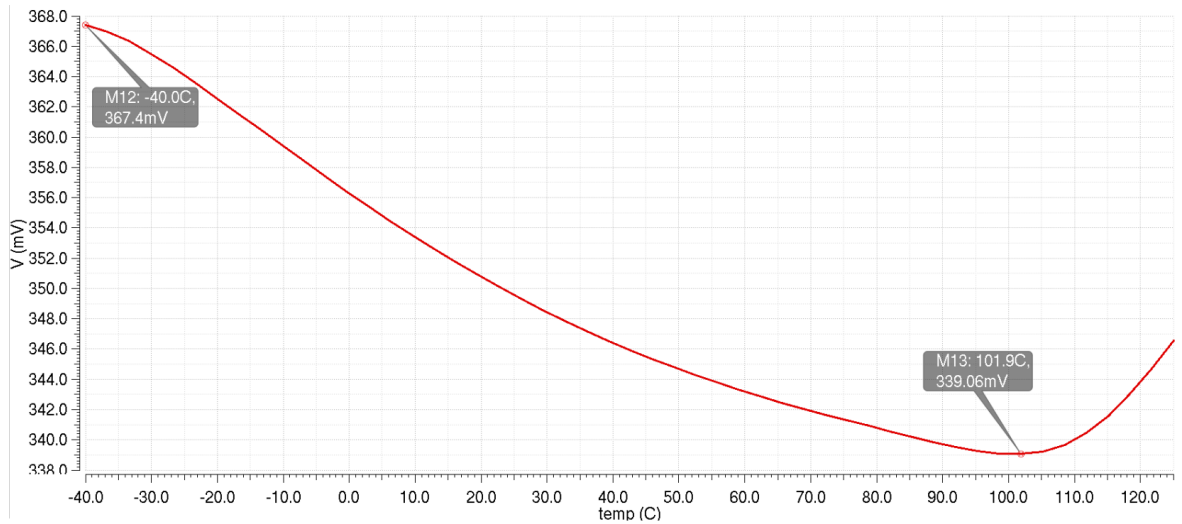
Figure 4.2. Positive and Negative Output Voltage of the Input Driver.

input voltage operating range of the SAR ADC is from -500 mV to 500 mV. Differential mode response of the proposed input driver swings from -463.36 mV to 474.19 mV as shown in Figure 4.3a. Ideally, absolute value of the maximum and minimum differential output voltage is expected to be equal. This asymmetry result from the non-linearity in temperature sensor, voltage variations of the bandgap reference circuit and the varied DC gain of the amplifiers over temperature range. Temperature sensor and bandgap reference design are not included in the input driver design. However, the same voltage buffers would be used to improve the symmetry at the expense of increased power consumption.

Figure 4.3b shows that common mode response of the input driver. Output common mode voltage represents the average of the positive and negative outputs at corresponding temperature point. The SAR ADC works at the input common mode voltage of 350 mV in optimum performance. However, the output common mode voltage of the input driver varies between 339.06 mV and 367.40 mV through operating temperature range. Simulation tests of the SAR ADC show that these variations are acceptable to its proper operation. To reduce the variation of the common mode response of the input driver, CMFB circuit performance must be improved by increasing its biasing current. Hence, this leads to consume much more power.



(a) Differential Mode Response of the Input Driver.

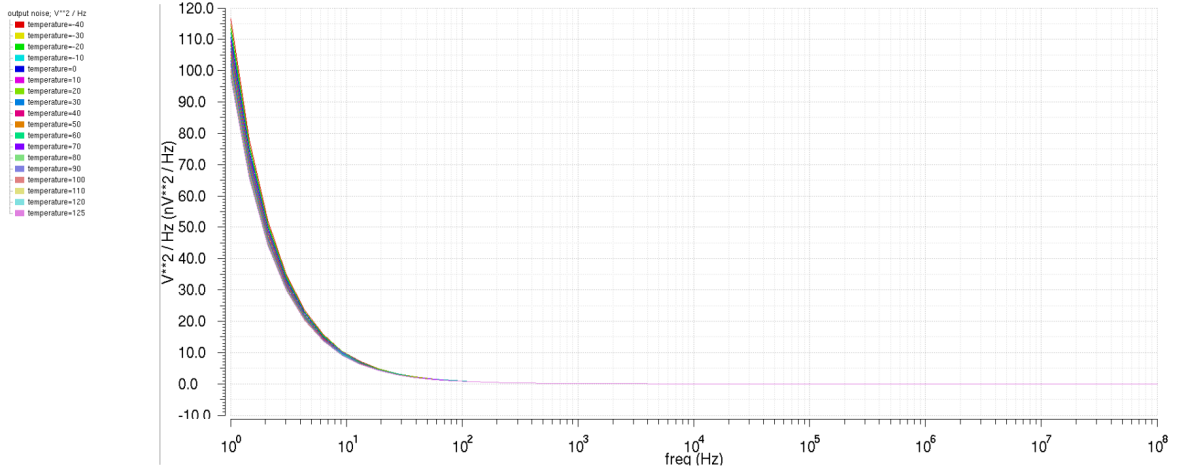


(b) Common Mode Response of the Input Driver.

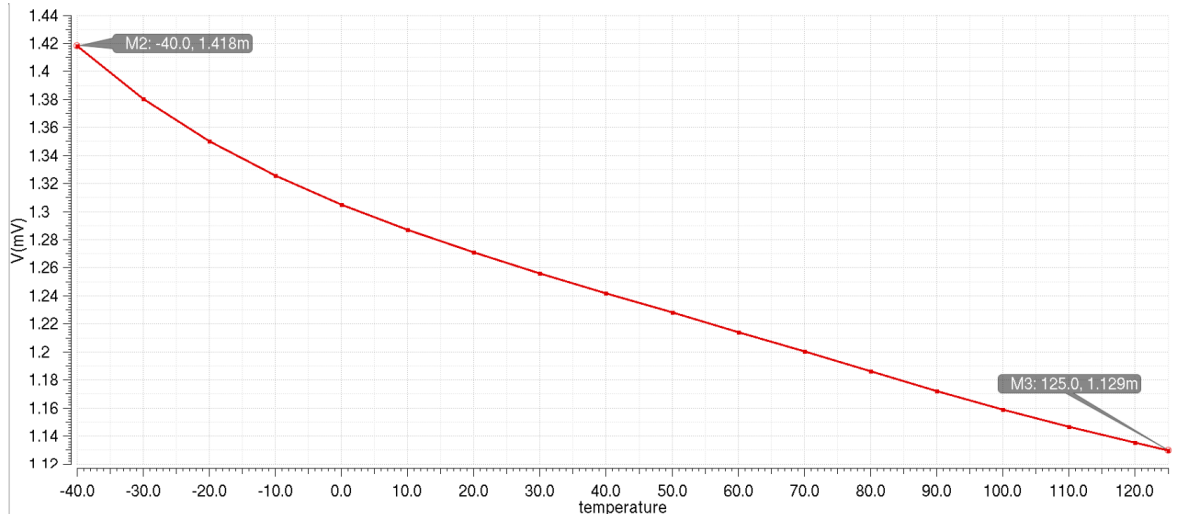
Figure 4.3. Differential Mode Response of the Input Driver and Common Mode Response of the Input Driver.

Noise performance of the input driver directly affects the resolution of the SAR ADC. The total output noise criterion is determined as being less than $\frac{1}{2}$ LSB to avoid lower resolution rather than it is expected. Figure 4.4a shows that the noise power spectral density for the output noise voltage at various temperature values. To obtain the total output noise, the integral of the noise power over all frequencies must be square rooted. The total output noise over temperature range is shown in Figure 4.4b. According to Figure 4.4b, the total output noise decreases as the temperature

increases. This results from the larger current consumption at higher temperature values and the larger current consumption improves the noise performance. The worst noise performance of the input driver is observed at $-40\text{ }^{\circ}\text{C}$ which has a value of 1.42 mV . This value is the less than the voltage value of $\frac{1}{2}\text{ LSB}$ and the noise performance of the input driver is suited for the operation of the 8 bit SAR ADC.



(a) Noise Power Spectral Density.



(b) Total Output Noise.

Figure 4.4. Noise Power Spectral Density and Total Output Noise.

Instead of the temperature sensor, ideal sinusoidal signal is applied as an input voltage to calculate the THD performance of the input driver. Peak-to-peak and DC voltage of the sine wave is chosen as full scale and common mode input voltage of

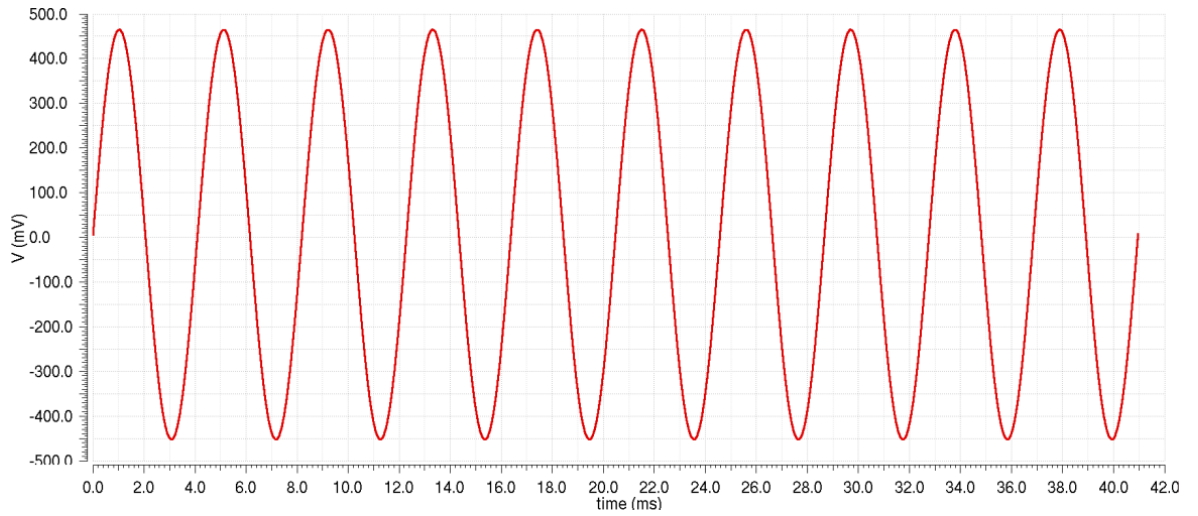
the temperature sensor, respectively. Several FFT analysis is performed with different sample counts and input frequencies. Sample frequency is set 100 KHz which is the sampling rate of the SAR ADC. For an accurate measurement, transient simulation time is chosen as ten periods of the sinusoidal input signal. The end frequency of FFT is the Nyquist frequency of the SAR ADC which is 50 KHz.

For 4096 point FFT, the required simulation time is at least 40.96 ms since one sample is taken per 10 μ s. Sample time is multiplied by the sample count and required minimum simulation time is obtained. The input frequency is set to 244.16025 Hz to obtain exact ten cycles of the input sine wave.

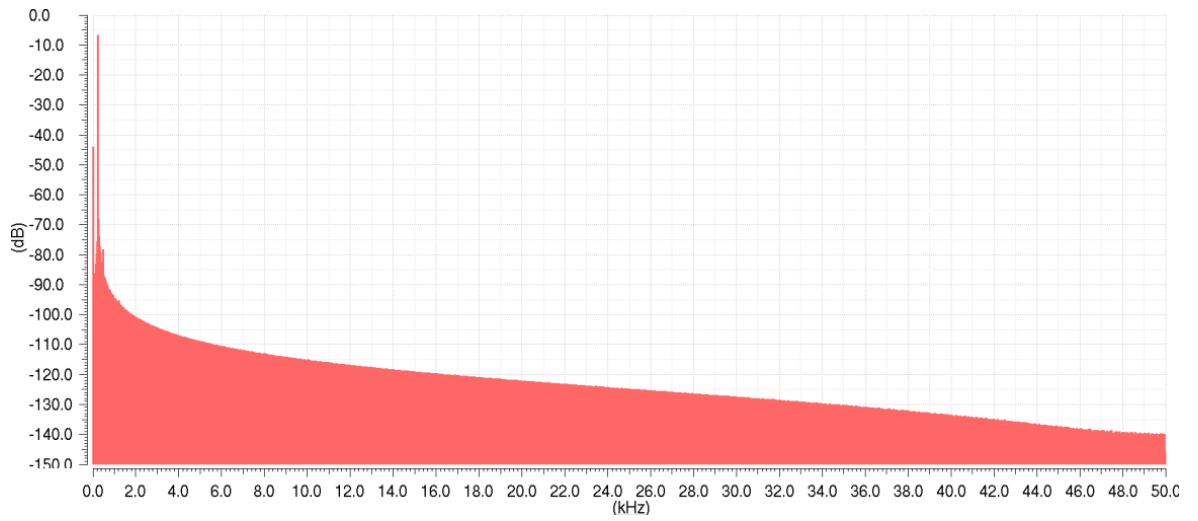
Figure 4.5 shows that the waveform of the differential output voltage and the FFT spectrum. The input driver has a THD of -72.51 dB with that input signal.

For 2048 point FFT, the required simulation time is at least 20.48 ms and the input frequency is set to 488.28125 Hz. Figure 4.6 shows that the waveform of the differential output voltage and the FFT spectrum. The input driver has a THD of -72.15 dB with that input signal.

For 1024 point FFT, the required simulation time is at least 10.24 ms and the input frequency is set to 976.5625 Hz. Figure 4.7 shows that the waveform of the differential output voltage and the FFT spectrum. The input driver has a THD of -70.88 dB with that input signal.

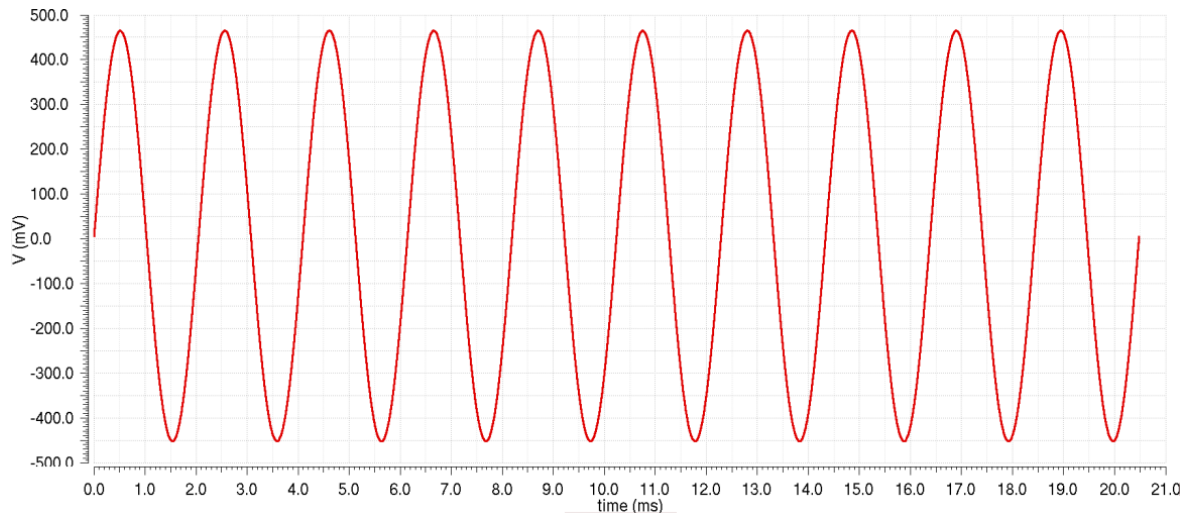


(a) Differential Output Voltage.

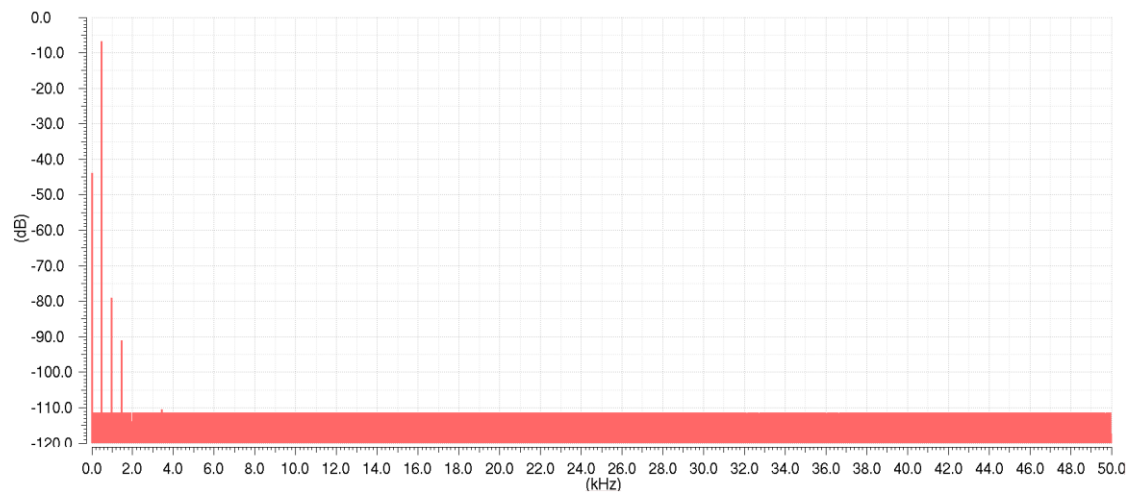


(b) 4096 Point FFT with Input Frequency of 244.16025 Hz.

Figure 4.5. Differential Output Voltage and 4096 Point FFT with Input Frequency of 244.16025 Hz.

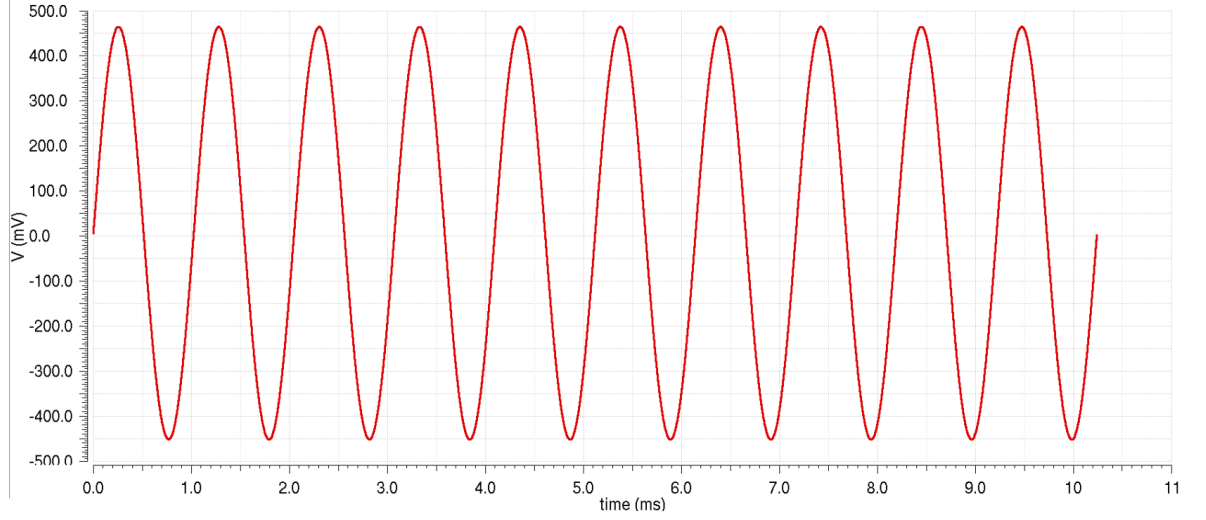


(a) Differential Output Voltage.

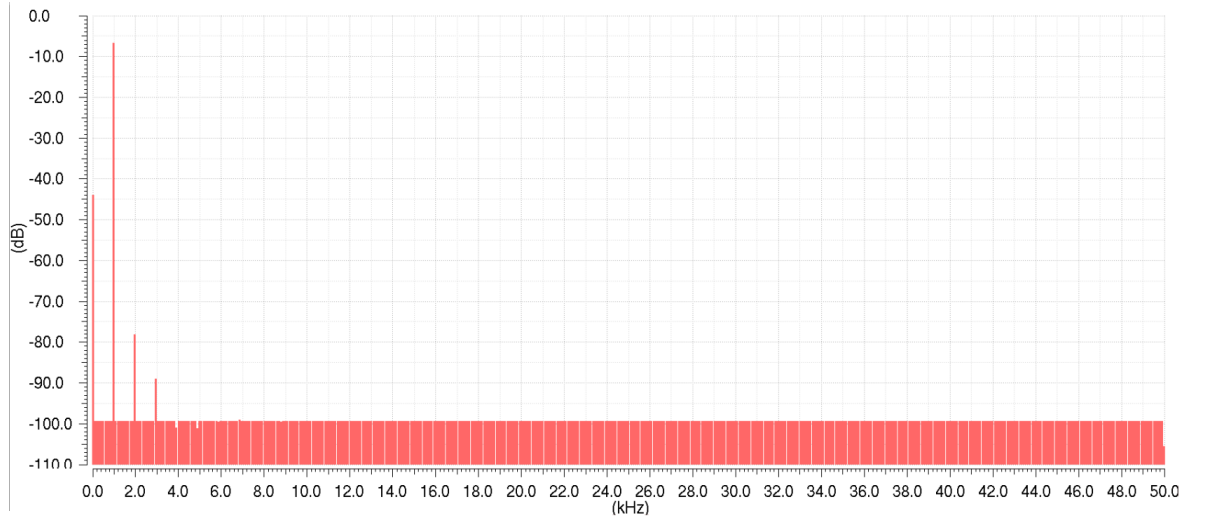


(b) 2048 Point FFT with Input Frequency of 488.28125 Hz .

Figure 4.6. Differential Output Voltage and 2048 Point FFT with Input Frequency of 488.28125 Hz.



(a) Differential Output Voltage.



(b) 1024 Point FFT with Input Frequency of 976.5625 Hz .

Figure 4.7. Differential Output Voltage and 1024 Point FFT with Input Frequency of 976.5625 Hz.

Ultra low power consumption is the most important design motivation of the input driver. Figure 4.8 shows that the current consumption of the sub-blocks such as the voltage buffer for common mode input voltage, the voltage buffer for the temperature sensor and the fully differential amplifier in the input driver. Average current-power consumption is listed in Table 4.1. Total current consumption is $159.33 \mu\text{A}$ and total power consumption is $111.53 \mu\text{W}$.

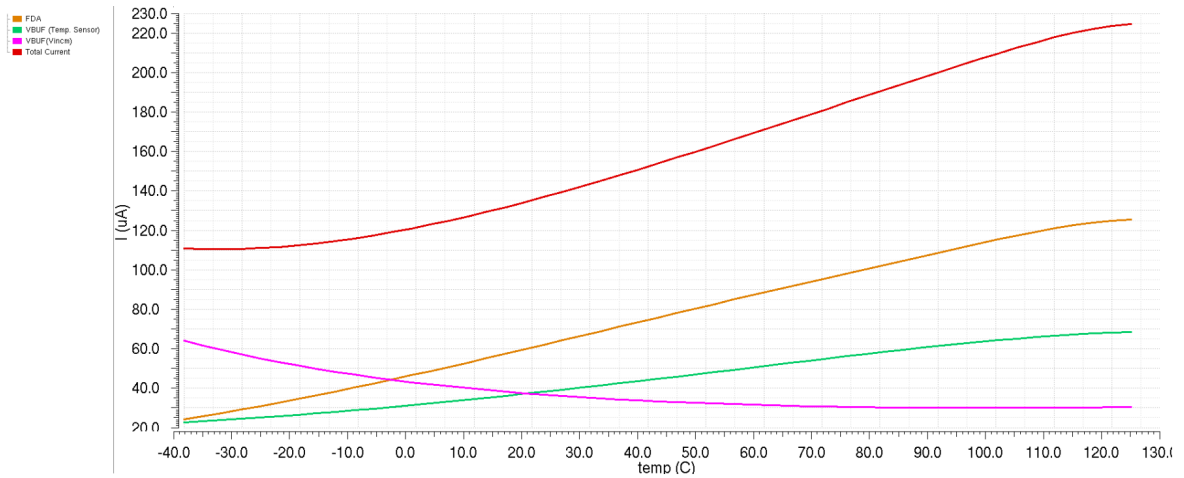


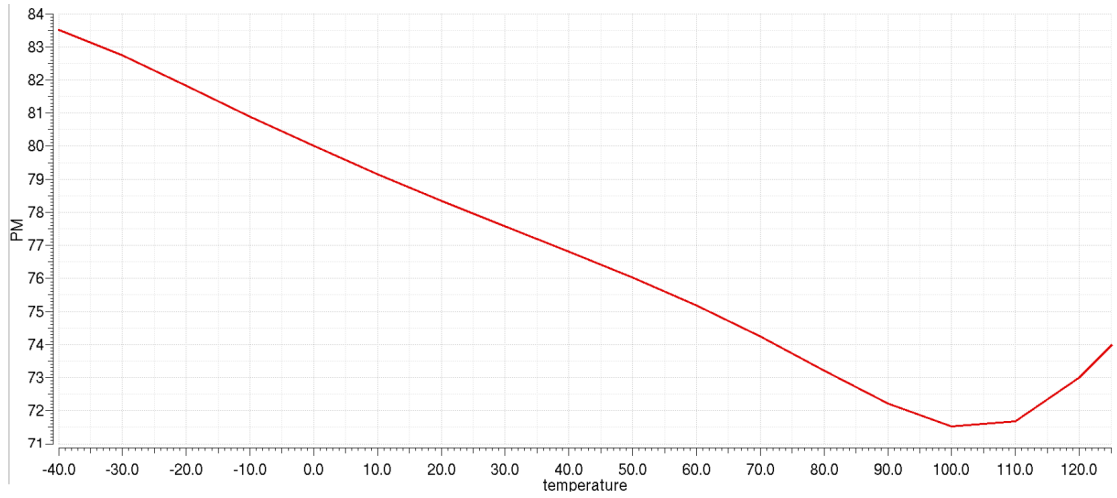
Figure 4.8. Current Consumption of the Sub-Blocks in the Input Driver and Total Current Consumption.

Table 4.1. Current-Power Consumption of the Proposed Input Driver.

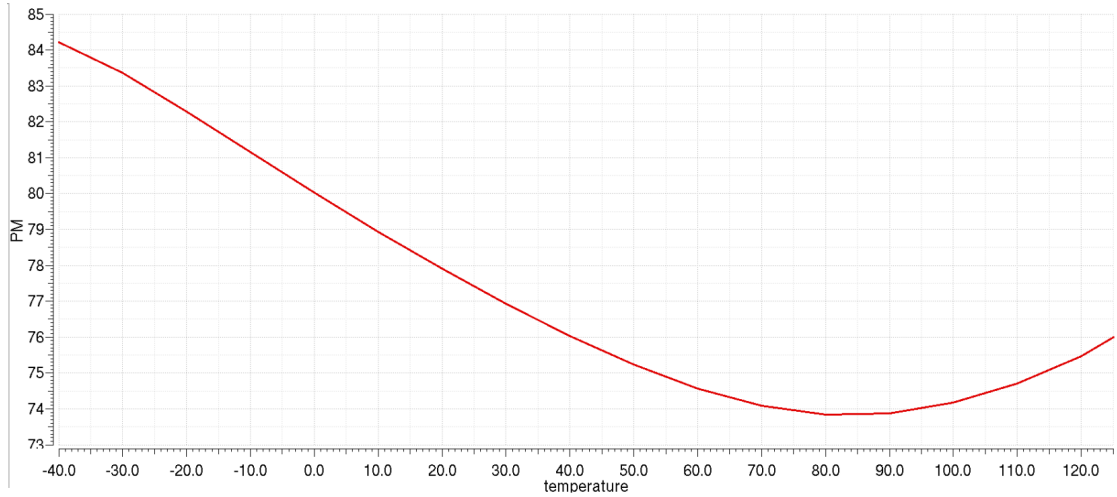
	I_{avg}	P_{avg}
Voltage Buffer for V_{INCM}	$44.85 \mu A$	$31.39 \mu W$
Voltage Buffer for Temperature Sensor	$41.58 \mu A$	$29.11 \mu W$
Fully Differential Amplifier	$72.90 \mu A$	$51.03 \mu W$
TOTAL	$159.33 \mu A$	$111.53 \mu W$

Closed loop stability must be maintained to avoid the oscillation of the system. For each amplifier, their phase margin is measured at various temperature values by breaking the loop and placing a stability probe. Figure 4.9 shows that the phase margin of each amplifier through operating temperature range.

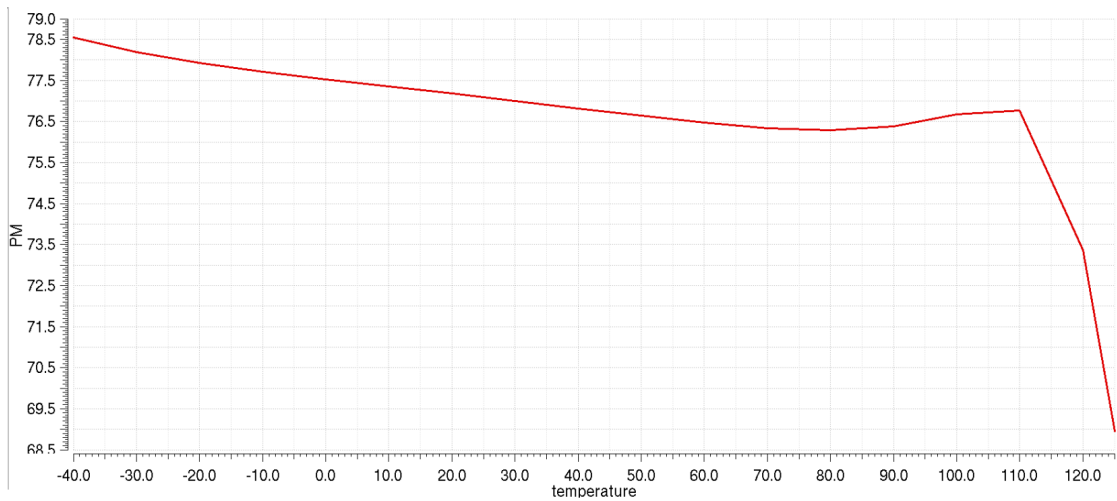
As a design specification, DC loop gain of the each amplifier should be larger than the quantization noise of 8 bit SAR ADC which equals to 49.92 dB. For the fully differential amplifier, DC loop gain falls below the quantization noise at 120°C. This critical temperature value is 122°C and 91°C for the voltage buffer of the temperature sensor and the input common mode voltage.



(a) Phase Margin of Fully Differential Amplifier .

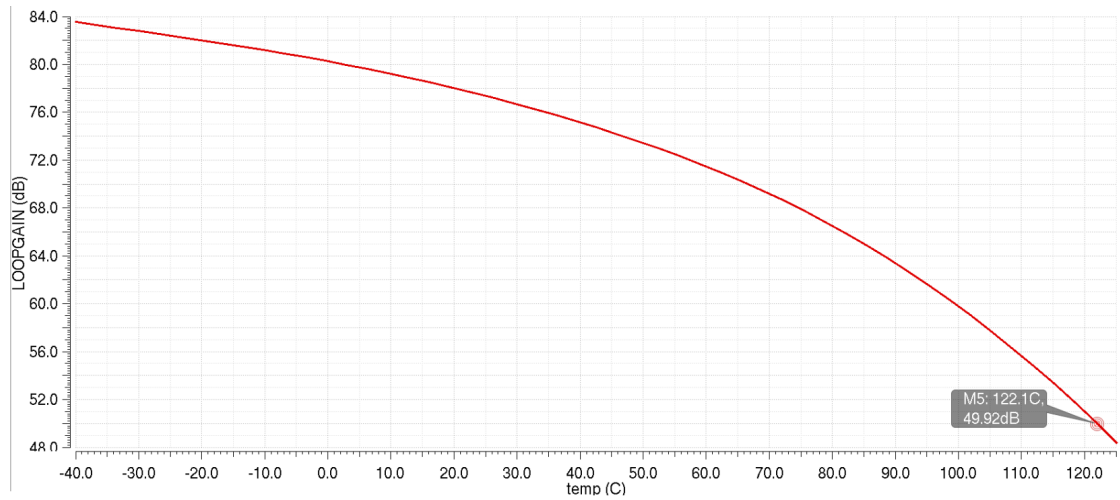


(b) Phase Margin of Voltage Buffer for Temperature Sensor.

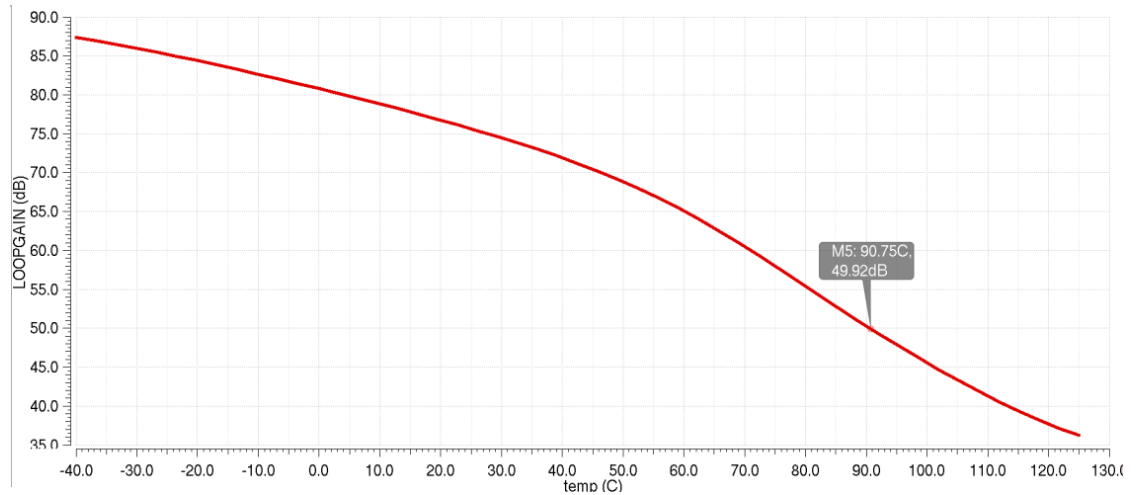


(c) Phase Margin of Voltage Buffer for Common Mode Input Voltage.

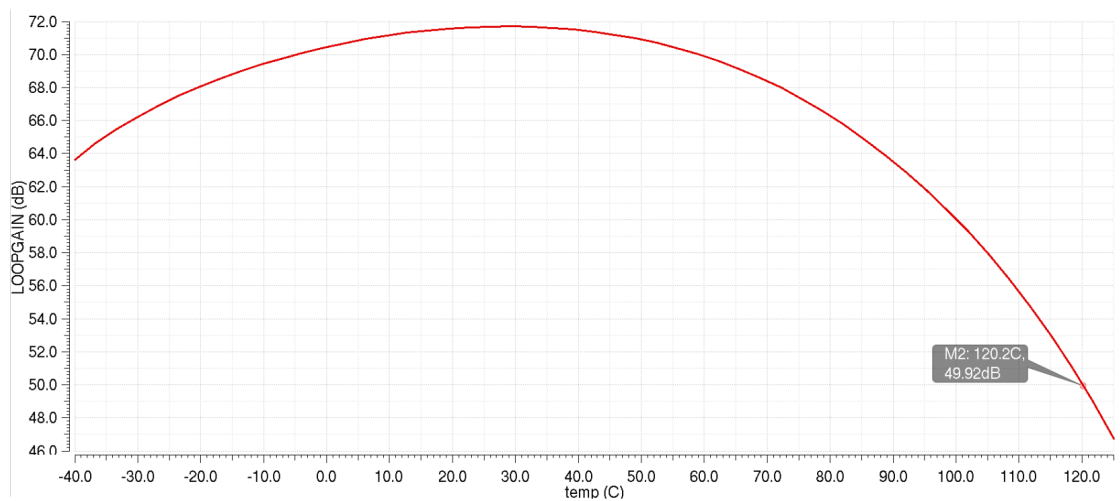
Figure 4.9. Phase Margin of Fully Differential Amplifier & Voltage Buffer for Temperature Sensor & Voltage Buffer for Common Mode Input Voltage.



(a) DC Loop Gain of Voltage Buffer for Temperature Sensor.



(b) DC Loop Gain of Voltage Buffer for Input Common Mode Voltage .



(c) DC Loop Gain of Fully Differential Amplifier.

Figure 4.10. DC Loop Gain of Voltage Buffer for Temperature Sensor& Voltage Buffer for Input Common Mode Voltage & Fully Differential Amplifier.

4.2. Post Layout Simulation Results of the Reference Driver

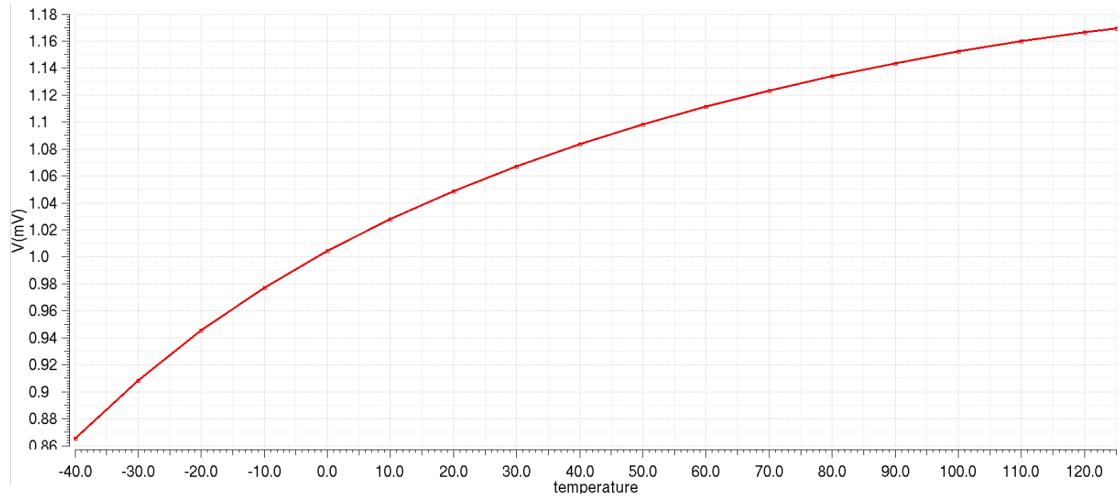
Table 4.2 provides a summary about the performance of the reference driver which includes the total current consumption, power consumption, settling time and phase margin. As shown in Table 4.2, the general trend is the faster settling time as the current-power consumption increases. Another deduction from the Table 4.2, is that overcompensation can lead to the slower settling time than it is expected.

Table 4.2. The Performance of the Reference Driver According to the Control Bits.

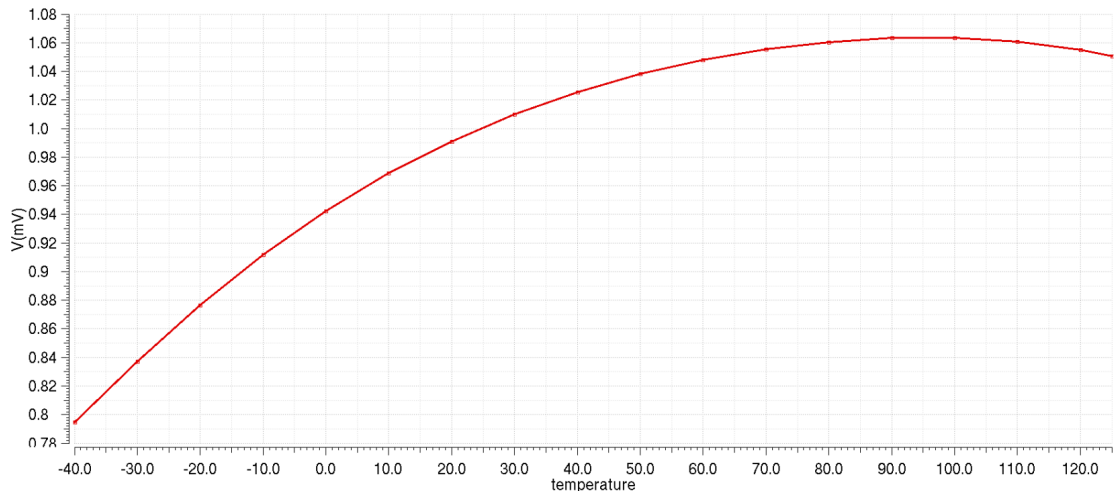
$b3$	$b2$	$b1$	$b0$	$c1$	$c0$	$I_{tot}(\mu A)$	$P(\mu W)$	$T_s(\mu S)$	$PM(^{\circ})$
0	0	0	0	1	1	104.35	73.045	0.716	58
0	0	0	1	1	1	98.45	68.915	0.748	58
0	0	1	0	1	1	92.47	64.729	0.775	58
0	0	1	1	1	1	86.56	60.592	0.8	57
0	1	0	0	1	1	80.55	56.385	0.833	57
0	1	0	1	1	1	74.64	52.248	0.853	56
0	1	1	0	1	1	68.64	48.048	0.875	56
0	1	1	1	1	0	62.71	43.897	1.235	60
1	0	0	0	1	0	57.07	39.949	1.295	59
1	0	0	1	1	0	51.15	35.805	1.314	58
1	0	1	0	1	0	45.15	31.605	1.176	56
1	0	1	1	0	1	39.22	27.454	1.574	59
1	1	0	0	0	1	33.2	23.24	1.429	56
1	1	0	1	0	0	27.26	19.082	1.702	53

Total output noise voltage should be less than $\frac{1}{2}$ LSB value as a design specification. Two extreme configurations which are the most current consuming and the least current consuming, are used to calculate the total output noise through the temperature range. Figure 4.11 shows that the total output noise of the reference driver for two extreme cases. For all temperature points, the total output noise is less than 1.96 mV which is the $\frac{1}{2}$ LSB of the SAR ADC.

There is no significant difference between the noise performances of the two cases since the noise performance is highly dominated by the input stage of the amplifier which is biased at lower current compared to the current of the output stage.



(a) 0000-11 ($b_3b_2b_1b_0 - c_1c_0$).



(b) 1101-00 ($b_3b_2b_1b_0 - c_1c_0$).

Figure 4.11. Total Output Noise Over the Temperature Range for Two Extreme Cases.

5. CONCLUSION

This thesis offers a driver circuit placed between 0.7 V supply ultra-low power temperature sensor and 0.7 V supply 8 bit SAR ADC. The main challenge of the design is the ultra-low power consumption by providing design specifications for 8 bit ADC operation through operating temperature range. The average power consumption over the temperature range is 111.53 μ W. THD results are -72.51 dB, -72.15 dB and -70.98 dB at 244.16025 Hz, 488.28125 Hz and 976.5625 Hz, respectively. Total output noise voltage equals to 1.418 mV at the -40°C which is the worst case. THD and noise performance of the input driver meet the specifications for 8 bit operation from -40°C to 125°C. The closed loop gain of the voltage buffer for input common mode voltage falls below the SNR value of 8 bit ADC from 91°C to 125°C. As a future work, the accuracy of the voltage buffer can be improved. Auto-zeroing and switched capacitor techniques can be utilized to design ultra-low power ADC driver and reduce low-frequency noise at the expense of complexity since these designs require clock generators. The proposed input driver architecture provides a simple design with low voltage and ultra-low power operation.

The proposed reference driver design offers a current controlled unity gain buffer. The user can change the current via control bits according to the design requirements such as settling time and power consumption. The proposed reference driver also controls the stability as the current varies.

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