DESIGN AND RADIATION ANALYSIS OF VARIOUS ANALOG TO DIGITAL CONVERTERS

by

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ABSTRACT

DESIGN AND RADIATION ANALYSIS OF VARIOUS ANALOG TO DIGITAL CONVERTERS

This study is on the schematic level design of various ADCs and their radiation analysis. In this context, ADCs with three different architectures, which are flash ADC, SAR ADC, and sigma-delta ADC, are designed and tested under temporary and permanent radiation effects.

The flash ADC is designed in Verilog-A, which is a modeling language for analog circuits, whereas SAR ADC and sigma-delta modulator are designed by utilizing transistors in 65nm CMOS technology. The designed ADCs are examined under the SET effect, which causes temporary effects on the circuit, and the TID effect, which causes permanent effects.

The designed flash ADC is examined only under the effect of TID, and the results of this effect are presented. For the SAR ADC, designs are made using two different capacitive DAC topologies to be able to compare with each other. These SAR ADCs are examined under the effects of TID and SET separately, and the results are explained. As a result of SET simulations of ADCs, the radiation performances of the designed ADCs are compared, and the sensitive nodes of the DACs are determined. In the sigma-delta ADC part, a first-order modulator is designed and investigated under the effects of TID and SET. In addition to the presented results, the sensitive nodes of the integrator are determined, and various inferences are made.

ÖZET

ÇEŞİTLİ ANALOG-DİJİTAL DÖNÜŞTÜRÜCÜLERİN TASARIMI VE RADYASYON ANALİZİ

Bu çalışma, çeşitli analog-dijital dönüştürücülerin şematik düzeyde tasarımı ve radyasyon analizi üzerinedir. Bu bağlamda paralel karşılaştırıcı (flash), ardışık yaklaşım (SAR) ve sigma-delta tipi olmak üzere üç farklı mimaride analog-djital dönüştürücüler tasarlanıp geçici ve kalıcı radyasyon etkisi altında test edilmiştir.

Paralel karşılaştırıcı tipi dönüştürücü, analog devreler için bir modelleme dili olan Verilog-A ile tasarlanırken ardışık yaklaşım ve sigma-delta tipi dönüştürücüler 65nm CMOS teknolojisinde transistörler ile tasarlanmıştır. Tasarlanan dönüştürücüler devrede geçici etki yaratan SET tipi ve kalıcı etki yaratan TID tipi radyasyon etkileri altında incelenmiştir.

Tasarlanan paralel karşılaştırıcı tipi dönüştürücü yalnızca TID etkisi altında incelenmiş olup bu etkinin yarattığı sonuçlar sunulmuştur. Ardışık yaklaşım tipi için ise birbirleriyle karşılaştırma yapabilmek adına iki farklı kapasitif dijital-analog dönüştürücü topolojisi kullanılarak tasarımlar yapılmıştır. Bu ardışık yaklaşım tipi analog-dijital dönüştürücüler ayrı ayrı TID ve SET etkileri altında incelenip elde edilen sonuçlar açıklanmıştır. Analog-dijital dönüştürücülerin SET simülasyonlarının sonucunda, incelenen iki analog-dijital dönüştürücünün radyasyon performansları karşılaştırılıp dijital-analog dönüştürücülerin hassas düğümleri belirlenmiştir. Sigma-delta dönüştürücü kısmında ise birinci dereceden bir modülatör tasarlanarak TID ve SET etkileri altında incelenmiştir. Sunulan sonuçların yanı sıra modülatör içerisindeki entegratörün hassas düğümleri belirlenmiş ve çeşitli çıkarımlar yapılmıştır.

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LIST OF SYMBOLS

C_u	Unit Capacitance Value
dB	Decibel
f_B	Signal Bandwith
f_s	Sampling Frequency
P_{noise}	Noise Power
P_{signal}	Signal Power
SiO_2	Silicon Dioxide
V_{CM}	Common-Mode Voltage
V_{DD}	Supply Voltage
V_{in}	Input Voltage
V_{out}	Output Voltage
V_{ref}	Reference Voltage
Φ	Clocks
σ	Standard Deviation

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ADC	Analog-to-Digital Converter
BiCMOS	Bipolar Complementary Metal–Oxide–Semiconductor
BPTM	Berkeley Predictive Technology Model
CDS	Correlated Double Sampling
CMFB	Common-Mode Feedback
CMOS	Complementary Metal–Oxide–Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
DDD	Displacement Damage Dose
DFF	D Flip-Flop
DNL	Differential Nonlinearity
ENOB	Effective Number of Bits
FSR	Full-Scale Range
INL	Integral Nonlinearity
LET	Linear Energy Transfer
LSB	Least Significant Bit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
NMOS	N-type Metal-Oxide-Semiconductor
OPAMP	Operational Amplifier
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PMOS	P-type Metal-Oxide-Semiconductor
PSD	Power Spectral Density
SAR	Successive Approximation Register
SEB	Single Event Burnout
SEE	Single Event Effect

SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SEHE	Single Event Hard Errors
SEL	Single Event Latch-up
SES/SESB	Single Event Snapback
SET	Single Event Transient
SEU	Single Event Upset
SNR	Signal to Noise Ratio
TID	Total Ionizing Dose
VCVS	Voltage Controlled Voltage Source

1. INTRODUCTION

Electronic equipment has become an indispensable part of life with the advancement of technology. At the core of many electronic applications is the analog-to-digital converter (ADC) that serves as a bridge between the analog and the digital electronic world [1]. In other words, it is an irreplaceable component in introducing real-world signals to equipment used in electronic applications. There are various ADC architecture types used depending on the features required by the application, such as resolution and speed.

Some recent studies on ADCs are being done intended for space applications. It is one of the most critical components in space electronics since it converts the data coming from external sensors into digital form. This allows us to check the condition of the spacecraft in terms of pressure, temperature, and health of the operation during mission-critical operations from a huge distance. In this way, it enables scientific research in space to make progress smoothly. However, the conditions on Earth and space are quite different from many perspectives. The main reasons that make space a harsh environment are cryogenic temperatures and high radiation.

The temperature in the space environment can decrease to a few Kelvin, which affects the operation of an ADC. An ADC designed for operation at room temperature cannot work as expected under cryogenic temperatures. There are several studies in literature [2–5] that investigate the effects of cryogenic temperatures on complementary metal–oxide–semiconductor (CMOS) circuits. According to these studies, leakage decreases in cryogenic temperatures. Also, the threshold voltage of an n-type metal-oxide-semiconductor (NMOS) transistor increases as a result of an increase in the mobility of charge carriers with a decrease in temperature. Through the studies in this area, it is proven that the freezing cold affects the CMOS circuits.

Radiation affects the circuit behavior, like the ambient temperatures. Radiation effects are classified as long-term, which are permanent, and short-term, which may be temporary or permanent. Long-term effects are caused by cumulative doses of radiation, whereas short-term effects are caused by a single event. One of the most known long-term effects is total ionizing dose (TID), which causes permanent changes, such as a shift in threshold voltage and an increase in leakage current [6], on CMOS transistors. These effects are observed on CMOS transistors due to the accumulated trapped charges at the gate oxide layer, which is due to radiation, as time goes on. On the other hand, the short-term effects are located under the single event effects (SEEs) main topic. There are various effects, which are temporary or permanent, under this topic. One of the most discussed temporary effects is single event transient (SET), which causes instantaneous changes in circuits such as glitches and random bit flips [7]. Circuits are affected in this manner since a particle hits a node in the circuit and causes an increase in charge at the hit area, which results in the occurrence of a response current in this region. Many studies have been done on radiation effects on ADCs [8–13] to clarify possible errors. Some of the studies involve testing with real-life setups, the others focus on SPICE simulations of the ADCs. The real-life experiments present more accurate results, but it is hard to apply radiation to blocks in the ADCs individually. SPICE simulations are cheaper, and they can present adequate information for use in radiation-hardened circuit designs.

1.1. Thesis Organization

This thesis consists of the design and SPICE-based radiation analysis of various ADCs; flash ADC, SAR ADC, and first-order sigma-delta ADC. Radiation effects are examined on ADCs as temporary and permanent. SET is preferred for temporary effect, whereas TID is chosen for permanent effect. The thesis is organized as follows:

Chapter 2 provides preliminary information about a variety of ADC architectures, and radiation effects.

Chapter 3 consists of the design of the 4-bit flash ADC, and TID analysis of this circuit. The flash ADC is designed in Verilog-A, and the TID effect is modeled as input offset voltage for the comparators in the mentioned architecture.

Chapter 4 involves the transistor-level design and radiation analysis of two different 8-bit SAR ADCs; split capacitor array DAC and C-2C ladder-based DAC. The TID effect is mimicked by adding external input offset voltage for the comparator in the ADC, whereas the SET is applied to the nodes of the capacitive DACs at various times. The radiation performances of the designed SAR ADCs are compared, and the sensitive nodes in the DACs are determined according to the temporary radiation simulations.

Chapter 5 presents the transistor-level design and radiation analysis of the first-order sigma-delta modulator. An additional offset voltage is added to the comparator in the modulator to perform the TID simulation of the designed sigma-delta modulator. Also, the SET effect is tested on the nodes of the integrator in the modulator by applying it at various times and various durations. The critical nodes in the integrator are determined as a result of SET simulations. Also, it is presented that SET application time and SET event duration are important in the performance degradation of the ADC.

Chapter 6 finalizes the thesis and mentions possible future works to expand the study on radiation effects on ADCs.

2. BACKGROUND

2.1. Analog-to-Digital Converters (ADCs)

Analog-to-digital converter (ADC) is an electronic circuit that is utilized in transforming an analog signal into a digital signal. Sensors, such as temperature, pressure, displacement, etc., give analog output signals. These have to be converted into digital to be stored or processed. ADCs are essential components for this purpose because analog signal values are represented by output codes, which consist of binary numbers, that are determined by ADC.

There are several types of ADCs, but they are grouped into two different categories in terms of operation; Nyquist rate ADCs and oversampling ADCs. This classification is made according to the oversampling ratio (OSR) of the ADC. OSR is defined by considering the Nyquist limit ($f_s/2$) and the signal band (f_B). The definition of oversampling ratio is provided as

$$OSR = \frac{fs}{2f_B}. \tag{2.1}$$

In Nyquist rate ADCs, the analog input signal is sampled at a frequency close to the Nyquist limit. To be able to name an ADC as Nyquist rate, the OSR is chosen generally less than 8 [1]. On the other hand, the OSR is chosen greater than 8 for the oversampling ADCs.

The difference between the working principles of the Nyquist rate and oversampling ADCs can be seen in Figure 2.1. In Nyquist rate ADCs, the signal and the noise squeeze into a region due to the OSR being limited. On the other hand, the sampling rate of oversampling ADCs' is higher than the Nyquist frequency. In this way, the signal exists in a small region in the Nyquist interval, but the noise spreads over the interval by using the oversampling technique as shown in Figure 2.1. In this way, a considerable part of the quantization noise stays out of the signal bandwidth. Then, the noise beyond the bandwidth is filtered by a digital filter. Therefore, the resolution

of the oversampling ADC is better since the noise power is less in the signal region compared to the Nyquist rate ADCs [1, 14, 15]. This is due to the signal to noise ratio (SNR) formula. The formula is expressed as

$$SNR_{dB} = 10log_{10}(\frac{P_{signal}}{P_{noise}}), \tag{2.2}$$

where P_{signal} is signal power and P_{noise} is noise power.

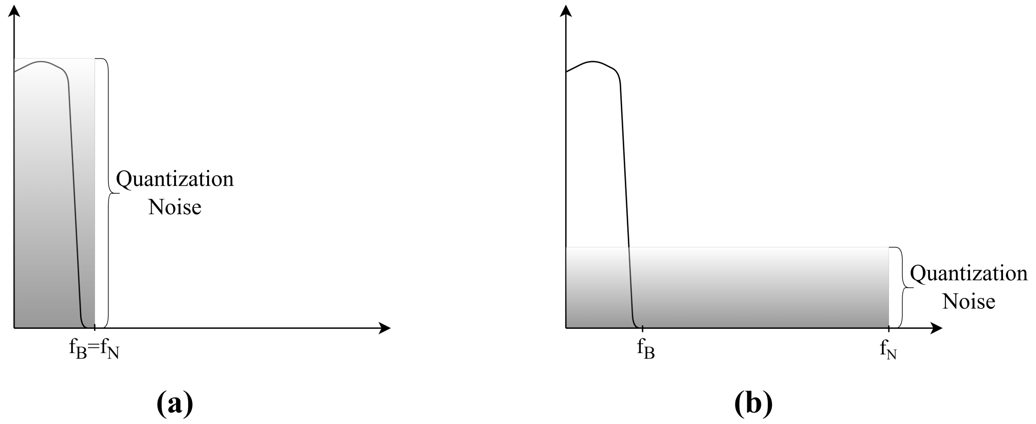

Figure 2.1. The comparison between operations of Nyquist rate ADCs and oversampling ADCs; (a)Nyquist rate ADC, (b)oversampling ADC.

There are several types of Nyquist rate ADCs, such as flash ADC, pipelined ADC, successive approximation register (SAR) ADC, etc. On the other hand, the most popular oversampling ADC type is sigma-delta ADC. These ADCs have two main restrictions; resolution and sampling rate. Resolution is defined as the change of the digital output with respect to the change of the analog input signal. If an ADC has a high resolution, the output code changes in return for a small change in analog input signal. Also, the sampling rate determines the conversion speed of an ADC. There is a trade off between sampling rate and resolution [16] as shown in Figure 2.2. The fastest conversion is done by flash ADC, but its resolution is limited. On the other hand, the most sensitive results are taken by sigma-delta ADC. In other words, more accurate results are obtained using this architecture, but it is slower.

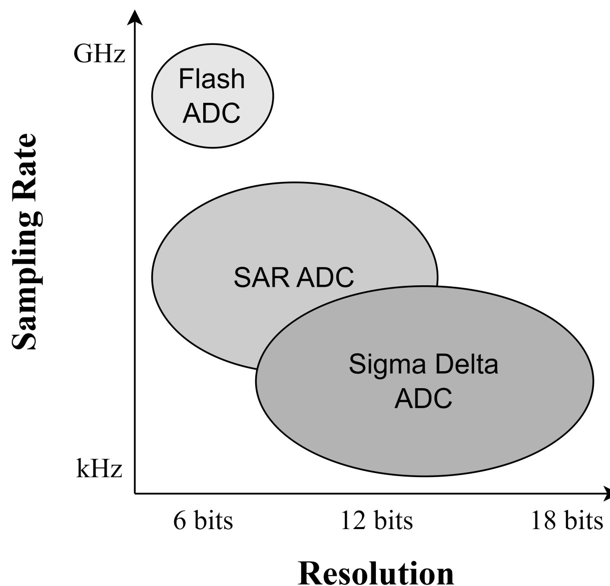

Figure 2.2. The resolution and sampling rate comparison between ADCs.

2.2. Radiation Effects

Radiation is defined as high energy that is emitted from a source in a form of a particle or wave. There are different types of particle radiation; alpha, beta, and neutron. An alpha particle, which has a positive charge, consists of protons and neutrons. A beta particle is an electron with high energy, whereas a neutron particle is an uncharged particle. It has been proven that high doses of radiation threaten human life. However, this high energy may harm non-living things as much as living creatures. Electronic devices are heavily affected by radiation. Radiation effects on electronic circuits can be examined from two different perspectives: cumulative effects and single event effects (SEEs). Cumulative effects are long-term, which are permanent effects. There are two types of cumulative effects; total ionizing dose (TID) and displacement damage dose (DDD). On the other hand, SEEs are short-term effects that may be either permanent, called hard errors, or temporary, called soft errors. SEEs are caused by a single energetic particle hit on the circuits. SEEs are classified under two subheadings; soft errors and hard errors, as shown in Figure 2.3.

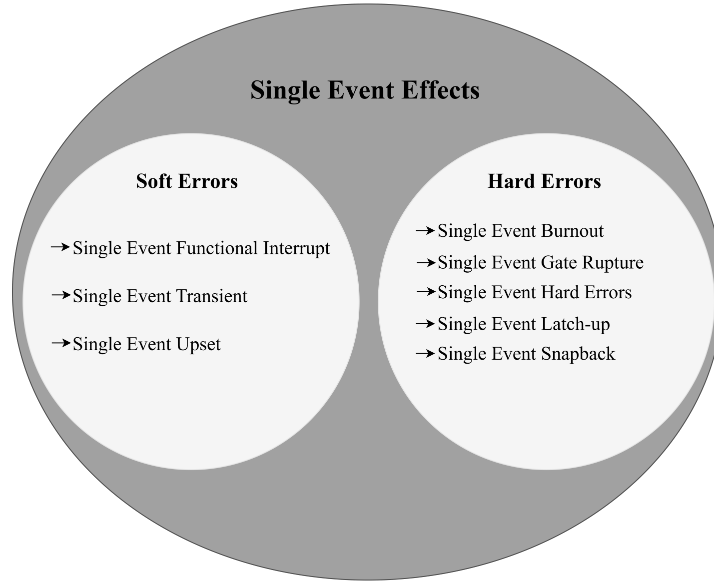

Figure 2.3. Single event effects types.

(i) Cumulative Effects
- Total Ionizing Dose (TID): It is a cumulative effect of radiation in which free charges due to ionizing radiation are trapped in the device and cause permanent changes.
- Displacement Damage Dose (DDD): It is another cumulative effect of radiation in which energetic radiative particles dislocate the silicon lattice atom due to the collision [17]. As a result of this displacement, permanent defects are observed.

(ii) Single Event Effects
- Single Event Functional Interrupt (SEFI): It is a soft error that makes the exposed device nonfunctional for a certain time. It may induce the device to reset, lock up, etc [18].
- Single Event Transient (SET): It is a type of soft error that causes instantaneous changes in the circuit, such as random voltage glitches [7].
- Single Event Upset (SEU): It is a soft error that may end up with changing of the state of a circuit, such as bit flip in memory elements. This type of SEEs mainly affects memory circuits.

- Single Event Burnout (SEB): It is a hard error that is more effective on power transistors. When a particle is radiated to a power transistor, it creates a high current that induces devastating failure [19]. This may cause an unrecoverable error.
- Single Event Gate Rupture (SEGR): It is a hard error in which a crashing particle forms a conduction path in gate oxide (SiO_2) layer of a metal-oxide-semiconductor field-effect transistor (MOSFET) [20]. A leakage current flows through this created path. This current may end up with damage to the silicon substrate [21].
- Single Event Hard Errors (SEHE): It is a type of hard error that causes stuck bits in the storage elements due to a single energized particle [22].
- Single Event Latch-up (SEL): It is a hard error that causes a high current flow as a result of a hit energized particle. The latch-up may be thrown off by turning off the affected device [23]. Otherwise, the melting of the device is within the bounds of possibility. CMOS and bipolar complementary metal–oxide–semiconductor (BiCMOS) devices are more sensitive to this effect.
- Single Event Snapback (SES/SESB): It is a destructive error very similar to single event latch-up. It results in a high current generated by the radiation damaging the device, such as local heating [24]. However, the effect of radiation may be eliminated without powering down the device, contrary to single event latch-up.

Cumulative effects and SEEs are explained briefly, but the radiation effects are classified as permanent and temporary effects in this thesis. The chosen permanent and temporary effects (TID and SET) are explained in detail in the following subheadings.

2.2.1. Permanent Radiation Effect

The permanent radiation effect is discussed as total ionizing dose (TID), which is the result of cumulative doses of radiation, in this thesis. The TID can be explained in Figure 2.4, which involves an NMOS transistor whose gate is positively biased. Under normal conditions (without radiation), electrons move to the gate, whereas holes go to the substrate. However, when the radiation comes through the oxide (SiO_2) layer of the NMOS transistor, electron-hole pairs occur in SiO_2 layer [21, 25]. Some of these free charges recombine, but all of these charged particles cannot recombine due to the electric field, which causes electrons and holes to drift. Electrons travel towards the gate, which is positively biased, and holes move to the substrate. Electrons can escape from SiO_2 layer since the electron's mobility is higher than the hole's. On the other hand, only a part of the holes can reach the substrate by leaving SiO_2 layer. In other words, some of the charges are trapped at SiO_2 layer. Accumulation of these trapped charges causes permanent effects for the corresponding transistor, such as shifts in threshold voltage and increases in leakage current [6]. TID is more effective on continuous-time analog circuits [25]. The effect of TID is modeled on the comparators of the designed ADCs as offset voltage thanks to RadiSPICE [26], which is a simulation tool for space applications.

2.2.2. Temporary Radiation Effect

Temporary radiation effects are called soft errors. These are located under the single event effects (SEEs) category as shown in Figure 2.3. There are also hard errors that result in permanent damage to the circuit. However, the effect of soft errors on the circuit is examined in this thesis. There are three different processes in soft errors; charge generation, charge collection, and circuit response. All of these processes are shown in Figure 2.5. Charge generation means that a single high-energy particle hits the transistor and generates electron-hole pairs along its path, which is tracked until its energy is used up, as shown in Figure 2.5. The amount of expended energy is called linear energy transfer (LET). As a result of forming electron-hole pairs, a funnel occurs

[27]. Then, free charges start to move the node, where the particle hits, with the effect of drift and diffusion [28–30]. This process is called charge collection, which also includes recombinations. All of these processes cause a current at the affected node as a circuit response, as shown in Figure 2.5. It creates a temporary effect, or non-permanent effect, on an electronic circuit [31]. The digital and switched-capacitor circuits are more affected by SEEs [25, 32]. There are three categories under soft errors; single event upset (SEU), single event transient (SET), and single event functional interrupt (SEFI). The most knowns are SEU and SET. SEU has more effect on sequential logic circuits, whereas SET creates more dramatic results on combinational logic circuits [33]. As a result of the striking particle, SEU causes bit flips on the memory elements, while SET causes voltage glitches on the nodes of a circuit that occur randomly [7], as shown in Figure 2.6. The circuit in which SET causes a voltage glitch is shown in Figure 2.7. It is a digital buffer, and the SET is applied to the inverted signal at 0.6μs for 10ns. The effect of SET is analyzed in this thesis to obtain the results of the temporary radiation on the ADCs.

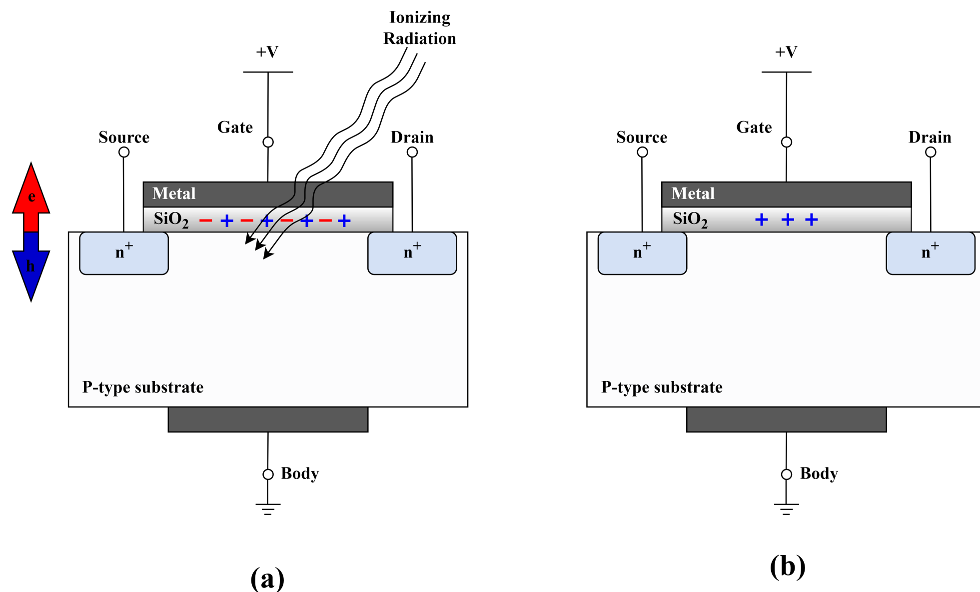

Figure 2.4. The total ionizing dose effect in an NMOS transistor.

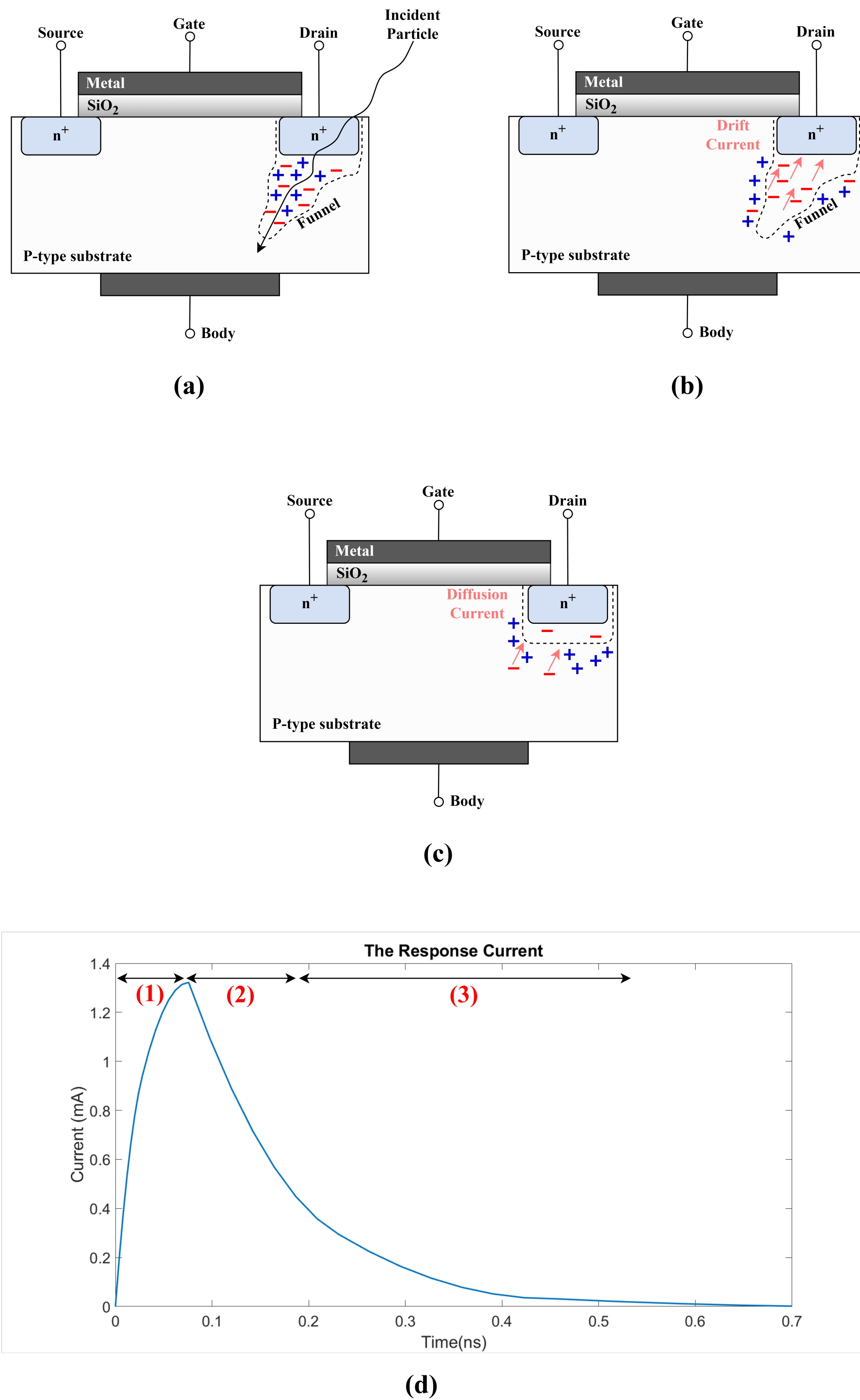

Figure 2.5. The occurrence of the SEEs in a MOSFET; (a) charge generation, (b) prompt charge collection, (c) diffusion charge collection, (d) the typical response current which forms as a result of SEEs, where (1) represents funnel creation, (2) shows funnel collection, (3) indicates diffusion.

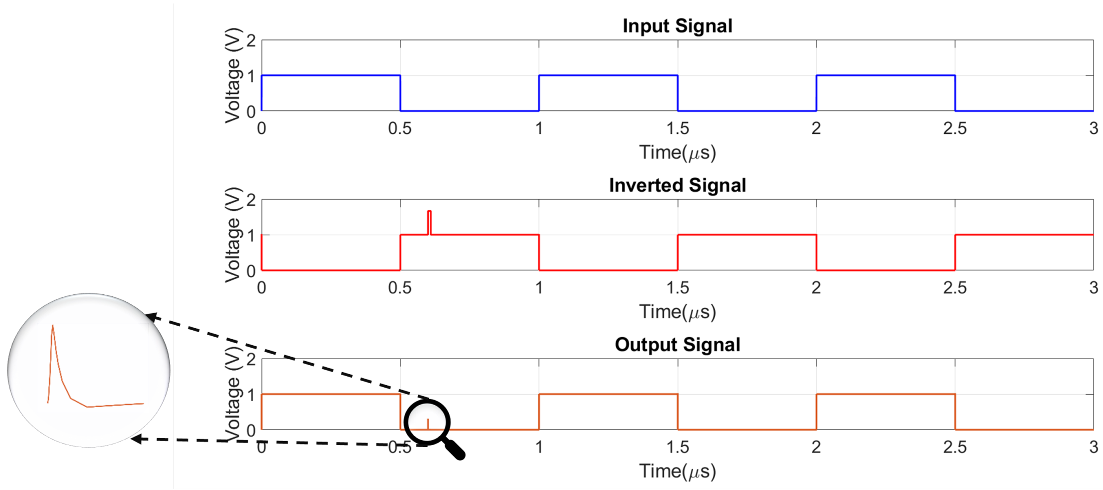

Figure 2.6. The glitching occurrence at the output of the digital buffer due to SET.

To be able to mimic the charge increase effect as a result of the striking particle, a current source can be used [33, 34], as in Figure 2.7. There are several types of current models to imitate the effect of SEEs; double exponential current model, diffusion current model [35], rectangular current model [34], etc. The double exponential current model, which is shown in Figure 2.5d, and the typical rectangular current model are the most preferred models to use for mimicking the SET. The rectangular current model is used in this study since it is easy to implement, and the amplitude of the applied current has been determined by RadiSPICE.

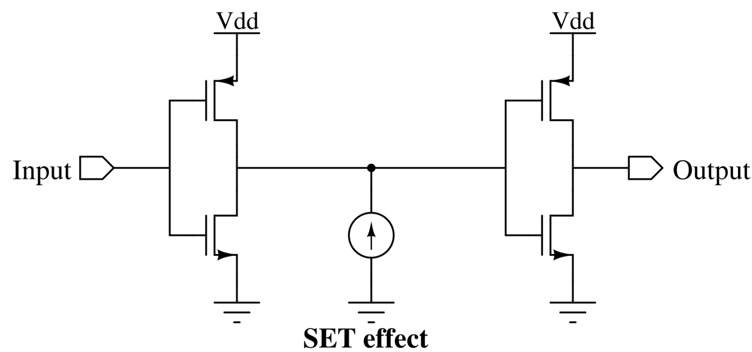

Figure 2.7. The SET model used in the simulations.

3. FLASH ANALOG-TO-DIGITAL CONVERTER

3.1. Designed Flash ADC

Flash analog-to-digital converter (flash ADC) is a type of analog-to-digital converter that is appropriate to use for applications with high speed. However, it provides low resolution [25]. A flash ADC consists of a voltage divider circuit, several voltage comparators, and a priority encoder to obtain an output code. This type of ADC involves $2^N - 1$ comparators, where N is the resolution of the ADC. The block diagram of a flash ADC is shown in Figure 3.1. A 4-bit flash ADC is constructed using Verilog-A, which is a modeling language for analog circuits. However, a latch comparator has been designed as a transistor-level circuit using the 65nm CMOS process model [36] to be able to model the comparator in Verilog-A in terms of the input offset voltage. The reference voltage is taken as 0.8V, which determines the full-scale range (FSR).

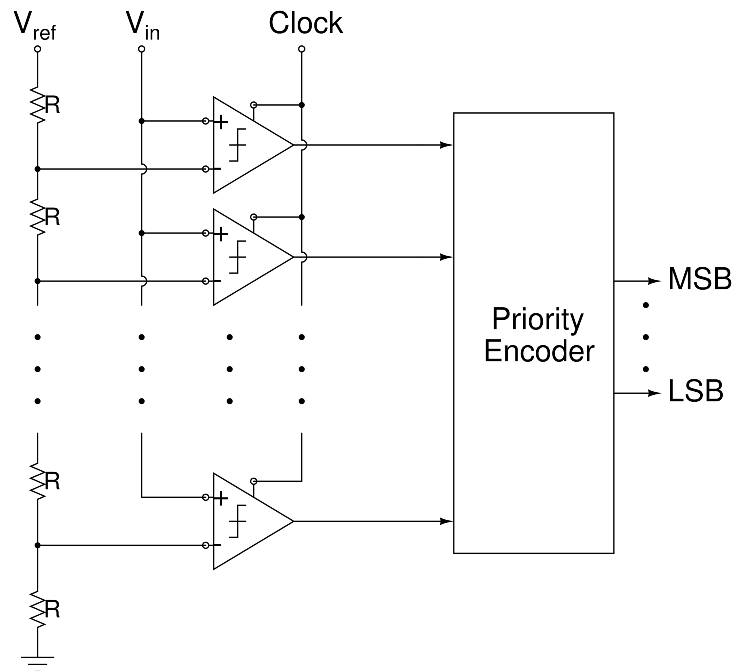

Figure 3.1. The block diagram of a flash ADC.

3.1.1. Blocks of the Designed Flash ADC

3.1.1.1. Comparator. The comparator block compares the applied voltage to its V_{in} input with the reference voltage and generates a digital result. In this study, a clocked comparator has been selected. Therefore, if the voltage at V_{in} input is greater than the voltage at V_{ref} input at the rising edge of the clock, the output is *1*. Otherwise, the result becomes *0*. A Strong ARM Latch Comparator [37] has been utilized in this work as shown in Figure 3.2. It has been designed at transistor-level using the 65nm CMOS process model [36] to be able to model the input offset voltage in Verilog-A. A sample simulation result is shown in Figure 3.3. A triangular signal that rises from 0.4V to 0.6V has been applied to V_{in} input, and 0.5V DC voltage has been determined as the reference voltage. As seen in the mentioned figure, *1* can be obtained when the input signal is greater than the reference voltage.

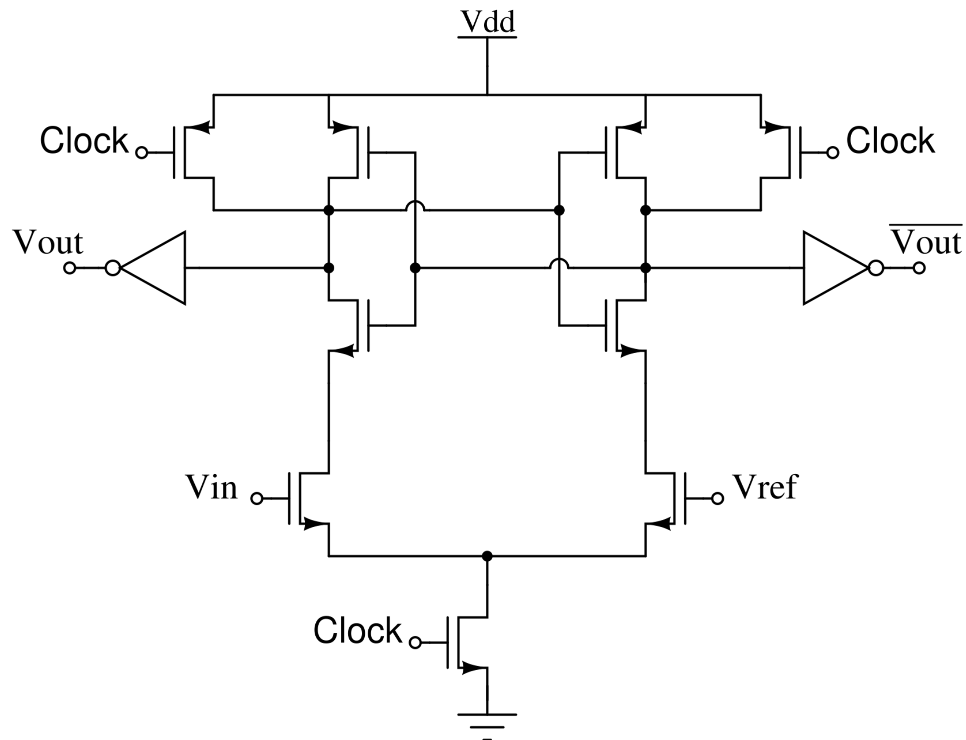

Figure 3.2. The comparator used in the designed flash ADC.

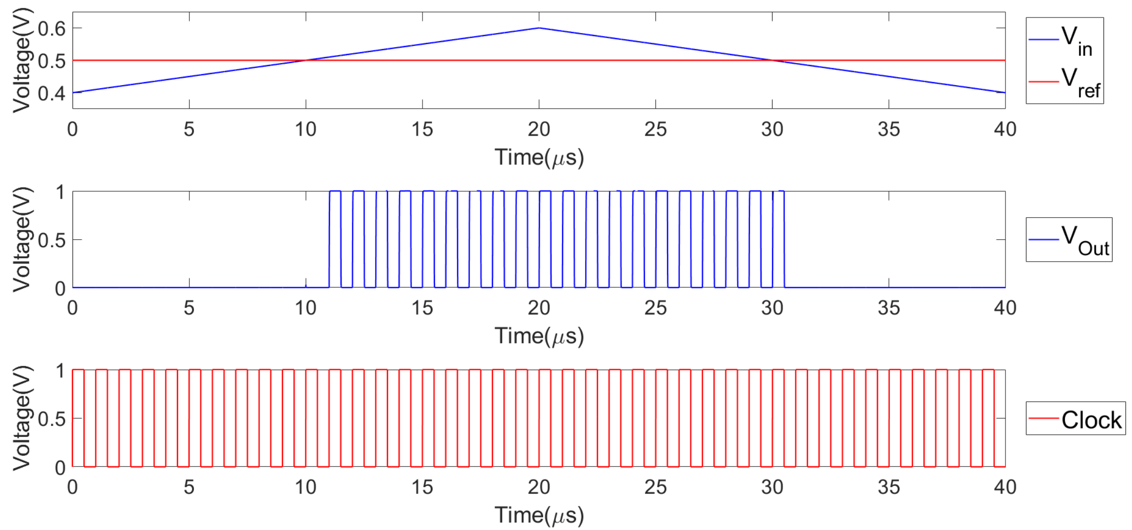

Figure 3.3. The simulation result of the clocked comparator used in the designed flash ADC.

On the other hand, it can be said that there is an input offset voltage as the output of the comparator turns into *1* in the second pulse of the clock cycle after V_{in} exceeds V_{ref}. A ramp signal that goes from 0V to 1V in 200μs has been applied to V_{in} input, and a 0.5V DC voltage has been applied to the V_{ref} input to be able to determine the offset voltage. In this case, the input offset voltage has been obtained as 5.16mV, as seen in Figure 3.4.

3.1.1.2. Priority Encoder. The priority encoder block is a combinational logic circuit that produces an output code considering the binary inputs. It produces N-bit output code using 2^N inputs [38]. Since the designed flash ADC is 4-bit, a 16 to 4 priority encoder has been constructed using multiplexers as shown in Figure 3.5. This circuit has been designed and simulated in Verilog-A. An example truth table of a 16 to 4 priority encoder is shown in Table 3.1.

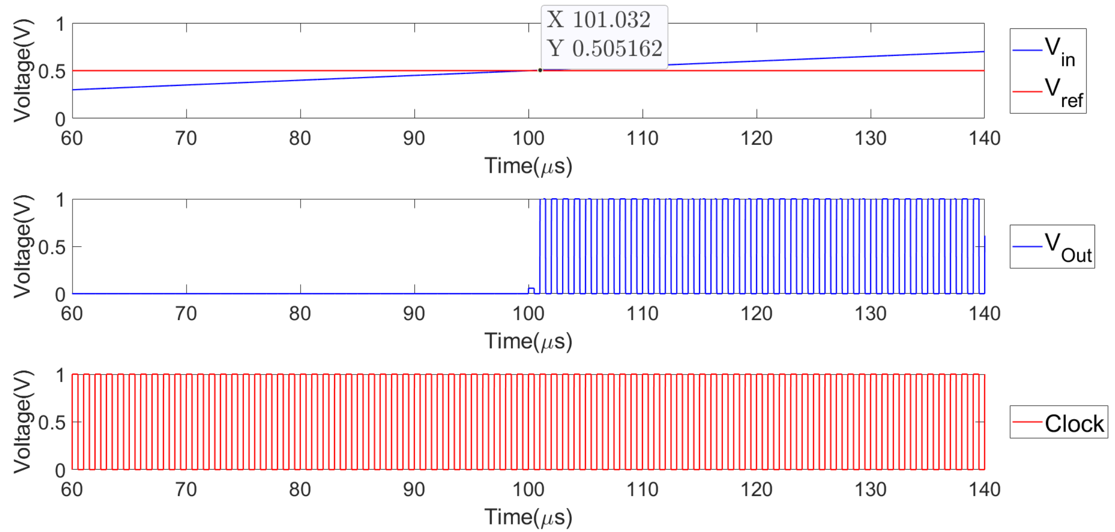

Figure 3.4. The simulation result of the clocked comparator used in the designed flash ADC to determine the input offset voltage.

Table 3.1. The truth table of a 16 to 4 priority encoder, where I15 has the highest priority, I0 has the lowest priority, and X represents don't care condition.

Inputs																Outputs			
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	X	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	X	X	X	X	X	0	1	0	1
0	0	0	0	0	0	0	0	0	1	X	X	X	X	X	X	0	1	1	0
0	0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	0	1	1	1
0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	1	0	0	0
0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	1	0	0	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	1	0	1	0
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	1	0	1	1
0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	1	1	0	0
0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	0	1
0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	0
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1

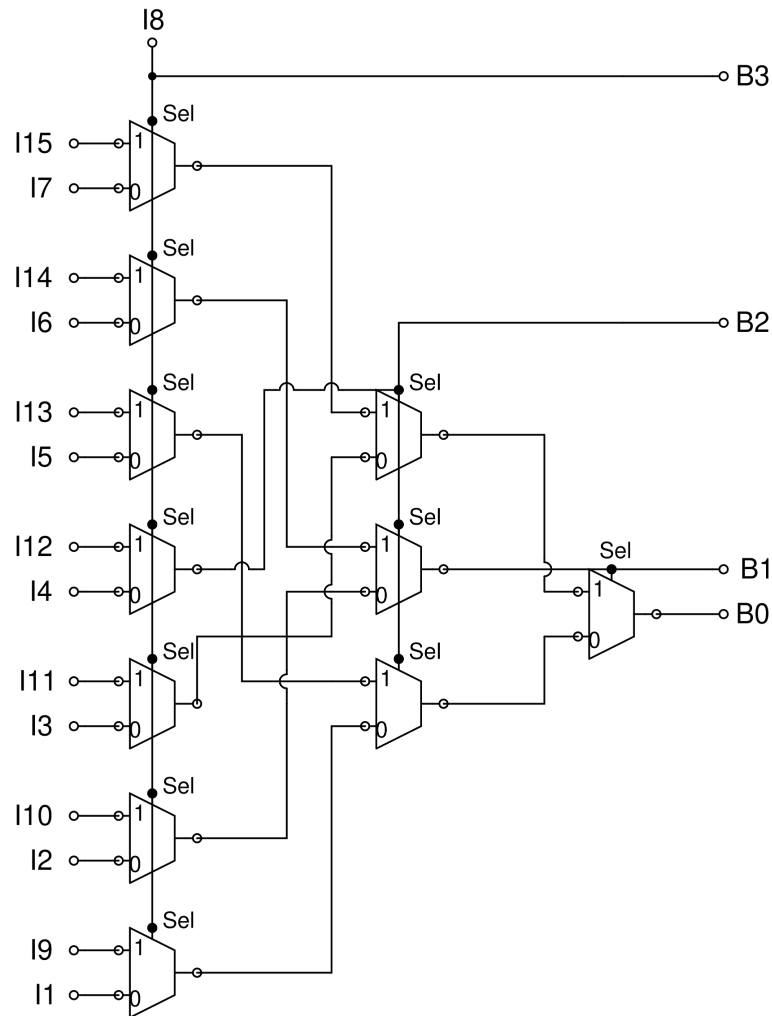

Figure 3.5. The designed priority encoder.

3.1.2. Operation of the Designed Flash ADC

The resistive voltage divider separates the reference voltage into 15 different voltage levels. Each of these voltages is compared with the input voltage by 15 different comparators. Then, these digital output signals are transmitted to the priority encoder. At the end of these processes, a 4-bit output code is obtained through the priority encoder. An analog input signal is converted into a digital signal by using this method.

To see if an ADC works properly, its differential nonlinearity (DNL) and integral nonlinearity (INL) values have to be examined. DNL formula is expressed as

$$DNL(c) = \frac{\Delta_o - \Delta_i}{\Delta_i}, \tag{3.1}$$

where $DNL(c)$ is the DNL of the corresponding output code, Δ_i is the ideal step width, and Δ_o is the obtained step width for the corresponding output code. The ideal step width is calculated as 50mV according to the least significant bit (LSB) formula. The least significant bit formula is expressed as

$$LSB = \frac{FSR}{2^n}. \tag{3.2}$$

In this equation, FSR is the full-scale range, and n is the resolution of the ADC. Since the designed ADCs have 4-bit resolution and the FSR is 0.8V, 1 LSB is found as 50mV. It means that the output code changes for every 50mV increase in the input voltage. On the other hand, the INL formula is expressed as

$$INL(k) = \sum_{i=1}^{k-1} DNL(i), \tag{3.3}$$

where DNL is as defined before.

The DNL and INL results of the flash ADC are shown in Figure 3.6, depicting proper operation. The first INL value is obtained as 0 since INL is the cumulative sum of the DNL. Therefore, the INL graphs in this thesis are constructed by eliminating the first INL value.

3.2. Radiation Performance of the Designed Flash ADC

The designed 4-bit flash ADC mentioned in this thesis has been tested under modeled radiation effects by using RadiSPICE [26], which is a simulation tool for space applications. TID is more vital on continuous-time analog circuits [25], whereas the digital and switched-capacitor circuits are more affected by the SET effect [25, 32]. Therefore, the comparators of the flash ADC have been only exposed to the TID effect.

3.2.1. Permanent Radiation Effect

TID causes offset changes on the comparator. The offset of the designed comparator was observed as 5.16mV. Therefore, the comparator gives *1* if the voltage applied to the V_{in} input of the comparator is 5.16mV greater than the voltage applied to the V_{ref} input. To be able to simulate the comparator under the TID effect, RadiSPICE has been used and the offset variation has been obtained as in Figure 3.7 as a result of the TID effect. The standard deviation (σ) of the comparator offset variation has been calculated as 13.58mV.

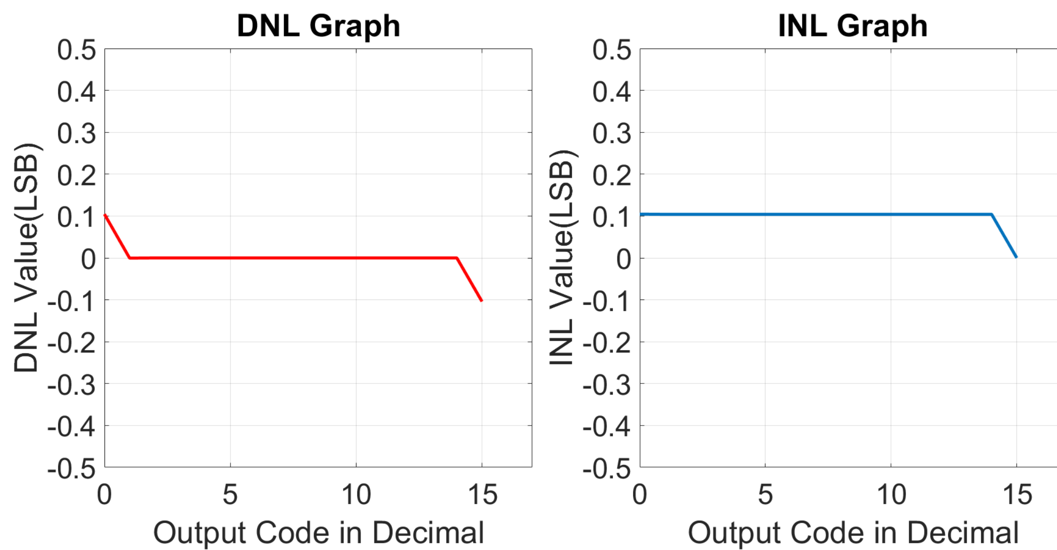

Figure 3.6. The simulation result of the flash ADC.

The permanent radiation effect is examined from two different perspectives. The first case is that all comparators have the same input offset voltage depending on the found σ value. The other one is that the values in the comparator offset variation are distributed randomly to the comparators in the designed flash ADC.

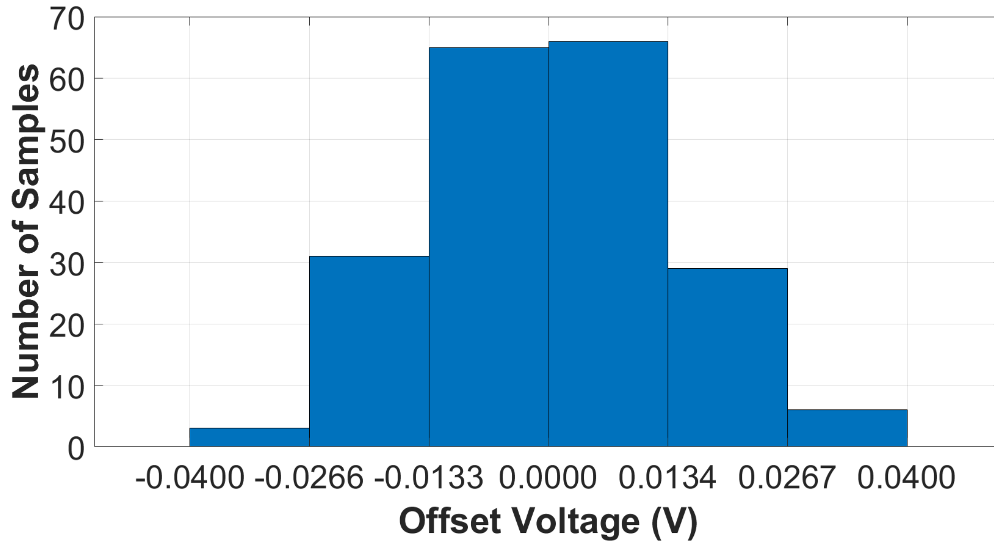

Figure 3.7. Comparator offset variation of the comparator used in the flash ADC under radiation exposure, simulated by RadiSPICE.

(i) All comparators have the same input offset voltage: To be able to implement the TID effect, the input offset voltage of the designed comparator, which is 5.16mV, has been changed according to the σ value of the offset variation. Three different simulations (comparators with $\pm 1\sigma$, and without external offset) have been conducted to be able to observe the TID effect on the designed flash ADC. The simulation results as DNL and INL graphs are shown in Figure 3.8. The DNL value of the first output code and the last output code have been observed as 0.28 LSB and -0.28 LSB respectively, in the case of the input offset voltage of the comparators being $+1\sigma$. The comparator offset of $+1\sigma$ means that the comparator result turns into *1* at the point the input voltage becomes 1σ V greater than the reference voltage. Since the beginning of the output code 1 in decimal is delayed due to the increased offset voltage, the DNL value of the output code 0 in decimal increases. The DNLs of the other output codes, except the last one, are not affected since both the beginning and the ending voltages are delayed. However, the full-scale range is restricted. Therefore, the DNL of the last output code becomes negative. The DNL value of the first output code,

which is 0.28 LSB, can be found by Equation (3.1), where Δ_o is 63.58mV and Δ_i is 50mV. On the other hand, the DNL of the first output code has been obtained around -0.28 LSB in the case of the comparators' offset voltage being in the magnitude of -1σ. This is due to decreased offset voltage, which is the inverse of the +1σ comparator offset case.

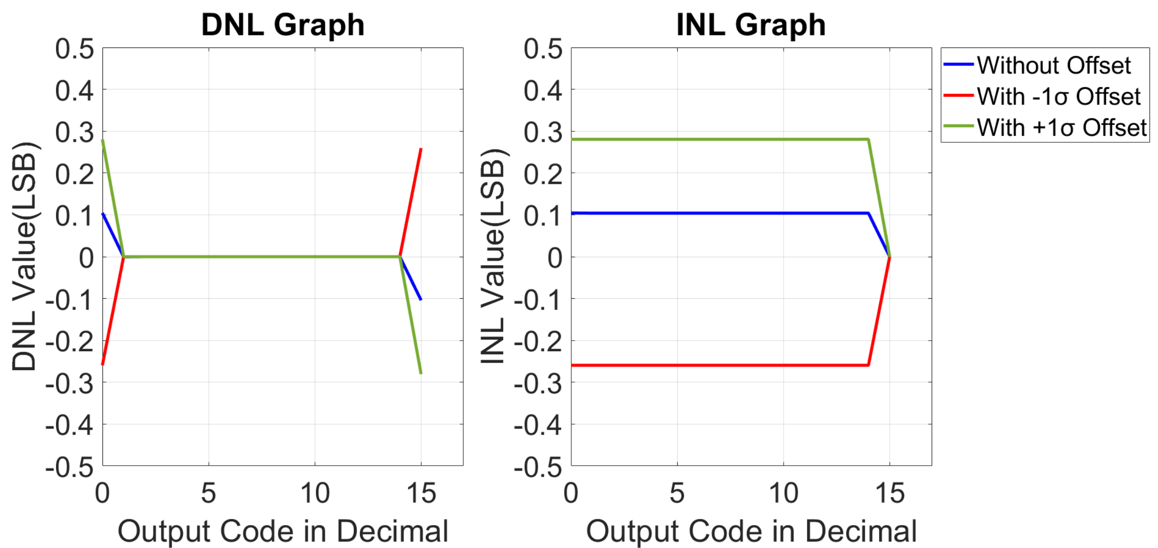

Figure 3.8. DNL and INL comparisons of the flash ADC, with and without fixed permanent radiation effect.

(ii) The offset values in the offset variation are distributed randomly: To obtain more realistic results, the comparator offsets obtained from RadiSPICE have been distributed randomly to the comparators in the flash ADC. In accordance with this purpose, a modified Verilog-A code has been constructed. This code consists of 15 different comparators and 200 different comparator offset values. In this code, a parameter called *seed_sel*, whose value has to be entered in the testbench, has been introduced to generate random numbers. According to the entered *seed_sel* value, the comparator offset values are assigned to the comparators randomly. As known, a random number generator produces the numbers in the same sequences in each call. The purpose of introducing the *seed_sel* parameter is to prevent

generating identical random number sequences. Each given value for the *seed_sel* parameter generates different numbers in different sequences.

The simulation results that belong to 10 different *seed_sel* values are shown in Figure 3.9. Also, the simulation result of the flash ADC without an additional offset exists in the mentioned figure. According to the DNL graph, it is obtained that non-fixed comparator offset values may cause missing output codes. It is seen that the output code 2 in decimal is missing in the case of the *seed_sel* parameter is 0. Also, the same situation is valid for the output code 14 in decimal when the *seed_sel* parameter is 7. These missing codes originate from inaccurate decisions of the comparators in the flash ADC.

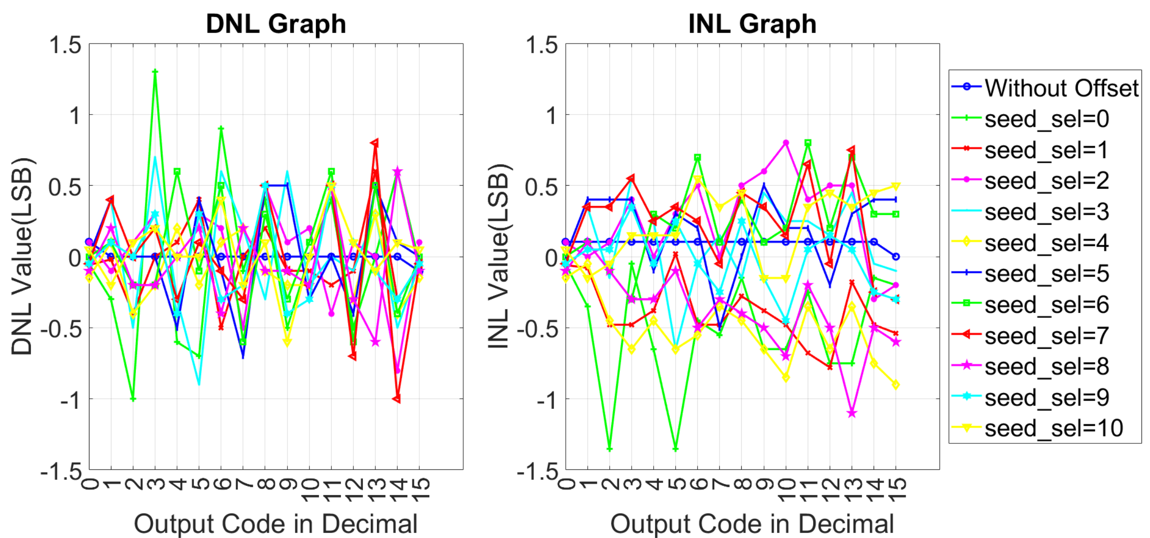

Figure 3.9. DNL and INL comparisons of the flash ADC, with and without non-fixed permanent radiation effect.

The simulation result of the flash ADC, which belongs to the *seed_sel* parameter is 0, is shown in Figure 3.10. After completing the output code 1 in decimal, bit B0 has to turn into *0*, and bit B1 has to become *1*. This result is represented as 2 in decimal. However, bit B0 does not turn into *0*, it continues to be *1*. As shown in Figure 3.5, the condition of having output code 2 in decimal, I3 has to be *0*

when bit B1 is *1*. The rule for I3, which is the output signal of the corresponding comparator, to be *0* is that the summing of V_{ref} and V_{offset}, which is -34.96mV, has to be greater than V_{in}. At the point of bit B1 being *1*, V_{in} is greater, as shown in Figure 3.10. Therefore, the output code 2 in decimal is missing.

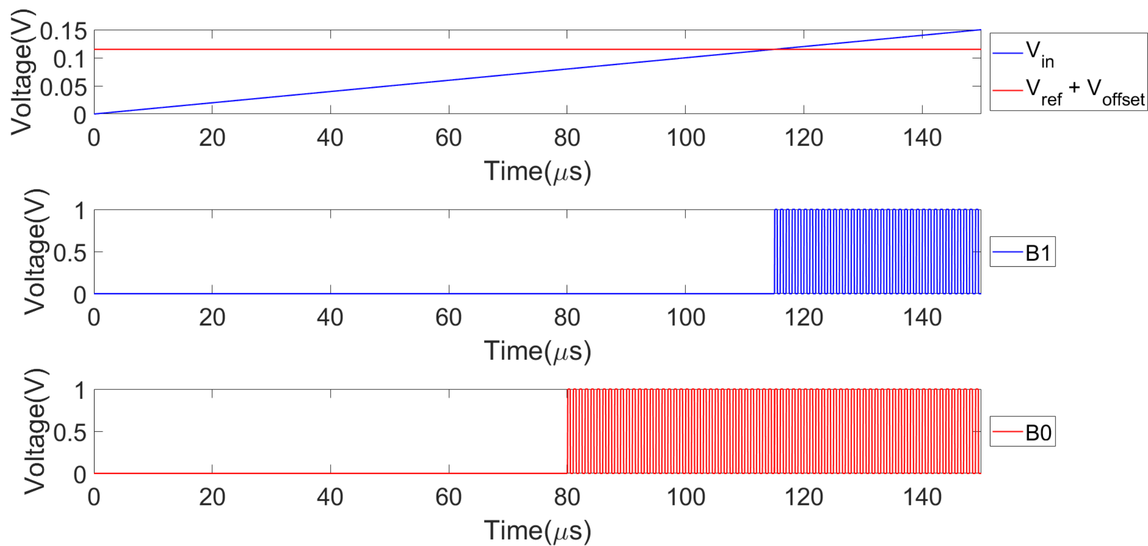

Figure 3.10. The simulation result of the flash ADC when the *seed_sel* is 0.

3.3. Conclusion

This chapter examines the permanent radiation effects on the 4-bit flash ADC. The ADC has been constructed in Verilog-A, and TID simulations have been conducted in the Cadence environment with the help of RadiSPICE. TID effect on the designed flash ADC has been investigated from two different perspectives; fixed and non-fixed permanent radiations. In the fixed permanent radiation case, input offset voltages of all comparators in the flash ADC have been set to ±13.58mV, which is the standard deviation of all RadiSPICE simulations of the designed transistor-level comparator. In this case, it has been obtained that TID causes DNL to decrease or increase in only the first and the last output code, which is not critical for the operation of the 4-bit flash ADC. In the non-fixed permanent radiation case, the obtained input offset voltages

from RadiSPICE have been distributed to the comparators randomly. In some cases, it has been observed that TID may cause missing codes, which shows that the ADC cannot work properly. However, since the source of the problem is input offset voltage, it can be canceled by using special techniques to design a flash ADC that is not affected by TID.

4. SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER

4.1. Designed SAR ADCs

Successive approximation register analog-to-digital converter (SAR ADC) is a type of analog-to-digital converter that is used for applications with medium-to-high resolution. SAR ADC uses binary search algorithm in determining the output codes [25, 39]. The block diagram of an SAR ADC is shown in Figure 4.1. Two different 8-bit SAR ADCs are designed using the 65nm CMOS process model [36]. The only difference between them is the DAC topology. The utilized DAC topologies are split capacitor array DAC and C-2C ladder-based DAC. The supply voltage is taken as $1V$.

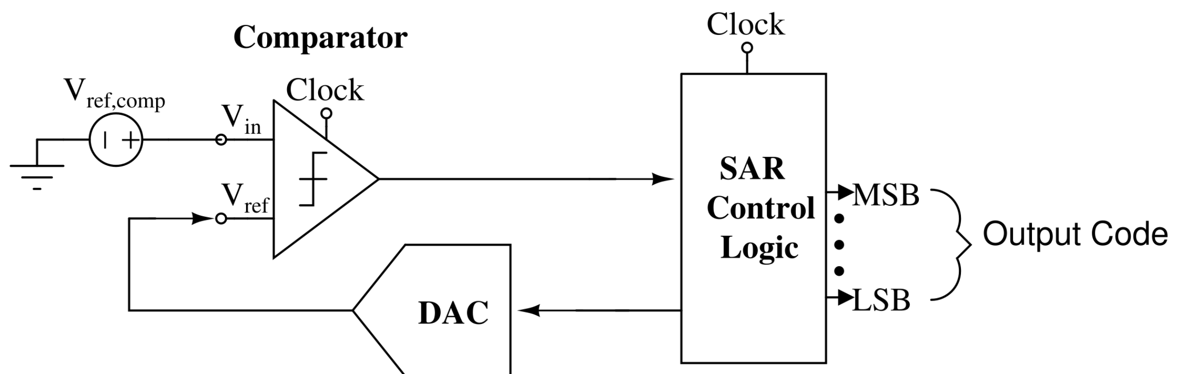

Figure 4.1. The block diagram of an SAR ADC [40].

4.1.1. Blocks of the Designed SAR ADCs

There are three different main blocks in a conventional SAR ADC: a comparator, an SAR control logic, and a digital-to-analog converter (DAC). The same comparators are used in both of the designed ADCs.

4.1.1.1. Comparator. In this work, the same latch comparator mentioned in Chapter 3 is used, but an input preamplifier has been added, as shown in Figure 4.2. The aim of adding a preamplifier is to minimize the charge injection effect. In addition, the offset of the comparator decreases thanks to the preamplifier since it amplifies the signal that is transmitted to the latch. $V_{ref,comp}$ is the reference voltage for the comparator that is compared to the voltage that comes from the DAC in Figure 4.1. It has been determined as half of the supply voltage, which is $0.5V$.

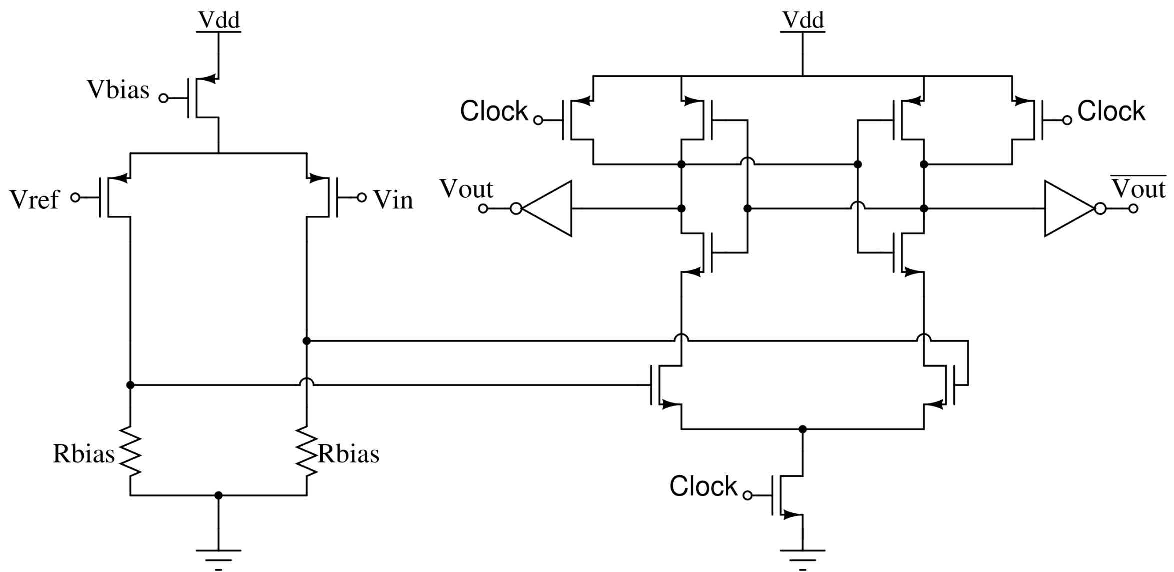

Figure 4.2. The comparator used in the designed SAR ADCs.

A sample simulation result is shown in Figure 4.3. A triangular signal from 0.4V to 0.6V has been applied to V_{in} input, a 0.5V DC voltage has been applied to V_{ref} input. As seen in the mentioned figure, the result turns into *1* at the rising edge of the clock where the input signal exceeds the reference voltage. To be able to measure the input offset voltage of the designed comparator, a ramp input from 0V to 1V, whose rise time is 200μs, has been applied to V_{in} input, and a 0.5V DC voltage has been given to V_{ref} input. The input offset voltage has been obtained as 25μV as in the simulation result, which is shown in Figure 4.4.

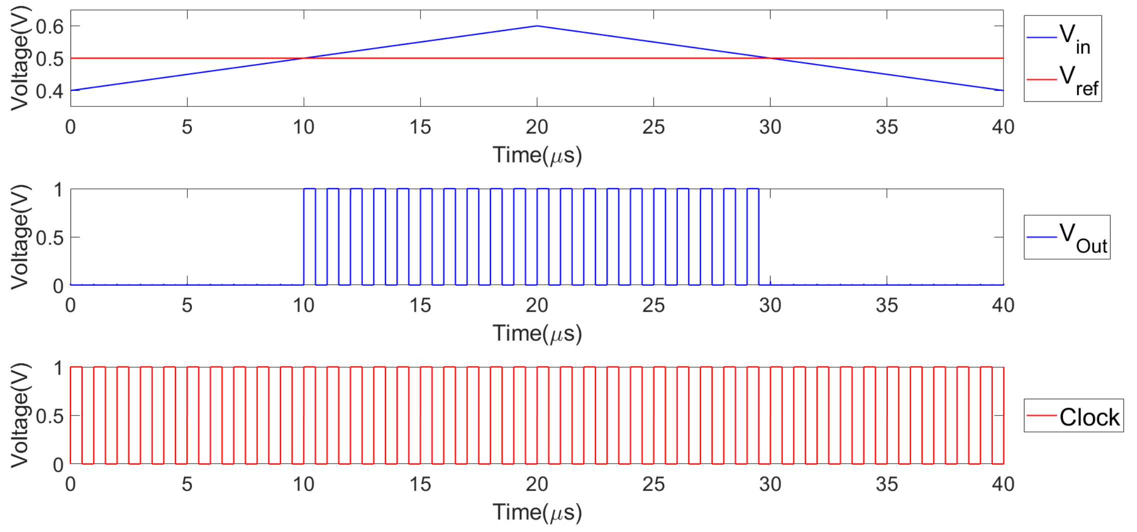

Figure 4.3. The simulation result of the clocked comparator used in the designed SAR ADCs.

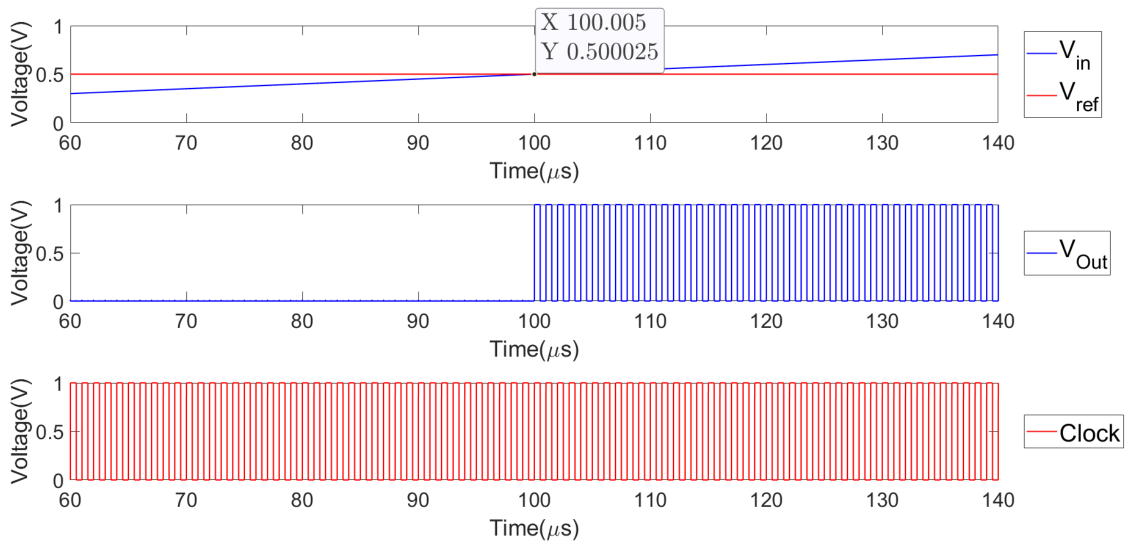

Figure 4.4. The simulation result of the clocked comparator used in the designed SAR ADCs to determine the input offset voltage.

<u>4.1.1.2. SAR Control Logic.</u> SAR control logic is a digital block that consists of D-flip flops in SAR ADC that are responsible for determining the values of the bits of the output code considering the comparator result. The decision is made for all bits individually, from the most significant bit (MSB) to the least significant bit (LSB). If the comparator result is *1*, the value of the corresponding bit is determined as *1*. The SAR control logic is shown using D flip-flops (DFFs) in Figure 4.5.

Figure 4.5. SAR control logic.

<u>4.1.1.3. DACs.</u> DAC is an electronic circuit that converts a digital signal into an analog signal. It divides the supply voltage into different voltage levels according to the desired number of bits. There are different types of DACs, but capacitive DACs have been chosen to examine in this thesis. The capacitive DAC section consists of several topologies. The most popular DAC topologies have been studied; the split capacitor array DAC and C-2C ladder-based DAC. The main aim of preferring these DAC topologies is to minimize the total capacitance value compared to the binary-weighted capacitor array DAC topology.

(i) Split Capacitor Array DAC: To decrease the total capacitance with respect to the binary-weighted capacitor array DAC, the split capacitor array DAC divides the capacitor array into two sub-arrays as LSB and MSB arrays by the attenuation capacitor C_{att}, as shown in Figure 4.6. In this topology, there is a dummy capacitor in the LSB array that has the same capacitance value as the capacitor

with the smallest capacitance (C_u). The capacitance values of the capacitors in LSB and MSB arrays move on from left to right by doubling the previous one. In the design of the split capacitor array DAC, the value of C_u has been determined as $300fF$ to obtain a similar output to the output of the ideal DAC. The capacitance value of the attenuation capacitor has been determined as

$$C_A = \frac{2^{n/2}}{2^{n/2}-1}C_u, \tag{4.1}$$

where C_A is the capacitance value of the attenuation capacitor, n is the resolution of the DAC, and C_u is the unit capacitance value.

(ii) C-2C Ladder-Based DAC: The other DAC topology in focus in the thesis is C-2C ladder-based DAC. This topology is also frequently preferred, as split capacitor array DAC, to reduce the total capacitance value in the DAC. There are two different capacitance values as C_u and $2C_u$ in this topology, as shown in Figure 4.7, where C_u has been adjusted as $400fF$ to be able to come close to the ideal DAC output.

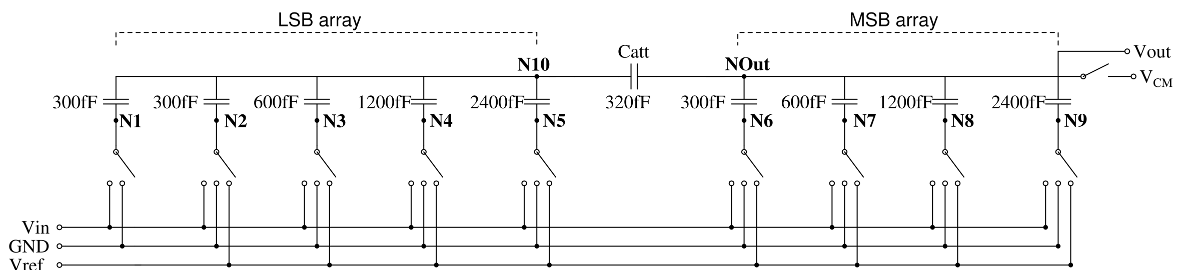

Figure 4.6. The split capacitor array DAC used in the SAR ADC [40].

4.1.2. Operation of the Designed SAR ADCs

The comparator compares the voltage that comes from the DAC with the external reference voltage. A digital result is produced according to the comparison in each conversion. Then, this digital result is transmitted to the SAR control logic. Also, the DAC produces an analog voltage for each conversion according to the coming bit values from the SAR control logic. This process continues eight times since the designed ADCs

have 8-bit resolution. At the end of the eight conversions, an output code is obtained. This code is the conversion of an analog signal to a digital signal.

The DNL and INL values of the designed SAR ADCs are examined to check for verifying their working. Since the designed ADCs have 8-bit resolution and FSR is 1V, 1 LSB is determined as 3.91mV according to Equation (3.2). The DNL and INL values have been calculated according to Equation (3.1) and Equation (3.3), respectively. The DNL and INL results of the SAR ADC with split capacitor array DAC are shown in Figure 4.8. Also, the DNL and INL results of the SAR ADC with C-2C ladder-based DAC are shown in Figure 4.9. Both figures demonstrate correct operation.

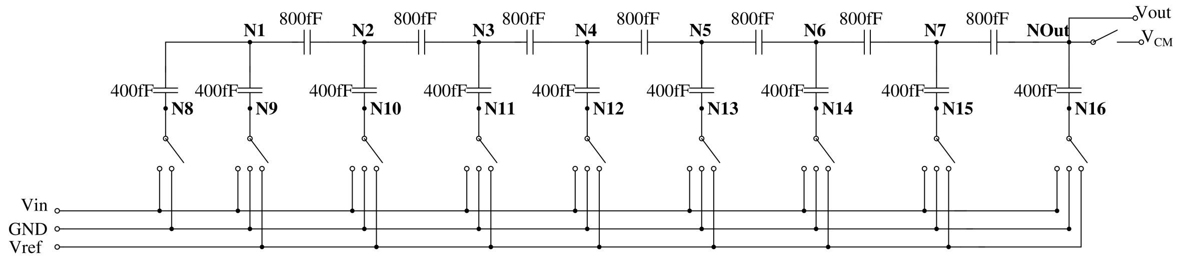

Figure 4.7. The C-2C ladder-based DAC used in the SAR ADC [40].

4.2. Radiation Performance of the Designed SAR ADCs

The designed 8-bit ADCs mentioned in this thesis have been exposed to radiation, which is modeled in the transistor-level circuits, with the help of RadiSPICE. As mentioned in Chapter 3, continuous-time analog circuits are more affected by the TID effect, and the SET effect is more vital on digital and switched-capacitor circuits [25, 32]. The SET event creates a similar effect on the comparator and the DAC. Also, TID affects the switches located in the DAC, but TID creates more critical faults in the comparator. Therefore, the TID effect has been only reflected in the comparator in the designed ADCs, whereas the SET effect has been applied to the designed DACs. The transistor-level simulations have been conducted in LTspice with the 65nm CMOS Berkeley Predictive Technology Model (BPTM) [36].

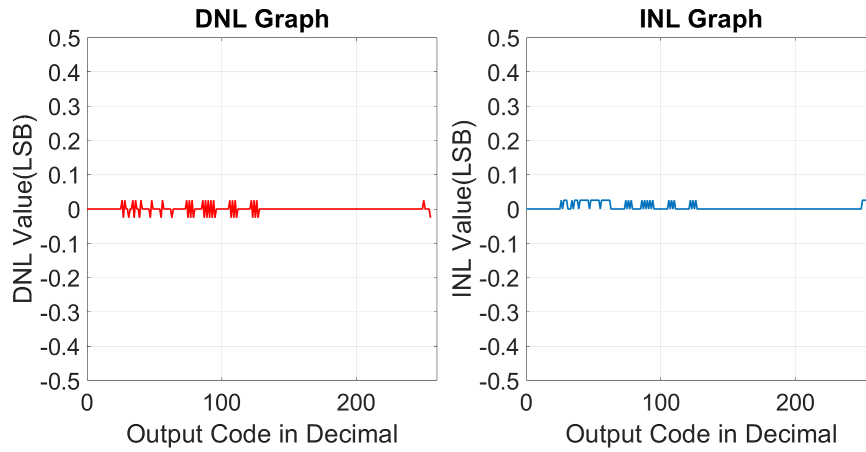

Figure 4.8. The simulation result of the SAR ADC with split capacitor array DAC.

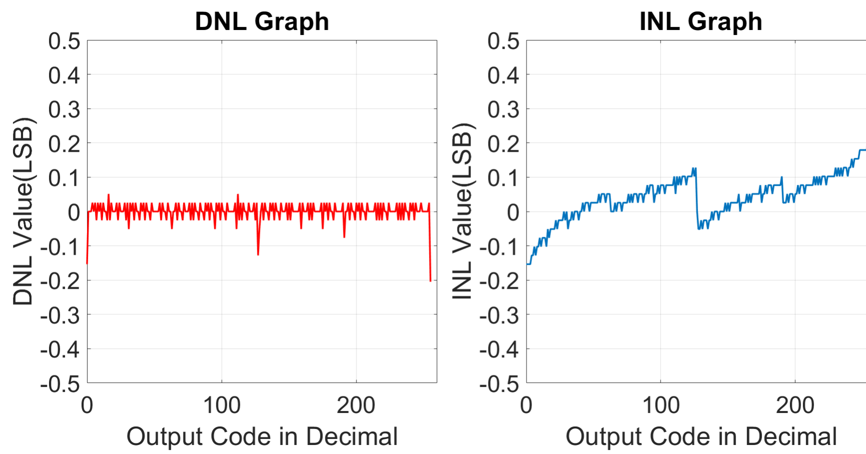

Figure 4.9. The simulation result of the SAR ADC with C-2C ladder-based DAC.

4.2.1. Permanent Radiation Effect

Input offset voltage shifts are observed due to TID in the comparator. The offset of the designed comparator without radiation effect was measured as 25 μV. Therefore, the comparator gives *1* if the voltage coming from the DAC is below 0.5V + 25 μV. RadiSPICE has been used to obtain the new input offset voltage of the comparator that shifts due to the TID event. Several TID simulations have been done for the comparator by RadiSPICE, and the offset variation obtained from the simulations is as in Figure 4.10. The value that is the standard deviation (σ) of the comparator offset variation has been calculated as 15.02mV to be able to use in the transistor-level TID simulations of the designed SAR ADCs.

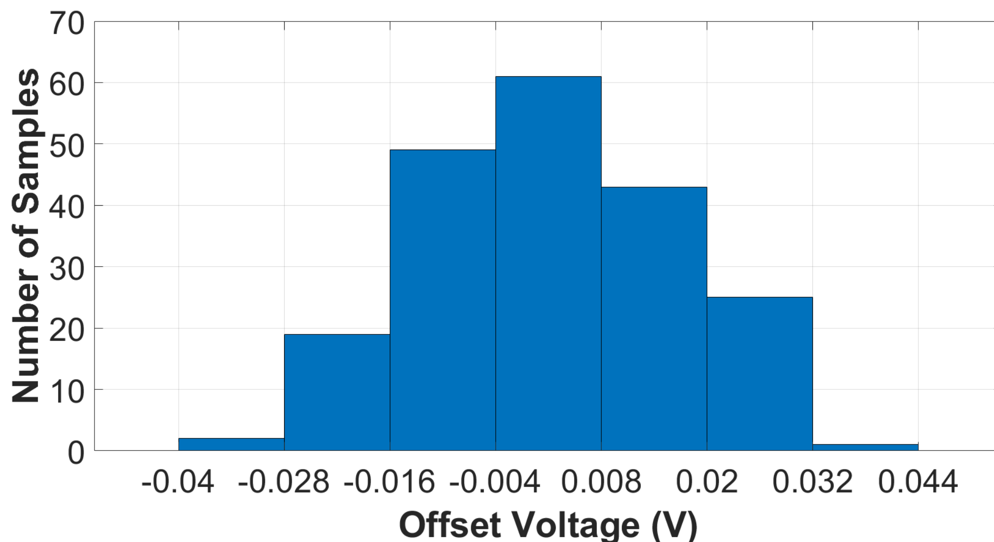

Figure 4.10. Comparator offset variation of the comparator used in the SAR ADCs under radiation exposure, simulated by RadiSPICE [40].

The reference voltage in the comparator, which is $V_{ref,comp}$ in Figure 4.1, has been modified with $V_{ref,comp}$ $\pm 1\sigma$ values in the designed ADCs to be able to model the TID effect. For both of the ADCs, three different simulations (comparator with $\pm 1\sigma$ offsets, and without external offset) have been done. Since the same comparator is used in

both ADCs, the TID effect is explained through the split capacitor array DAC-based SAR ADC:

The voltage values of the bits that are the output of the DAC are calculated as

$$V_n = V_{CM} - V_{in} + \sum_{i=n}^{N-1} \frac{V_{ref}}{2^{N-i}} b_i, \tag{4.2}$$

where V_{CM} is the common-mode voltage of the DAC, V_{in} is the input voltage of the DAC, V_{ref} is the reference voltage of the DAC, N is the resolution of the ADC, n is the order of the corresponding bit (from MSB to LSB), and b_i is the logic value of the corresponding bit [41].

The graphs that indicate the DNL and INL of the SAR ADC with split capacitor array DAC as a result of the TID event are shown in Figure 4.12. The DNL and INL values have been obtained by processing the simulation results using MATLAB.

The transient simulation result that points out the output of the DAC in the SAR ADC with $+1\sigma$ comparator offset is shown in Figure 4.11. The expected code is 00000000 when the applied input voltage is 0V. However, the output code that is given by the ADC is observed as 00000011, as seen in Figure 4.11. According to Equation (4.2), taking 3.91mV as 1 LSB, 1σ comparator offset of 15.02mV corresponds to -3.85 LSB. This shows that there are no first three output codes as shown in Figure 4.12. On the other hand, -1σ comparator offset of -15.02mV corresponds to the DNL of 3.85 LSB for the first output code, according to Equation (4.2). As the first output code is shifted by 3.85 LSB, the last three output codes are missing.

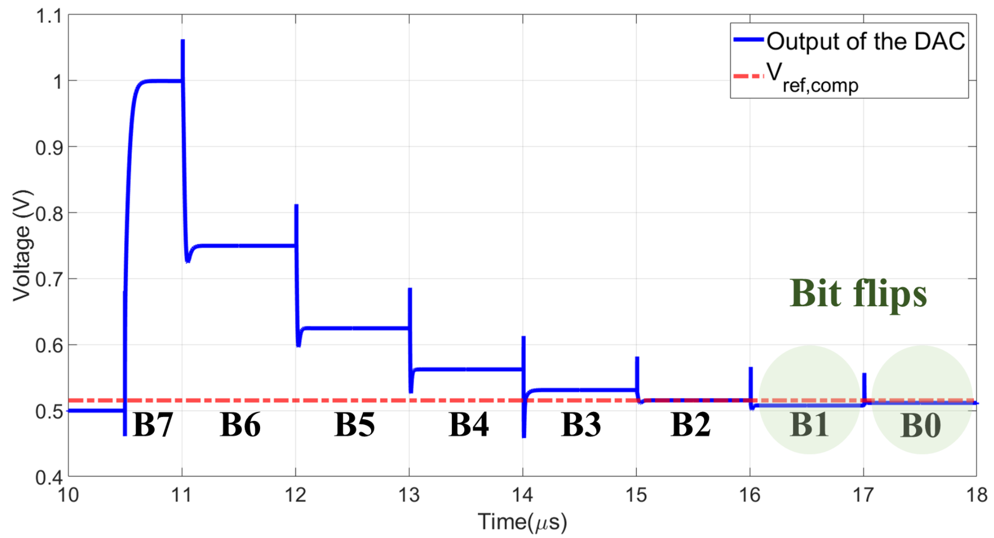

Figure 4.11. The output of the DAC in the SAR ADC with $+1\sigma$ comparator offset for 0mV input voltage [40].

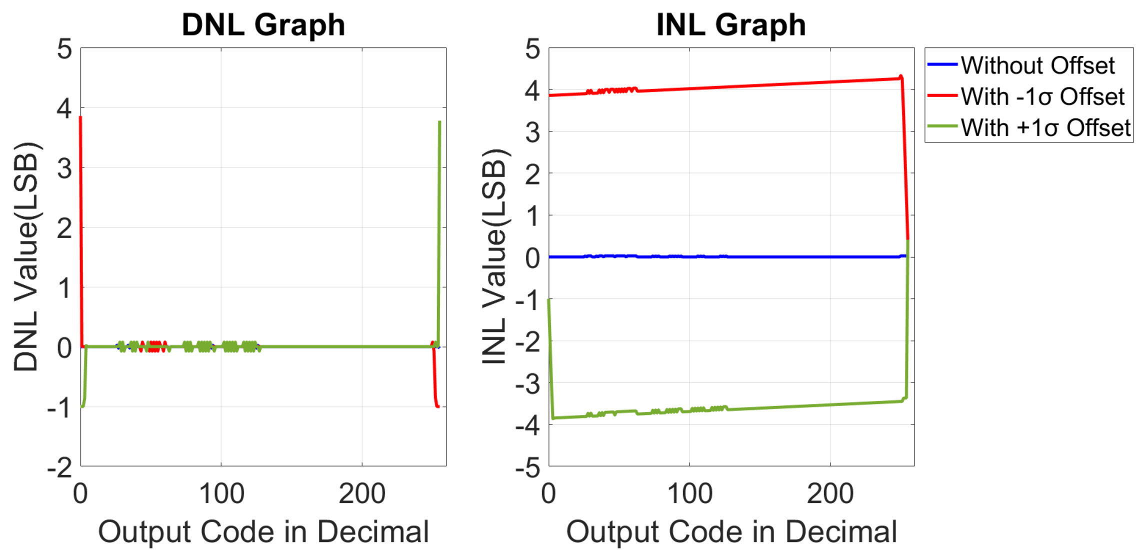

Figure 4.12. DNL and INL comparisons of the split capacitor array DAC-based SAR ADC, with and without permanent radiation effect.

4.2.2. Temporary Radiation Effect

To be able to model the SET event on the DAC, current pulses in rectangular-shaped as in Figure 4.13, have been implemented to the nodes at several different times. In this way, the effect of charge increase that occurs when a particle strikes a node is modeled [26]. The amplitude of the SET current pulse is determined by RadiSPICE, the MATLAB code is shown in Appendix A. The output codes that are obtained from the ADC conversion under SET are shown in Table 4.1 and Table 4.2, where the node names are referred to Figure 4.6 and Figure 4.7. In these tables, the expected output code is 00000000 when there is no SET event. The times in the mentioned tables indicate when the SET is applied to the corresponding node. These times can be checked in Figure 4.14 and Figure 4.15 to observe which bit conversion is done in the corresponding application time.

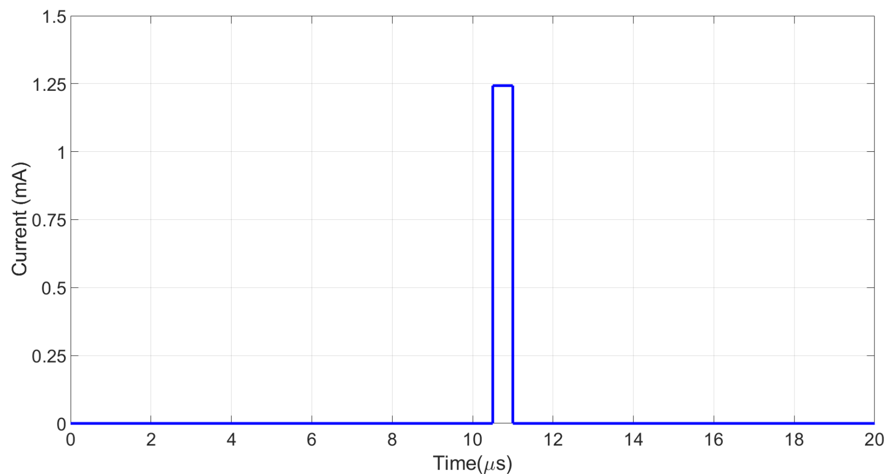

Figure 4.13. An example current pulse that is applied at 10.5μs to a node of the DACs for modeling the temporary radiation on the SAR ADC.

There are several incorrect output codes due to bit flips caused by SET in Table 4.1, which belongs to the split capacitor array DAC-based SAR ADC. If SET occurs during the MSB decision phase, the ADC has the largest number of inaccurate results. Another finding is applying SET to the node $N9$ creates the largest output error.

Sample transient simulation results of the split capacitor array DAC exist in Figure 4.14. The reference voltage, which is $V_{ref,comp}$, is presented by the red dotted line, and circled regions symbolize bit flips. The blue plot shows the simulation result when the SET is applied to the node $N9$ at 10.5μs. As seen in this figure, the voltage levels of bits B5, B3, B2, and B1 stay below the reference voltage despite the expected code being 00000000. Since the SET occurs at the node $N9$ during the MSB decision phase, the voltage at this node, which is the MSB decision node, increases. This situation causes erroneous charge distribution in the DAC and the voltage difference between the MSB and the other bits increases as in Figure 4.14. In other words, the voltage value of the MSB increases compared to the expected voltage value, whereas the voltage values of the other bits decrease. However, the voltage difference between the other nodes (except the MSB node), which are calculated using Equation (4.2), does not change despite their voltages being reduced. As a result, bit flips in the bits B5, B3, B2, and B1 are observed, and they turn into 1 mistakenly. The green plot in Figure 4.14 represents the simulation result when the SET occurs at the node $NOut$ at the MSB decision phase. In this condition, the current pulse, which models the SET event, is directly applied to the output of the DAC. This emerged charge boosts the voltage value of each bit. However, the expected code is obtained in spite of the SET event since the voltage values of the bits are still above $V_{ref,comp}$.

Table 4.1. ADC output codes with split capacitor array DAC under SET [40].

Expected Code : 00000000						
Applied Nodes	**Temporary radiation is applied at**					
	0 µs	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	00000000	00000000	00000000	00000000	00000000	00000000
N9	000000**1**0	00**1**0**111**0	000**11111**	00000**111**	000000**11**	0000000**1**
N8	00000000	000**111**0**1**	000**1**000**1**	00000**111**	000000**11**	0000000**1**
N6	00000000	000000**1**0	00000000	00000000	0000000**1**	0000000**1**
N5	00000000	000000**11**	00000000	00000000	00000000	00000000
N2	00000000	0000000**1**	00000000	00000000	00000000	00000000

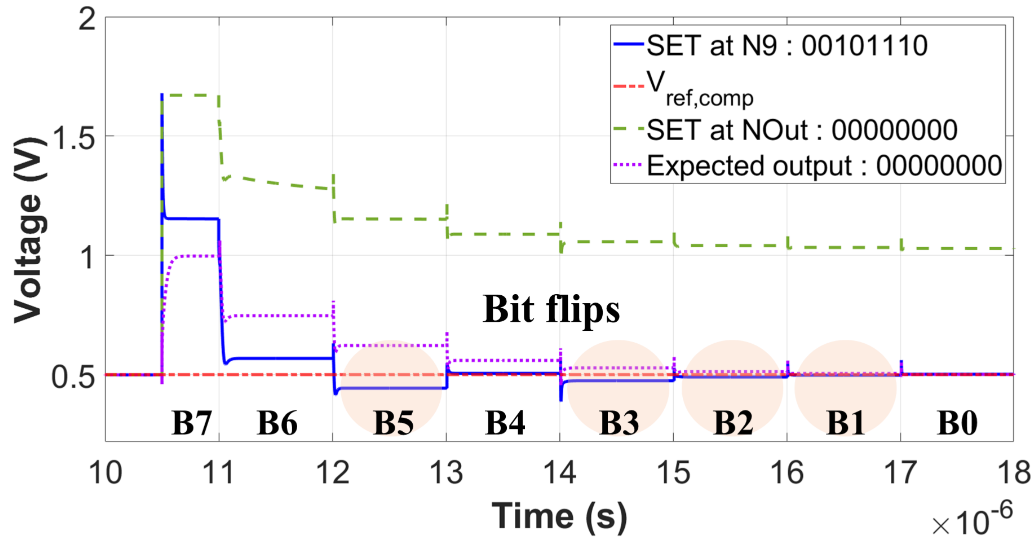

Figure 4.14. The split capacitor array DAC result under SET at 10.5µs. The expected code is 00000000 [40]. (DAC voltages below $V_{ref,comp}$ result as 1.)

Table 4.2. ADC output codes with C-2C ladder-based DAC under SET [40].

Expected Code : 00000000						
Applied Nodes	**Temporary radiation is applied at**					
	0 µs	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	00000000	00000000	00000000	00000000	00000000	00000000
N16	00000000	00100101	00011111	00000111	00000011	00000001
N7	00000001	00001101	00000000	00000000	00000000	00000000
N15	00000000	00101111	00010010	00000111	00000011	00000001
N4	00000000	00000000	00000000	00000000	00000000	00000000
N12	00000000	00000100	00000000	00000000	00000000	00000001
N1	00000000	00000000	00000000	00000000	00000000	00000000
N9	00000000	00000010	00000000	00000000	00000000	00000000

According to Table 4.2, which is constructed when the expected code is 00000000, applied temporary radiation at B7 (MSB) sequence causes the most error compared to the other application times for the SAR ADC with C-2C ladder-based DAC. In addition, it can be said that the largest error is observed when the SET occurs at the

nodes $N15$ or $N16$. Figure 4.15 shows transient simulation results for the nodes $N16$ and $NOut$. There are bit flips in bits B5, B2, and B0 in the blue plot for the same reason as in the split capacitor array DAC results.

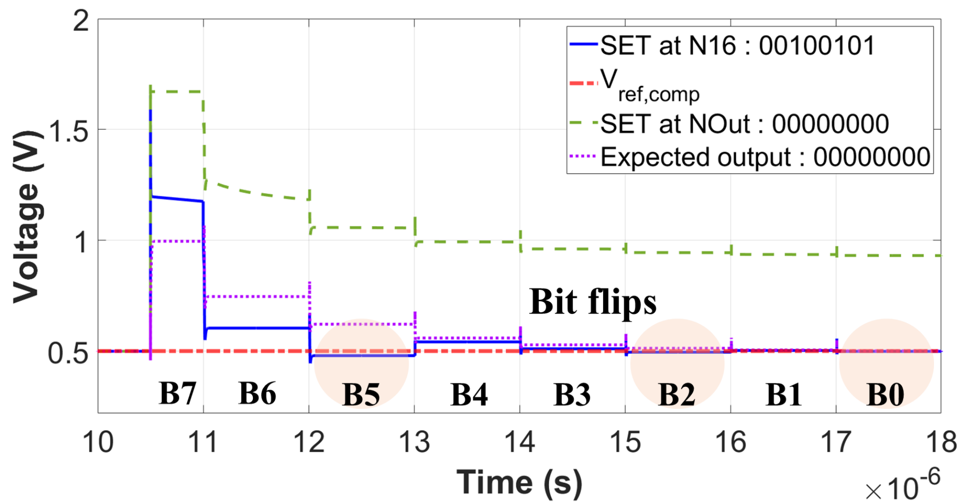

Figure 4.15. The C-2C ladder-based DAC result under SET at 10.5µs. The expected code is 00000000 [40]. (DAC voltages below $V_{ref,comp}$ result as 1.)

Similar tables to Table 4.1 and Table 4.2, which are shown in Appendix B and Appendix C, have been created for four more different expected output codes, which are 55, 128, 179, and 255 in decimal. They have been constructed with the same SET event timings and DAC nodes. The obtained bit errors in all of the constructed tables are converted into LSB values as shown in Table 4.3. According to this table, it can be obtained that the SAR ADC with split capacitor array DAC is more insensitive to SET events compared to the SAR ADC with C-2C ladder-based DAC by taking into consideration the average LSB errors. Also, average error tables have been constructed for the DACs as Table 4.4 and Table 4.5 to be able to compare the nodes. According to Table 4.4, it can be reached that the node $NOut$ is the most sensitive node in the split capacitor array DAC. On the other side, the nodes $NOut$, $N7$, $N4$, and $N1$ are more sensitive to SET compared to the other nodes in the C-2C ladder-based DAC as seen in Table 4.5.

Table 4.3. ADC errors due to SET for different expected codes [40].

Input Voltage	Expected Code in Decimal	Average Error in ADC with:		Maximum Error in ADC with:	
		Split Capacitor	C-2C	Split Capacitor	C-2C
2mV	0	4.31 LSB	3.67 LSB	46 LSB	47 LSB
216.8mV	55	3.83 LSB	7.98 LSB	55 LSB	55 LSB
502mV	128	3.61 LSB	10.46 LSB	128 LSB	128 LSB
701.1mV	179	8.58 LSB	18.96 LSB	179 LSB	179 LSB
998mV	255	9.14 LSB	25.46 LSB	255 LSB	255 LSB

Table 4.4. ADC errors due to SET for the nodes in the split capacitor array DAC.

Node	Average Error
NOut	24.23 LSB
N9	6.10 LSB
N8	4.37 LSB
N6	0.43 LSB
N5	0.17 LSB
N2	0.07 LSB

Table 4.5. ADC errors due to SET for the nodes in the C-2C ladder-based DAC.

Node	Average Error
NOut	24.23 LSB
N4	24.23 LSB
N1	24.23 LSB
N7	22.90 LSB
N16	5.40 LSB
N15	4.97 LSB
N12	0.33 LSB
N9	0.13 LSB

4.3. Conclusion

This chapter analyzes the temporary and permanent radiation effects on two different 8-bit SAR ADC topologies: split capacitor array DAC and C-2C ladder-based DAC. The designed transistor-level SAR ADCs have been simulated under TID and SET events thanks to RadiSPICE. At the end of the TID simulations, it has been concluded that permanent radiation leads to missing output codes in the SAR ADCs. The reason for this situation is the change in the input offset voltage, which can be canceled, of the comparator. In addition to this, it has been observed that SET may cause bit flips, which are difficult to cancel out, in the output codes due to the charge increase at specific circuit nodes. Also, SET applied during MSB conversion of the ADCs causes the largest number of erroneous output codes. At the end of SET simulations, sensitive nodes in the DACs have been determined, and it has been concluded that split capacitor array DAC is more immune to SET events.

5. SIGMA-DELTA ADC

5.1. Designed Sigma-Delta Modulator

Sigma-delta analog-to-digital converter (Σ-Δ ADC) is an analog-to-digital converter type that is used for high-resolution applications. On the other hand, it can not operate in high-bandwidth applications compared to flash ADC and SAR ADC [14]. The sigma-delta ADC is different from flash ADC and SAR ADC in terms of operation. Flash and SAR ADCs are in the Nyquist rate ADC category, and sigma-delta ADC is in the oversampling ADC category, as explained in Chapter 2.

Sigma-delta ADC consists of analog and digital blocks [42]. The analog block is called sigma-delta modulator. Digital blocks consist of a digital filter and a decimator. The block diagram of the designed sigma-delta modulator is shown in Figure 5.1. The sigma-delta modulator takes an analog signal and creates a bitstream. Also, there are a digital filter and a decimator at the output of the sigma-delta modulator in the sigma-delta ADC. The digital filter eliminates the noise at high frequencies. Also, the output code is obtained by processing the bitstream through the decimator.

In this thesis, only a first-order sigma-delta modulator has been designed, and the bitstream taken from the output of the sigma-delta modulator has been processed using MATLAB. In this way, there is no need for a digital filter and a decimator. A sigma-delta modulator consists of an integrator, a clocked comparator, and a DAC, as shown in Figure 5.1. The integrator and the DAC are constructed using the 65nm CMOS process model [36], whereas the comparator is modeled as an ideal component using an ideal operational amplifier (OPAMP) and DFF. The supply voltage is taken as $1V$. Also, the OSR is determined as 128, and the frequency of the input signal is chosen as 124Hz.

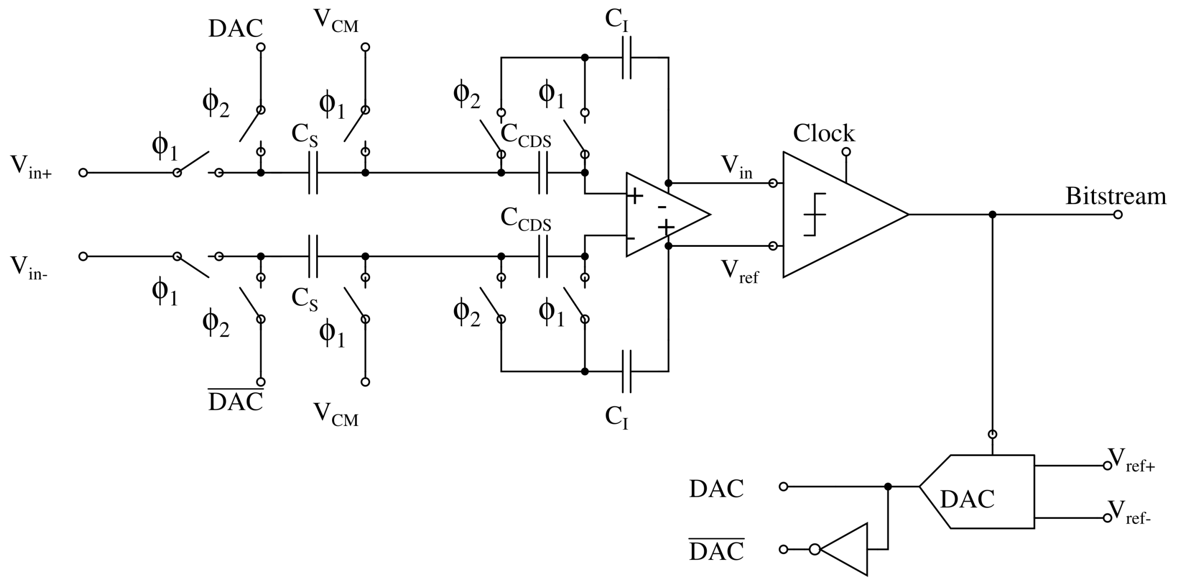

Figure 5.1. The block diagram of the designed sigma-delta modulator.

5.1.1. Blocks of the Designed Sigma-Delta Modulator

5.1.1.1. Integrator. Integrator is a block that realizes the integration process. In other words, it takes time integral of its input and reflects it to the output. This block is responsible for noise shaping in the sigma-delta modulator by shifting the quantization noise to the higher frequencies, and this noise can be filtered by a filter at the output of the sigma-delta modulator. A switched-capacitor integrator, which consists of an operational transconductance amplifier (OTA), capacitors, and switches, has been designed in this thesis. The designed switched-capacitor integrator, which also includes correlated double sampling (CDS) to eliminate the OTA's offset, is shown in Figure 5.2. The clocks ϕ_1 and ϕ_2 that control the integrator are nonoverlapping clocks. During the ϕ_1 phase, the input voltage is sampled on the capacitor C_S. After this phase, the ϕ_2 phase starts, and a charge emerges by C_S in proportion to a voltage value as the difference between the input voltage and the output of the DAC [1].

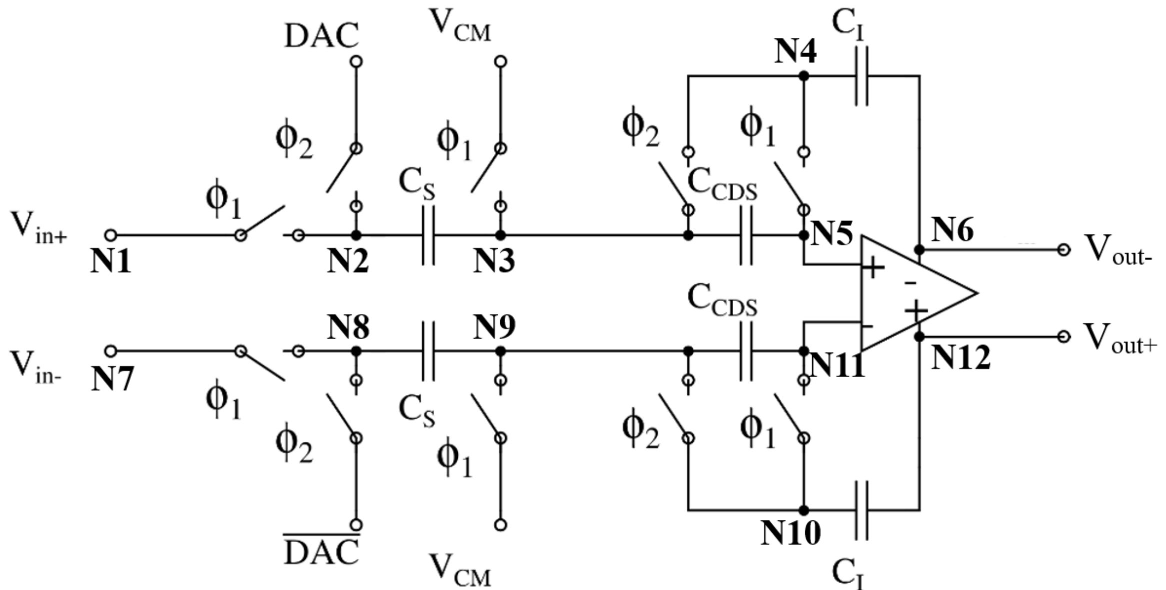

Figure 5.2. The designed switched-capacitor integrator.

- Operational Transconductance Amplifier (OTA): OTA is an analog circuit that produces an output current according to the applied input voltages. It amplifies the differential input voltage, and creates a current at the output. This output current is converted into an analog voltage with the help of output resistance. OTA is a key component in a sigma-delta modulator to be able to achieve a high SNR value, which determines the effective number of bits (ENOB) of the system. Open-loop gain of the OTA has to be large to be able to obtain a satisfying SNR value.

  Fully differential folded cascode OTA topology, which is shown in Figure 5.3, has been used in the sigma-delta modulator. M1, M2, M5, and M6 provide current to the circuit by behaving as current sources, and M7, M8, M9, and M10 increase the output resistance, which results in an increase in the current. Also, the folded cascode OTA needs a common-mode feedback (CMFB) circuit and a bias circuit. The common-mode feedback circuit controls the PMOS transistor (M2 in Figure 5.3), which takes charge in providing current. It provides a bias voltage for the mentioned transistor to keep the bias voltage at the desired voltage. The

preferred common-mode feedback circuit involves a voltage controlled voltage source (VCVS), two resistors with high resistances, and a voltage source as the reference voltage for the common-mode feedback circuit. The schematic of the common-mode feedback circuit is shown in Figure 5.4. In addition to that, ideal voltage sources are used in the OTA to bias the transistors instead of designing a bias circuit.

The open-loop gain of the designed OTA has been obtained as 58.24 dB in the AC simulation as shown in Figure 5.5. Also, the transient simulation result is shown in Figure 5.6, where the input signal is 200µV.

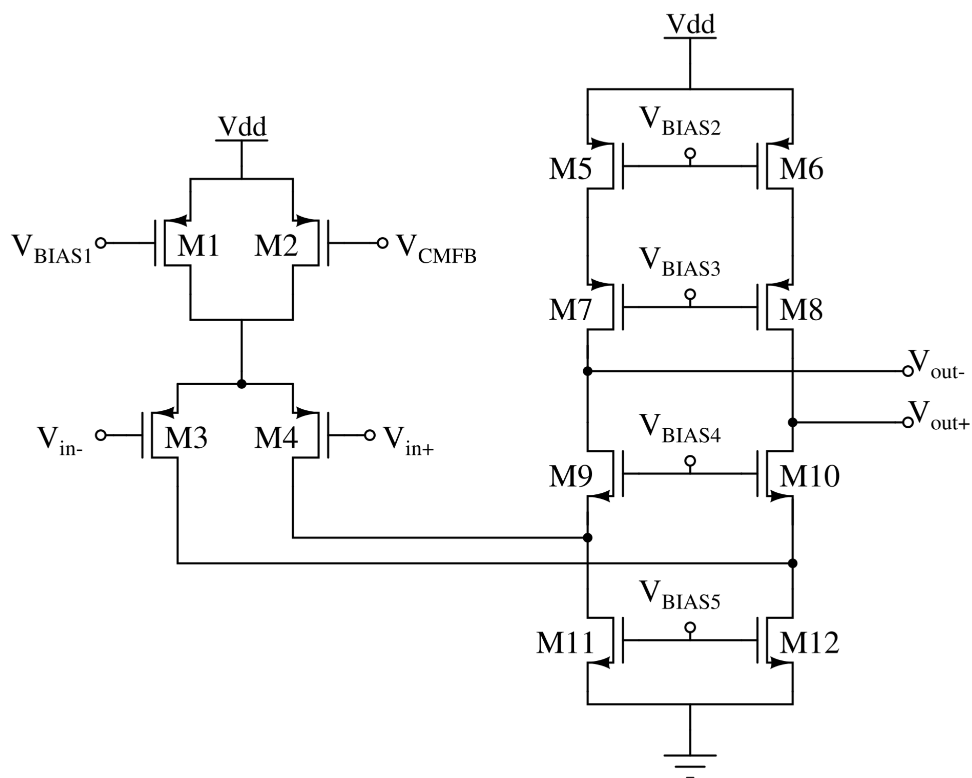

Figure 5.3. The designed folded cascode OTA.

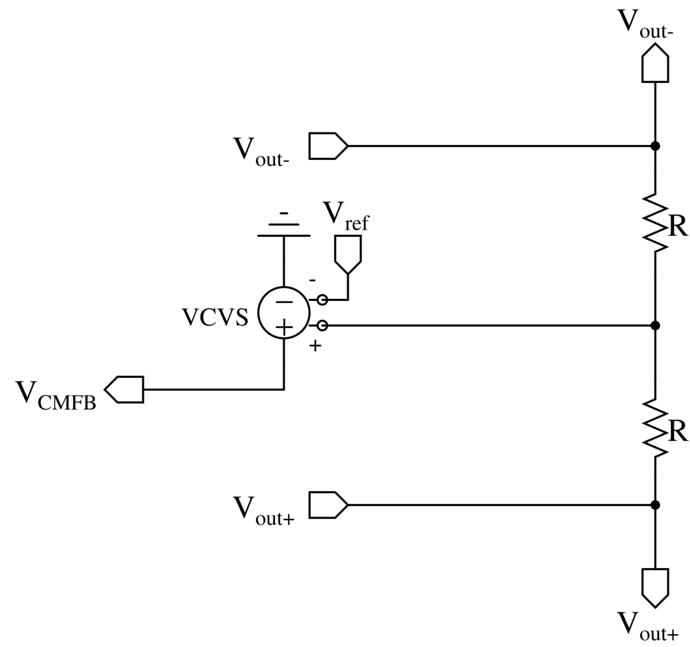

Figure 5.4. The designed common-mode feedback circuit.

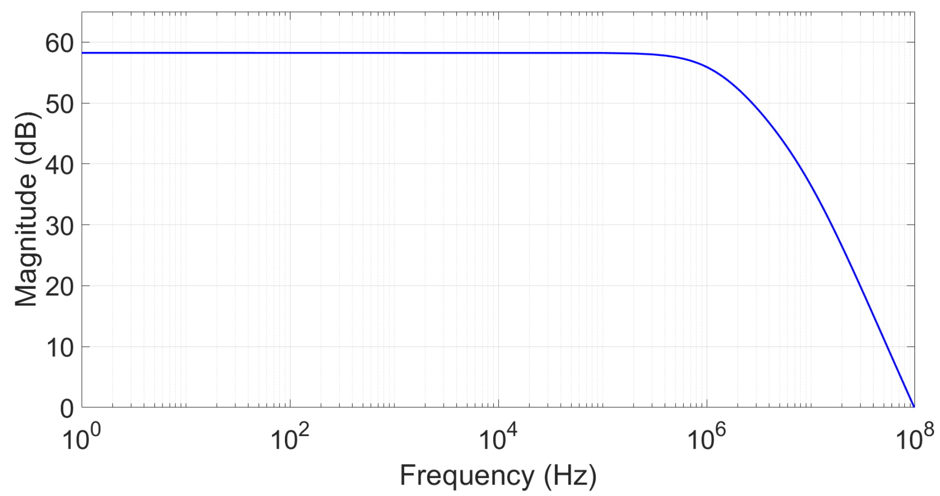

Figure 5.5. The AC simulation result of the designed OTA.

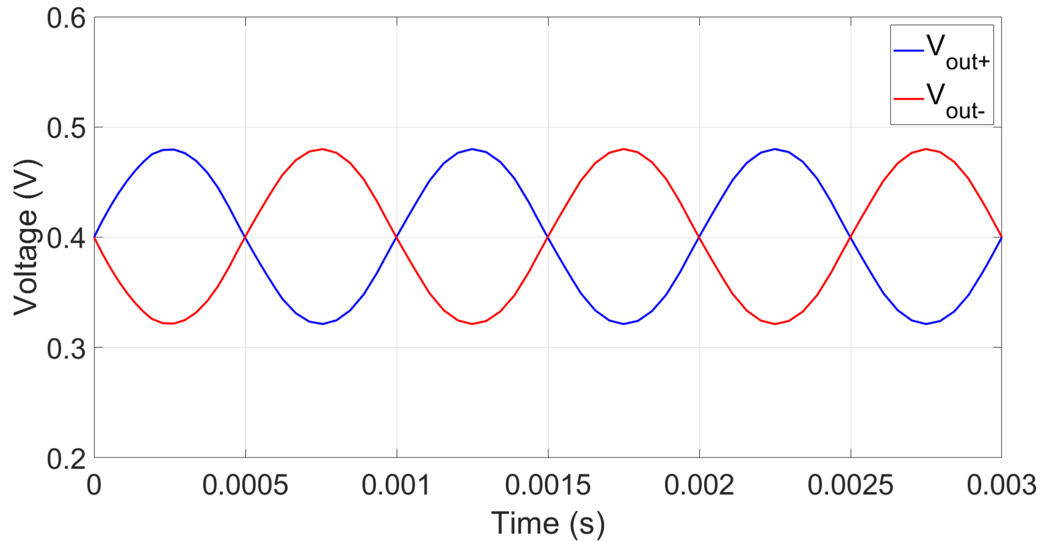

Figure 5.6. The transient simulation result of the designed OTA.

5.1.1.2. Comparator. Contrary to the previous chapters, an ideal clocked comparator has been designed for this study to be able to speed up the simulations. The designed comparator consists of an ideal OPAMP and a DFF as shown in Figure 5.7. If the input V_{in} is greater than the input V_{ref} at the rising edge of the clock, the clocked comparator gives *1* as mentioned in the previous chapters.

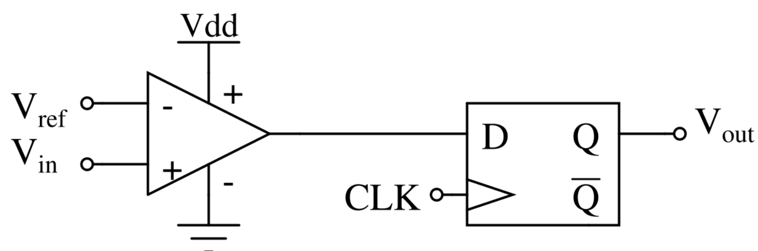

Figure 5.7. The designed ideal clocked comparator.

5.1.1.3. DAC. A 1-bit DAC is used since there are only two analog inputs (V_{ref+} and V_{ref-}) for the DAC. The designed DAC is shown in Figure 5.8. If the signal (V_{cnt}) that controls the DAC is *1*, it transmits V_{ref+} to the output. Otherwise, V_{ref-} is observed.

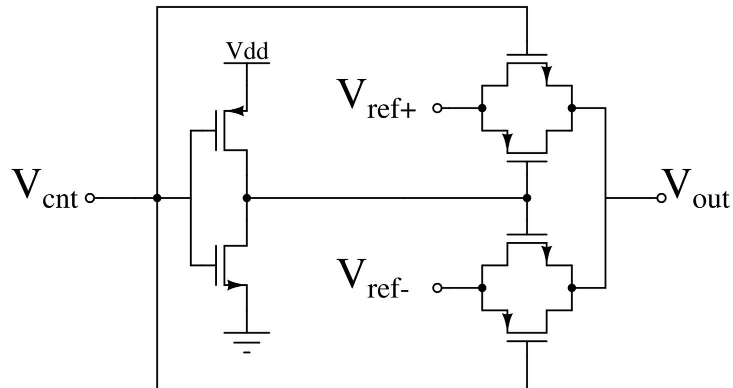

Figure 5.8. The designed 1-bit DAC.

5.1.2. Operation of the Designed Sigma-Delta Modulator

The input voltage is sampled by the sample and hold circuit. Then, the output voltage of the DAC is subtracted from the sampled input voltage. After that, the integrator gets involved in integrating the obtained voltage by adding it to the value from the previous integration step. Integrated signals, which are the outputs of the integrator, are compared by the comparator, and *0* or *1* is obtained at the output of the sigma-delta modulator. This output controls the DAC to give V_{ref+} or V_{ref-} as feedback for the next conversion. As a result of several conversions, a bitstream is obtained at the output of the sigma-delta modulator as shown in Figure 5.9. This bitstream is converted into an output code through the digital filter and decimator.

Table 5.1 shows the maximum achievable SNR and ENOB values for a first-order sigma-delta modulator according to the chosen OSR value. The relationship between the SNR and ENOB is as

$$ENOB = \frac{SNR_{db} - 1.76}{6.02}, \tag{5.1}$$

where SNR_{db} is as defined before.

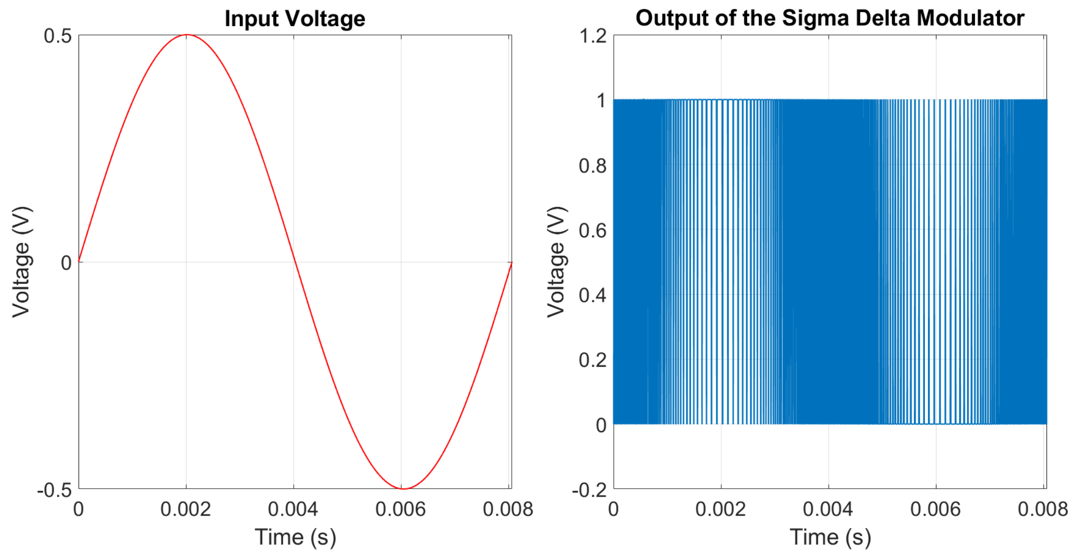

Figure 5.9. The input and the output of the sigma-delta modulator.

The obtained SNR value at the end of the simulation of the designed sigma-delta modulator is 52.1 dB, whose ENOB equivalent is 8.36 bits. The power spectral density (PSD) of the output of the designed sigma-delta modulator is shown in Figure 5.10.

Table 5.1. The maximum achievable SNR and ENOB values for a first-order sigma-delta modulator according to the chosen OSR value.

OSR	**SNR**	**ENOB**
32	41.74 dB	6.64 bits
64	50.77 dB	8.14 bits
128	59.80 dB	9.64 bits
256	68.83 dB	11.14 bits
512	77.85 dB	12.64 bits

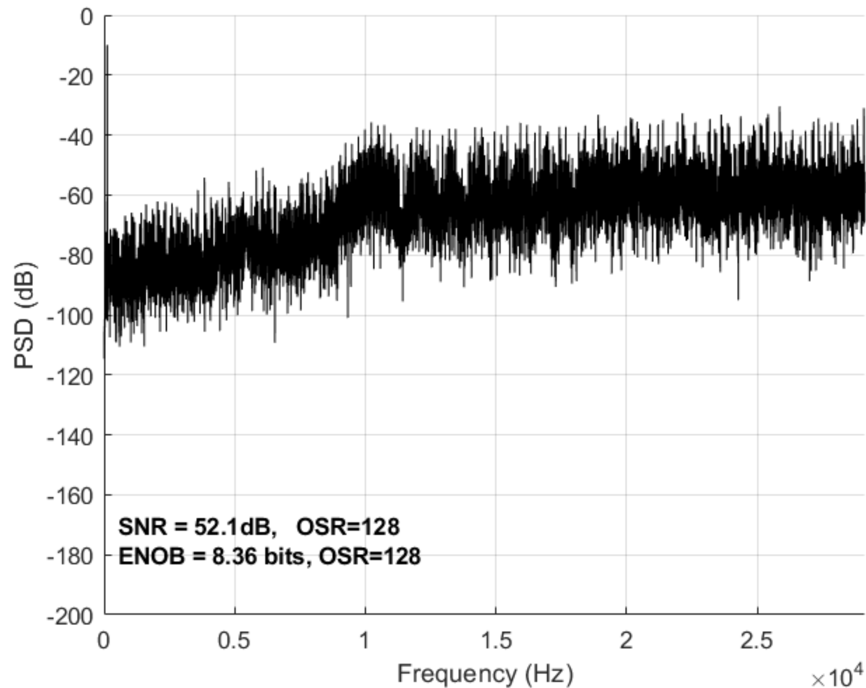

Figure 5.10. The PSD of the output of the designed sigma-delta modulator.

5.2. Radiation Performance of the Designed Sigma-Delta Modulator

The designed transistor-level sigma-delta modulator has been tested under modeled radiation, as in previous chapters. Since TID has more effect on continuous-time analog circuits, the comparator has been exposed to TID. On the other hand, the nodes in the integrator have been simulated under SET since this type of radiation creates more dramatic results for the switched-capacitor circuits. These simulations have been done in LTspice using the 65nm CMOS BPTM model [36].

5.2.1. Permanent Radiation Effect

The input offset voltage of the comparator is shifted by $\pm 1\sigma$ offsets to be able to reflect the TID effect to the sigma-delta modulator. At this point, σ value has been chosen as 15.02mV as obtained in the RadiSPICE simulations of the comparator,

as in Figure 4.10. A series voltage source with $\pm1\sigma$ voltages to V_{in} input of the comparator has been added to shift the input offset voltage for the TID simulations of the sigma-delta modulator as in Figure 5.11, where $N13$ represents the output V_{out-} of the integrator. Three different simulations (with $\pm1\sigma$ offsets and without external additional offset) have been performed.

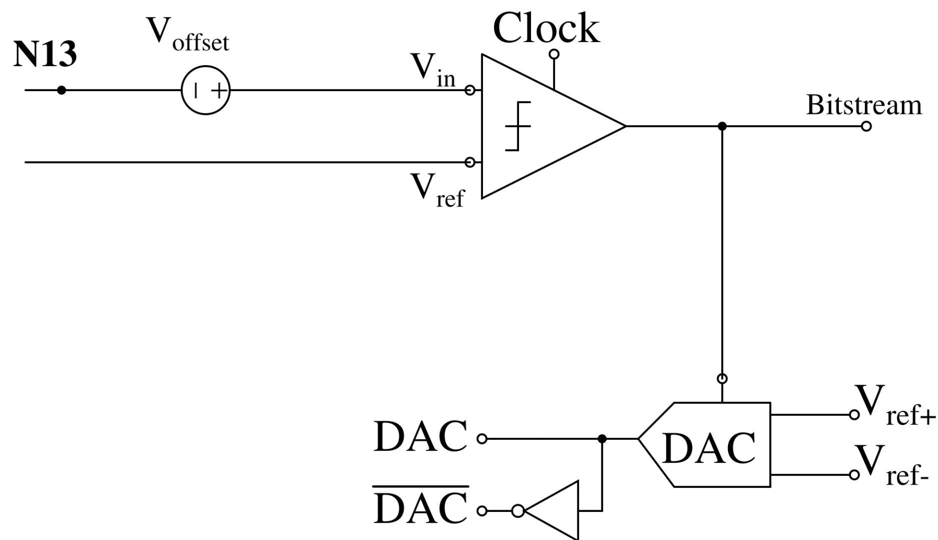

Figure 5.11. The added offset voltage to the comparator.

The PSD of the output of the sigma-delta modulator with and without TID is shown in Figure 5.12. Although the expected SNR value is 52.1 dB, the SNR values of the sigma-delta modulator with $+1\sigma$ comparator offset and -1σ comparator offset are obtained as 43.4 dB and 43.1 dB, respectively. It is seen in Figure 5.12 that there is a low-frequency noise, which cannot be suppressed due to TID compared to the result without permanent radiation. For this reason, a decrease in SNR is observed.

To be able to understand the reason for the SNR decrease and examine the effect of TID on the comparator, the inputs of the comparator, which are the outputs of the integrator, have been focused on. The first inaccurate decision made by the comparator has been examined for this reason. Figure 5.13 shows the comparator inputs and bitstream taken by the sigma-delta modulator without radiation, whereas

Figure 5.14 figures out the input of the comparator and the bitstream in which the comparator of the sigma-delta modulator has $+1\sigma$ offset. The mentioned figures involve a small portion of the simulation result. When the mentioned graphs are compared, it is seen that the differences between the bitstreams start around 280μs. This time can be examined in the comparator inputs. As marked in Figure 5.13, the V_{ref} input of the comparator is greater than the V_{in} input. Therefore, the comparator gives *0* as the output, and DAC transmits V_{ref-} to the integrator. However, the comparator gives *1* due to $+1\sigma$ offset of the comparator in the permanent radiation case in Figure 5.14. Also, the green plot belongs to the voltage before adding the additional offset ($N13$ in Figure 5.11), which is also less than V_{ref}. The bitstream is not affected before 280μs since the voltage differences between V_{in} and V_{ref} are much more than $+1\sigma$ offset. Since the bitstream is changed compared to the radiation-free case, the DAC, which is controlled by the comparator output, transmits inaccurate voltages to the integrator. Then, the integrator cannot work properly. As a result of this, the operation of the sigma-delta modulator is affected negatively.

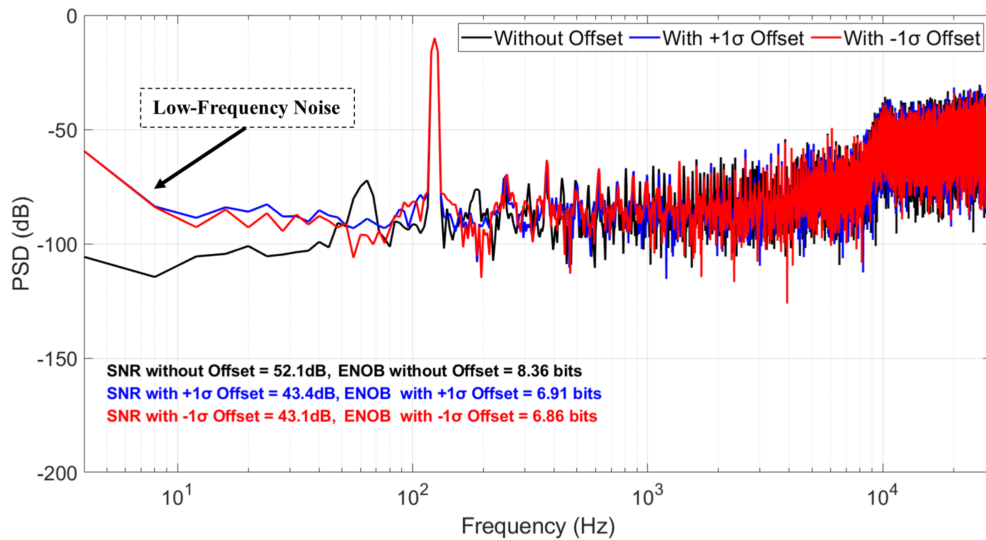

Figure 5.12. The PSD of the output of the designed sigma-delta modulator with and without permanent radiation.

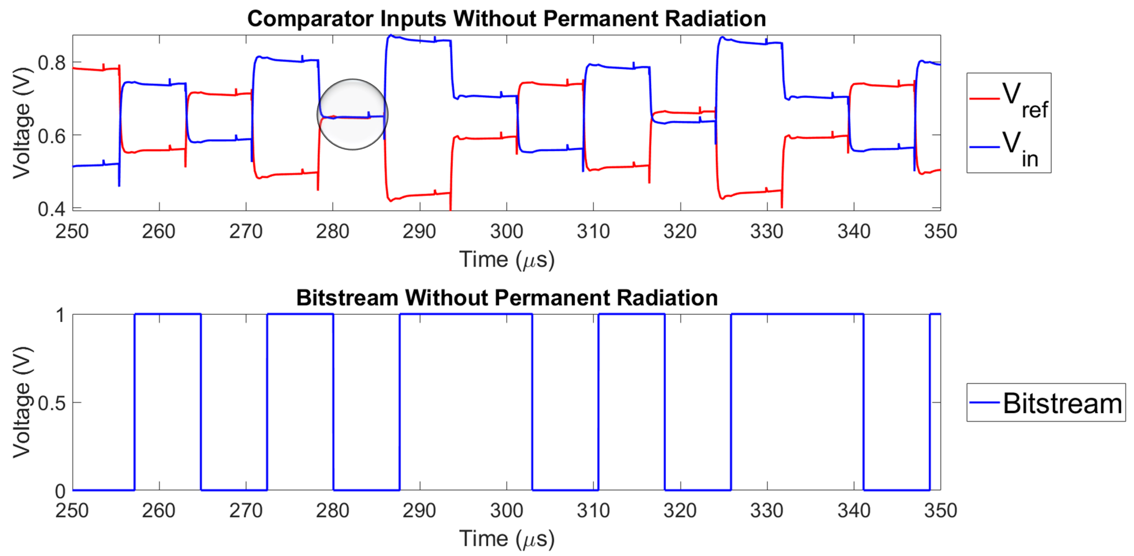

Figure 5.13. The comparator input voltages and the bitstream without TID.

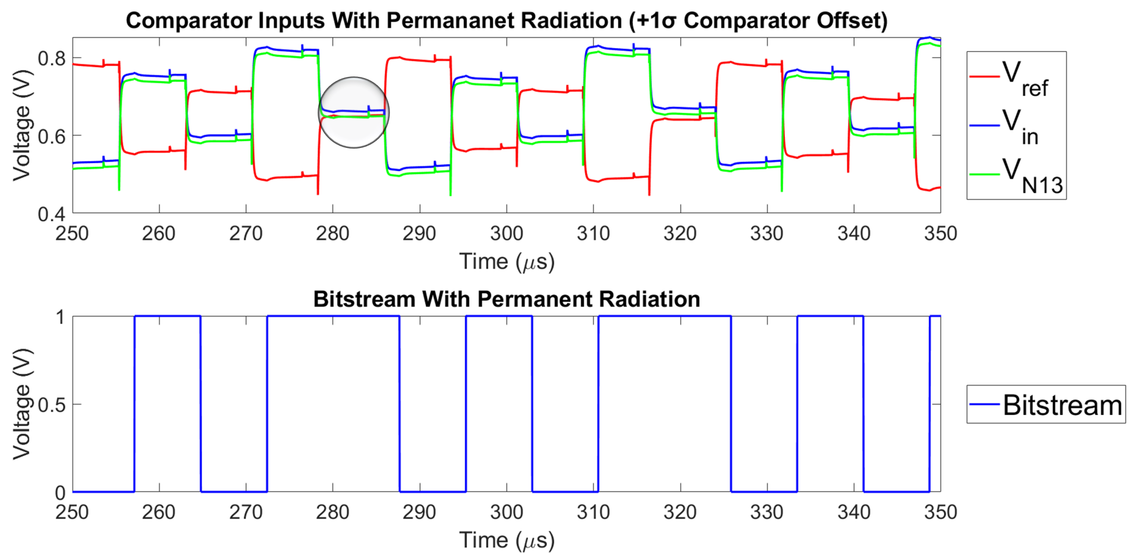

Figure 5.14. The comparator input voltages and the bitstream with TID.

For the case of -1σ comparator offset, the simulation results can be obtained as in $+1\sigma$ offset case. There is a small portion of the simulation result in Figure 5.15, which belongs to the radiation-free case. Also, the simulation result with -1σ comparator

offset with the same time interval exists in Figure 5.16. The first difference between the bitstreams is observed at around 105μs, which are marked on the mentioned figures. As seen in Figure 5.15, the V_{in} input of the comparator is greater than V_{ref}, which results in *1* in the bitstream. However, the decision is made inaccurately at the mentioned time in Figure 5.16. This is due to the decreased comparator offset. The V_{in} input of the comparator is pulled down by 15.02mV compared to the green plot, which belongs to the voltage before adding -1σ offset, in the corresponding figure. Since the input V_{in} stays below the input V_{ref}, an erroneous bit decision is made at this time. This wrong decision causes the sigma-delta modulator to work improperly.

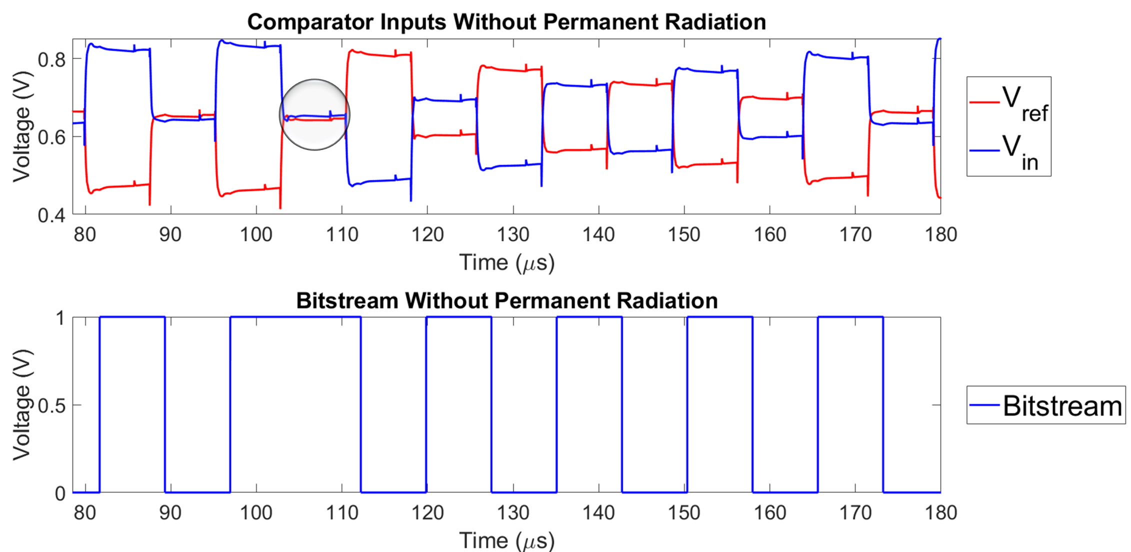

Figure 5.15. The comparator input voltages and the bitstream without TID.

5.2.2. Temporary Radiation Effect

Rectangular-shaped current pulses with three different ON times have been applied to the nodes in the integrator, which are shown in Figure 5.2, to mimic the SET effect. The applied current pulses represent the charge increase effect of the SET event. The ENOB values have been measured when the SET event occurs at different nodes at four different times. The determined application times can be seen in Figure 5.17.

One of the created tables is shown in Table 5.2. This table shows the ENOB values when the duration of the SET is 1.69μs which also equals the ON time of the clocks in the sigma-delta modulator. The expected ENOB value is 8.36 bits, which has been obtained at the end of the simulation of the sigma-delta modulator without radiation. According to this table, it can be seen that there is no expected ENOB value, the SNR of the sigma-delta modulator is affected by the SET event in all circumstances. However, this is observed from Table 5.2 that applying SET to the nodes $N3$, $N4$, $N5$, $N9$, $N10$, and $N11$ individually creates the largest ENOB errors.

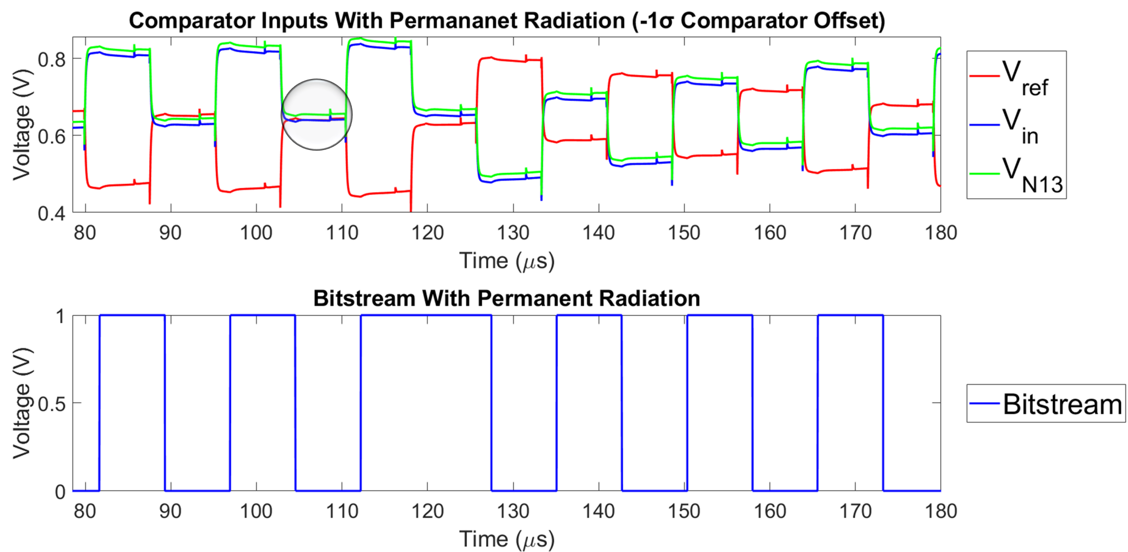

Figure 5.16. The comparator input voltages and the bitstream with TID.

The simulation results that focus on the output of the integrators with and without temporary radiation are shown in Figure 5.18. This figure shows the simulation result in which temporary radiation is applied to the node $N5$ at 2.02 ms for 1.69μs. As shown in this figure, there is a voltage increase in V_{out+} and a voltage decrease in V_{out-} when temporary radiation is applied. This arises due to a charge increase effect of SET, which is applied to the node $N5$ of the integrator. However, this effect disappears for the next conversion cycles, as can be seen in the corresponding figure, and the integrator outputs start to give closer values to the expected voltages. The effect of

this radiation on the output of the sigma-delta modulator can be seen in Figure 5.19, which includes a part of the simulation. The output of the sigma-delta modulator turns into *0* at 2.02ms in the temporary radiation case. Since V_{out+} of the integrator, which is connected to V_{ref} input of the comparator, increases and V_{out-}, which is connected to V_{in} input of the comparator, decreases as in Figure 5.18, the comparator gives *0* at 2.02ms. However, the bitstreams start to be the same around 3.45ms, the sigma-delta modulator compensates for the effect of SET. Since the sigma-delta modulator has a feedback circuit, the integrator continues to give outputs properly after a certain point. Nevertheless, the change in the bitstream for 1.43ms causes missing 3.83 bits in ENOB.

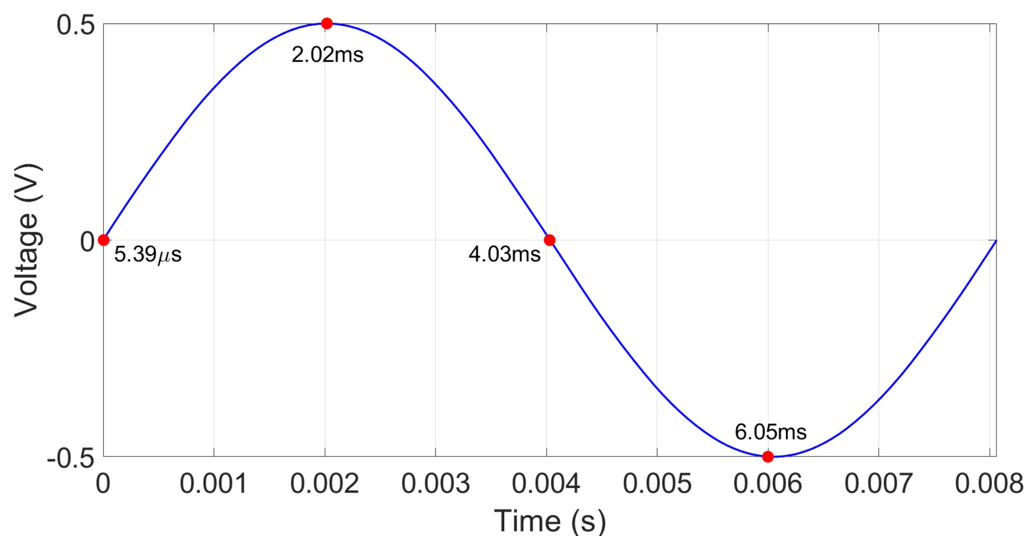

Figure 5.17. The application times of SET shown on the input sinus wave.

When the PSD of the output of the sigma-delta modulator (with and without SET), which is in Figure 5.20, is examined, it is seen that there is an unsuppressed noise in the low-frequency region, which causes a drop in ENOB, as in permanent radiation. Contrary to the permanent radiation case, the noise around the signal region in the temporary radiation case is also much greater than the expected noise.

Table 5.2. ADC ENOBs under SET with 1.69μs duration.

Expected ENOB : 8.36 bits				
Applied	**Temporary radiation is applied at**			
Nodes	**5.39µs**	**2.02ms**	**4.03ms**	**6.05ms**
N1	6.35	6.74	6.21	5.93
N2	6.68	7.21	6.82	6.58
N3	5.03	4.5	4.88	6.59
N4	5	4.5	4.88	6.59
N5	5	4.53	4.88	6.59
N6	7.54	7.55	7.46	7.67
N7	6.34	6.01	6.36	7.31
N8	6.65	6.39	6.62	7.16
N9	4.99	6.06	5.09	4.46
N10	4.96	6.06	5.09	4.46
N11	4.99	6.06	5.09	4.47
N12	7.68	7.39	7.73	7.74

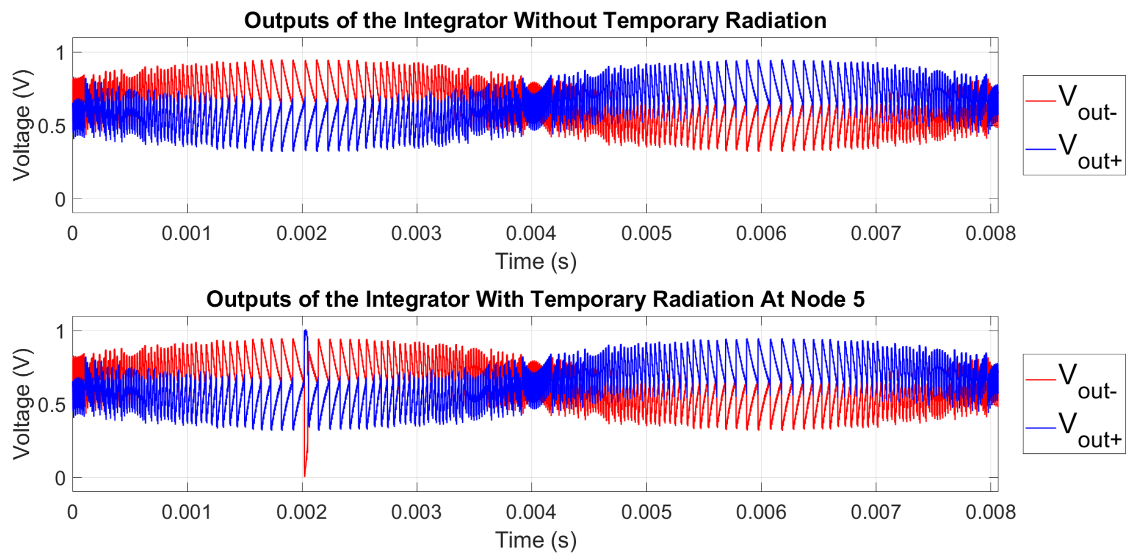

Figure 5.18. Outputs of the integrator with and without temporary radiation at node 5. Temporary radiation is applied at 2.02ms in the lower figure.

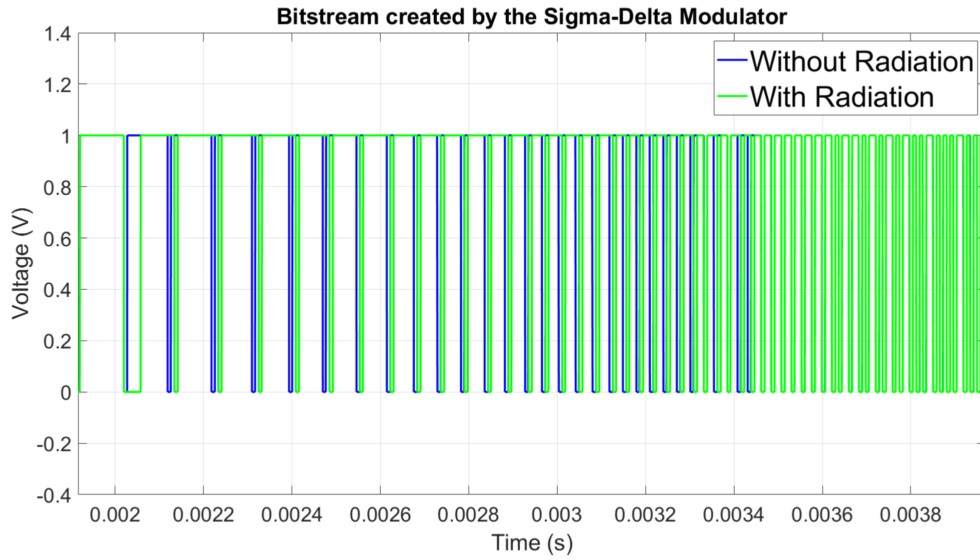

Figure 5.19. Output of the sigma-delta modulator with and without temporary radiation at node 5. Temporary radiation is applied at 2.02ms in the green plot.

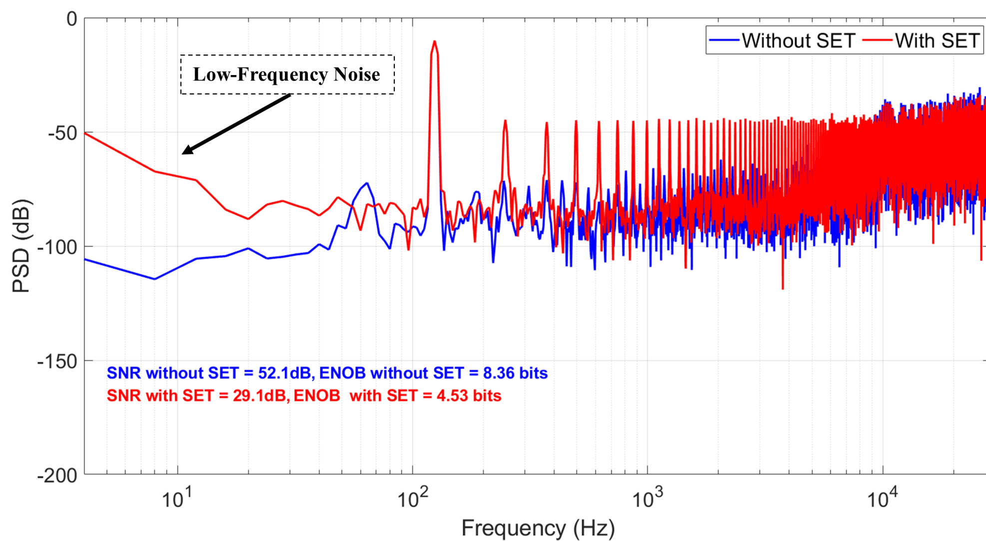

Figure 5.20. The PSD of the output of the designed sigma-delta modulator with and without temporary radiation.

Similar tables, which are shown in Appendix D, to Table 5.2 have been constructed for two additional SET durations; 8.48µs and 50µs. The application times and the applied nodes are the same as in the given above. The aim of constructing the tables for three different SET duration is to generalize about the sensitive nodes and the application times that create more vital failures. Also, it can be observed how much effect different SET durations have on ENOB. The average error table, which is shown in Table 5.3, has been constructed for the nodes in the integrator. According to this table, it can be generalized that nodes $N3$, $N4$, $N5$, $N9$, $N10$, and $N11$ are more sensitive to the SET events. Also, Table 5.4 shows that applying SET at 5.39µs and 4.03ms causes more decrease in ENOB. In addition to these, using Table 5.5, it has been proved that if the SET duration is prolonged, ENOB decreases more.

Table 5.3. ADC average ENOB errors in bits due to SET for the nodes in the integrator.

Nodes	**N1**	**N2**	**N3**	**N4**	**N5**	**N6**	**N7**	**N8**	**N9**	**N10**	**N11**	**N12**
Average Error	-2.52	-1.36	-3.55	-3.55	-3.55	-1.69	-2.44	-1.39	-3.63	-3.63	-3.63	-1.49

Table 5.4. ADC average ENOB errors in bits due to SET for different application times.

Applied at	**5.39µs**	**2.02ms**	**4.03ms**	**6.05ms**
Average Error	-2.9	-2.58	-2.86	-2.47

Table 5.5. ADC average ENOB errors in bits for different SET durations.

Duration	**1.69µs**	**8.48µs**	**50µs**
Average Error	-2.31	-2.44	-3.35

5.3. Conclusion

In this chapter, the designed sigma-delta modulator is tested under temporary and permanent radiation effects. The TID simulations, which involve additional input offset voltage for the comparator, show that permanent radiation causes low-frequency noise to cannot be suppressed, which results in a decrease in SNR. On the other side, the integrator of the sigma-delta modulator is exposed to temporary radiation, which is mimicked using a rectangular-shaped current pulse. It is seen that amount of decrease in SNR varies depending on the affected node, application time, and duration of the event. The most sensitive nodes are determined as $N3$, $N4$, $N5$, $N9$, $N10$, and $N11$. Also, applying temporary radiation at the starting point and the midpoint of the input sinus wave, which are 5.39μs and 4.03ms, causes lower SNR. In addition to these inferences, a generalization can be made, which is the longer the temporary radiation, the lower the SNR.

6. CONCLUSION AND FUTURE WORK

In this thesis, designs and radiation analyses of three different ADCs are presented. Each ADC is examined under permanent and temporary radiation effects individually.

In Chapter 3, a 4-bit flash ADC is designed, and it is analyzed under permanent radiation, which is TID. It has been observed that non-fixed permanent radiation causes missing codes of the output codes of the flash ADC, whereas fixed permanent radiation only changes the DNL of the first and the last output codes.

In Chapter 4, two different SAR ADCs with capacitive DACs, which are split capacitor array DAC and C-2C ladder-based DAC, are designed. These ADCs have been tested under permanent and temporary radiation effects separately. It has been observed that the permanent radiation effect causes missing output codes, whereas the temporary radiation effect may induce bit flips. The sensitive nodes in the DACs are detected through temporary radiation simulations. It is proved that the SAR ADC with split capacitor array DAC has better performance under temporary radiation compared to the SAR ADC with C-2C ladder-based DAC.

In Chapter 5, a sigma-delta modulator is designed to test under permanent and temporary radiation effects. It is reached that permanent radiation reduces the SNR of the sigma-delta modulator since the low-frequency noise cannot be suppressed. Similar to permanent radiation, it is obtained that temporary radiation also causes a drop in SNR. The amount of decrease differs from the applied node, application time, and duration of the radiation event. The sensitive nodes in the integrator are specified according to temporary radiation simulations. Also, it is presented which application time causes how much reduction in SNR. In addition, it is demonstrated that the drop in SNR is directly proportional to the duration of the temporary radiation.

This study aims to contribute to improved radiation-hardened ADC designs by providing valuable information.

6.1. Future Work

Schematic-level radiation simulations of the flash ADC, SAR ADC, and sigma-delta modulator have been completed, and the results have been obtained. In the next step, layout-level radiation simulations for these ADC architectures can be performed, and this study can be taken a step further.

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APPENDIX A: THE MATLAB CODE USED FOR THE SET SIMULATIONS

```
format long
filename='TestDost.txt';
Qin=0.25e-12;
imaxin=200;
imax=imaxin;

A2 = regexp( fileread(filename), '\n', 'split');
 ntemp=size(A2);
 nson=ntemp(2);
  ctest=0;
  cname=0;
  for ifirst = 1:nson
   if (A2{1,ifirst}(1)=='C')
        A1=split(A2{ifirst});
        Cname(cname+1)=A1(1);
       Cnode(ctest+1)=A1(2);
        Cnode(ctest+2)=A1(3);
        ctest=ctest+2;
        cname=cname+1;
   end
end
Cnodefinal=unique(Cnode);
rows=size(Cnodefinal');
columns=imaxin+1;
fid6 = fopen('CapacitorSET.cir', 'w');
fclose(fid6);

    fid2 = fopen('CapacitorSET.cir','w');
    fwrite= '*currentlist';
    dlmwrite('CapacitorSET.cir', fwrite, 'delimiter','');
    for ison=1:imax
        if (ison>1)
        fwrite= '.alter';
    dlmwrite('CapacitorSET.cir', fwrite,'-append', 'delimiter','');
        end
   for j=1:size(Cnodefinal')
          rtau1=0.025e-9;
          ftau1=4*rtau1;
        if(j==1)
          rd1=100e-6;
        else
           rd1=(fd1+(75*ftau1)+100e-6);
        end

  fd1=rd1+(3*rtau1);
  Q=normrnd(Qin,0.02e-12);
  I2=Q/(rtau1+ftau1+(fd1-rd1)-(rtau1*exp((rd1-fd1)/rtau1)));

I1=num2str(0 );
I2new=num2str(I2,16);
rd=num2str(rd1,16);
fd=num2str(fd1,16);
ftau=num2str(ftau1,16);
rtau=num2str(rtau1,16);
c=sprintf('Ix%d',j);
        fwrite1= ['Ix' num2str(j) ' ' '0'  ' ' Cnodefinal(j)   ' exp( ' I1 ' ' I2new ' ' rd ' ' rtau ' ' fd ' ' ftau ' )' ];
        dlmwrite('CapacitorSET.cir', fwrite1, '-append','delimiter','','precision',35);
      CurrentSources(j,1)=j;
        CurrentSources(j,ison+1)=I2;
   end
    end
fclose(fid2);

xlswrite('CurrentSources.xlsx',CurrentSources);
```

Figure A.1. The MATLAB code that determines the amplitude of the SET current pulse, which is used in the SET simulations of the designed ADCs.

APPENDIX B: TEMPORARY RADIATION RESULTS OF THE SAR ADC WITH SPLIT CAPACITOR ARRAY DAC

Table B.1. ADC output codes with split capacitor array DAC under SET when the expected output code is 00110111.

Expected Code : 00110111						
Applied Nodes	**Temporary radiation is applied at**					
	0 µs	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	00110111	00**000**0**000**	001**0**0**000**	00110**000**	001101**00**	0011011**0**
N9	0011**1000**	0**1001**11**0**	0011**1**111	00110111	00110111	00110111
N8	00110111	0**100**0**0**1**0**	0011**100**1	00110111	00110111	00110111
N6	00110111	0011**1000**	00110111	00110111	00110111	00110111
N5	00110111	0011**100**1	00110111	00110111	00110111	00110111
N2	00110111	0011**1000**	00110111	00110111	00110111	00110111

Table B.2. ADC output codes with split capacitor array DAC under SET when the expected output code is 10000000.

Expected Code : 10000000						
Applied Nodes	**Temporary radiation is applied at**					
	0 µs	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	10000000	**0**0000000	10000000	10000000	10000000	10000000
N9	10000000	**01111111**	10000000	10000000	10000000	10000000
N8	10000000	**01111111**	10000000	10000000	10000000	10000000
N6	10000000	10000000	10000000	10000000	10000000	10000000
N5	10000000	10000000	10000000	10000000	10000000	10000000
N2	10000000	10000000	10000000	10000000	10000000	10000000

Table B.3. ADC output codes with split capacitor array DAC under SET when the expected output code is 10110011.

Expected Code : 10110011						
Applied Nodes	**Temporary radiation is applied at**					
	0 µs	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	10110011	00000000	10100000	10110000	10110000	10110000
N9	10110011	01111111	10110011	10110011	10110011	10110011
N8	10110011	01111111	10110011	10110011	10110011	10110011
N6	10110011	10110011	10110011	10110011	10110011	10110011
N5	10110011	10110011	10110011	10110011	10110011	10110011
N2	10110011	10110011	10110011	10110011	10110011	10110011

Table B.4. ADC output codes with split capacitor array DAC under SET when the expected output code is 11111111.

Expected Code : 11111111						
Applied Nodes	**Temporary radiation is applied at**					
	0 µs	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	11111111	00000000	11100000	11110000	11111100	11111110
N9	11111111	11111111	11111111	11110111	11111111	11111111
N8	11111111	11111111	11111111	11110111	11111111	11111111
N6	11111111	11111111	11111111	11110111	11111111	11111111
N5	11111111	11111111	11111111	11111111	11111111	11111111
N2	11111111	11111111	11111111	11111111	11111111	11111111

APPENDIX C: TEMPORARY RADIATION RESULTS OF THE SAR ADC WITH C-2C LADDER BASED DAC

Table C.1. ADC output codes with C-2C ladder-based DAC under SET when the expected output code is 00110111.

Expected Code : 00110111						
Applied	**Temporary radiation is applied at**					
Nodes	**0 µs**	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	00110111	00000000	00100000	00110000	00110100	00110110
N16	00110111	01000101	00111111	00110111	00110111	00110111
N7	00110111	00001101	00100000	00110000	00110100	00110110
N15	00110111	01000010	00111000	00110111	00110111	00110111
N4	00110111	00000000	00100000	00110000	00110100	00110110
N12	00110111	00111011	00110111	00110111	00110111	00110111
N1	00110111	00000000	00100000	00110000	00110100	00110110
N9	00110111	00111001	00110111	00110111	00110111	00110111

Table C.2. ADC output codes with C-2C ladder-based DAC under SET when the expected output code is 10000000.

Expected Code : 10000000						
Applied	**Temporary radiation is applied at**					
Nodes	**0 µs**	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	10000000	00000000	10000000	10000000	10000000	10000000
N16	10000000	01111111	10000000	10000000	10000000	10000000
N7	10000001	00001110	10000000	10000000	10000000	10000000
N15	10000000	01111111	10000000	10000000	10000000	10000000
N4	10000000	00000000	10000000	10000000	10000000	10000000
N12	10000000	10000001	10000000	10000000	10000000	10000000
N1	10000000	00000000	10000000	10000000	10000000	10000000
N9	10000000	10000000	10000000	10000000	10000000	10000000

Table C.3. ADC output codes with C-2C ladder-based DAC under SET when the expected output code is 10110011.

Expected Code : 10110011						
Applied	**Temporary radiation is applied at**					
Nodes	**0 µs**	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	10110011	00000000	10100000	10110000	10110000	10110010
N16	10110011	01111111	10110011	10110011	10110011	10110011
N7	10110011	00001110	10100000	10110000	10110000	10110010
N15	10110011	01111111	10110011	10110011	10110011	10110011
N4	10110011	00000000	10100000	10110000	10110000	10110010
N12	10110011	10110011	10110011	10110011	10110011	10110011
N1	10110011	00000000	10100000	10110000	10110000	10110010
N9	10110011	10110011	10110011	10110011	10110011	10110011

Table C.4. ADC output codes with C-2C ladder-based DAC under SET when the expected output code is 11111111.

Expected Code : 11111111						
Applied	**Temporary radiation is applied at**					
Nodes	**0 µs**	**10.5µs**	**13.01µs**	**14.75µs**	**16.01µs**	**17.01µs**
NOut	11111111	00000000	11100000	11110000	11111100	11111110
N16	11111111	11111111	11111111	11110111	11111111	11111111
N7	11111111	00001110	11100000	11110000	11111100	11111110
N15	11111111	11111111	11111111	11110111	11111111	11111111
N4	11111111	00000000	11100000	11110000	11111100	11111110
N12	11111111	11111111	11111111	11111111	11111111	11111111
N1	11111111	00000000	11100000	11110000	11111100	11111110
N9	11111111	11111111	11111111	11111111	11111111	11111111

APPENDIX D: TEMPORARY RADIATION RESULTS OF THE SIGMA-DELTA MODULATOR

Table D.1. ADC ENOBs under SET with 8.48μs duration.

Expected ENOB : 8.36 bits				
Applied Nodes	**Temporary radiation is applied at**			
	5.39µs	**2.02ms**	**4.03ms**	**6.05ms**
N1	5.94	7.02	5.87	5.53
N2	6.97	7.35	7.04	7.23
N3	4.7	4.28	4.74	6.4
N4	4.7	4.27	4.74	6.4
N5	4.7	4.29	4.74	6.4
N6	7.04	7.34	7.37	7.16
N7	6.1	5.52	6.19	7.05
N8	6.62	6.87	7.02	7.52
N9	4.72	5.92	4.72	4.21
N10	4.72	5.92	4.71	4.2
N11	4.7	5.92	4.72	4.22
N12	7.3	7.7	7.78	7.85

Table D.2. ADC ENOBs under SET with 50μs duration.

Expected ENOB : 8.36 bits				
Applied Nodes	**Temporary radiation is applied at**			
	5.39µs	**2.02ms**	**4.03ms**	**6.05ms**
N1	4.73	6.9	4.73	4.24
N2	7.16	7.14	7.13	6.86
N3	3.84	3.17	3.89	5.85
N4	3.84	3.17	3.89	5.85
N5	3.84	3.17	3.89	5.85
N6	5.18	6.5	5.24	4.13
N7	4.74	4.24	4.77	6.5
N8	7.27	7.02	7.34	7.22
N9	3.82	5.92	3.85	3.15
N10	3.82	5.92	3.85	3.15
N11	3.83	5.85	3.86	3.15
N12	5.26	4.19	5.26	6.71

APPENDIX E: ABOUT THE FIGURES WITH REFERENCES

All of the figures with references are taken from the conference paper, in which I am the first author. These figures are used in this thesis in accordance with the "publishing policy valid for the reuse of the text and graphics produced by the author" on the website of the publisher of the paper.