

SOLUTIONS TO RESTRICTIONS OF THE CURRENT CONVEYOR BASED
CIRCUITS

by

Erkan Yüce

B.S., Electrical and Electronics Engineering, Middle East Technical University, 1994

M.S., Electrical and Electronics Engineering, Pamukkale University, 1998

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ABSTRACT

SOLUTIONS TO RESTRICTIONS OF THE CURRENT CONVEYOR BASED CIRCUITS

Current conveyor (CC) is one of the most widely used versatile active components. It potentially provides higher accuracy, wider bandwidth, greater linearity and larger dynamic range. The advantages of the CCs have brought widespread usage in some technical areas such as current-mode analog communication systems and signal processing. It was initially proposed by Sedra and Smith in 1968. A modified version is presented as a second-generation current conveyor (CCII) in 1970. The CCII continues to receive much more attention, and finds numerous applications in many fields of electronics. This growing interest to the CC has led us to focus on this basic building block and its extensively used applications such as simulated inductors and active analog filters.

Inductors are not desirable passive elements in most electronic circuits because the behavior of them is not very close to the ideal element behavior and they are physically larger and heavier than other components. In addition, it is very difficult to realize large-valued inductors in integrated circuit (IC) technology and maximum a few nH inductors with low Q can only be implemented with current technology. Instead of large-valued physical inductors, simulated inductors employing CCs or other active components are widely used in many analog circuits. Such inductors with capacitors and other components can be used to form tuned circuits to build filters.

CC based circuits suffer from several restrictions such as parasitic impedance and frequency dependent non-ideal gain effects in addition to signal limitations stemmed from the restricted DC power supply voltages and limited allowable input currents. In fact, such restrictions also exist in other circuits realized with different active building blocks. The mentioned limitations usually result in some undesired conditions such as stability problems and distortions at the output terminals.

In this thesis, the restrictions of the CC based current-mode and voltage-mode analog filters as well as simulated inductors that can be used as building blocks for analog filtering functions are investigated in detail. Throughout this thesis, some methods to overcome these restrictions have been proposed.

A number of novel simulated inductors and analog filters with reduced parasitic impedance effects are presented as alternative circuits. Several experimental results using the commercially available active devices, AD844s are shown. Moreover, time and frequency domain as well as Monte Carlo analysis using SPICE and MATLAB programs are performed to verify the theory of the designed inductors and analog filter circuits.

ÖZET

AKIM TAŞIYICI TABANLI DEVRELERDEKİ SINIRLAMALARA ÇÖZÜMLER

Akım taşıyıcı (CC), yaygın olarak kullanılan çok yönlü aktif devre elemanlarından birisidir. Akım taşıyıcılar potansiyel olarak daha yüksek doğruluk, daha yüksek bant genişliği, daha yüksek doğrusallık, ve daha büyük çalışma aralığı gibi üstünlükler sunar. Akım taşıyıcıların sahip olduğu bu üstünlükler, onların akım modlu analog haberleşme sistemleri ve işaret işleme gibi bir çok teknik uygulama alanında yaygın olarak kullanımını beraberinde getirmiştir. Akım taşıyıcı kavramı ilk kez 1968 yılında, Sedra ve Smith tarafından literatüre kazandırılmıştır. Değiştirilmiş sürümü ise, 1970 yılında ikinci kuşak akım taşıyıcı (CCII) olarak sunulmuştur. Bu andan itibaren CCII'lara olan ilgi devamlı olarak artmış ve bir çok alanda sayısız uygulama olanağı bulmuş ve bulmaya da devam etmektedir. CC'lara artan ilgi, bizim bu temel yapı bloklarına ve söz konusu tümleşik devre yapılarının geniş uygulamaları olan yapay endüktans ve analog aktif filtre gerçeklemelerine odaklanmamızı sağlamıştır.

Endüktanslar ideal durumdaki çalışma karakteristiğine yakın bir davranış gösteremediklerinden ve diğer devre elemanlarından fiziksel olarak daha büyük ve daha ağır olduklarından dolayı elektronik devrelerin çoğunda arzu edilmezler. Buna ek olarak, tümleşik devre teknolojisinde büyük değerli endüktansları gerçekleyebilmek oldukça zordur ve günümüz teknolojisinde düşük kalite faktörlü maksimum birkaç nH endüktanslar elde edilebilmektedir. Büyük değerli fiziksel endüktanslar tasarlamak yerine, diğer aktif devre elemanlarını veya CC'ları kullanarak gerçekleştirilen yapay endüktanslar bir çok analog devrede yaygın bir biçimde kullanılmaktadır. Bu şekilde elde edilen endüktanslar, kapasitörler ve diğer elemanlar ile birlikte kullanılarak belli işaret frekanslarını süzmede kullanılır.

CC tabanlı devreler, parazit empedans ve frekans bağımlı ideal olmayan kazançlar ve buna ek olarak CC'lerin maksimum giriş akımı ve devrenin sınırlı DC besleme gerilimlerinden kaynaklanan işaret sınırlamalarından etkilenirler. Aslında bu tür sınırlamalar, farklı aktif yapı blokları ile gerçekleştirilen diğer devreler için de söz konusudur. Bahsedilen sınırlamalar, genellikle kararlılık problemleri ve çıkış terminallerindeki gerilimlerde bozulmalar gibi arzu edilmeyen durumlara neden olurlar.

Bu tez çalışmasında, CC tabanlı akım ve gerilim modlu filtreler ve analog filtreleme fonksiyonları için yapı blokları olarak kullanılabilen yapay endüktanslar üzerindeki sınırlamalar ayrıntılı olarak incelenecektir. Yapay endüktans ve aktif filtreler üzerindeki kısıtlamaların üstesinden gelmek için tez boyunca bazı yöntemler verilecektir.

Ayrıca tezde, literatürdeki devrelere alternatif olarak parazit empedans etkileri azaltılmış bir çok yeni yapay endüktans ve analog filtre gerçeklemeleri tasarlanmıştır. Ticari olarak mevcut olan AD844 tümleşik devrelerini kullanarak çeşitli deneyler gerçekleştirilmiş ve elde edilen sonuçlar sunulmuştur. Ayrıca, tasarlanan endüktans ve analog filtre devrelerinin teorisini doğrulamak amacıyla SPICE ve MATLAB programları kullanılarak zaman ve frekans domeni ve Monte Carlo analizleri gerçekleştirilmiştir.

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LIST OF SYMBOLS / ABBREVIATIONS

H_{AP}	All-pass filter transfer function
ω_o	Angular resonance frequency
H_{BP}	Band-pass filter transfer function
I_o	Bias current of the CCCII
$I_{all-pass}$	Current-mode all-pass analog filter response
I_{bp}	Current-mode band-pass analog filter response
I_{hp}	Current-mode high-pass analog filter response
I_{lp}	Current-mode low-pass analog filter response
I_{notch}	Current-mode notch analog filter response
ω_c	Cut-off frequency
α_o, γ_o	DC current gains of the conveyor
β_o	DC voltage gain of the conveyor
β_F	Forward current gain of BJT
$\alpha(j\omega), \gamma(j\omega)$	Frequency dependent non-ideal current gains of the conveyor
$\beta(j\omega)$	Frequency dependent non-ideal voltage gain of the conveyor
K	Gain of the analog filter response
H_{HP}	High-pass filter transfer function
I_{in}	Input current
V_{in}	Input voltage
R_x	Intrinsic resistor or X terminal parasitic resistor
H_{LP}	Low-pass filter transfer function
V_{SS}	Negative DC power supply voltage
H_{NF}	Notch filter transfer function
V_{DD}	Positive DC power supply voltage
Q	Quality factor

V_r	Rated voltage
β_R	Reverse current gain of BJT
V_T	Thermal voltage
$V_{all-pass}$	Voltage-mode all-pass analog filter response
V_{bp}	Voltage-mode band-pass analog filter response
V_{hp}	Voltage-mode high-pass analog filter response
V_{lp}	Voltage-mode low-pass analog filter response
V_{notch}	Voltage-mode notch analog filter response
BJT	Bipolar Junction Transistor
C	Capacitance
CDBA	Current Differencing Buffered Amplifier
CFOA	Current Feedback Operational Amplifier
CF	Current Follower
CM	Current-mode
DDCC	Differential Difference Current Conveyor
DXCCII	Dual X second-generation Current Conveyor
FI	Floating Inductor
CCI	First-generation Current Conveyor
FDNR	Frequency Dependent Negative Resistor
FTFN	Four Terminal Floating Nullor
GVCC	Gain Variable Current Conveyor
IC	Integrated Circuit
L	Inductance
MOS	Metal Oxide Semiconductor
NIC	Negative Impedance Converter
OA	Operational Amplifier
R	Resistance
CCII	Second-generation Current Conveyor
CCIII	Third-generation Current Conveyor
TF	Transfer Function

VF	Voltage Follower
VM	Voltage-mode

1. INTRODUCTION

The development of very large scale integration (VLSI) process eases large amount of component realizations on a single chip. The main purpose of the analog integrated circuit (IC) implementation is to obtain circuit architectures with high performance. Oscillators, D/A and A/D converters, voltage comparators, rectifiers, current and voltage amplifiers, immittance and transfer function simulators, analog filters and simulated inductors. Analog filters and simulated inductors are under consideration in this thesis are required in many VLSI systems. Analog circuits should be designed with consideration of the trade-off between speed and power consumption. The trend in the technology towards to low voltage low power systems, limits the dynamic range of the designed circuits. Thus, such restrictions mainly resulting from the limited DC power supply voltages of the active elements severely limit the maximum allowable terminal currents of the active devices that in turn limit the passive element values.

New active devices have been popular since the beginning of the electronics engineering which has led to birth of transistors used in amplifiers, operational amplifiers (OAs) and current conveyors (CCs). Particularly, OAs have become the basic building block, and have been very popular in the market because of the advent of the first analog IC. Nevertheless, there is a new impulse towards to the current-mode (CM) circuits instead of voltage-mode (VM) ones such that CM ones can overcome the restriction of the constant gain-bandwidth product and the trade-off between speed and bandwidth. In other words, the performance of the CM ones is improved in terms of low-voltage characteristics, slew rate and bandwidth. Furthermore, CM circuits do not need a high voltage gain.

A CC is a fundamental building block realized in an analog circuit design, and represents an effective alternative to the OA for the analog circuit designers. Fortunately, the practical characteristics of the CCs and OAs are very close to the ideal ones.

Different open-loop current-mode active devices with low and fixed current gains have been discussed so far. The gain of these active devices is set without any external

feedback between the input and output. However, there may be local feedback circuits instead of global ones. Using current-mode devices, it is possible to implement different types of amplification with a high gain range despite their low and fixed current gains which can be set directly by the transistor aspect ratios of the active devices or alternatively by controlling the impedance levels at the input and output of the amplifiers. Therefore, either voltage to current or current to voltage conversion is possible.

First-generation current conveyor (CCI) was introduced in 1968 by Sedra and Smith [1] and [2]. CCI is as a general building block like the OA. However, the OA does not work well in applications where a current output signal is required. CC based networks can be operated without external feedback thus they have a different high frequency behavior compared to the OA based ones. Nevertheless, CCI is no longer a general purpose CC, and is only a current buffer with low input impedance when one of its input ports is tied to ground. This circuit becomes important for the input stage of the current-mode signal processing systems. In many applications, only one of the virtual grounds in terminals X and Y of the CCI is used and the unused terminal should be grounded or connected to a suitable potential. This grounding process should be performed carefully because a poorly grounded input terminal may cause unwanted negative impedance at the other input terminal. Also, a high impedance terminal is desired for many applications, which is achieved by one high, one low input impedance terminal of the CCs or second-generation current conveyors (CCII) introduced in 1970 by Sedra and Smith [3]. CCII is different from the CCI in that the Y terminal of the CCII is a high input impedance port. In other words, there is no current flowing into the Y terminal thus it is called a voltage input terminal. Moreover, the Z terminal is a current output and the X terminal can be used either as a voltage output or as a current input port. As a result, the CCII can easily be used to process both of the current-mode and voltage-mode signals unlike the CCI and OA.

The operation of the third-generation current conveyor (CCIII) is similar to that of the CCI with the exception that the currents in ports X and Y flow in opposite directions. The input current flows into the Y terminal and out from the X terminal or vice versa in the CCIII thus the X and Y terminals behave like a short circuit. Nonetheless, CCIII has high input impedances with common-mode current signals. For this reason, common-mode

currents can push the input terminals out from the proper operation range. Unfortunately, CCI and CCIII have very few applications even if CCIII can be used for current probing.

The CCII is widely used because CCII is functionally flexible and versatile [4] besides a commercially available active device such as AD844 [5] can be used as CCII. CCII has voltage follower (VF) properties (between ports Y and X) as well as current follower (CF) properties (between ports X and Z) so a circuit employing CCIIs can be used to implement electronic functions operating in either current-mode or voltage-mode and also in both modes. In a point of view of a monolithic integration, the most important building block for the realization of the CCIIs is to use a voltage follower for synthesizing inputs Y and X and complementary current mirrors that copy the current on port X to the output port Z. If the VF of the CCII is obtained from an OA used like a buffer, the CCII takes an advantage at high frequencies because of low-valued series parasitic resistance on port X. Nevertheless, like the OA, the CCII has less serious but similar drawbacks such as reduced cut-off frequency, increased power consumption and enlarged silicon area. In many designs, the VF is realized using mixed translinear loop using complementary BJTs, which causes the CCII to have cut-off frequencies up to several MHz. The CCII has series parasitic resistances whose value can be negligible in some topologies, and has little variations up to several MHz.

Current-mode building blocks are not limited to these mentioned above. Other building blocks such as operational transconductance amplifier (OTA), operational mirrored amplifier (OMA), current feedback operational amplifier (CFOA), four terminal floating nullor (FTFN), differential voltage current conveyor (DVCC), current differencing buffered amplifier (CDBA), dual-X CCII (DXCCII), inverting CCII (ICCI) and gain variable CC (GVCC) [6] have been emerged as an important class of circuits with features enabling them to rival their voltage-mode counterparts in a large range of applications. Apart from these, some useful versatile active devices such as second-generation current controlled conveyors (CCCIIs) have been introduced [7].

It is worth to mention that a current-mode approach is not only restricted to current processing but also offers certain advantages such as higher usable gain, more reduced voltage excursion at sensitive nodes, greater linearity, lower power consumption, wider

bandwidth, better accuracy and larger dynamic range compared to its voltage-mode counterparts [8] and [9].

Current conveyors as active elements are basic building blocks receiving much attention in synthetic inductance design because it is very difficult to implement large-valued inductors in IC process. Maximum a few nH inductors with low Q can only be implemented with current technology [10]. For this reason, quite a large number of circuits such as grounded simulated inductors [3] and [11]-[22] besides floating inductances (FIs) [23]-[42] used in many areas such as oscillator designs, filter implementations and negative inductance realizations used for inductance cancellations employing various current-mode active components have been presented. It is well known that passive inductors in conjunction with capacitors and other components can form tuned circuits to build filters. Apart from this, realizations of second-order current-mode analog filters [43]-[67] and second-order voltage-mode analog filters [68]-[79] widely used in analog communication systems and signal processing have been proposed in the literature.

It is an essential issue for a circuit to employ only grounded passive elements especially grounded capacitors and without requirement for component matching conditions and/or cancellation constraints because such a circuit is very convenient for IC technology. A circuit using a minimum number of active and passive components, in other words occupying less chip area is important from VLSI implementation, power consumption and total cost point of views. If a current-mode circuit has low input and high output impedances, it enables easy cascadability. Similarly, if a voltage-mode circuit has high input and low output impedances, it can easily be cascaded with other circuits. Nevertheless, the mentioned properties for a circuit are not adequate for a high performance design and restrictions of the active devices such as non-ideal gain and parasitic impedance effects, signal limitation problems should be taken into account because the performance of the active devices in any circuit play an essential role on the overall performance of the designed circuit. It is clear that various limitations of the active circuits cause deviations in the overall circuit parameters and distortion in the signal waveforms. Fortunately, several studies on such restrictions of the circuits [80]-[86] and several methods to reduce them [87]-[89] have been reported.

The aim of this thesis is to evaluate the non-ideality problems such as non ideal gain and parasitic impedance effects in CC based circuits with main emphasis on analog filters and inductance simulators. For this purpose, several analog filters and synthetic inductors are analyzed and their advantages and disadvantages are comparatively shown. The methods used and the results presented are expected to give guidelines to evaluate and compare similar circuits in the literature.

In this thesis, restrictions of the simulated inductors and second-order analog filters as well as the solutions to reduce them are investigated in depth. Moreover, frequency dependent non-ideal current and voltage gains causing stability problems and parasitic impedances such as X terminal parasitic resistors (in series) and Y and Z terminal parasitic resistors and capacitors (in parallel) of the conveyor affecting the performance of the circuits such as simulated inductors and analog filters at low and high frequencies are studied. Signal limitations stemmed from the limited DC power supply voltages and maximum allowable terminal currents of the active devices affect the operation frequency ranges of the active circuits such as the inductor simulators and analog filters, which is clarified in detail.

It is worth to mention that the relative importance of various non-idealities change with the trends in the technology. For example, there is a trend towards low voltage and low power systems, this in turn limits the signal swing possibilities for a circuit. Therefore, dynamic range issues are today more important than in the past. Therefore, in the thesis, dynamic range and signal swing capabilities are examined extensively.

For each analysis in the thesis, only the effects of one of the restrictions are considered and the effects of other restrictions are ignored.

The thesis is organized as follows:

In chapter 2, a new three-port active device namely plus-type gain variable third-generation current conveyor (GVCCIII+) is introduced and a novel grounded inductor simulator using a minimum number of components is developed. The GVCCIII+ can be constructed using AD844s to perform the experimental test of the introduced inductor simulator. The voltage gain of the GVCCIII+ can be adjusted arbitrarily with external

resistors thus non-ideal gain analysis considering frequency dependent non-ideal voltage gain of the GVCCIII+ of the simulated inductor is performed. Signal limitations of the simulated inductors, non-ideal gain and parasitic impedance effects on the performance of the simulated inductors are explained in great depth using the proposed GVCCIII+ based grounded inductance simulator. Also, several time and frequency domain simulations using SPICE program is performed. The layout using MAGIC program in $0.25\mu\text{m}$ TSMC technology, parasitic impedances and noise model of the GVCCIII+ as well as novel floating inductor simulators with their experimental and simulation results are given. Further, a compensation technique for reducing the effects of the Z terminal parasitic impedance of the simulated inductor is developed, which can be applied to other circuits composed of active devices having high impedance current output terminals similar to the Z terminals of the CCs.

In chapter 3, non-ideal voltage and current gain effects on the performance of the CCII based simulated inductors and signal limitations stemmed from the maximum allowable X terminal currents of the CCIIs are investigated in detail. For this purpose, two new and three previously reported grounded inductor simulators are chosen. Simulation results using MATLAB and SPICE program are given to confirm the theory. In addition to these, two novel grounded inductor simulators employing a single new active device called modified current feedback operational amplifier (MCFOA) with their experimental and simulation results are given as alternative grounded inductors.

In chapter 4, two novel electronically tunable current mode-filters using CCCII and only grounded capacitors are examined to illustrate the parasitic impedance effects. If a capacitor is connected in series to the X terminal of the CCCII of a filter, the operation of the filter is not satisfactory at high frequencies especially because of the effects of the X terminal parasitic resistors on the performance of the filter. Second-order and high-order filters not suffering from X terminal parasitic resistances of the CCII/ CCCII are developed as alternative analog filters. Moreover, a unified circuit using a single negative impedance converter (NIC), realizing both of the current-mode and voltage-mode filter responses as well as inductor simulator is proposed as an alternative. Simulation results using SPICE program and experimental analysis using AD844s are given to verify the

theory. A new current-mode universal filter employing a single novel active device namely MCFOA and two novel voltage-mode universal filters are proposed in this chapter.

In chapter 5, a new current-mode filter using CCIIIs and only grounded capacitors is presented to exhibit its signal limitations due to restricted DC power supply voltages and maximum allowable terminal current of the active devices. Simulation and experimental results are given to confirm the theory as well as to show the performance of the developed filters.

In chapter 6, an approach for the evaluation of stability of current conveyor based filters is presented. For this purpose, stability problems of the active filters stemmed from the non-ideal current and voltage gain effects are investigated. To perform the stability analysis by using a single pole model, three electronically tunable current-mode universal filters using CCCIIIs and only grounded capacitors in addition to a simple filter employing a single CCII are introduced. Simulation results using MATLAB program verify the theory as expected where Routh and Bode stability tests are used.

Finally, conclusions are given in the last chapter, chapter 7.

2. A NOVEL INDUCTOR SIMULATOR AND ANALYSIS OF MAIN RESTRICTIONS IN SIMULATED INDUCTORS

Simulated inductors find many applications in electronic instrumentation, thus numerous simulated inductors are available in the literature. However, restrictions of the inductor simulators such as signal limitations, parasitic impedance effects, non-ideal gain effects, stability problems and the methods to reduce the restrictions of the inductor simulators have not been investigated so far. All simulated inductors behave like ideal inductors only in a frequency range depending on the passive element values, applied input current/voltage magnitude, power supply voltages and maximum allowable terminal currents of the conveyors, which can be denoted as the application limitations of the inductor simulators. Also, inductor simulators have other restrictions affecting their low and high frequency performances, parasitic impedance and frequency dependent non-ideal gain effects. Apart from these, inductor simulators may have stability problems due to non-ideal gain and parasitic impedance effects.

The signal limitations of the inductor simulators is mainly due to the maximum current source and/or sink capability and maximum voltage capability at the terminal nodes of the active device used in the simulator circuit, which causes the terminal voltage/current limitation of the simulated inductor. Either grounded or floating inductor simulators suffer from four kinds of signal limitations, which can be categorized as **(i)** restrictions of the simulated inductors due to terminal voltages of the conveyors which should be less than DC power supply voltages when the applied input is a voltage source, **(ii)** restrictions of simulated inductors due to maximum allowable terminal currents of the active devices when the applied input is a voltage source. In other words, an inductor simulator has a limit at low frequencies when a voltage source is applied to its input port. In this chapter **(i)** and **(ii)** are explained in detail. Similarly, **(iii)** restrictions of simulated inductors stemmed from the maximum allowable terminal currents of the active devices when the applied input is a current source, which is explained in detail in the next chapter, **(iv)** restrictions of simulated inductors stemmed from the terminal voltage of the conveyor less than restricted DC power supply voltages of the inductor simulator circuits when the applied input is a

current source, which resembles previous conditions. As a result, inductor simulators have a limit at high frequencies when a current source is applied.

In summary, signal limitations of the inductor simulators besides their non-ideal gain and parasitic impedance effects are investigated in this chapter. Here, a novel grounded inductor simulator using a minimum number of passive components and a new active device called gain variable third-generation current conveyor (GVCCIII) is given as an example.

Three new floating inductor simulator examples, two of them being lossless positive floating inductor, employing CCCIs are proposed. They have only resistive components and no capacitors connected in series to the X terminals of the CCCIs. Thus, both of the floating inductors can be operated at higher frequencies. Nevertheless, both of the novel floating inductors suffer from the Z and Y terminal parasitic resistors which limit the low frequency performance of the inductor simulators. Fortunately, a compensation method improving the low frequency performance of circuits is given. This new method reduces the Z and Y terminal parasitic resistor effects which in turn increase the useful frequency range of the inductor simulators considerably if only parasitic impedance effects are considered.

2.1. Gain Variable Current Conveyor

In this section, a new gain variable third-generation current conveyor (GVCCIII) is presented. It is used to implement the proposed grounded inductances whose restrictions are investigated in detail. The GVCCIII has adjustable voltage gain in addition to the other standard properties of the CCIII.

Parasitic impedance and non-ideal gain effects as well as signal limitations of the simulated inductors are explained by using a GVCCIII which can be characterized by the following matrix equation:

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} \beta & 0 & 0 \\ 0 & -\gamma & 0 \\ 0 & \pm \alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (2.1)$$

The + and – signs of α are used for the GVCCIII+ and GVCCIII-, respectively. The terminal currents I_x , I_y and I_z , and the terminal voltages V_x , V_y and V_z in equation (2.1) correspond to the terminals X, Y and Z, respectively. Current convention is such that all currents flow into the GVCCIII. The parameters α and γ are the frequency dependent current gains (ideally equal to unity) and the parameter β is the frequency dependent voltage gain of the conveyor.

The novel CMOS structure of the GVCCIII+ shown in Figure 2.1 has a variable voltage gain by changing the resistors R_1 and R_2 . The grounded resistors R_1 and R_2 of the GVCCIII+ can also be realized employing MOS transistors to tune the voltage gain of the GVCCIII+ electronically [90] in which $\beta \cong R_2 / R_1$ at low and medium frequencies. However, due to the parasitic impedance effects, $\beta \cong R_2 / R_1$ is only valid for small-valued R_1 and R_2 .

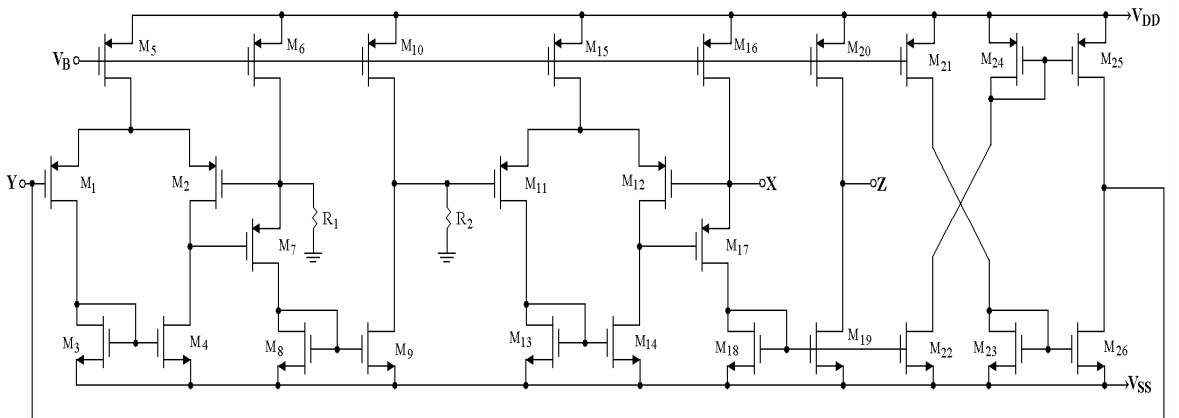


Figure 2.1. Internal structure of the GVCCIII+ using resistors R_1 and R_2

In this circuit, the current mirror M_{18} - M_{19} is used to sense the current flowing from the X terminal, and mirror it to the high impedance Z terminal. A feedback at terminal Y provides equal currents of the terminals Y and X.

Assuming that the output resistances of the transistors M_{11} to M_{14} are equal to r_o , the resistances seen at terminals X and Y are respectively found as

$$R_X = \left(\frac{r_{o17} + \frac{r_{o18}}{1 + g_{m18}r_{o18}}}{1 + r_{o17}g_{m17} \left(1 + \frac{r_o}{2} g_{m12} \right)} \right) \parallel r_{o16} \cong \frac{2}{g_{m17}r_o g_{m12}} \quad (2.2)$$

$$R_Y = \frac{r_{o25}r_{o26}}{r_{o25} + r_{o26}} \quad (2.3)$$

where r_{oi} and g_{mi} are the output resistance and transconductance of the i -th transistor, respectively. The high output impedance at the Z terminal is ensured, being Z a drain terminal and calculated as

$$R_Z = \frac{r_{o19}r_{o20}}{r_{o19} + r_{o20}} \quad (2.4)$$

The proposed GVCCIII+ can also be implemented using plus-type second-generation current conveyors (CCII+s) and external resistors as shown in Figure 2.2.

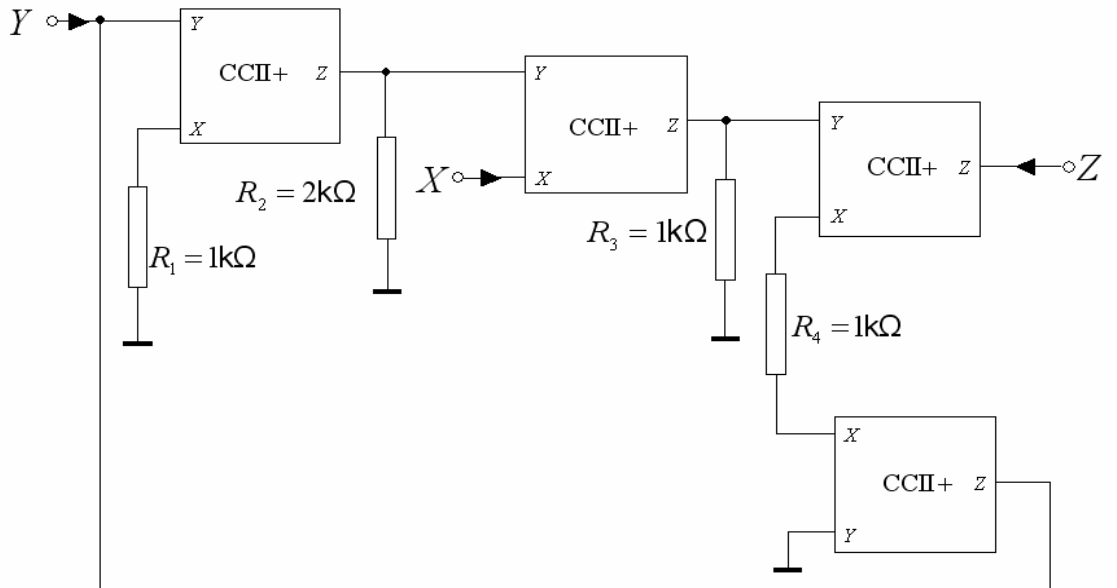


Figure 2.2. Realization of the GVCCIII+ using CCII+s and resistors

The proposed new circuit for realizing grounded inductance is shown in Figure 2.3. The circuit employs a GVCCIII+, two resistors and one capacitor. Also, one can use the GVCCIII- instead of the GVCCIII+ as shown in Figure 2.4.

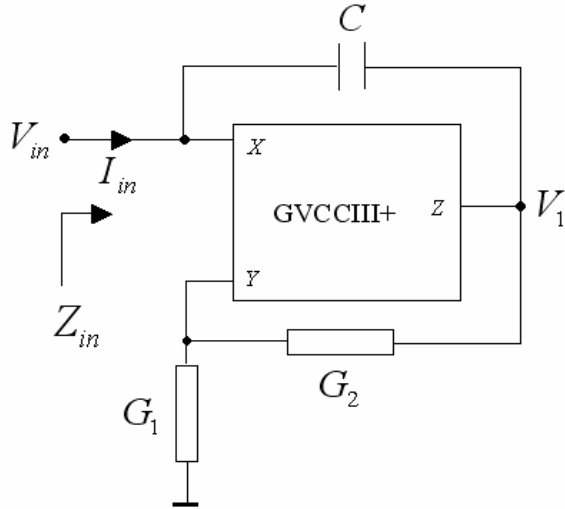


Figure 2.3. The proposed simulated inductor using a GVCCIII+

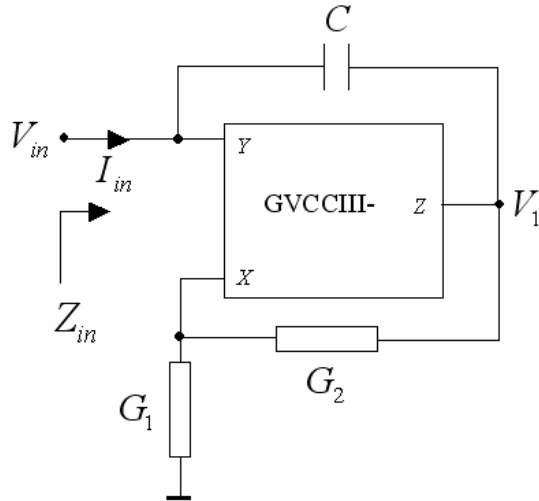


Figure 2.4. An alternative for the proposed simulated inductor using a GVCCIII-

If DC voltage gain $\beta_0 = 2$ for the GVCCIII+ where β_0 is the value of β at low frequencies and $\beta_0 = 1/2$ for the GVCCIII- are chosen, routine analysis of the circuits shown in Figures 2.3 and 2.4 gives the following input admittance:

$$Y_{in} = \frac{1}{sL_{in}} + G_{in} = \frac{G_1 G_2}{2sC} + \frac{2G_1 - G_2}{2} \quad (2.5)$$

where $L_{in} = 2C / G_1 G_2$ and $G_{in} = (2G_1 - G_2) / 2$. Consequently, the circuits can realize an inductor in parallel with a resistor. The quality factor Q for both of the proposed inductors is calculated as $Q = G_1 G_2 / (\omega C (2G_1 - G_2))$, where ω is the angular frequency.

From equation (2.5), we can obtain three types of inductors depending on the selection of the G_1 and G_2 as follows:

- (a) A lossless simulated inductor if $2G_1 = G_2$.
- (b) A lossy simulated inductor with a parallel negative resistor if $2G_1 < G_2$.
- (c) A lossy simulated inductor with a parallel positive resistor if $2G_1 > G_2$.

In case (a), selecting $G_1 = G$ and $G_2 = 2G$, the input impedance of the circuits is found as

$$Z_{in} = sL = \frac{sC}{G^2} \quad (2.6)$$

where $L = C / G^2$.

For the circuit in Figure 2.3, if α , β and γ effects are taken into account, the impedance with $G_1 = G$ and $G_2 = 2G$ is found as

$$Z_{in} = \frac{2G\beta[\gamma - \alpha] + sC\beta\gamma}{2G^2 + sCG\{3[1 + \alpha] - 2\beta[1 + \alpha] + 2\gamma[\beta - 1]\}} \quad (2.7)$$

Here, the parameter β (frequency dependent variable voltage gain) can be used as a tool to adjust the term $CG\{3[1 + \alpha] - 2\beta[1 + \alpha] + 2\gamma[\beta - 1]\}$ in equation (2.7) equal to zero. In fact, selecting the frequency dependent voltage gain $\beta = (3[1 + \alpha] - 2\gamma) / (2[1 + \alpha - \gamma])$ results in

$$Z_{in} = R_s + sL_s = \frac{2G\beta[\gamma - \alpha] + sC\beta\gamma}{2G^2} \quad (2.8)$$

where $R_s = \beta[\gamma - \alpha]/G$ and $L_s = C\beta\gamma/(2G^2)$. Therefore, the circuit can realize a lossy inductance in non-ideal case. However, the value of the series resistor R_s for nominal values of the non-ideal parameters is equal to zero.

In non-ideal case, the quality factor of the realized grounded inductance is found as

$$Q_s = \frac{\omega C\gamma}{2G[\gamma - \alpha]} \quad (2.9)$$

From equation (2.7), if only β is taken into account with $\alpha = \gamma = 1$ (nominal values), the equivalent admittance of the circuit can be found as

$$Y_{in} = \frac{2[2 - \beta]G}{\beta} + \frac{2G^2}{sC\beta} = \frac{1}{R_p} + \frac{1}{sL_p} \quad (2.10)$$

where $L_p = C\beta/(2G^2)$ and $R_p = \beta/(2[2 - \beta]G)$. Hence, the circuit of Figure 2.3 can be modeled as an inductance L_p in parallel with a resistance R_p .

Then, for this case Q_p is found as

$$Q_p = \frac{G}{[2 - \beta]\omega C} \quad (2.11)$$

From equation (2.10), we obtain three kinds of inductors depending on $\beta = \beta_o$ values. These are classified as

- a)** A lossless simulated inductor that is equal to equation (2.6) for $\beta_o = 2$.
- b)** A gainy simulated inductor with a parallel negative resistor for $\beta_o > 2$.
- c)** A lossy simulated inductor with a parallel positive resistor for $0 < \beta_o < 2$.

Similar results can be found for the circuit in Figure 2.4. Moreover, adjusting the voltage gain of the GVCCIII results in a negative or positive resistor with the lossless inductor thus the circuits can be used in realizing oscillators.

Note that both of the inductors employ a floating capacitor, which can be easily implemented by using advanced IC technologies. These IC technologies offer a second poly layer (poly2), which enables also the realization of the floating capacitors as double poly (poly1-poly2) capacitor [91]. They are commonplace today, and can be used very commonly in analogue IC designs. On the other hand, floating resistor used in the circuits of Figures 2.3 and 2.4 can also be implemented in CMOS technology. For this purpose, the floating resistor circuit reported in [92] can be used.

2.2. Non-Ideal Gain Effects

In this section, the effects of the current conveyor frequency dependent voltage gain on the simulated grounded inductors, are investigated. A single-pole model for $\beta(j\omega)$ can be given by

$$\beta(j\omega) = \frac{\beta_o}{1 + \frac{j\omega}{\omega_\beta}} \quad (2.12)$$

where ω_β is the corner frequency of the $\beta(j\omega)$. Similarly, the current gains of the conveyor can be expressed as

$$\alpha(j\omega) = \frac{\alpha_o}{1 + \frac{j\omega}{\omega_\alpha}} \quad (2.13)$$

$$\gamma(j\omega) = \frac{\gamma_o}{1 + \frac{j\omega}{\omega_\gamma}} \quad (2.14)$$

The value of the corner frequency ω_β depends on the fabrication of the devices. Here, we assumed that the corner frequency of the voltage gain of the conveyor is much smaller than the corner frequencies of the current gains of the conveyor ($\omega_\beta \ll \min\{\omega_\alpha, \omega_\gamma\}$). Then, we can investigate the admittance in equation (2.10) where only voltage gain effect is taken into account.

Case I: In this case, we assume that the frequency of operation is much less than the corner frequency ($\omega \leq 0.1\omega_\beta$). Hence, the single pole model in equation (2.12) becomes $\beta(j\omega) \cong \beta_o$. By replacing s with $j\omega$ in equation (2.10), it is found that

$$Y_{in} = \frac{2(2 - \beta_o)G}{\beta_o} + \frac{2G^2}{j\omega C\beta_o} \quad (2.15)$$

As a result, an inductor in parallel with a resistor is obtained in which the resistor value can be positive, negative and zero depending on $(2 - \beta_o)$ value.

Case II: If the frequency of operation is in the range defined by $0.1\omega_\beta \leq \omega \leq 10\omega_\beta$, the single pole model in equation (2.12) remains without change. By replacing s with $j\omega$, the admittance in equation (2.10) becomes

$$Y_{in} = \frac{2G^2}{j\omega C\beta_o} + \frac{G(2G + 2C\omega_\beta(2 - \beta_o))}{C\omega_\beta\beta_o} + \frac{j4\omega G}{\omega_\beta\beta_o} \quad (2.16)$$

Thus, a parallel combination of inductor, capacitor and resistor is obtained where resistor value can be positive, negative and zero depending on $2C\omega_\beta(2 - \beta_o)$ and $2G$ values.

Case III: In this case, it is assumed that the frequency of operation is much greater than the corner frequency ($\omega \geq 10\omega_\beta$) thus the single pole model in equation (2.12) can be approximated by $\beta(j\omega) \cong \beta_o\omega_\beta / j\omega$. As a result, by replacing s with $j\omega$, the admittance in equation (2.10) is found as

$$Y_{in} = \frac{G(2G - 2C\omega_\beta\beta_o)}{\omega_\beta C\beta_o} + \frac{j4\omega G}{\omega_\beta\beta_o} \quad (2.17)$$

Consequently, a capacitor in parallel with a resistor whose value can be positive, negative or zero depending on the values of $2G$ and $2C\omega_\beta\beta_o$, is realized.

As stated in [93] ‘A linear time-invariant one-port network is short-circuit stable if and only if all the poles of $Y(s) = 1/Z(s)$ are in the open left half plane (LHP). Dually, a linear time-invariant one-port network is open-circuit stable if and only if all the poles of $Z(s)$ are in the open LHP’. Therefore, the design engineers should perform stability analysis on the circuits using specific GVCCIII+s with corner frequencies ω_α , ω_β and ω_γ .

To compare the stability of the five grounded inductor simulators using CCIIIs, their non-ideal gain effects at low frequencies are taken into account in the next chapter. On the other hand, the transfer function of both of the current-mode and voltage-mode filters should be searched to check the stability by using Routh’s stability criteria [94]. Also, stability problem stemmed from the frequency dependent non-ideal current and voltage gain effects of the simulated inductors and analog filters are discussed in this thesis.

2.3. Frequency Limitations

In this section, we show that the simulated inductors in general behave linearly in a restricted frequency range called useful frequency range due to the power supply voltage restrictions causing terminal voltage limitations of the active devices, parasitic impedance effects, maximum allowable terminal current of the active devices and non-ideal gain effects.

2.3.1. Terminal Voltage Limitation

It is well known that terminal voltages of the active devices in an inductor simulator like all other circuits using current conveyors can not exceed the rated voltage which is less than symmetrical DC power supply voltages. Therefore,

$$|V_j| \leq V_{rj} \quad (2.18)$$

where $V_{rj} = \min\{V_{rj+}, -V_{rj-}\}$ as well as $V_{rj+} < V_{DD}$ and $V_{rj-} > V_{SS}$. It is well known that each node voltage should be less than rated voltages V_{rj+} and V_{rj-} due to the DC positive V_{DD} and negative V_{SS} power supply voltages, respectively. The rated voltage of the GVCCIII+ in Figure 2.1 is approximately calculated as $V_r = 320\text{mV}$ where $V_{DD} = 1.5\text{V}$ and $V_{SS} = -1.5\text{V}$. Similarly, the rated voltage of the GVCCIII+ in Figure 2.2 is approximately computed as $V_r = 12\text{V}$ where $V_{DD} = 15\text{V}$ and $V_{SS} = -15\text{V}$. It is well known that if the values of the power supply voltages are increased, the rated voltage increases. However, power consumption increases considerably.

Assume that a simulated inductor employs a single current conveyor with n terminals ($n \geq 3$), d resistors ($d \geq 2$) and a single capacitor. The terminal voltages of the current conveyor V_j ($j = 1, 2, \dots, n$) depend on the frequency of operation, the resistors and capacitor values as well as the applied input voltage (V_{in}). Consequently, the terminal voltages V_j can be expressed with functions ψ_j as follows:

$$V_j = \psi_j(C, R_1, R_2, \dots, R_d, f)V_{in} = \left(\frac{A_j}{f} + a_j \right) V_{in} \quad (2.19)$$

where A_j and a_j are respectively pure imaginary and real numbers (see Appendix A). It is well known that each terminal voltage V_j should be between the corresponding positive and negative rated voltages (V_{rj+} and V_{rj-}) of the current conveyor to avoid clipping and distortion. Hence, we can write

From equations (2.18) and (2.19), the low frequency range is found as

$$f \geq f_{LV} = \max \left\{ \frac{|A_j|}{\sqrt{\left(\frac{V_r}{V_{in}} \right)^2 - a_j^2}} \right\} \quad (j = 1, 2, \dots, n) \quad (2.20)$$

Here f_{LV} is called the low frequency limit of the simulator due to the limited node voltages. It is seen from equation (2.20) that an inductor operates well at low frequencies if V_{jr} is very high and magnitudes of A_j and a_j are very small.

For the circuit in Figure 2.3, the equations (2.18) and (2.19) for the terminal voltage V_1 can be written as:

$$V_1 = V_{in} \left(1 - \frac{G}{j4\pi fC} \right) \quad (2.21)$$

$$|V_1| \leq V_r \quad (2.22)$$

Then,

$$a_1 = 1 \quad (2.23)$$

$$A_1 = \frac{jG}{4\pi C} \quad (2.24)$$

From equation (2.21), it can be realized that as the frequency decreases to zero, the magnitude of the terminal voltage V_1 increases arbitrarily. Consequently, for the proposed simulated inductor in Figure 2.3, the frequency must be greater than f_{LV} which is calculated as

$$f_{LV} = \frac{1}{4\pi GL_{eq} \sqrt{\left(\frac{V_r}{V_{in}} \right)^2 - 1}} \quad (2.25)$$

where $L_{eq} = C / G^2$.

2.3.2. Current Conveyor X-Terminal Current Limitation

The second frequency limitation of the current conveyor-based simulated inductors is the X-terminal current limitation or limitation stemmed from the maximum allowable terminal currents of the conveyors as given below.

$$I_i = \varphi_i(C, R_1, R_2, \dots, R_r, f) V_{in} = \left(\frac{B_i}{f} + b_i \right) V_{in} \quad (i=1, 2, \dots, m) \quad (2.26)$$

where B_i and b_i are respectively pure imaginary and real numbers and $|I_i| \leq I_M$. It is well known that the current conveyor has a maximum allowable input current denoted by I_M (for example 5mA for the commercially available active device, AD844 [5]) at terminal X.

If in the realization of the GVCCIII+ shown in Figure 2.2, we use AD844s instead of the CCII+s, I_M of the GVCCIII+ is also 5mA.

Using SPICE program, I_{Mi} of the GVCCIII+ in Figure 2.1 is calculated as $58.2\mu\text{A}$. Fortunately, I_{Mi} can be increased by increasing aspect ratios of the relevant CMOS transistors of the GVCCIII+ in Figure 2.1. Therefore, the useful frequency range limited by I_{Mi} of the GVCCII+ is given by

$$f \geq f_{LC} = \max \left\{ \frac{|B_i^2|}{\sqrt{\left(\frac{I_{Mi}}{V_{in}}\right)^2 - b_i^2}} \right\} \quad (2.27)$$

We show this limitation on the simulated inductor in Figure 2.3. If the input voltage V_{in} is applied to the circuit in Figure 2.3, the terminal current of the GVCCIII, I_x is found as

$$I_x = \frac{2G^2 - j\omega CG}{2j\omega C} V_{in} = \left(\frac{B}{f} + b \right) V_{in} \quad (2.28)$$

where $B = -jG^2/(2\pi C)$ and $b = -G/2$.

From equation (2.28), we can conclude that, if a voltage source is applied to the simulated inductor, there is a low frequency limit denoted by f_{LC} due to the X-terminal current limitation of the GVCCII.

Consequently, the frequency range of operation restricted by the X-terminal current can be defined as

$$f \geq f_{LC} = \frac{1}{\pi L_{eq}} \frac{1}{\sqrt{4\left(\frac{I_M}{V_{in}}\right)^2 - G^2}} \quad (2.29)$$

where $L_{eq} = C / G^2$.

Using equations (2.20) and (2.27), the useful frequency range can be found as

$$f \geq \max\{f_{LV}, f_{LC}\} \quad (2.30)$$

The passive elements are selected as $C = 1\text{nF}$, $G_1 = 1\text{mS}$ and $G_2 = 2\text{mS}$, which results in $L = 1\text{mH}$ for the grounded inductor in Figure 2.3. Moreover, for the GVCCIII+ in Figure 2.1, $I_M = 58.2\mu\text{A}$ and $V_r = 320\text{mV}$ as given before. Also, the applied input $V_{in} = 5\text{mV}$ is chosen to evaluate the limits at low frequencies thus $f_{LV} = 1.24\text{kHz}$ and $f_{LC} = 13.683\text{kHz}$ are computed and the useful frequency range considering only signal limitations of the simulated inductors is found to be $f \geq \max\{f_{LV}, f_{LC}\} = 13.683\text{kHz}$.

It is observed that if the value of I_M of the GVCCIII+ in Figure 2.1 is set to $641.76\mu\text{A}$ by increasing the dimensions of the relevant CMOS transistors, $f_{LC} = 1.24\text{kHz}$ is obtained. For this reason, the useful frequency range becomes $f \geq 1.24\text{kHz}$. Note that I_M and V_r of the GVCCIII+ in Figure 2.1 can be further increased by changing the dimensions of the CMOS transistors and the values of both resistors, which results in reducing the limit at low frequencies.

2.3.3. Current Conveyor Parasitic Impedance Effect Limitation

The parasitic impedance effects change the impedance of the simulated inductor. It is well known that parasitic capacitors of the GVCCIII appear in parallel at the Y and Z terminals.

The impedance of a current conveyor-based inductor simulator using a single external capacitor with p parasitic capacitors can be expressed as

$$Z(s) = \frac{a_m s^m + a_{m-1} s^{m-1} + \dots + a_1 s + a_0}{b_r s^r + b_{r-1} s^{r-1} + \dots + b_1 s + b_0} \quad (2.31)$$

where $\max\{m, r\} \leq p + 1$.

It is obvious from equation (2.31) that a_0 affects the low frequency performance of the inductor simulator. Fortunately, a method to reduce a_0 is going to be given in the last section. The other terms in equation (2.31) except a_0 , a_1 and b_0 affect the high frequency performance of the inductor simulator. Note that the impedance in equation (2.31) can ideally be given as $Z(s) = a_1 s / b_0$.

For the inductance simulator, a frequency range of operation can be defined as in the following in which it operates as an ideal inductance

$$f_{LP} \leq f \leq f_{HP} \quad (2.32)$$

where f_{LP} and f_{HP} are the lower and higher frequency limits of the simulator due to the parasitic impedance effects, respectively.

For example, the impedance in equation (2.6) for the simulated inductor in Figure 2.3 with series parasitic resistance R_x at the terminal X and parallel parasitic capacitances C_z and C_y at the terminals Z and Y as seen in Figure 2.5 becomes

$$Z(s) = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (2.33)$$

where

$$\left. \begin{aligned}
 a_0 &= 2G^2 R_x \\
 a_1 &= 2[C + C_z] + R_x [3CG + G[2C_y + 3C_z]] \\
 a_2 &= C_y R_x [C + C_z] \\
 b_0 &= 2G^2 \\
 b_1 &= G[2C_y + 3C_z] + 2CG^2 R_x \\
 b_2 &= 2C[C_y + C_z] + C_y C_z + CGR_x [2C_y + 3C_z] \\
 b_3 &= CC_y C_z R_x
 \end{aligned} \right\} \quad (2.34)$$

Regarding that the parasitic capacitors are on the order of fF and R_x is a few tens ohms, we can ignore the second and third order terms in equation (2.33) for the frequency of operation less than a few hundred megahertz.

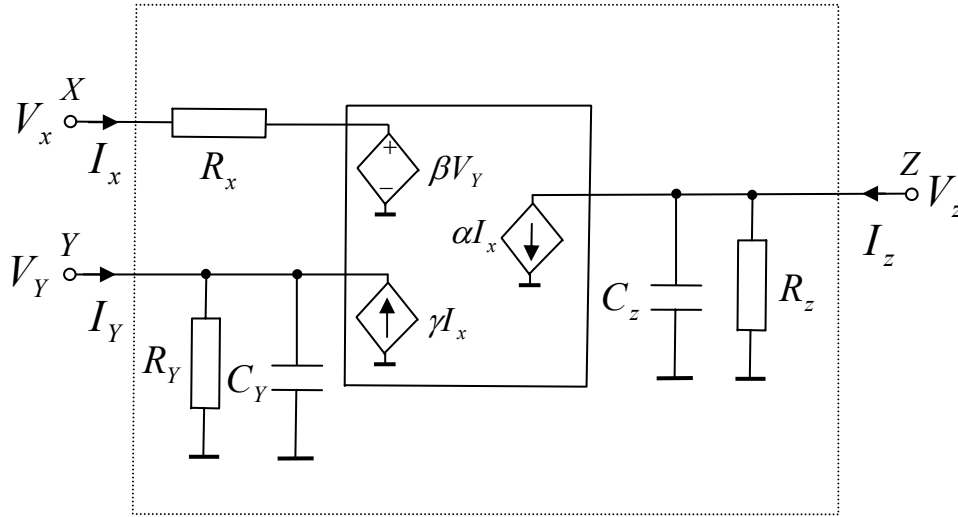


Figure 2.5. Model of the GVCCIII+ with non-ideal gains and parasitic impedances

Then, the impedance of the inductor in equation (2.33) can be approximated as

$$Z(s) \cong \frac{a_1 s + a_0}{b_1 s + b_0} \quad (2.35)$$

As a result, in order to obtain characteristic of an ideal inductor with $Z(s) = a_1 s / b_0$, we should have $a_0 / a_1 \ll \omega \ll b_0 / b_1$. Hence, the lower and upper frequency limits of the proposed simulator due to the parasitic impedance effects can be given as

$f_{LP} = 10a_o / (2\pi a_1)$ (see Appendix B) and $f_{HP} = 0.1b_o / (2\pi b_1)$ within 0.5% error, respectively.

It is seen from Figure 2.5 that if $\gamma=0$ is taken, we obtain the parasitic impedance model of a CCII+. Also, if R_x in Figure 2.5 is controlled electronically with a bias current I_o , we obtain the parasitic impedance model of a CCCII+. The parasitic impedances of the other Z terminal/ terminals have the same property like the Z terminal in Figure 2.5.

2.3.4. Current Conveyor Non-Ideal Gain Effect Limitation

We have investigated the lower frequency limitation in sections 2.3.1-2.3.3. There is also a high frequency restriction due to frequency dependent voltage and current gains, which can be formulized as

$$f \leq f_{HN} \quad (2.36)$$

Here, in general, assuming that $\omega_\beta \ll \min\{\omega_\alpha, \omega_\gamma\}$ f_{HN} can be given by

$$f_{HN} = \frac{0.1}{2\pi} \omega_\beta \quad (2.37)$$

Considering the frequency ranges in equations (2.30), (2.32) and (2.36), the overall frequency range of the simulator can be given by

$$\max\{f_{LV}, f_{LC}, f_{LP}\} < f < \min\{f_{HP}, f_{HN}\} \quad (2.38)$$

The frequency range given in equation (2.38) can be called useful frequency range in which a simulated inductor operates well.

In the next two sections, useful experimental and simulation results are given to exhibit the performance of the proposed inductor simulator employing a minimum number of

components. Moreover, the theory based on the signal limitations of the grounded inductor simulator is verified when the applied signal to its input port is a voltage source.

2.4. Experimental and Simulation Results

The GVCCIII+ shown in Figure 2.1 is simulated with symmetrical DC power supply voltages $V_{DD} = -V_{SS}=1.5V$ and bias voltage $V_B = 0.584V$ in $0.25\mu m$ TSMC CMOS technology.

The dimensions of the MOS transistors in the GVCCIII+ structure are given in Table 2.1. Level 49 MOS model parameters given in Table 2.2 are used for simulations. By selecting appropriate values for the resistors in Figure 2.1 ($R_1 = 1k\Omega$ and $R_2 = 3.1k\Omega$), the DC voltage gain of the GVCCIII+ in Figure 2.1 is obtained as $\beta_0 = 2$. The layout of the proposed GVCCIII+ is shown in Figure 2.6.

Table 2.1. The dimensions of the MOS transistors in the GVCCIII+ of Figure 2.1

PMOS Transistors	$W(\mu m) / L(\mu m)$
M ₁ , M ₂ , M ₅ , M ₁₅ , M ₁₆ and M ₁₉	1/0.25
M ₆ , M ₁₀ , M ₂₀ , M ₂₄ , M ₂₅ , M ₂₈ and M ₂₉	2/0.25
M ₇ and M ₂₁	40/0.25
NMOS Transistors	$W(\mu m) / L(\mu m)$
M ₃ , M ₄ , M ₈ , M ₉ , M ₁₇ , M ₁₈ , M ₂₂ , M ₂₃ , M ₂₆ , M ₂₇ and M ₃₀	0.5/0.25

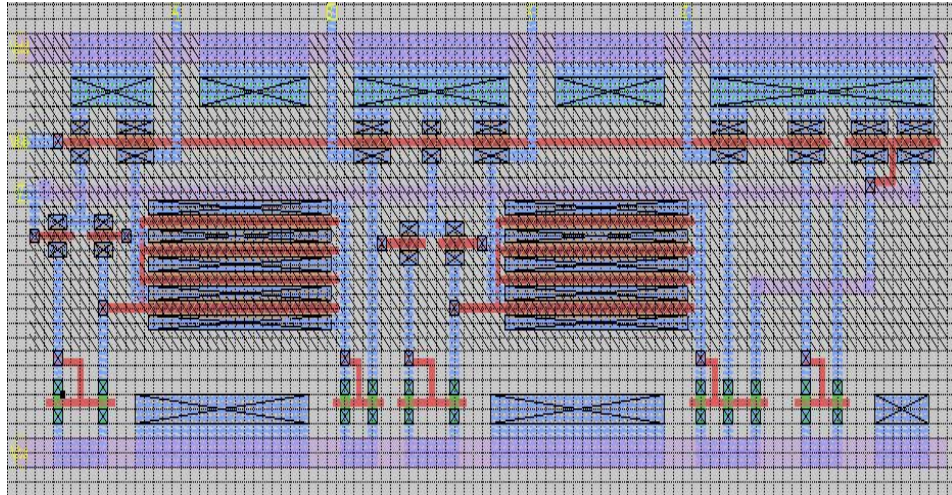


Figure 2.6. Layout of the proposed GVCCIII+ of Figure 2.1 using MAGIC program

Table 2.2. 0.25 μ m TSMC CMOS technology parameters

LEVEL 49, 0.25 μ m TSMC CMOS parameters
.MODEL CMOSN NMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 5.7E-9 XJ = 1E-7 NCH = 2.3549E17 + VTH0 = 0.3814211 K1 = 0.4746705 K2 = 1.660277E-4 K3 = 1E-3 K3B = 2.3122706 W0 = 1E-7 NLX = 1.589929E-7 + DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.6187888 DVT1 = 0.5994888 DVT2 = -0.3669704 U0 = 294.4108005 + UA = -1.358819E-9 UB = 2.573394E-18 UC = 3.77946E-11 VSAT = 1.214475E5 A0 = 1.8588721 + AGS = 0.3383369 B0 = -5.446135E-8 B1 = 7.4622E-8 +KETA = -7.443745E-3 + A1 = 9.745731E-5 A2 = 0.5578728 RDSW = 189.7568315 PRWG = 0.2559162 + PRWB = -0.181174 WR = 1 WINT = 0 LINT = 0 XL = 0 XW = -4E-8 + DWG = -1.457919E-8 DWB = 9.540311E-10 VOFF = -0.0981967 + NFACTOR = 1.2611167 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 +CDSCB = 0 + ETA0 = 4.919832E-3 ETAB = 2.025436E-4 DSUB = 0.0242961 + PCLM = 1.593914 PDIBLC1 = 1 PDIBLC2 = 2.640837E-3 + PDIBLCB = 0.0386436 DROUT = 1 PSCBE1 = 7.081828E8 + PSCBE2 = 2.180247E-4 PVAG = 0 DELTA = 0.01 RSH = 4.2 MOBMOD = 1 + PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 + UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 + WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 + CAPMOD = 2 XPART = 0.5 CGDO = 4.23E-10 CGSO = 4.23E-10 + CGBO = 5E-10 CJ = 1.749012E-3 PB = 0.99 MJ = 0.462496 + CJSW = 4.279349E-10 PBSW = 0.9622079 MJSW = 0.3165822 + CJSWG = 3.29E-10 PBSWG = 0.9622079 MJSWG = 0.3165822 CF = 0 + PVTH0 = -7.011825E-3 PRDSW = -9.9645069 PK2 = 3.616258E-3 + WKETA = 0.0105311 LKETA = -3.468158E-4)
.MODEL CMOSP PMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 5.7E-9 XJ = 1E-7 NCH = 4.1589E17 + VTH0 = -0.5744204 K1 = 0.6490426 K2 = -1.773363E-3 K3 = 0 + K3B = 10.0463289 W0 = 1.003172E-6 NLX = 1.289797E-8 +DVT0W = 0 + DVT1W = 0 DVT2W = 0 DVT0 = 2.0444478 DVT1 = 0.8171636 + DVT2 = -0.1766344 U0 = 104.3965309 UA = 1.149129E-9 UB = 1.889317E-21 + UC = -1E-10 VSAT = 1.704423E5 A0 = 1.0827869 AGS = 0.2100781 + B0 = 1.078897E-6 B1 = 4.897652E-6 KETA = 0.0122695 A1 = 0.0387643 + A2 = 0.300003 RDSW = 1.868086E3 PRWG = -2.456532E-4 + PRWB = -0.1100494 WR = 1 WINT = 0 LINT = 2.873182E-8 XL = 0 + XW = -4E-8 DWG = -3.82622E-8 DWB = 6.704642E-10 VOFF = -0.1377156 + NFACTOR = 0.9782443 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 + ETA0 = 0.4874648 ETAB = -0.0877264 DSUB = 1.274066 + PCLM = 1.2131124 PDIBLC1 = 4.890103E-3 PDIBLC2 = 2.759062E-10 + PDIBLCB = -8.153931E-4 DROUT = 0.0637363 PSCBE1 = 1.745651E10 + PSCBE2 = 3.933324E-9 PVAG = 0.0149263 DELTA = 0.01 RSH = 3.1 + MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 + UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 + WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 + LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 4.93E-10 + CGSO = 4.93E-10 CGBO = 5E-10 CJ = 1.893734E-3 PB = 0.9889579 + MJ = 0.4705132 CJSW = 3.124347E-10 PBSW = 0.8 MJSW = 0.2786992 + CJSWG = 2.5E-10 PBSWG = 0.8 MJSWG = 0.2786992 CF = 0 + PVTH0 = 5.048835E-3 PRDSW = -0.3854504 PK2 = 2.391215E-3 + WKETA = 0.0247713 LKETA = -8.933358E-3)

SPICE program is used to calculate the parasitic resistances and capacitances of the GVCCIII+ in Figure 2.1. The following results are obtained: $R_x = 126.8\Omega$, $R_z = 57.33k\Omega$, $R_y = 51.9k\Omega$, $C_z = 4.9fF$ and $C_y = 11.15fF$. The area of the layout of the proposed GVCCIII+ in Figure 2.6 is calculated as $47.4624\mu m^2$. The variations of the current and voltage gains of the GVCCIII+ in Figure 2.1 with respect to frequency are given in Figure 2.7.

In order to exhibit the frequency domain performance of the proposed inductor in Figure 2.3, two sets of values for the passive elements are selected as $C = 1nF$, $G = 1mS$ and $C = 0.1nF$, $G = 0.1mS$, which results in $L = 1mH$ and $L = 10mH$, respectively. Both of the GVCCIII+s in Figures 2.1 and 2.2 are used in simulations thus the current-mode filter in Figure 2.8 for simultaneously realizing low-pass, band-pass and high-pass responses is simulated. This filter has the GVCCIII+ in Fig. 1 as well as $R_p = 1k\Omega$, $C_p = 1nF$ and $L = 1mH$, which results in a resonance frequency of $f_0 = 159.15kHz$ and quality factor of $Q = 1$. Consequently, the results are shown in Figure 2.9. This filter is constructed experimentally in which GVCCIII+ of Figure 2.2 is used. Commercially available AD844s are replaced instead of the CCII+s in Figure 2.2 with DC power supply voltages $\pm 15V$.

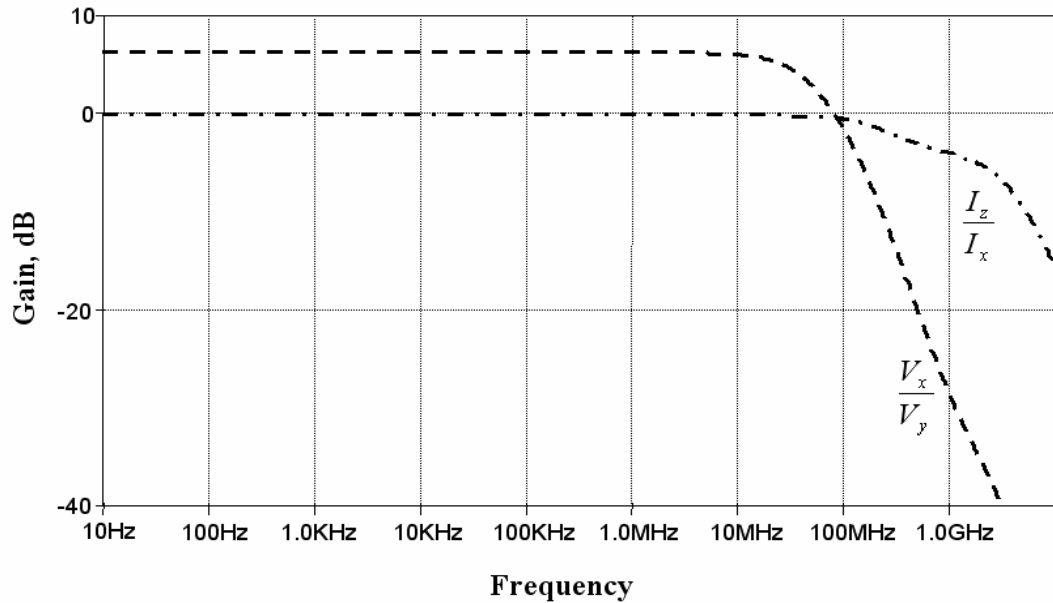


Figure 2.7. Variations of the current and voltage gains of the GVCCIII+ with respect to frequency

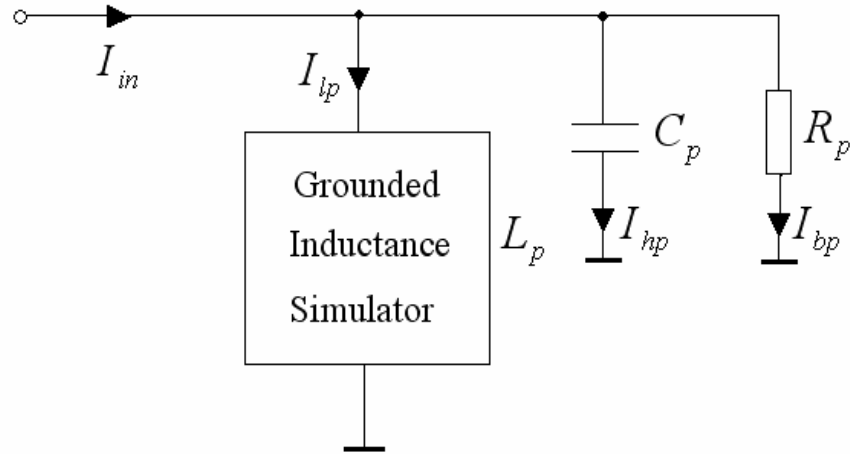


Figure 2.8. A current-mode filter used to test the proposed inductor in Figure 2.3

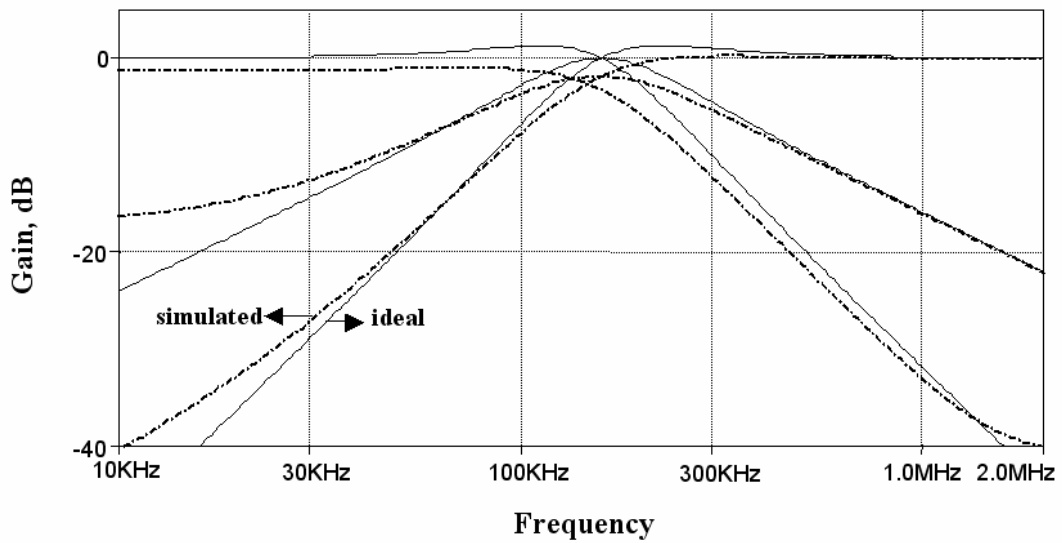


Figure 2.9. Ideal and simulated low-pass, band-pass and high-pass responses of the filter in Figure 2.8

The ideal, simulated and experimental frequency response of the filter in Figure 2.8 is shown in Figure 2.10 in which $R_p = 1\text{k}\Omega$, $C_p = 1\text{nF}$ and $L = 1\text{mH}$ are selected.

Using the GVCCIII+ given in Figure 2.1, the impedance magnitude and phase responses of the proposed inductor for $L = 1\text{mH}$ are tested. The results are shown in Figure 2.11.

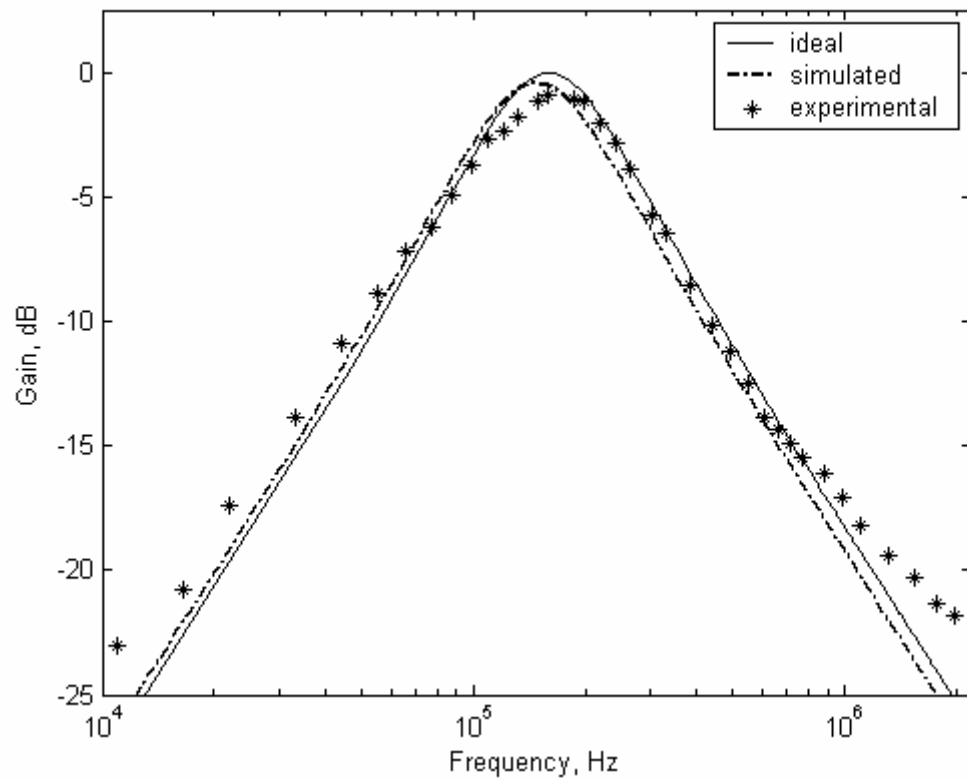


Figure 2.10. Ideal, simulated and experimental band-pass responses of the filter in Figure 2.8

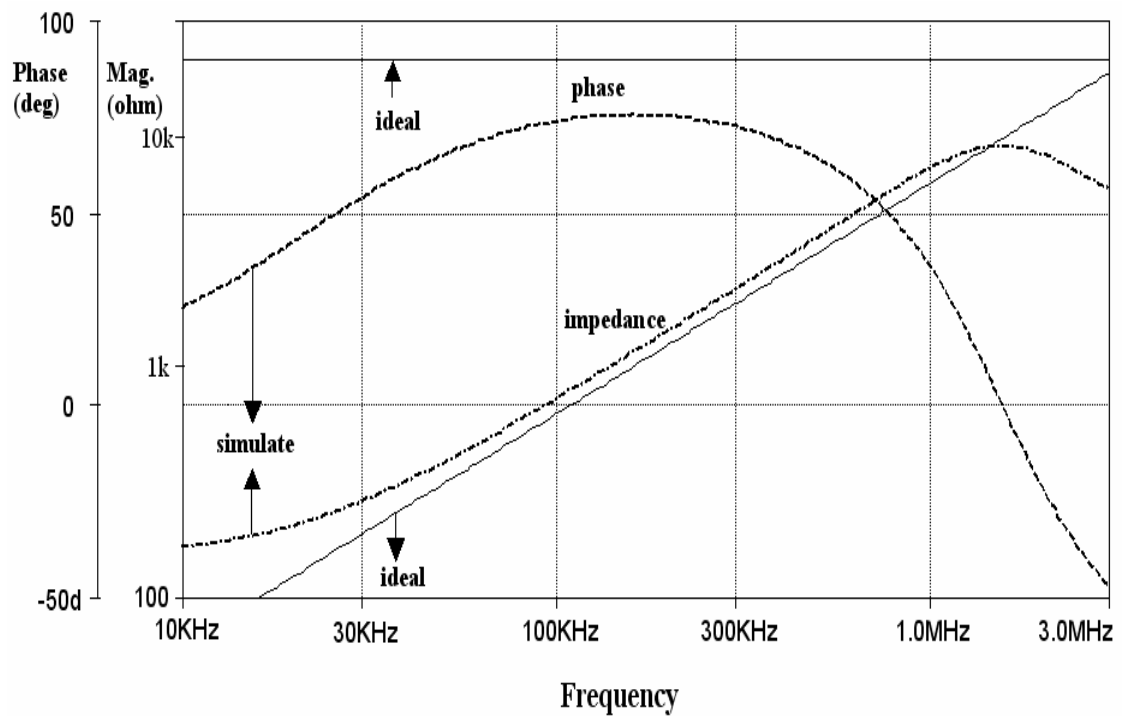


Figure 2.11. Phase and magnitude response of the impedance of the proposed inductor

Time domain responses of the simulated inductor are given in Figure 2.12. It shows the signal limitations of the inductor simulator where the grounded inductor simulator using GVCCII+ in Figure 2.2 is used. To show this, 310mV peak sinusoidal input voltage at 2 kHz is applied to the inductor with $L = 10\text{mH}$ where AD844s with DC power $\pm 15\text{V}$ are used. Both ideal and simulated terminal voltages (V_1 in Figure 2.3) are depicted in Figure 2.12.

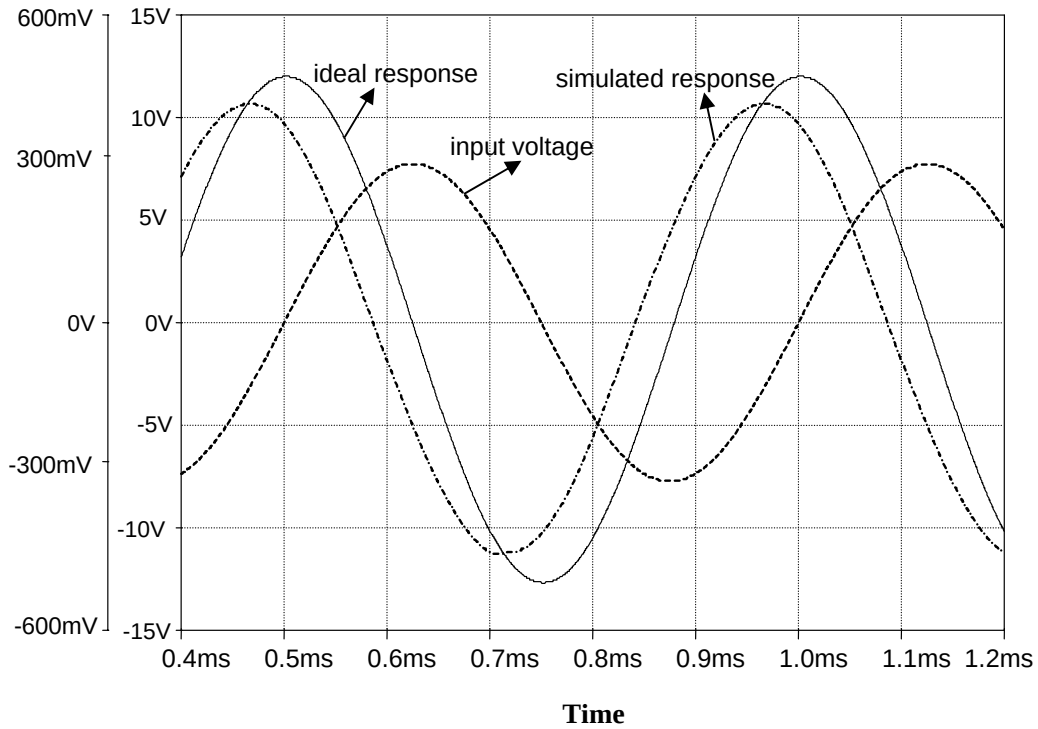


Figure 2.12. Time domain responses of the simulated inductor

From SPICE simulations $\omega_\beta = 90\pi \times 10^6 \text{ rad/s}$, $\omega_\alpha \cong \omega_\gamma = 1040\pi \times 10^6 \text{ rad/s}$, and $\beta_0 = 2.038$ are calculated, which confirms the condition $\omega_\beta \ll \min\{\omega_\alpha, \omega_\gamma\}$ given before. Also, if $R_1 = 20\text{k}\Omega$ and $R_2 = 45\text{k}\Omega$ are chosen, $\beta_0 = 1.959$ and $\omega_\beta = 405\pi \times 10^6 \text{ rad/s}$ are obtained. In general, the larger R_1 and R_2 are selected, the higher ω_β is obtained. Alternatively, if $R_1 = 20\text{k}\Omega$, $R_2 = 45\text{k}\Omega$ and only dimension of the MOS transistor M_{21} is reduced from $40/0.25 \mu\text{m}$ to $10/0.25 \mu\text{m}$, $\beta_0 = 1.89$ and $\omega_\beta = 940\pi \times 10^6 \text{ rad/s}$ are obtained.

As explained before, when the rated voltage and maximum allowable terminal currents of the conveyors are increased, the inductor simulators can be operated in wider

useful frequency ranges. The ideal, experimental and simulated results are in good agreement as expected. The difference among ideal, experimental and simulated responses mainly stems from the parasitic impedance and non-ideal gain effects of the GVCCIII+. In the next section, some important analysis such as noise analysis is given.

2.5. Further Analysis for the GVCCIII+

The noise equivalent circuit of the GVCCIII+ in Figure 2.1 is given in Figure 2.13 thus the power spectral densities of the model components (including only dominant terms) are given as in the following:

$$\overline{I_{nx}^2} = 4KT\gamma(g_{m20} + g_{m21}) \quad (2.39)$$

$$\overline{V_{nx}^2} = 4KT\gamma\left(\frac{g_{m16} + g_{m18}}{g_{m16}^2}\right) \quad (2.40)$$

$$\overline{I_{ny}^2} = 4KT\gamma(g_{m29} + g_{m30}) \quad (2.41)$$

$$\overline{V_{ny}^2} = 4KT\gamma\left(\frac{g_{m1} + g_{m3}}{g_{m1}^2}\right) \quad (2.42)$$

Here, $K = 1.38 \cdot 10^{-23}$ J/K is the Boltzman constant, T is the temperature in Kelvin and γ is a coefficient that equals to about 2.5 in some $0.25 \mu\text{m}$ MOS devices.

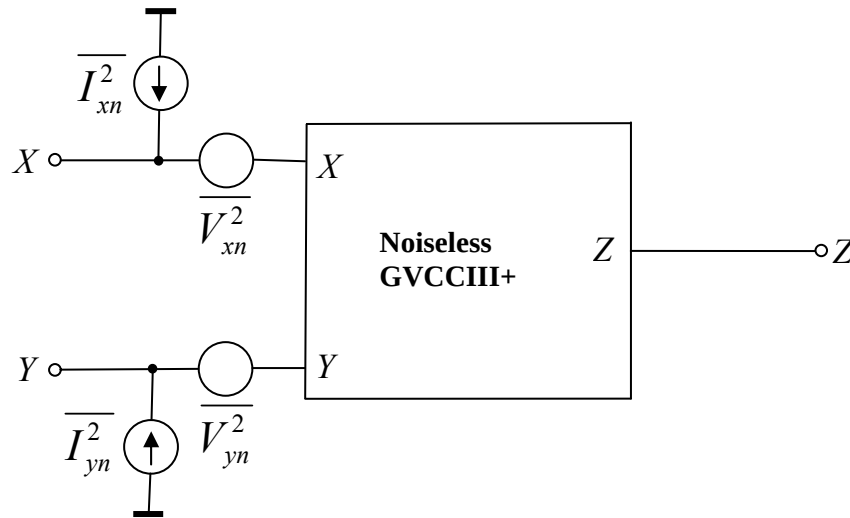


Figure 2.13. Equivalent noise model of the GVCCIII+

After a hundred runs, Monte Carlo analysis of the filter in Figure 2.8 for $250\ \mu\text{A}$ peak sinusoidal input at $159\ \text{kHz}$ is given in Figure 2.14. The following components: $R_p = 1\ \text{k}\Omega$, $C_p = 1\ \text{nF}$, $L = 1\ \text{mH}$ ($G = 1\ \text{mS}$ and $C = 1\ \text{nF}$ are selected for the simulated inductor in Figure 2.3) and GVCCIII+ of Figure 2.1 are chosen. Here, widths (W) of the MOS transistors in Figure 2.1 are taken as variables. Also, device tolerances and lot tolerances are chosen 10% and 1%, respectively.

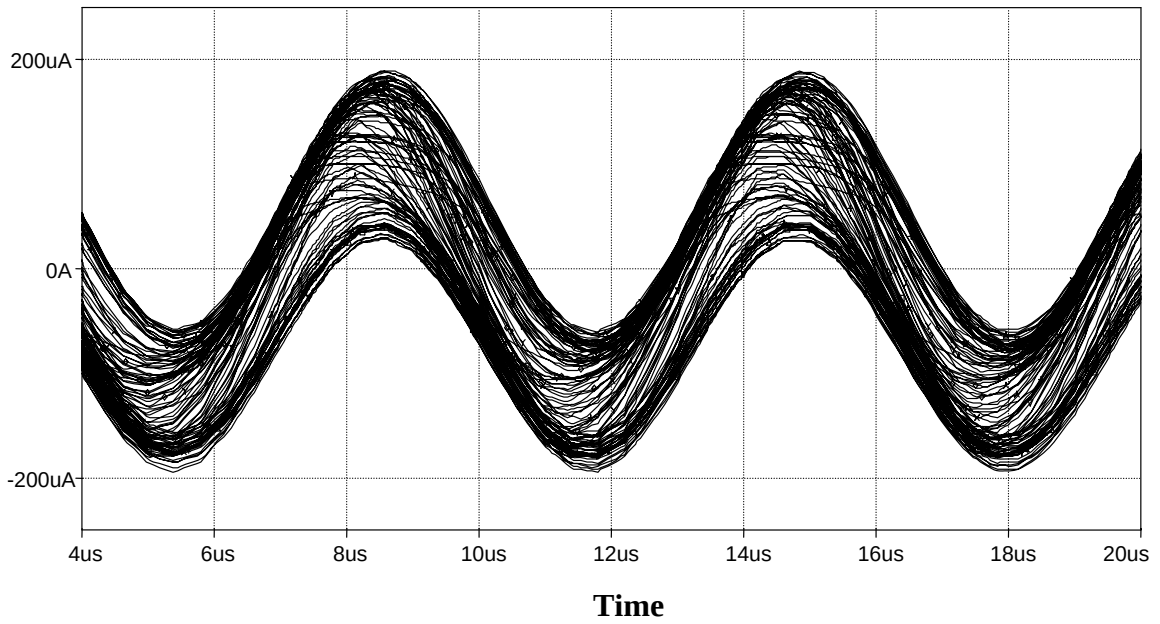


Figure 2.14. Monte Carlo analysis of the filter in Figure 2.8

In the next section, novel lossless floating inductor simulators employing CCCIs with reduced parasitic impedance effects are given as alternatives because they have no capacitor connected in series to the X terminals of the CCCIs.

2.6. Floating Inductors

Here, CCCII based positive and negative electronically tunable floating inductors (FIs) with improvements against the X terminal parasitic resistance effects are proposed. In other words, a novel negative FI and a new lossless floating inductor derived from the negative inductor employing a grounded capacitor, a dual output CCCII (DO-CCCI) and two plus-type CCCIs (CCCII+s) are developed. They have no capacitors connected in series to the X terminals of the CCCIs thus they can be operated high frequencies [82]. However, both

FIs have a limit at low frequencies stemmed from the Z and Y terminal parasitic resistors of the CCCIs. Fortunately, this problem is going to be solved in section (2.7) using parasitic impedance compensation technique. A novel lossless FI using three port CCCIs is given as example because it uses no capacitors connected in series to the X terminals of the CCCIs. Moreover, it can be constructed using commercially available active devices, AD844s.

2.6.1. Floating Inductors Employing a Grounded Capacitor

The DO-CCCII is a four-port current controlled conveyor represented by the following equations:

$$I_Y = 0 \quad (2.43)$$

$$I_{z+} = \alpha I_x \quad (2.44)$$

$$V_x = \beta V_Y + R_x I_x \quad (2.45)$$

$$I_{z-} = -\gamma I_x \quad (2.46)$$

where R_x is the parasitic resistance at terminal X of the conveyor found as [7]

$$R_x = \frac{V_T}{2I_o} \quad (2.47)$$

In equation (2.47), V_T is the thermal voltage (approximately 26mV at 25°C) and I_o is the bias current of the conveyor. Also, a CCCII+ is a three-port current conveyor described by equations (2.43) - (2.45). The frequency dependent non-ideal current gains α , γ and non-ideal voltage gain β are ideally equal to unity. Current convention is such that all currents flow into the conveyor. For the circuit shown in Figure 2.15, one can write

$$I_1 = -I_2 = -\frac{V_{Y1}}{R_{x1}} \quad (2.48)$$

$$V_{Y1} = \frac{V_1 - V_2}{R_{x2} + R_{x3}} \cdot \frac{1}{sC} \quad (2.49)$$

where R_{xi} ($i = 1, 2, 3$) is the intrinsic resistance at terminal X of the i -th CCCII and V_{Y1} is the voltage at terminal Y of the first CCCII.

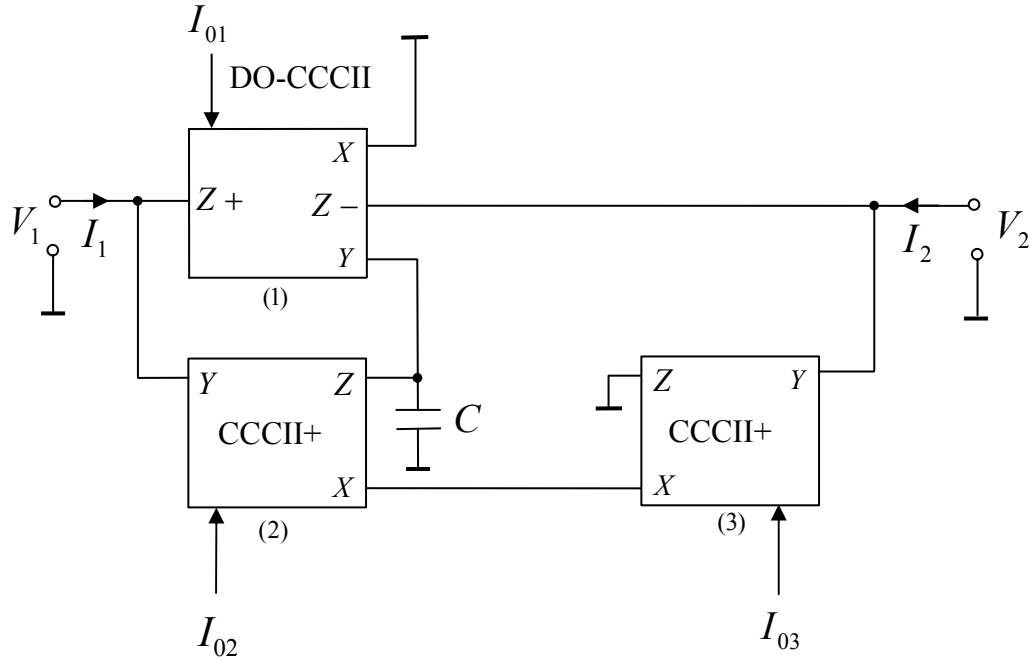


Figure 2.15. The proposed negative floating inductor simulator

Substituting equations (2.49) into equation (2.48) results in

$$I_1 = -I_2 = -\frac{V_1 - V_2}{sCR_{x1}(R_{x2} + R_{x3})} \quad (2.50)$$

The equation in (2.50) can be written in matrix form as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = -\frac{1}{sCR_{x1}(R_{x2} + R_{x3})} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (2.51)$$

Therefore, the circuit of Figure 2.15 realizes a negative lossless floating inductance whose impedance is equal to $Z_1 = -sCR_{x1}(R_{x2} + R_{x3}) = sL_{eq}$.

Similarly, one can find that the circuit shown in Figure 2.16 realizes a positive lossless floating inductor with impedance equal to $Z_2 = sCR_{x1}(R_{x2} + R_{x3}) = sL_{eq}$.

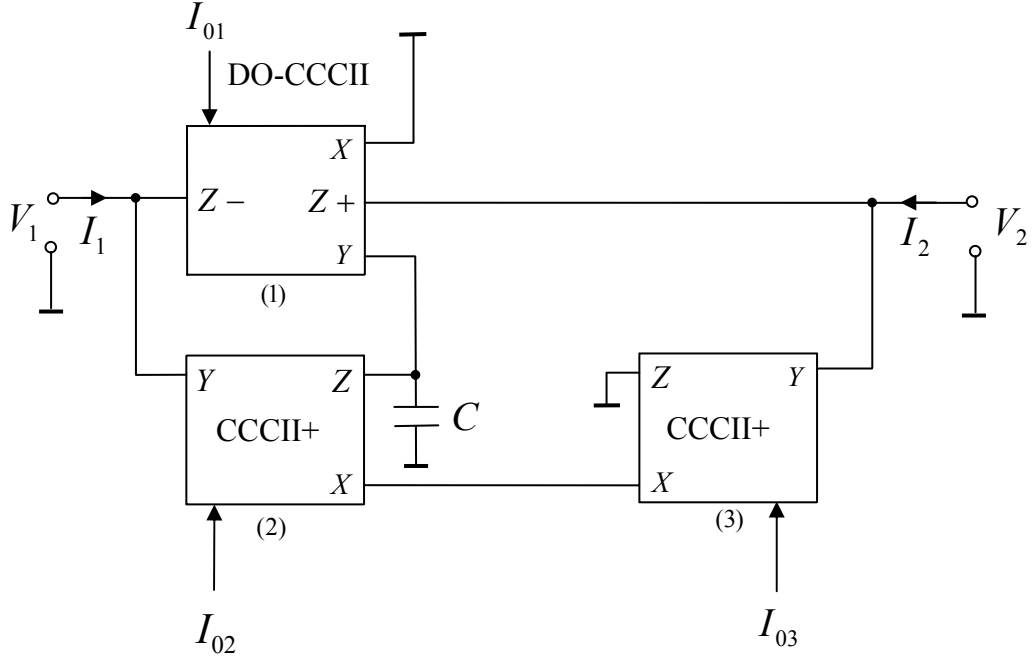


Figure 2.16. The proposed positive floating inductor simulator

The equivalent simulated inductance $L_{eq} = CR_{x1}(R_{x2} + R_{x3})$ of the circuits in Figures 2.15 and 2.16 can be tuned electronically by changing the biasing currents I_{01} , I_{02} , and I_{03} of the corresponding CCCIs. It is worthwhile to note that the circuit in Figure 2.16 is obtained by interchanging Z- and Z+ terminals of the DO-CCCI in Figure 2.15. As an example, the proposed circuits in Figures 2.15 and 2.16 with respective inductance values of $L_1 = -L_{eq} - \Delta L$ and $L_2 = L_{eq}$, can be connected in parallel resulting in a new inductance equal to

$$L_T = \frac{L_{eq}(L_{eq} + \Delta L)}{\Delta L} \quad (2.52)$$

From equation (2.52), it is observed that for small values of ΔL , large-value inductances can be obtained.

Similarly, routine analysis of the circuits given in Figures 2.15 and 2.16 yields

$$[Y_1] = \frac{\alpha_2}{Z_1} \begin{bmatrix} \alpha_1 & -\alpha_1 \\ -\gamma_1 & \gamma_1 \end{bmatrix} \quad (2.53)$$

$$[Y_2] = \frac{\alpha_2}{Z_2} \begin{bmatrix} \gamma_1 & -\gamma_1 \\ -\alpha_1 & \alpha_1 \end{bmatrix} \quad (2.54)$$

Here, α_i and γ_i are the non-ideal current gains of the i -th current controlled conveyor in Figures 2.15 and 2.16 and Y_1 and Y_2 are respectively the short circuit admittance matrices.

In this section, the proposed network in Figure 2.16 is used in the structure of a third-order low-pass ladder filter shown in Figure 2.17. The ladder filter is simulated using SPICE program. The DO-CCCIIs are simulated using the schematic implementation shown in Figure 2.18 with DC supply voltages equal to ± 2.5 V.

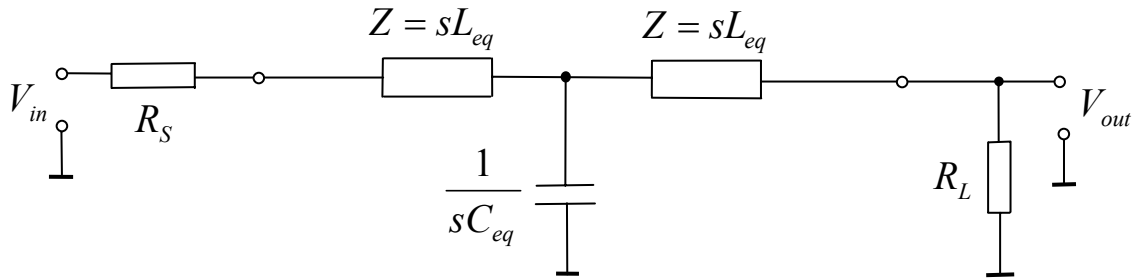


Figure 2.17. Third-order low-pass filter example

The PNP and the NPN transistors in the DO-CCCIi implementation are simulated using the parameters of the NR100N and PR100N bipolar array transistors ALA400 from AT&T given in Table 2.3 [95].

The passive components of the ladder filter are selected as $R_S = R_L = 1\text{k}\Omega$, $C_{eq} = 2\text{nF}$ and $L_{eq} = CR_{x1}(R_{x2} + R_{x3}) = 1\text{mH}$ ($C = 1\text{nF}$, $I_{01} = 13\mu\text{A}$ and $I_{02} = I_{03} = 26\mu\text{A}$). They result in a Butterworth response with 3-dB frequency of 159.15 kHz.

The ideal and simulated responses are shown in Figure 2.19. It can be seen that the ideal and simulation results are in quite good agreement.

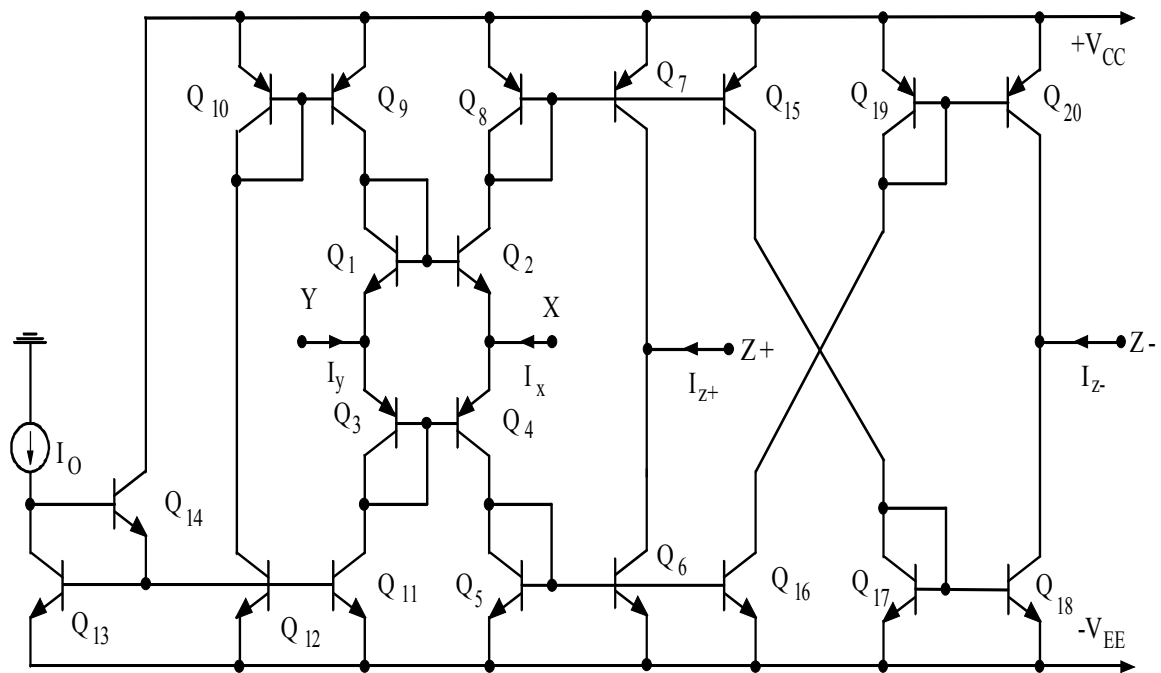


Figure 2.18. Internal structure of the DO-CCCII

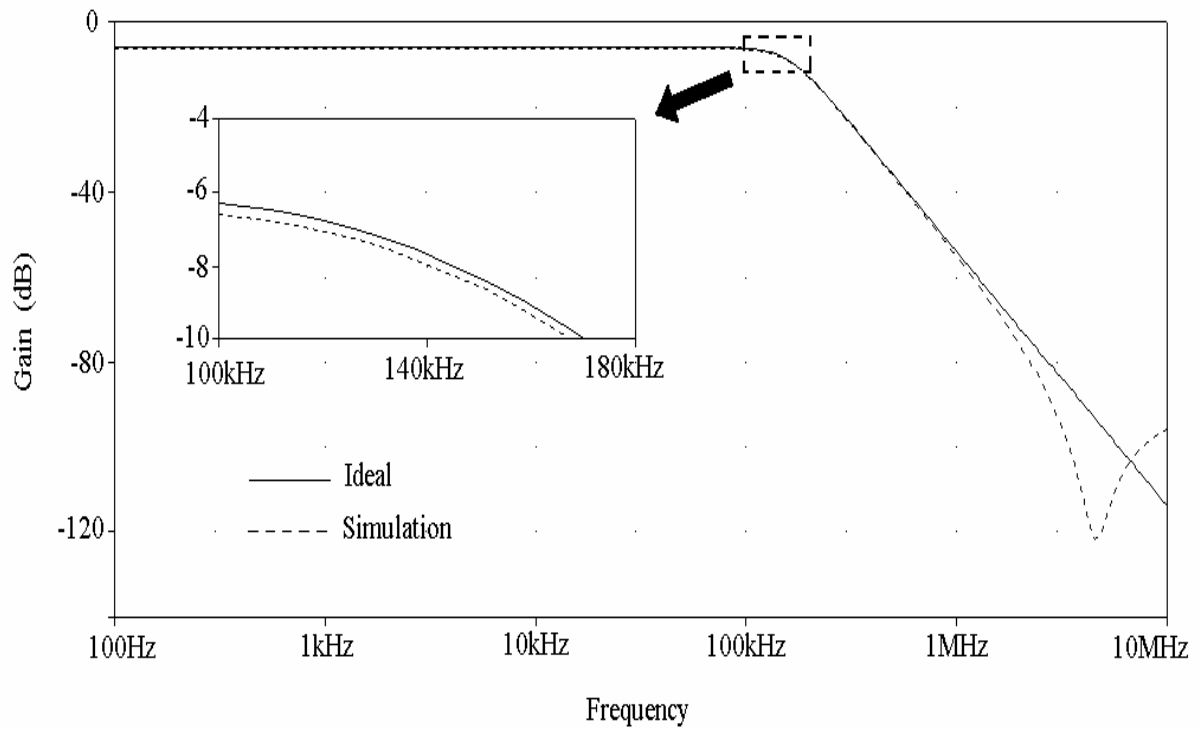


Figure 2.19. Ideal and simulated frequency responses of the filter given in Figure 2.17

The large signal behavior of the circuit in Figure 2.17 is tested by investigating the dependence of the output harmonic distortion of the low-pass response on the amplitude of

the sinusoidal input signal. The results are shown in Figure 2.20. The total harmonic distortion (THD) for a sinusoidal input voltage with peak value of 100mV at 159 kHz is found to be 2.77%. It can be seen that the harmonic distortion rapidly increases if the input signal amplitude is increased beyond 100mV.

Table 2.3. Parameters of the NR100N and PR100N bipolar array transistors

.MODEL NR100N NPN (IS=121E-018 BF=137.5 VAF=159.4 IKF=6.974E-3 + ISE=36E-16 NE=1.713 BR=0.7258 VAR=10.73 IKR=2.198E-3 RE=1 RB=524.6 + RBM=25 RC=50 CJE=0.214E-12 VJE=0.5 MJE=0.28 CJC=0.983E-13 VJC=0.5 + MJC=0.3 XCJC=0.034 CJS=0.913E-12 VJS=0.64 MJS=0.4 FC=0.5 TF=0.425E-9 + TR=0.425E-8 EG=1.206 XTB=1.538 XTI=2)

.MODEL PR100N PNP (IS=73.5E-018 BF=110 VAF=51.8 IKF=2.359E-3 + ISE=25.1E-16 NE=1.650 BR=0.4745 VAR=9.96 IKR=6.478E-3 RE=3 RB=327 + RBM=24.55 RC=50 CJE=0.180E-12 VJE=0.5 MJE=0.28 CJC=0.164E-12 VJC=0.8 + MJC=0.4 XCJC=0.037 CJS=1.03E-12 VJS=0.55 MJS=0.35 FC=0.5 TF=0.610E-9 + TR=0.610E-8 EG=1.206 XTB=1.866 XTI=1.7)

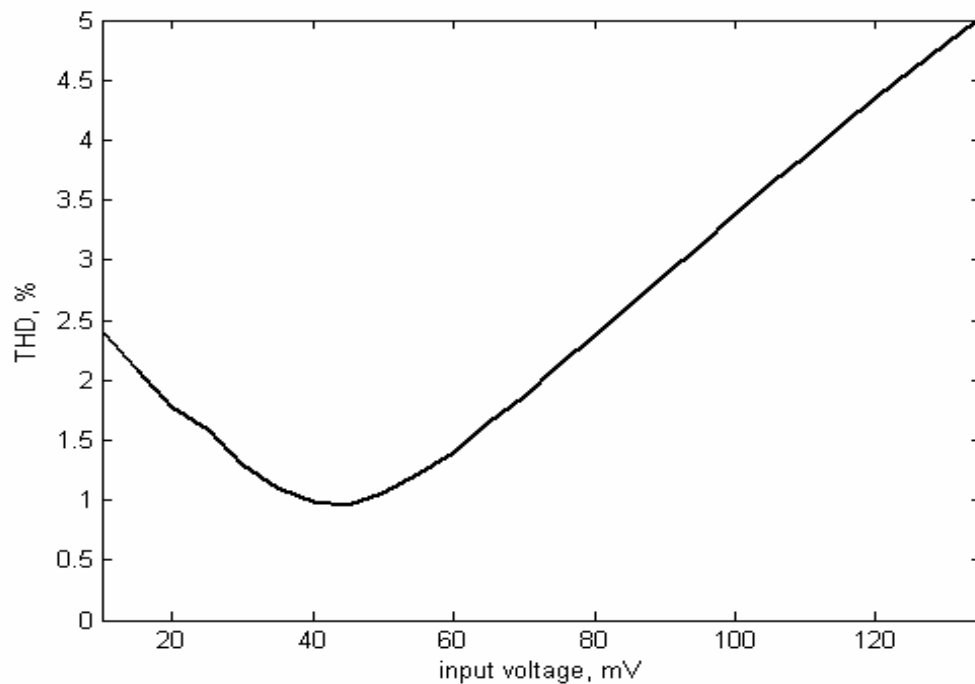


Figure 2.20. Output total harmonic distortion of the filter in Figure 2.17 for different input signal amplitudes

2.6.2. A Floating Inductor Using Single Output CCCIs

Routine analysis of the proposed new circuit in Figure 2.21 gives the following short circuit admittance matrix:

$$[Y_i] = \frac{1}{sC(R_{x1} + R_{x2})R_{x3}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} = \frac{1}{sL_{eq}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \quad (2.55)$$

The simulated lossless inductance of the circuit in Figure 2.21 is found as $L_{eq} = C(R_{x1} + R_{x2})R_{x3}$, where R_{xk} , $k = 1, 2, 3$, is the parasitic resistance of the k th CCCII. It can be seen that the inductance value can be controlled electronically by adjusting the biasing currents I_{o1} , I_{o2} and I_{o3} . Also, its equivalent circuit is given in Figure 2.22.

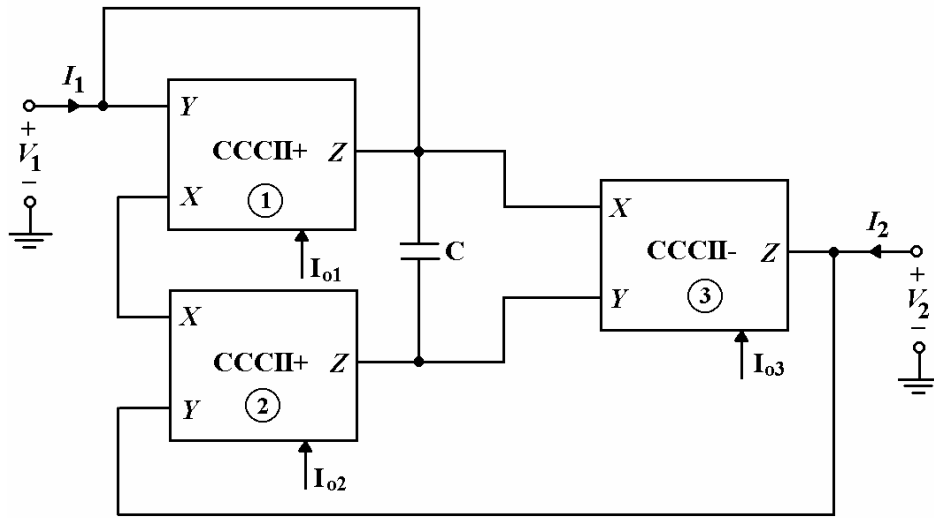


Figure 2.21. Proposed lossless floating inductor simulator

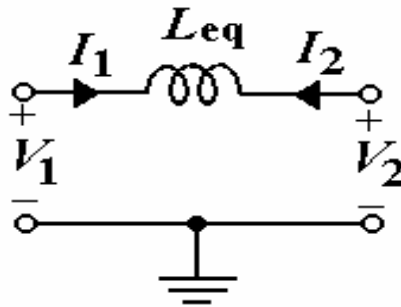


Figure 2.22. The equivalent circuit for the FI in Figure 2.21

Sensitivity analysis of the circuit shows that

$$S_{R_{x3}}^{L_{eq}} = S_C^{L_{eq}} = 1 \quad S_{R_{x1}}^{L_{eq}} = \frac{R_{x1}}{R_{x1} + R_{x2}} \quad S_{R_{x2}}^{L_{eq}} = \frac{R_{x2}}{R_{x1} + R_{x2}} \quad (2.56)$$

which are all no more than unity.

Taking into account α and β effects on the circuit in Figure 2.21, it can be found that

$$I_1 = \frac{sC(R_{x1} + R_{x2})(1 - \beta_3)V_1 + (sCR_{x3}(\alpha_2 - \alpha_1) + \alpha_2\beta_3)(V_1\beta_1 - V_2\beta_2)}{sL_{eq}} \quad (2.57)$$

$$I_2 = \frac{sC(R_{x1} + R_{x2})(\beta_3 - 1)\alpha_3V_1 + \alpha_2\alpha_3\beta_3(V_2\beta_2 - V_1\beta_1)}{sL_{eq}} \quad (2.58)$$

By setting $V_2 = 0$, the proposed circuit can also be used as a grounded inductance. In this case, the α and β non-ideal gain effects of the CCCIs on the resulting grounded inductor in Figure 2.21 can be expressed as follows:

$$V_1 = \frac{sL_{eq}}{sC((R_{x1} + R_{x2})(1 - \beta_3) + R_{x3}(\alpha_2 - \alpha_1)\beta_1) + \alpha_2\beta_1\beta_3} I_1 \quad (2.59)$$

Thus, an extra parallel resistance $(R_{x1} + R_{x2})R_{x3}/((R_{x1} + R_{x2})(1 - \beta_3) + R_{x3}(\alpha_2 - \alpha_1)\beta_1)$ due to the non-idealities is found for the inductor. Also the value of the simulated inductance changes to $L_{eq}/(\alpha_2\beta_1\beta_3)$. The quality factor of the grounded inductor (Q_L) is calculated as

$$Q_L = \frac{\alpha_2\beta_1\beta_3}{\omega C((R_{x1} + R_{x2})(1 - \beta_3) + R_{x3}(\alpha_2 - \alpha_1)\beta_1)} \quad (2.60)$$

where ω is the angular frequency.

On the other hand, one can obtain a lossless grounded inductor even under non-ideality conditions by selecting $V_1 = 0$. In this case, the voltage at the second port is found as

$$V_2 = \frac{sL_{eq}}{\alpha_2\alpha_3\beta_2\beta_3} I_2 \quad (2.61)$$

In the next two subsections, simulation and experimental results using the the floating inductor in Figure 2.22 are given to exhibit the performance of the inductor.

2.6.2.1. Simulation Results

The lossless inductance simulator in Figure 2.22 is used to construct a fifth-order Chebyshev low-pass filter as shown in Figure 2.23 [37].

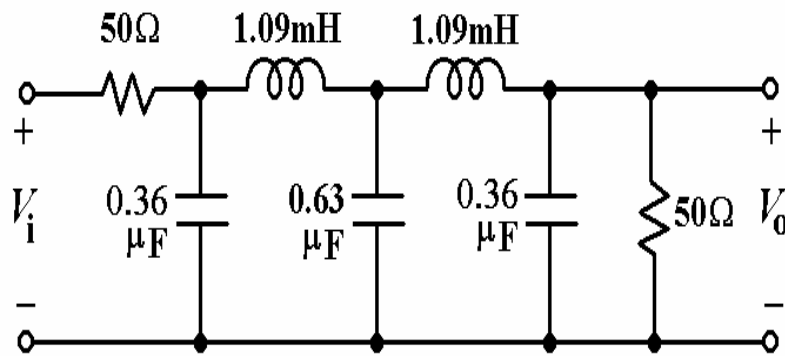


Figure 2.23. Fifth-order low-pass filter

The circuit of Figure 2.23 has been simulated using SPICE circuit simulation program. The active and passive elements of the inductance simulator are chosen as $I_{o1} = I_{o2} = I_{o3} = 20\mu\text{A}$ and $C = 1.2899\text{nF}$ in order to obtain a synthetic inductance of $L_{eq} = 1.09\text{mH}$. The filter specifications with DC power supply voltages $\pm 2.5\text{ V}$ are as follows:

- 1- 10 kHz bandwidth with 0.1 dB in-band ripple.
- 2- Stop-band attenuation equal to 30 dB.
- 3- Equal terminating resistance of 50Ω .

The frequency response of the filter is shown in Figure 2.24. It can be seen that the simulation and ideal results are in good agreement. The deviation from the ideal characteristics at low frequencies stems from the parasitic impedance effects of the CCCIs.

The large signal behavior of the circuit in Figure 2.23 is tested with investigation of the dependence of the output harmonic distortion for the low-pass response on the amplitude of the sinusoidal input signal. The obtained results are given in Table 2.4. The total harmonic distortion (THD) as seen from the Table 2.4 for a sinusoidal input voltage with peak value of 10mV at 159.15 kHz (resonance frequency) is obtained as 2.5 %. The total power dissipation of the filter is found to be 3.17mW.

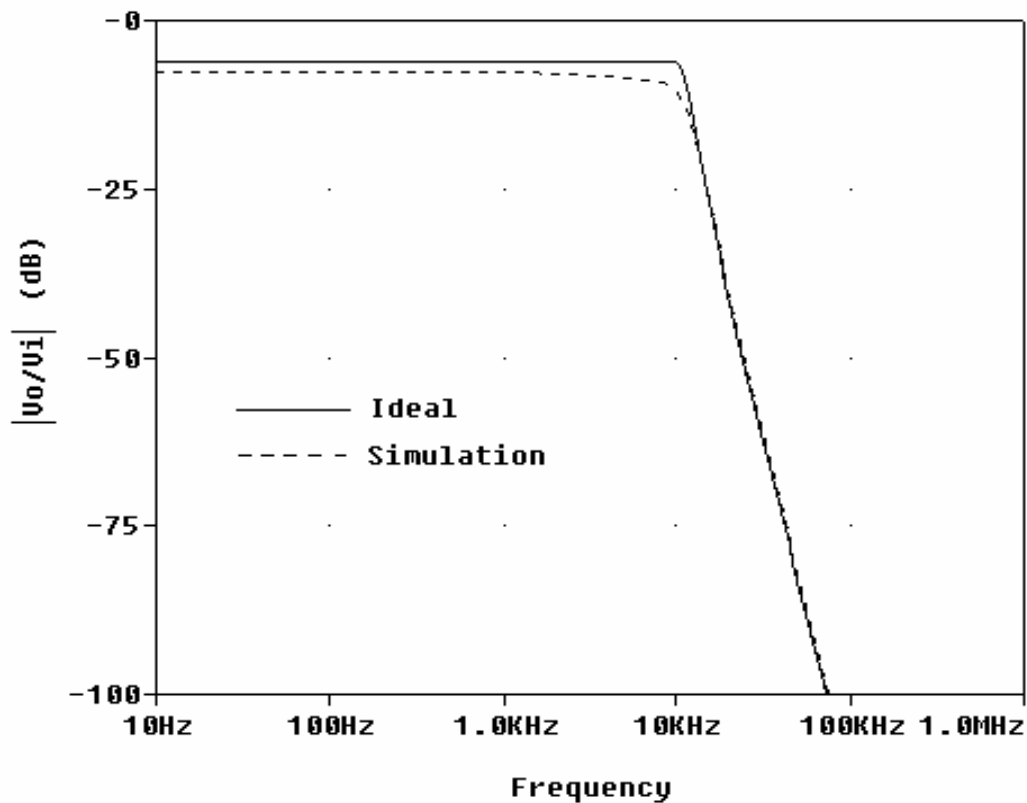


Figure 2.24. Simulated and ideal characteristic of the low-pass filter

Table 2.4. THD of the fifth-order filter in Figure 2.23

Amplitude (mV)	Total Harmonic Distortion (%)
1	0.7
5	1.47
10	2.5
50	5.2
100	11.8

2.6.2.2. Experimental Results

The proposed inductance of Figure 2.22 is constructed using AD844s, 1% tolerance discrete resistors and polystyrene capacitors to perform an experimental on the functionality. To implement a CCII-, two CCII+s are used as shown in Figure 2.25. External resistors of $1\text{k}\Omega$ are used instead of the intrinsic resistances, $R_{x1} + R_{x2}$ and R_{x3} . Also, $C=1\text{nF}$ is selected, which results in an inductance value of 1mH . The supply voltages are chosen as $\pm 5\text{V}$. The constructed inductance is tested in a series RLC circuit shown in Figure 2.26, which has the following transfer function:

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{10^6 s}{s^2 + 10^6 s + 10^{12}} \quad (2.62)$$

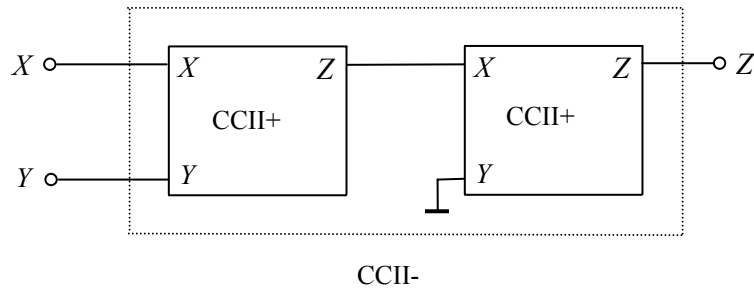


Figure 2.25. CCII- implementation using CCII+s

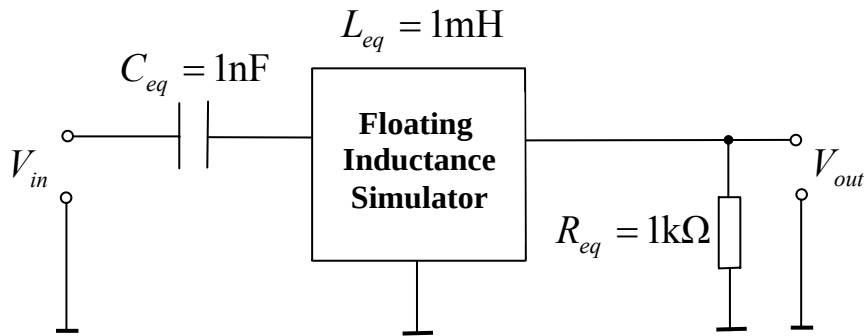


Figure 2.26. A series RLC circuit used as a voltage-mode band-pass filter

The filter in Figure 2.26 realizes a second-order band-pass filter with angular resonance frequency and quality factor equal to $f_0 = 159.15\text{ kHz}$ and $Q = 1$, respectively.

The ideal, simulated and experimental frequency responses of the band-pass filter of Figure 2.26 are depicted in Figure 2.27.

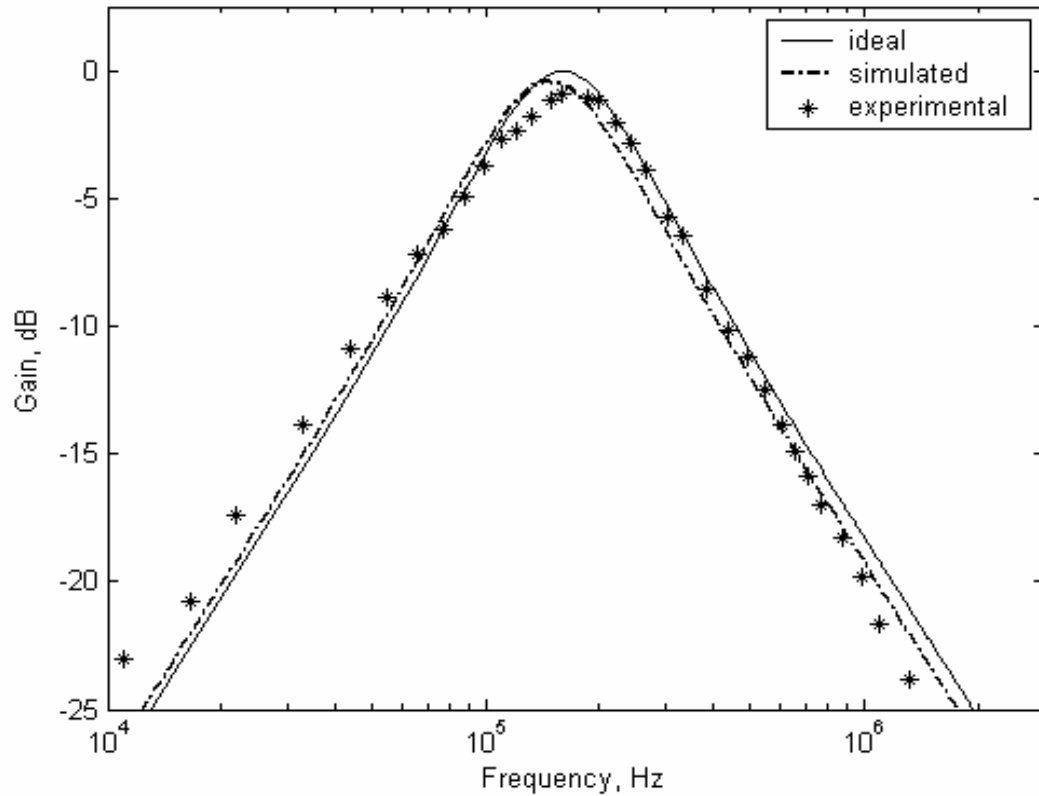


Figure 2.27. Ideal, simulated and experimental frequency responses of the filter in Figure 2.26

It can be seen that the experimental results are in good agreement with theoretical analysis as expected.

Also, by changing the value of the external resistor used instead of R_{x3} , we tested the tunability of the proposed lossless floating inductance.

The variability of the inductance value is shown in Figure 2.28.

It can be seen that the proposed inductance can be tuned between 0.1mH and 100mH with a quite good accuracy.

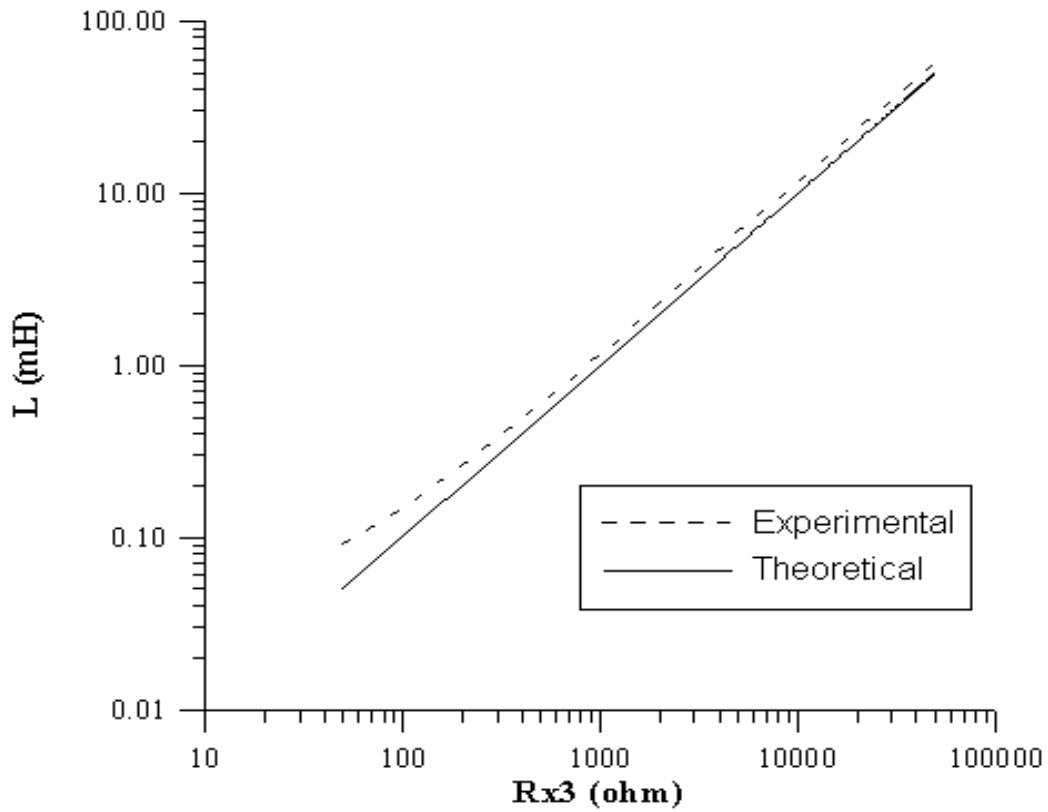


Figure 2.28. Tuning of the simulated floating inductance

The proposed inductance can also realize inductance values more than 100mH by selecting higher values for R_{x3} , however the amplitude of the input signal must be kept small enough.

We have given three FIs, two of them positive FIs. They can be operated at high frequencies as explained before. Fortunately, in the next section, the limit at low frequencies due to the Z and Y terminal parasitic resistors is reduced by using a technique namely parasitic impedance compensation technique. Consequently, FIs and grounded inductor simulators can be operated properly at both low and high frequencies if parasitic impedance effects are the dominant non-ideality.

2.7. Parasitic Impedance Effect Reduction

We show that for some topologies, certain parasitic resistance effects especially at low frequencies can be reduced and the low frequency performance of the circuit can be

improved. In this section such a CFOA based inductor simulator is given to exhibit how the parasitic impedance effects (Z terminal parasitic resistance effects) are reduced.

Using standard notation, the CFOA can be represented by the following matrix equation:

$$\begin{bmatrix} I_z \\ I_y \\ V_x \\ V_w \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & sC_z + 1/R_z \\ 0 & 0 & sC_y + 1/R_y & 0 \\ R_x & 0 & 1 & 0 \\ 0 & R_w & 0 & 1 \end{bmatrix} \begin{bmatrix} I_x \\ I_w \\ V_y \\ V_z \end{bmatrix} \quad (2.63)$$

Here, parasitic resistances (R_x and R_w in series are ideally zero, $R_z = 1/G_z$ and $R_y = 1/G_y$ in parallel, are ideally infinite) and capacitances (C_z and C_y in parallel are ideally zero) bring extra terms to the impedances of the introduced inductor derived from the gyrators in [20] and [21] and given in Figure 2.29 thus the high and low frequency performance of the presented grounded inductor simulator are effected.

In the above matrix equation, the parallel parasitic elements are connected to the corresponding terminals with their other terminal grounded.

Straightforward analysis of the proposed circuit in Figure 2.29 gives the following driving point impedance:

$$Z_{in} = \left(\frac{1}{sC_{z2} + \frac{1}{R_{z2}}} \right) // \left((R_1 + R_{x1})(R_2 + R_{x2} + R_{w1}) \left(s(C + C_{z1} + C_{z3} + C_{y3}) + \frac{1}{R_{z1}} + \frac{1}{R_{z3}} + \frac{1}{R_{y3}} - \frac{1}{R_3 + R_{x3}} \right) \right) \quad (2.64)$$

Using equation (2.64), the limitation at low frequencies is given by

$$f \gg f_\beta = \frac{1}{2\pi} \frac{\frac{1}{R_{z1}} + \frac{1}{R_{z3}} + \frac{1}{R_{y3}} - \frac{1}{R_3 + R_{x3}}}{C + C_{z1} + C_{z3} + C_{y3}} \quad (2.65)$$

Here, f_β is the low frequency pole of the impedance of the inductor in Figure 2.29 thus if $f \geq 10f_\beta$ is chosen (see Appendix B), the effects of the parasitic resistances in equation (2.65) remain within less than one per cent error. Consequently, $R_3 \geq R_z / 2 - R_{x3}$ should be connected in series to the X terminals of the third CFOA thus $Z_3 = -((R_z / 2 - R_x) + R_x) // R_z = -R_z$ for $R_3 = R_z / 2 - R_{x3}$ is obtained.

It is well known that R_{y3} is very large thus it can be ignored. Hence, the limitation at low frequencies completely vanishes so the useable frequency range increases. On the other hand, the component $1/(sC_{z2} + 1/R_{z2})$ in equation (2.64) affects the high frequency performance of the circuit in Figure 2.29. Fortunately, if the filter in Figure 2.30 is constructed, this filter suffers less from the low frequency restrictions besides the high frequency restrictions stemmed from the parasitic impedance effects.

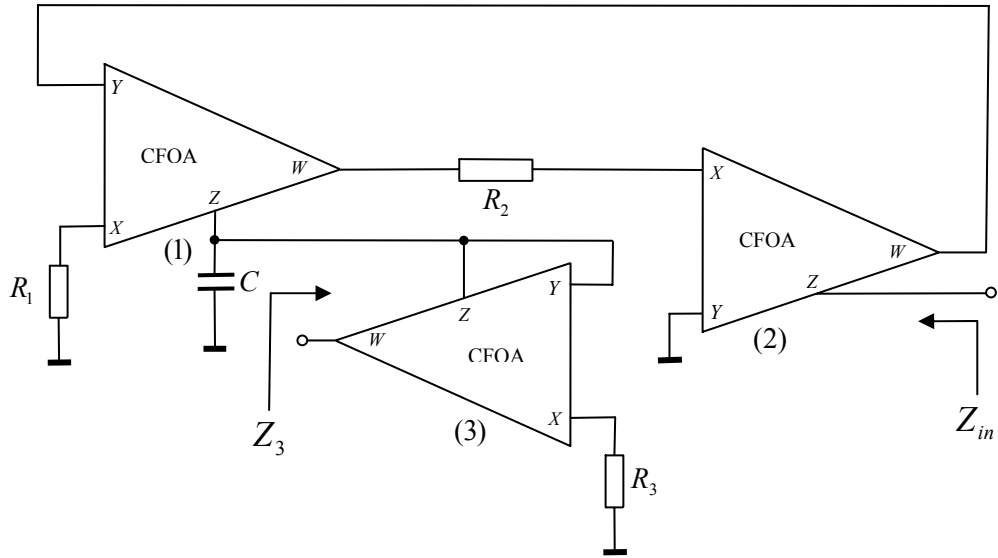


Figure 2.29. Proposed inductor simulator with reduced parasitic impedance effects

In general, for the circuit in Figure 2.29, the following inequality is given by:

$$\frac{1}{R_{3\min} + R_{x3\min}} \leq \frac{1}{R_{z1\max}} + \frac{1}{R_{z3\max}} + \frac{1}{R_{y3\max}} \quad (2.66)$$

Here, $R_{3\min} = R_3 - \Delta R_3$ thus $R_3 = R_{3\min} + \Delta R_3$ should be chosen, $R_{z1\max} = R_{z1} - \Delta R_{z1}$, $R_{x3\min} = R_{x3} - \Delta R_{x3}$, $R_{z3\max} = R_{z3} + \Delta R_{z3}$ and $R_{y3\max} = R_{y3} + \Delta R_{y3}$. The component ΔR is the maximum deviation of the resistors. Also, in the worst case, the parasitic resistance R_T seen at the Z terminal of the first CFOA in Figure 2.29 is computed as

$$\frac{1}{R_T} = \frac{1}{R_{z1\min}} + \frac{1}{R_{z3\min}} + \frac{1}{R_{y3\min}} - \frac{1}{R_{3\max} + R_{x3\max}} \quad (2.67)$$

where R_T is the overall parasitic resistance across the Z terminal. Routine analysis of the filter in Figure 2.30 without considering the component $1/(sC_{z2} + 1/R_{z2})$ gives the following filter TF:

$$\frac{V_{out}}{V_{in}} = \frac{s \frac{\omega_0}{Q}}{s^2 + s \frac{\omega_0}{Q} + \omega_0^2} \quad (2.68)$$

where $\omega_0 = 1/\sqrt{L_{eq}C_{eq}}$ and $Q = \omega_0 R_{eq} C_{eq}$.

Here, $L_{eq} = s(C + C_{z1} + C_{z3} + C_{y3})(R_1 + R_{x1})(R_2 + R_{x2} + R_{w1})$ in which the effects of R_z are eliminated.

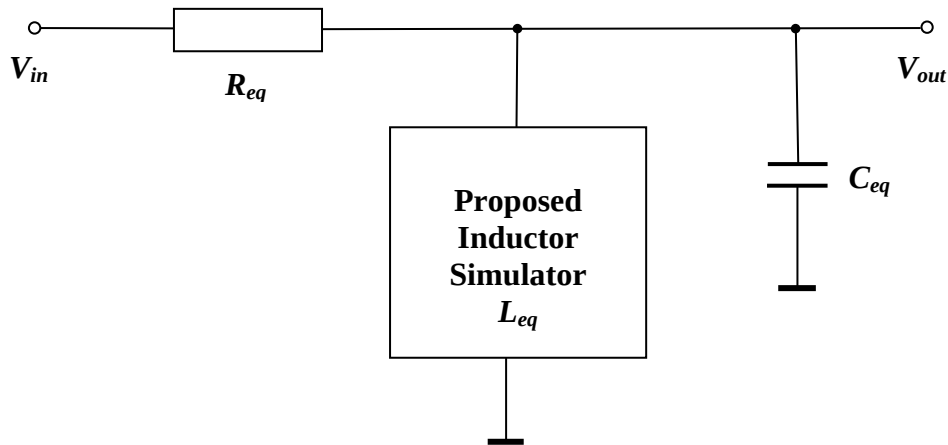


Figure 2.30. Band-pass filter example

Similarly, applying straightforward analysis for the filter in Figure 2.30 and taking into account the component $1/(sC_{z2} + 1/R_{z2})$ gives the following filter TF:

$$\frac{V_{out}}{V_{in}} = \frac{s \frac{\omega_{onew}}{Q_{new}}}{s^2 + s \frac{\omega_{onew}}{Q_{new}} + \omega_{onew}^2} \quad (2.69)$$

where $\omega_{onew} = 1/\sqrt{L_{eq}(C_{eq} + C_{z2})}$ and

$$Q_{new} = \omega_{onew} (R_{eq} // R_{z2})(C_{eq} + C_{z2}).$$

Note that only the parameters ω_o and Q of the filter are affected slightly. Furthermore, simulations of the presented circuit are performed using commercially available active devices with DC power supply voltages $\pm 15V$. The passive elements $R_1 = 50k\Omega$, $R_2 = 50k\Omega$, $R_3 = 1.5M\Omega$ and $C = 1nF$ are selected for the proposed inductor to obtain $L_{eq} = 2.5H$. The performance of the simulated inductor is shown in Figure 2.31.

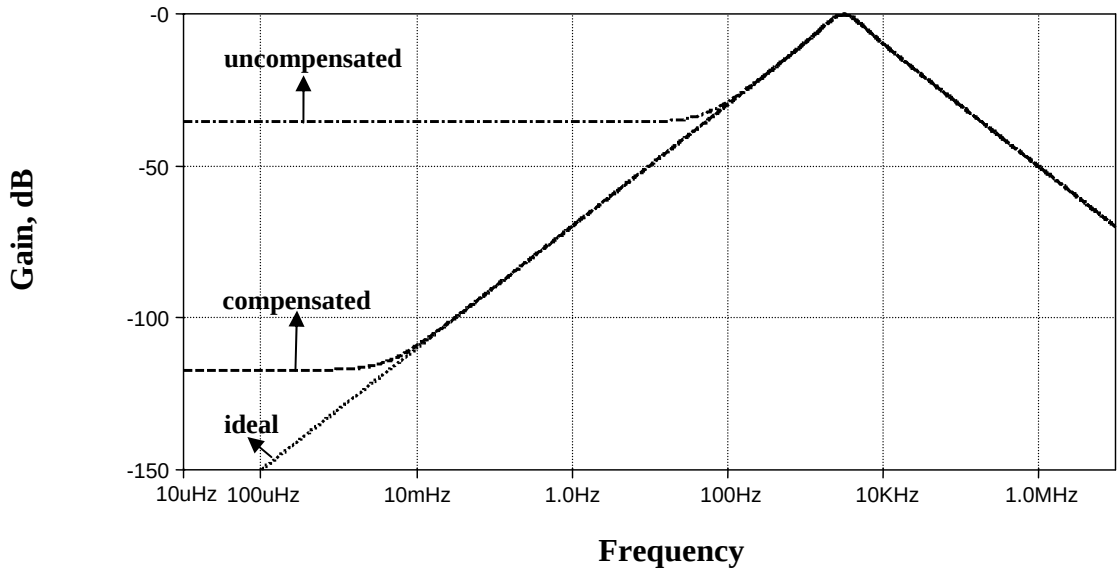


Figure 2.31. Compensated and uncompensated frequency domain responses of the filter depicted in Figure 2.30

In Figure 2.31, a band-pass filter example exhibited in Figure 2.30 with $C_{eq} = 1\text{nF}$ and $R_{eq} = 50\text{k}\Omega$ is chosen thus $\omega_0 = 20\text{k rad/s}$ and $Q = 1$. In summary, the proposed inductor in Figure 2.29 is simulated both with the third CFOA (compensated inductor) and without third CFOA (uncompensated inductor). Both compensated and uncompensated inductors in addition to an ideal inductor are used in the filter construction in Figure 2.30.

Solutions for increasing the useful frequency range of the simulated inductors can be summarized as follows:

- i) The effects of the frequency dependent non-ideal current and voltage gains must be reduced especially their corner frequencies must be increased by proper designs. In the next chapter, novel grounded inductor simulators with reduced non-ideal gain effects are going to be proposed.
- ii) The effects of parasitic impedance can be decreased by proper design of simulated inductors or using extra compensation circuits [87].
- iii) It is observed that if applied input is a voltage source, the inductor has a limit at low frequencies thus the inductor simulator should be operated at high frequencies if it is driven by a voltage source.
- iv) It is going to be explained in the next chapter that if applied input is a current source, the simulated inductor has a limit at high frequencies so it should be operated at lower frequencies if it is driven by a current source.
- v) An inductor simulator should have only resistive components but no capacitors connected in series to the X terminals of the conveyor if it is desired to be operated at high frequencies. Nevertheless, it has a limit at low frequencies. Fortunately, a parasitic impedance compensation technique for reducing the limit at low frequencies can be used in the inductor simulator.

In the next chapter, non-ideal gain effects with their reduction and signal limitations of the simulated inductors stemmed from the maximum allowable terminal currents of the active devices, AD844 ICs of Analog Devices are investigated where applied input is a current source.

3. NON IDEAL GAIN EFFECTS OF THE ACTIVE DEVICE AND TERMINAL CURRENT LIMITATIONS OF THE SIMULATED INDUCTORS

The non-ideal gains of the CCII_s cause deviations from the ideal inductive impedance in synthetic inductance simulator circuits. The derivation of analytical expressions for the impedances in terms of current conveyor non-ideal gains will be helpful for the designer to evaluate and compare the performances and thus to select the most suitable topology for a given application.

The terminal current limitations of the CCII_s result in restrictions in passive element, operating frequency and applied input current source values for the realized circuits. If passive element values and the frequency are fixed, the terminal current of each CCII depends on the externally applied current. Thus, there is an allowable range of applied input current for proper operation and acceptable distortion level.

In this chapter, two new and three previously published grounded inductance configurations are investigated to illustrate the effects of CCII non-idealities on the impedances of these inductors. Analytical expressions for the inductor impedances are derived to evaluate the deviations due to CCII non-ideal gains. Hence, one can determine the requirements for the CCII non-ideality terms (current and voltage gains) to obtain better performance for these grounded inductances. Moreover, the effects of the terminal current restrictions on the applied input currents for the specified resistance, capacitance and frequency values are given. The inductances with better properties with respect to the non-ideal gains or terminal current limitations of CCII_s are also shown.

Also, two novel inductor simulators and two analog filters employing a single new active device called modified current feedback operational amplifier (MCFOA) are developed. Six novel inductor simulators with reduced non-ideal effects can easily be obtained by using these two inductor simulators.

3.1. Equivalent Impedance of the Circuits

In this section, equivalent impedances of two novel and three previously published CCII based grounded simulated inductors are investigated. The CCII is described with the following matrix equation:

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} \beta & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (3.1)$$

In the above matrix equation, all the current directions are taken into the device. The frequency dependent non-ideal current gain $+\alpha$ corresponds to the CCII+, and $-\alpha$ corresponds to the CCII-. The frequency dependent non-ideal voltage gain β and α are ideally equal to unity. The new presented inductors are given in Figures 3.1 and 3.2, and previously published inductors are shown in Figures 3.3 – 3.5. They are denoted as circuits 1-5, respectively.

Routine analysis of these circuits, the following input impedances are given below: The presented first network in Figure 3.1 with $R_3 = R_1 R_2 / (R_1 + R_2)$ has the following input impedance:

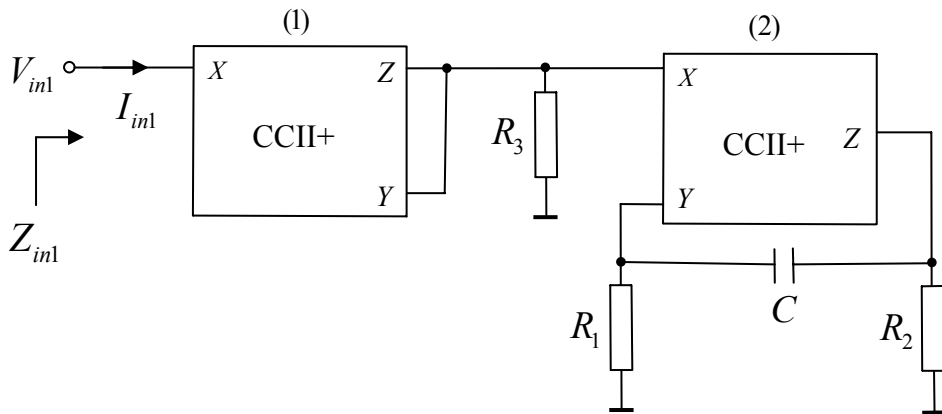


Figure 3.1. The proposed first circuit realizing lossless simulated grounded inductor employing two CCII+s as active components with $R_3 = R_1 R_2 / (R_1 + R_2)$

$$Z_{in1} = sCR_1R_2 = sL_1 \quad (3.2)$$

The presented second circuit in Figure 3.2 with $R_3 = R_1$ presents the following impedance at its input port:

$$Z_{in2} = \frac{sCR_1R_2}{2} = sL_2 \quad (3.3)$$

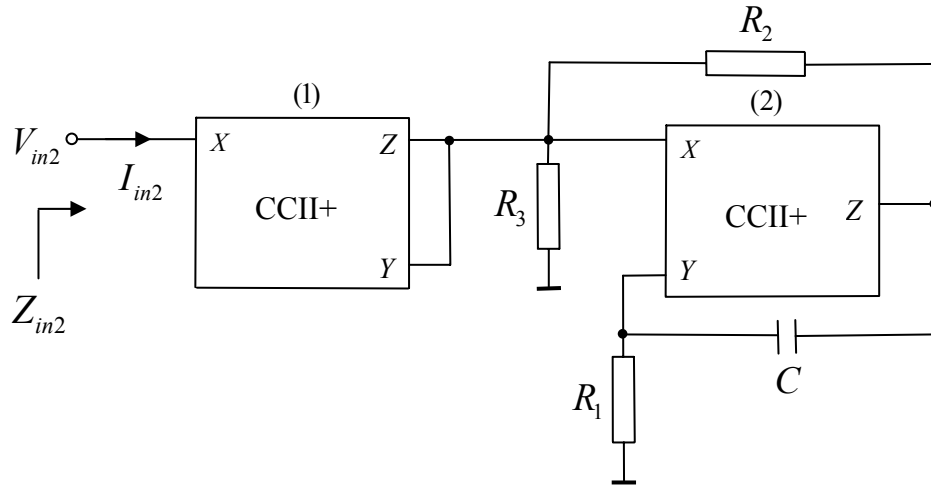


Figure 3.2. The proposed second circuit realizing lossless simulated grounded inductor employing two CCII+s as active components with $R_3 = R_1$

The equivalent input impedance of the Sedra-Smith gyrator [3] depicted in Figure 3.3 can be given as

$$Z_{in3} = sCR_1R_2 = sL_3 \quad (3.4)$$

The inductance simulator shown in Figure 3.4 shows the following input impedance:

$$Z_{in4} = sCR_1R_2 = sL_4 \quad (3.5)$$

Finally, in Figure 3.5 with $G_3 = G_4$ and $2G_1 = G_2 - G_3$ where $G_p = 1/R_p$ ($p = 1, 2, 3, 4$), and has the following input impedance:

$$Z_{in5} = \frac{sCR_1^2}{2} = sL_5 \quad (3.6)$$

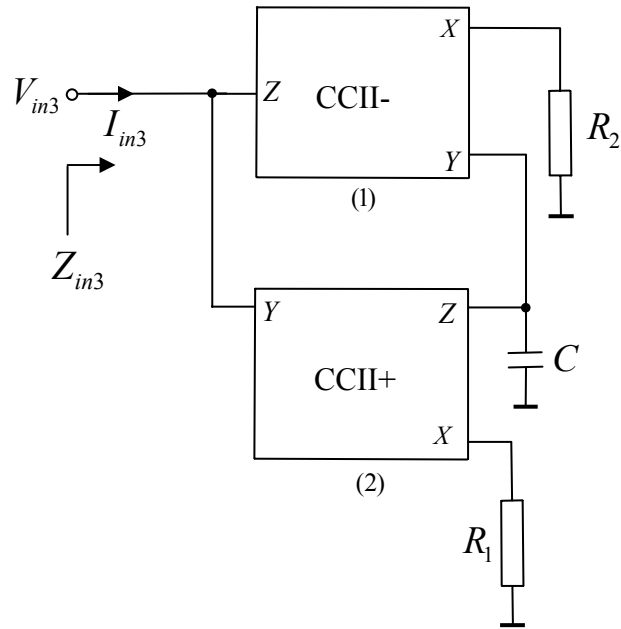


Figure 3.3. Sedra-Smith gyrator based grounded inductance

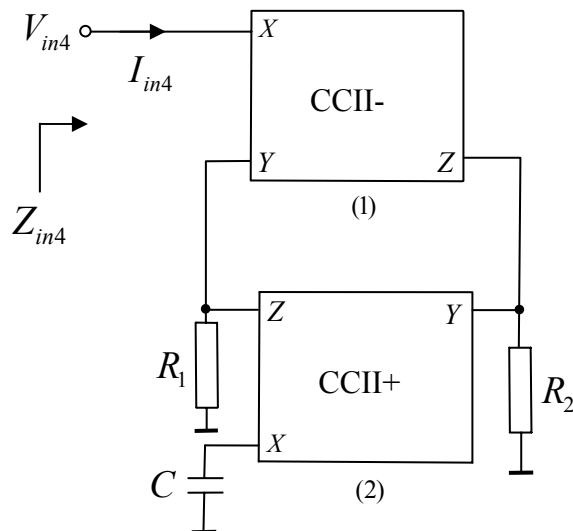


Figure 3.4. Alternative gyrator based inductor

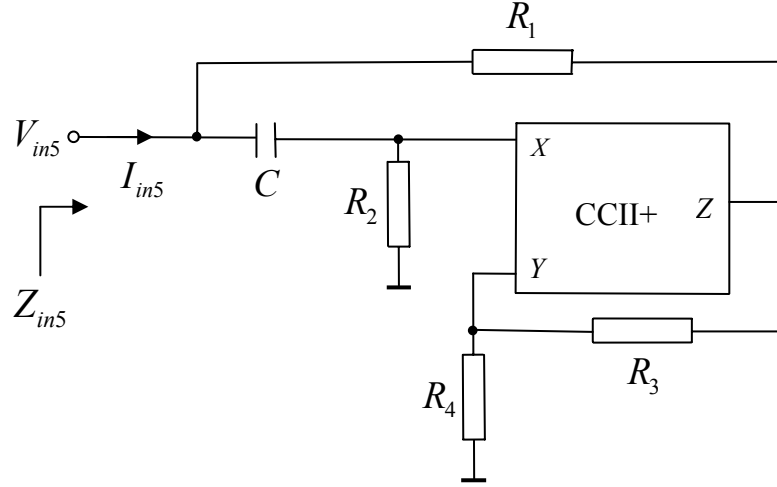


Figure 3.5. Soliman grounded inductor with $G_3 = G_4$ and $2G_1 = G_2 - G_3$

In the next two sections, we will illustrate the voltage-current non-ideal gain effects and current limitations for these circuits.

3.2. Non-Ideal Gain Effects

A simulated lossless grounded inductance with active element current gain $\alpha = 1$ and voltage gain $\beta = 1$ has an impedance $Z(s)$, and can be represented by

$$Z(s) = sL \quad (3.7)$$

However, a simulated inductance with non-ideal active element gains employing l current conveyors, c capacitors and r resistors can give in general driving point impedance $Z(s)$ as in the following form:

$$Z(s) = \frac{a_n s^n + a_{n-1} s^{n-1} + \dots + a_1 s + a_0}{b_m s^m + b_{m-1} s^{m-1} + \dots + b_1 s + b_0} \quad (3.8)$$

where $l \geq 1$, $c \geq 1$, $r \geq 2$, $\max\{n, m\} \leq c$, $n \geq 1$, $m \geq 0$. Under ideal conditions, the equation (3.8) reduces to $Z(s) = a_1 s / b_0$.

All coefficients in equation (3.8) except positive a_1 and b_0 can in general be either positive or negative depending on the effect of the non-ideal gains. Therefore, there is a possibility that the circuit with input impedance in equation (3.8) may be unstable [93].

If voltage and current gains α and β are taken into account, the impedances in equations (3.2) - (3.6) are found to be

For the presented first network in Figure 3.1,

$$Z_{in1}(s) = \frac{sCR_1R_2\alpha_1\alpha_2\beta_1\beta_2}{sC(R_1 + R_2)(1 - \alpha_2\beta_2) + 1} \equiv \frac{sa_1}{sb_1 + b_0} \quad (3.9)$$

where $b_1 \equiv C(R_1 + R_2)(1 - \alpha_2\beta_2)$ is an undesired term, and $Z_{in1}(s)$ represents a parallel inductor $L_1 = CR_1R_2\alpha_1\alpha_2\beta_1\beta_2$ and resistor $R_{eq1} = R_1R_2\alpha_1\alpha_2\beta_1\beta_2 / ((R_1 + R_2)(1 - \alpha_2\beta_2))$ combination. If $\alpha_2\beta_2 > 1$ is taken, the impedance in equation (3.9) has a stability problem.

For the presented second circuit in Figure 3.2,

$$Z_{in2}(s) = \frac{sCR_1R_2\alpha_1\alpha_2\beta_1\beta_2}{sC(R_1(1 + \alpha_2)(1 - \beta_2) + R_2(1 - \alpha_2\beta_2)) + 1 + \alpha_2} \equiv \frac{sa_1}{sb_1 + b_0} \quad (3.10)$$

In equation (3.10) given above, $b_1 \equiv C(R_1(1 + \alpha_2)(1 - \beta_2) + R_2(1 - \alpha_2\beta_2))$ is an unwanted term, and Z_{in2} behaves like a parallel connected resistance and inductance due to non-ideal gains with values $R_{eq2} = R_1R_2\alpha_1\alpha_2\beta_1\beta_2 / (R_1(1 + \alpha_2)(1 - \beta_2) + R_2(1 - \alpha_2\beta_2))$ and $L_2 = CR_1R_2\alpha_1\alpha_2\beta_1\beta_2 / (1 + \alpha_2)$, respectively. If $R_1(1 + \alpha_2)(1 - \beta_2) + R_2(1 - \alpha_2\beta_2) < 0$, the impedance in equation (3.10) would have a stability problem. For the Sedra-Smith gyrator in Figure 3.3,

$$Z_{in3}(s) = \frac{sCR_1R_2}{\alpha_1\alpha_2\beta_1\beta_2} \quad (3.11)$$

Hence, Z_{in3} is a lossless inductor, $L_3 = CR_1R_2 / (\alpha_1\alpha_2\beta_1\beta_2)$, and there is no resistive components.

For the circuit in Figure 3.4,

$$Z_{in4}(s) = sCR_1R_2\alpha_1\alpha_2\beta_1\beta_2 \quad (3.12)$$

Thus, Z_{in4} is a lossless inductor, $L_4 = CR_1R_2\alpha_1\alpha_2\beta_1\beta_2$, and there is no lossy component i.e. resistor.

For the Soliman's inductance,

$$Z_{in5}(s) = \frac{sC\alpha\beta + (2G_1 + G_3)(\alpha\beta - 1)}{sC\{G_3(\alpha\beta - 1) + G_1(-2 + \beta + \alpha(-2 + 3\beta))\} + 2G_1^2\alpha\beta + G_1G_3(\alpha\beta - 1)} \equiv \frac{sa_1 + a_0}{sb_1 + b_0} \quad (3.13)$$

As a result, $b_1 \equiv C\{G_3(\alpha\beta - 1) + G_1(-2 + \beta + \alpha(-2 + 3\beta))\}$, $a_0 \equiv (2G_1 + G_3)(\alpha\beta - 1)$ are undesired terms, and due to the coefficients a_0 (causes series resistance) and b_1 (causes parallel resistance), Z_{in5} behaves like a parallel and series connected one inductor and two resistors. For the conditions, $G_3(\alpha\beta - 1) + G_1(-2 + \beta + \alpha(-2 + 3\beta)) < 0$ and $2G_1^2\alpha\beta + G_1G_3(\alpha\beta - 1) > 0$ (the circuit will not be open circuit stable) and/or $(2G_1 + G_3)(\alpha\beta - 1) < 0$ (the circuit will not be short circuit stable), the impedance in equation (3.13) may have a stability problem. Moreover, if $2G_1^2\alpha\beta + G_1G_3(\alpha\beta - 1) < 0$, the value of the inductance becomes negative.

Since the impedances of both of the inductances remain lossless when α and β effects are considered, Sedra-Smith gyrator and the gyrator in Figure 3.4 are good in case of non-ideal gain effects.

The non-ideal driving point input impedances of the circuits under consideration as given in equations (3.2) – (3.6) as well as ideal counterparts as given in equations (3.9)–(3.13), respectively are repeated in Table 3.1 for easy comparison.

Note that in the above analysis α and β are assumed to be constants. In reality, they are frequency dependent quantities. For a more detailed analysis $\alpha(s)$ and $\beta(s)$ functions may be used. In this case, equation (3.8) is still valid but equations (3.9) – (3.13) will be

modified and a Hurwitz test should be applied for stability analysis. This however needs tedious analytical work and usually ignored. Spice simulations or experimental tests would be easier to perform.

Table 3.1. Ideal and non-ideal driving point impedances of the simulated inductances in Figures 3.1 – 3.5

# of the circuits	Ideal $Z_{in\ a}$	Non-ideal $Z_{in\ a}$
1	sCR_1R_2	$\frac{sCR_1R_2\alpha_1\alpha_2\beta_1\beta_2}{sC(R_1 + R_2)(1 - \alpha_2\beta_2) + 1}$
2	$\frac{sCR_1R_2}{2}$	$\frac{sCR_1R_2\alpha_1\alpha_2\beta_1\beta_2}{sC(R_1(1 + \alpha_2)(1 - \beta_2) + R_2(1 - \alpha_2\beta_2)) + 1 + \alpha_2}$
3	sCR_1R_2	$\frac{sCR_1R_2}{\alpha_1\alpha_2\beta_1\beta_2}$
4	sCR_1R_2	$sCR_1R_2\alpha_1\alpha_2\beta_1\beta_2$
5	$\frac{sCR_1^2}{2}$	$\frac{sC\alpha\beta + (2G_1 + G_3)(\alpha\beta - 1)}{sC\{G_3(\alpha\beta - 1) + G_1(-2 + \beta + \alpha(-2 + 3\beta))\} + 2G_1^2\alpha\beta + G_1G_3(\alpha\beta - 1)}$

3.3. Terminal Current Limitations

The AD844, integrated circuit [5] can be used as the CCII+ thus we select this component because it is a widely used commercially available versatile active device. It is a six terminal device that exhibits some limitations on its terminals like all other active devices. For example, the X-terminal current I_x limitation of AD844 in its data sheet is given as

$$-5\text{mA} \leq I_x \leq 5\text{mA} \quad (3.14)$$

A synthetic grounded inductance employing l CCIIIs, c capacitors and r resistors has l X-terminal currents, and these currents are expressed as

$$I_j = g_j(R_1, R_2, \dots, R_r, C_1, C_2, \dots, C_c, f, I_{in}) \quad (3.15)$$

where $l \geq 1$, $c \geq 1$, $r \geq 2$, and I_j represents the X-terminal current of the j th current conveyor ($j = 1, 2, \dots, l$).

Obviously, $|I_j| \leq 5 \text{ mA}$ is the condition for all j in order to keep the CCIIIs in their linear operating regions. Now, we evaluate the X-terminal currents of the current conveyors in Figures 3.1 – 3.5. Here, I_{ab} is the X-terminal current of the CCII, and the subscript a denotes the number of circuits ($a = 1, 2, 3, 4, 5$), the subscript b represents the number of current conveyors in each circuit ($b = 1, 2$), and $I_{in\ a}$ represents the value of the applied input current to the circuits.

The proposed first network has two CCII+s.

$$|I_{11}| = |I_{in1}| \leq 5 \text{ mA}, |I_{12}| = |I_{in1}(1 + j2\pi fC(R_1 + R_2))| \leq 5 \text{ mA} \quad (3.16)$$

Hence, we have two conditions for the terminal current limitation, $|I_{in1}| \leq 5 \text{ mA}$, $|I_{in1}| \leq 5 \text{ mA} / |1 + j2\pi fL_1(1/R_1 + 1/R_2)|$.

The presented second circuit employs two CCII+s.

$$|I_{21}| = |I_{in2}| \leq 5 \text{ mA}, |I_{22}| = \left| \frac{I_{in2}(1 + j2\pi fCR_2)}{2} \right| \leq 5 \text{ mA} \quad (3.17)$$

The conditions in this case are $|I_{in2}| \leq 5 \text{ mA}$, $|I_{in2}| \leq 10 \text{ mA} / |1 + j2\pi fL_2/R_1|$.

Similarly, the Sedra-Smith gyrator consists of two CCIIIs.

$$|I_{31}| = |I_{in3}| \leq 5 \text{ mA}, |I_{32}| = |j2\pi fCR_2I_{in3}| \leq 5 \text{ mA} \quad (3.18)$$

Hence, $|I_{in3}| \leq 5 \text{ mA}$, $|I_{in3}| \leq 5 \text{ mA} / (2\pi fL_3/R_1)$.

The gyrator in Figure 3.4 has also two CCIIIs.

$$|I_{41}| = |I_{in4}| \leq 5 \text{ mA}, |I_{42}| = |j2\pi fCR_2I_{in4}| \leq 5 \text{ mA} \quad (3.19)$$

As a result, $|I_{in4}| \leq 5 \text{ mA}$, $|I_{in4}| \leq 5 \text{ mA} / (2\pi f L_4 / R_1)$.

Finally, the inductance proposed in [15] employs only one CCII.

$$|I_5| = \left| I_{in5} \frac{2G_1^2 + G_1G_3 - j2\pi f C(G_1 + G_3)}{2G_1^2} \right| \leq 5 \text{ mA} \quad (3.20)$$

In this case, we have a single X-terminal current limiting condition for the inductor in Figure 3.5, $|I_{in5}| \leq 5 \text{ mA} / |1 + G_3 / (2G_1) - j2\pi f L_5 (G_1 + G_3)|$ where $G_1 = 1 / R_1$.

The maximum allowable inductor currents due to I_{a1} and I_{a2} are given in Table 3.2.

Table 3.2. The input current limitations of the simulated inductances in Figures 3.1 - 3.5
(AD844 is used instead of CCII+)

# of the circuits	Maximum allowable inductor currents	
	Due to I_{a1}	Due to I_{a2}
1	5mA	$5 \text{ mA} / 1 + j2\pi f L_1 (1/R_1 + 1/R_2) $
2	5mA	$10 \text{ mA} / 1 + j2\pi f L_2 / R_1 $
3	5mA	$5 \text{ mA} / (2\pi f L_3 / R_1)$
4	5mA	$5 \text{ mA} / (2\pi f L_4 / R_1)$
5	$5 \text{ mA} / 1 + G_3 / (2G_1) - j2\pi f L_5 (G_1 + G_3) $	

Obviously, the maximum allowable inductor current for each circuit is given by $I_{in a} \leq \min\{I_{a1}, I_{a2}\}$. We observe that the X-terminal currents are functions of the passive element values, inductor terminal current and frequency. To be able to make a comparison, inductor terminal current is written as a function of other variables where equivalent inductor value L is also introduced. This permits comparison of different circuits realizing equal inductance value, for example $L = 1 \text{ mH}$. Now, we evaluate the inductor current limitations for the DC or low frequency case and for the high frequency case separately.

The X-terminal current limitations of all current conveyors for each circuit, in the DC case, are obtained by putting $f = 0$ for $L_a = 1\text{mH}$ in the appropriate condition.

$$|I_{11}| = |I_{in1}| \leq 5\text{ mA}, |I_{12}| \cong |I_{in1}| \leq 5\text{ mA} \quad (3.21)$$

Thus, the acceptable inductor current range is given by $|I_{in1}| \leq \min\{I_{11}, I_{12}\} \leq 5\text{ mA}$.

For the second inductor,

$$|I_{21}| = |I_{in2}| \leq 5\text{ mA}, |I_{22}| \cong \left| \frac{I_{in2}}{2} \right| \leq 5\text{ mA} \quad (3.22)$$

Thus, the acceptable inductor current range is found to be $|I_{in2}| \leq \min\{I_{21}, I_{22}\} \leq 5\text{ mA}$.

For the third and fourth inductors,

$$|I_{31}| = |I_{in3}| \leq 5\text{ mA}, |I_{32}| \cong |0| \leq 5\text{ mA} \quad (3.23)$$

$$|I_{41}| = |I_{in4}| \leq 5\text{ mA}, |I_{42}| \cong |0| \leq 5\text{ mA} \quad (3.24)$$

As a result, the acceptable inductor current ranges for equations (3.23) and (3.24) are computed as $|I_{in3}| \leq \min\{I_{31}, I_{32}\} \leq 5\text{ mA}$, $|I_{in4}| \leq \min\{I_{41}, I_{42}\} \leq 5\text{ mA}$, respectively.

For the fifth inductor,

$$|I_5| \cong \left| I_{in5} \frac{2G_1^2 + G_1G_3}{2G_1^2} \right| \leq 5\text{ mA} \quad (3.25)$$

Therefore, $|I_{in5}| \leq 5\text{ mA} \cdot 2G_1^2 / (2G_1^2 + G_1G_3)$.

For the DC, and also approximately valid for the low frequency case, the last inductor has the worst property unless $G_3 \cong 0$ is taken.

Next, we evaluate the input current limitations for the high frequency case. From equations (3.21) – (3.25), the following input signals at high frequencies with $k = 5\text{ mA } R_1 / (2\pi f L_a)$

are obtained with $L_a = 1\text{mH}$ thus $k = 5[A/H]R_1/(2\pi f)$ and R_1 (it is assumed that R_1 has the same value for each inductor).

The proposed first network has the following current limitations with:

For the condition $2\pi f C(R_1 + R_2) \gg 1$, I_{12} given in equation (3.21) becomes as $|I_{12}| \cong |j2\pi f C(R_1 + R_2)I_{in1}| \leq 5\text{ mA}$. Thus, $|I_{in1}| \leq 5[A/H]/(2\pi f(1/R_1 + 1/R_2))$, and due to I_{11} , $|I_{in1}| \leq 5\text{ mA}$. Note that the limiting condition is the former one. Hence, for sufficiently high frequencies, the acceptable inductor current range is found to be $|I_{in1}| \leq kR_2/(R_1 + R_2)$.

Next, we calculate the current limitations for the second presented circuit,

For $2\pi f CR_2 \gg 1$, I_{x22} given in equation (3.22) becomes $|I_{22}| \cong |j2\pi f CR_2 I_{in2}/2| \leq 5\text{ mA}$. Thus, $|I_{in2}| \leq 10[A/H]/(2\pi f/R_1)$, and due to I_{21} , $|I_{in2}| \leq 5\text{ mA}$. Therefore, for sufficiently high frequencies, the acceptable inductor current range is the smaller of them or $|I_{in2}| \leq 2k$.

The Sedra-Smith gyrator has the following current limitations:

I_{32} given in equation (3.23) becomes as $|I_{32}| \cong |j2\pi f CR_2 I_{in3}| \leq 5\text{ mA}$. Therefore, $|I_{in3}| \leq 5[A/H]/(2\pi f/R_1)$, moreover due to I_{31} , $|I_{in3}| \leq 5\text{ mA}$. Therefore, for sufficiently high frequencies, the acceptable inductor current range is given as $|I_{in3}| \leq k$.

The current limitations for the circuit in Figure 3.4,

I_{42} given in equation (3.24) becomes $|I_{42}| \cong |j2\pi f CR_2 I_{in4}| \leq 5\text{ mA}$. As a result, $|I_{in4}| \leq 5[A/H]/(2\pi f/R_1)$, Moreover, due to I_{41} , $|I_{in4}| \leq 5\text{ mA}$. Thus, for sufficiently high frequencies, the acceptable inductor current range is given by $|I_{in4}| \leq k$.

Finally, Soliman's inductance has the following current limitation:

For $2\pi fC(G_1 + G_3) \gg 2G_1^2 + G_1G_3$ in equation (3.25), the input current of the fifth inductor $|I_5| \cong |j2\pi fC(G_1 + G_3)I_{in5}/(2G_1^2)| \leq 5 \text{ mA}$ can be represented as $|I_{in5}| \leq 5 [A/H]/(2\pi f(G_1 + G_3))$. Consequently, for sufficiently high frequencies, the acceptable simulated inductor current range in Figure 3.5 is calculated as $|I_{in5}| \leq 5/(2\pi f(G_1 + G_3)) = kR_3/(R_1 + R_3)$.

The maximum allowable inductor currents at high frequencies are tabulated in Table 3.3.

For the higher frequencies, only the second inductor possesses the best property.

It is observed that inductor simulators have a limit at low frequencies when applied input is a voltage source as discussed in chapter 2. Similarly, simulated inductors have a limit at high frequencies when applied input is a current source, which is generalized as follows:

The terminal currents of the conveyor I_i ($i = 1, 2, \dots, m$ and $m \geq 3$) can be expressed as

$$I_i = \phi_i(C, R_1, R_2, \dots, R_r, f)I_{in} = (C_i f + c_i)I_{in} \quad (3.26)$$

where C_i and c_i are respectively pure imaginary and real numbers. It is well-known that the current conveyor has a maximum allowable terminal current denoted by I_M as given in chapter 2. Hence, we can write $|I_i| \leq I_{Mi}$, where I_{Mi} is the maximum allowable current for the i -th terminal.

As a result, the useful frequency range restricted by I_M as explained above in great depth is given by

$$f \leq f_{HC} \quad (3.27)$$

where

$$f_{\text{HC}} = \min \left\{ \frac{\sqrt{\left(\frac{I_{\text{Mi}}}{I_{\text{in}}} \right)^2 - c_i^2}}{|C_i|} \right\} \quad (3.28)$$

Here, f_{HC} is called the high frequency limit of the simulator due to the terminal current limitation of the conveyor. Also, if I_{Mi} increases without increasing I_{in} , C_i and c_i are reduced and f_{HC} increases considerably.

Similarly, the terminal voltages of the conveyor V_j ($j = 1, 2, \dots, n$ and $n \geq 3$) can be expressed as

$$V_j = \Phi_j(C, R_1, R_2, \dots, R_r, f)I_{\text{in}} = (D_j f + d_j)I_{\text{in}} \quad (3.29)$$

where D_j and d_j are pure imaginary and real numbers, respectively. It is well-known that j -th terminal of the current conveyors has a rated voltage V_{rj} as defined in chapter 2. As a result, we can write $|V_j| \leq V_{rj}$ where V_{rj} is the rated voltage of the j -th terminal of the active devices.

The useful frequency range restricted by V_r is given as

$$f \leq f_{\text{HV}} \quad (3.30)$$

where

$$f_{\text{HV}} = \min \left\{ \frac{\sqrt{\left(\frac{V_{rj}}{I_{\text{in}}} \right)^2 - d_j^2}}{|D_j|} \right\} \quad (3.31)$$

Here, f_{HV} is called the high frequency limit of the simulator due to the terminal voltage limitation of the conveyor. Also, if V_{ri} increases, D_i and d_i are reduced and f_{HV} increases considerably.

Finally, combining (3.27) and (3.30) yields,

$$f \leq \min\{f_{HC}, f_{HV}\} \quad (3.32)$$

On the other hand, in order to show the effect of the non-ideal gains of the current conveyors on the impedance of the circuits in Figures 3.1 - 3.5, two arbitrary sets of α and β values, $\alpha = 0.95$, $\beta = 1.05$ and $\alpha = 1.05$, $\beta = 0.95$ are selected and the magnitude of the impedance function is evaluated. The magnitude of the impedances for the first set will be given in this section. In order to calculate and plot the impedances $L_a = 1\text{mH}$ is used and other passive element values are selected to obtain 1mH inductance value.

The magnitudes of the impedances for $\alpha = 0.95$ and $\beta = 1.05$ in equations (3.9) – (3.13) can be rewritten as follows:

Table 3.3. At high frequencies, the input current limitations of the simulated inductances depicted in Figures 3.1-3.5 with $k = (5\text{mA}) R_1 / (2\pi f L_a)$ and $L_a = 1\text{mH}$

# of the circuits	Maximum Allowable Inductor Currents $k = 5 R_1 / (2\pi f)$ (amperes)
1	$k R_2 / (R_1 + R_2)$
2	$2k$
3	k
4	k
5	$k R_3 / (R_1 + R_3)$

If the magnitude of the equation (3.9) is taken with $R_1 = 1\text{k}\Omega$, $R_2 = 1\text{k}\Omega$, $R_3 = 0.5\text{k}\Omega$ and $C = 1\text{nF}$, the following equation is obtained:

$$|Z_{in1}(j\omega)| = \frac{796005\omega}{\sqrt{64 \times 10^{16} + 16\omega^2}} \quad (3.33)$$

The magnitude of equation (3.10) with $R_1 = 1\text{k}\Omega$ and $R_3 = 1\text{k}\Omega$, $R_2 = 2\text{k}\Omega$ and $C = 1\text{nF}$ is found to be

$$|Z_{in2}(j\omega)| = \frac{796005\omega}{\sqrt{60.84 \times 10^{16} + 5929\omega^2}} \quad (3.34)$$

The magnitude of equation (3.11) with $R_1 = 1\text{k}\Omega$, $R_2 = 1\text{k}\Omega$ and $C = 1\text{nF}$ is given by

$$|Z_{in3}(j\omega)| = 1.005 \times 10^{-3} \omega \quad (3.35)$$

The magnitude of equation (3.12) with $R_1 = 1\text{k}\Omega$, $R_2 = 1\text{k}\Omega$ and $C = 1\text{nF}$ is given as

$$|Z_{in4}(j\omega)| = 0.995 \times 10^{-3} \omega \quad (3.36)$$

The magnitude of equation (3.13) with $R_1 = R_3 = R_4 = 1\text{k}\Omega$, $R_2 = 0.333\text{k}\Omega$ and $C = 2\text{nF}$ is calculated as

$$|Z_{in5}(j\omega)| = \sqrt{\frac{3.515 \times 10^{16} + 2.4875 \times 10^9 \omega^2}{24.81 \times 10^{14} + 49\omega^2}} \quad (3.37)$$

Note that the additional terms appear in equations (3.9), (3.10) and (3.13) and in equations (3.33), (3.34) and (3.37) so that some deviations from the linear dependence of the magnitude of $Z_{in a}$ to the frequency are obvious.

The signals that the simulated inductors handle are assumed to be sinusoidal signals. Time domain transient responses or responses to different signal waveforms at the input terminal of the inductor are not considered. A rapidly changing inductor current signal may force large inductor voltages which are clipped due to limited supply voltage. However, a wide application area for inductors is analog filter design where the above analysis is useful.

The magnitude impedance functions in equations (3.33) – (3.37) are plotted with MATLAB in Figure 3.6. One can see that, all of the magnitudes of the impedances in Figure 3.6 have approximately the same characteristics up to 1 MHz.

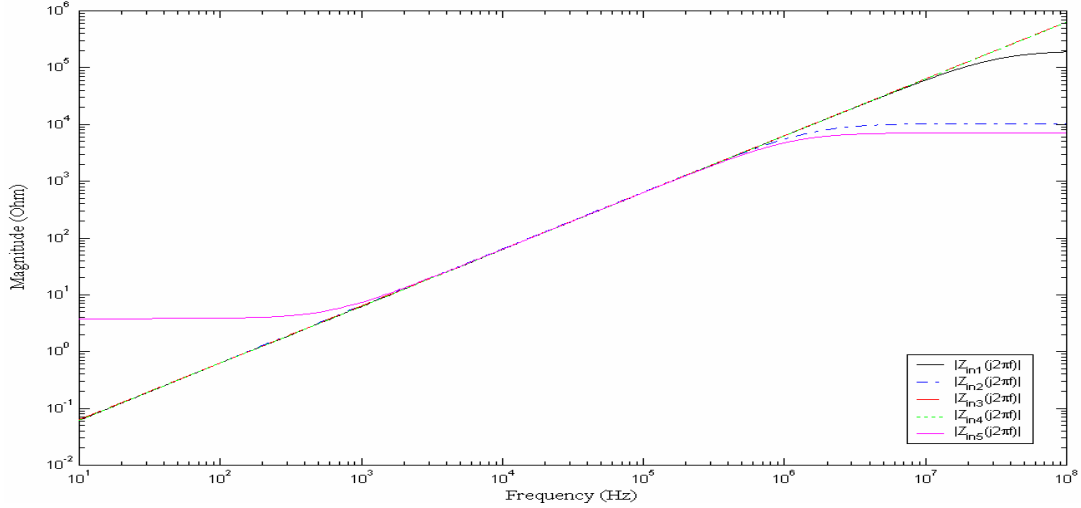


Figure 3.6. Magnitude of the impedances of the circuits in Figures 3.1 - 3.5 for $\alpha = 0.95$ and $\beta = 1.05$

Similarly, the impedances in equations (3.9)-(3.13) for $\alpha = 1.05$ and $\beta = 0.95$ are plotted with MATLAB in Figure 3.7. It is observed that all of the magnitudes of the impedances in Figure 3.7 have approximately the same characteristics up to 1 MHz.

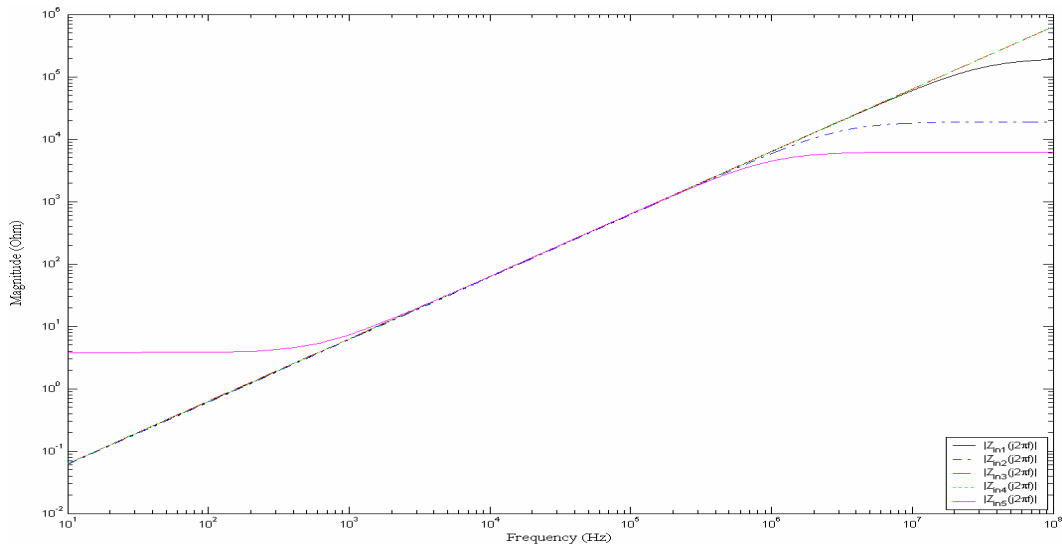


Figure 3.7. Magnitude of the impedances of the circuits in Figures 3.1 - 3.5 for $\alpha = 1.05$ and $\beta = 0.95$

To illustrate the functionality of the two novel presented circuits, they are simulated with two AD844s that have DC power supply voltages equal to $\pm 15\text{V}$ thus $R_1 = 1\text{k}\Omega$, $R_2 = 1\text{k}\Omega$, $R_3 = 0.5\text{k}\Omega$ and $C = 1\text{nF}$ are taken for the first inductance, and $R_1 = 1\text{k}\Omega$, $R_2 = 2\text{k}\Omega$, $R_3 = 1\text{k}\Omega$ and $C = 1\text{nF}$ are taken for the second inductance to obtain $L = 1\text{mH}$. Two identical triangular currents I_{in} with 2mA peak to peak value at $f = 100\text{ kHz}$ are applied to each of the presented inductance and an ideal inductor. It is expected to obtain square wave output voltages V_{out} as shown in Figures 3.8 and 3.9.

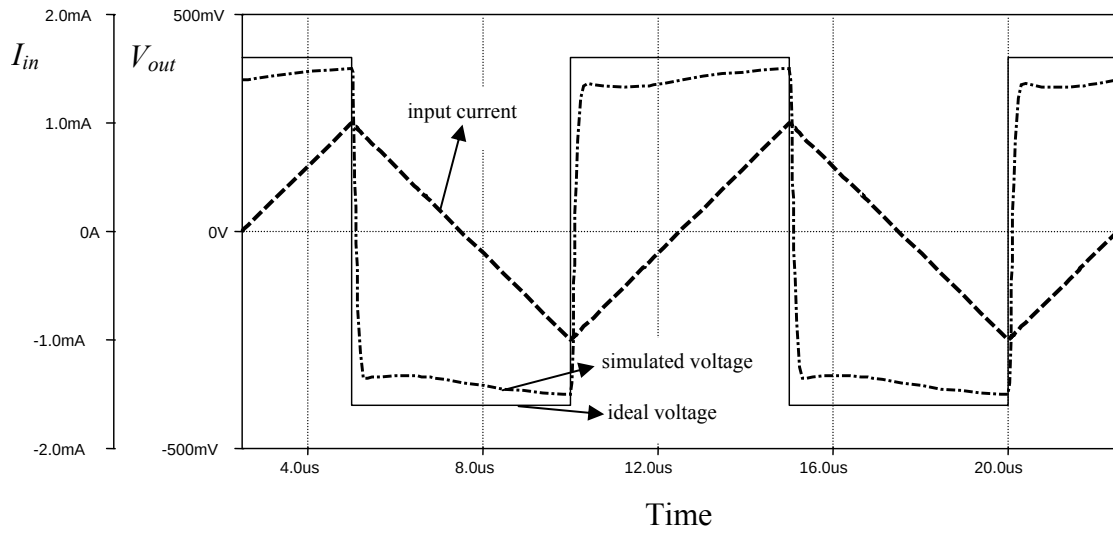


Figure 3.8. Time domain performance of the first proposed inductor depicted in Figure 3.1

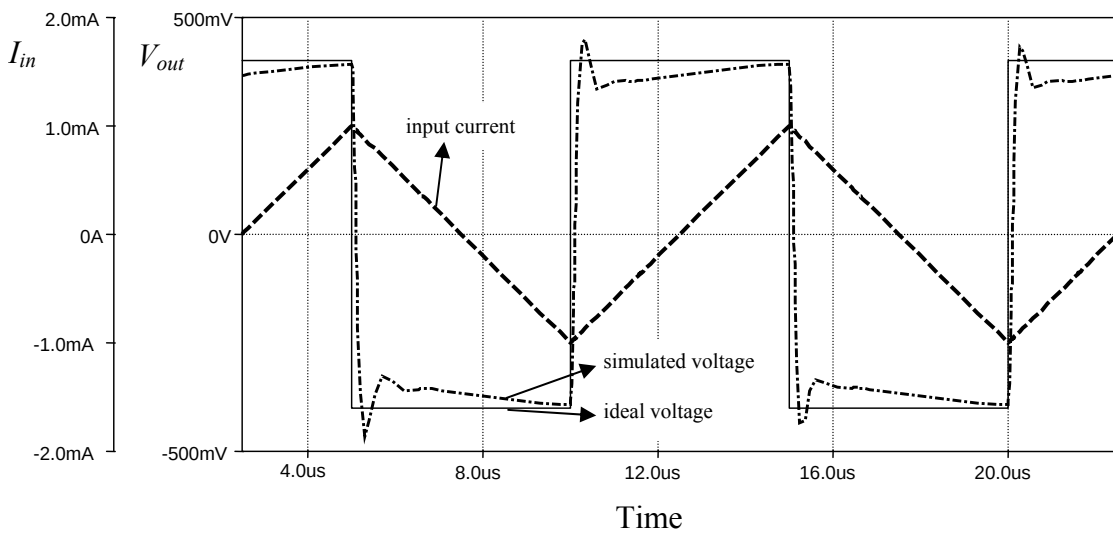


Figure 3.9. Time domain performance of the second presented inductor in Figure 3.2

Time domain performances of the proposed inductances in Figures 3.1 and 3.2 are quite close to the ideal inductor as observed from Figures 3.8 and 3.9.

In this chapter, we have discussed the effects of the non-ideal active element gains of the five inductor simulators, two of which are novel, ignoring their pole frequencies which are taken as infinity. It is observed that some of the inductor simulators have stability problems stemmed from the non-ideal gain effects. It is well known that the impedances of the inductors change due to parasitic impedances and non-ideal gain effects thus they should be considered together for simulated inductor. Nonetheless, we only considered the non-ideal gain effects on the impedances of the simulated inductors to test their stability by ignoring parasitic impedance effects because of simplicity. Also, signal limitations of the five inductor simulators stemmed from maximum allowable terminal currents of the CCIIIs are investigated. It is observed that simulated inductors have a limit at high frequencies when the applied input is a current source. Fortunately, one of the five inductor simulators analyzed in this chapter has good properties when compared to others.

In the next section, novel grounded inductor simulators and analog filters using a single new active device called modified current feedback operational amplifier (MCFOA) is introduced and many experimental and simulation results are shown. Also, layout and noise model of the MCFOA are given. Signal limitations of the analog filters are examined shortly in the next section. A more detailed study will be given in chapter 5.

3.4 Grounded Inductors with Reduced Non-ideal Gain Effects

Firstly, in this section, we present a new four port MCFOA, which is a useful block in analog signal processing. Also, we propose two new circuits for realizing inductor, capacitor multiplier, and FDNR based on using single MCFOA. Contrary to the previously reported circuits [3] and [11]-[22], the proposed circuits use a minimum number of active and passive components. The MCFOA first was reported in [96] as a composite current conveyor by using two second-generation current conveyors (CCIIIs). However, no realization for the reported block has been introduced so far. On the other hand, signal limitations of the current-mode and voltage-mode filters employing a single MCFOA based inductor simulator are given in this section. It is observed that one of the grounded

simulators is suitable for the inductor simulator. The other one is a Frequency Dependent Negative Resistor (FDNR) simulator and it operates at only high frequencies. On the other hand, non-ideal gain effects of the proposed grounded simulators can be completely reduced by performing six different connection of two simulators in which one simulator is connected by replacing one of the three admittances of the other simulator or identical simulator.

3.4.1. Proposed MCFOA

The defining matrix equation of the MCFOA given in Figure 3.10 can be given as follows:

$$\begin{bmatrix} I_Z \\ I_Y \\ V_X \\ V_W \end{bmatrix} = \begin{bmatrix} \alpha_1 & 0 & 0 & 0 \\ 0 & -\alpha_2 & 0 & 0 \\ 0 & 0 & \beta_1 & 0 \\ 0 & 0 & 0 & \beta_2 \end{bmatrix} \begin{bmatrix} I_X \\ I_W \\ V_Y \\ V_Z \end{bmatrix} \quad (3.38)$$

The current convention is such that all current directions are into the MCFOA. The non-ideal current gains α_j ($j = 1, 2$) and voltage gains β_j are ideally equal to unity.

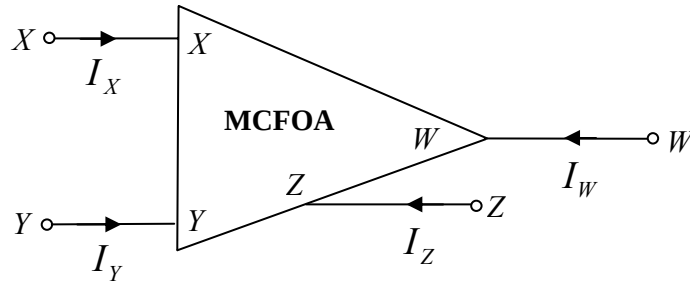


Figure 3.10. Symbolic representation of the MCFOA

As can be seen from equation (3.38), the MCFOA is different from the current feedback operational amplifier (CFOA) [20] and [21] since the W-terminal current of the MCFOA is copied to the Y terminal in opposite direction. However, it is well known that Y terminal current of the conventional CFOA is zero. The proposed CMOS implementation for the MCFOA is shown in Figure 3.11.

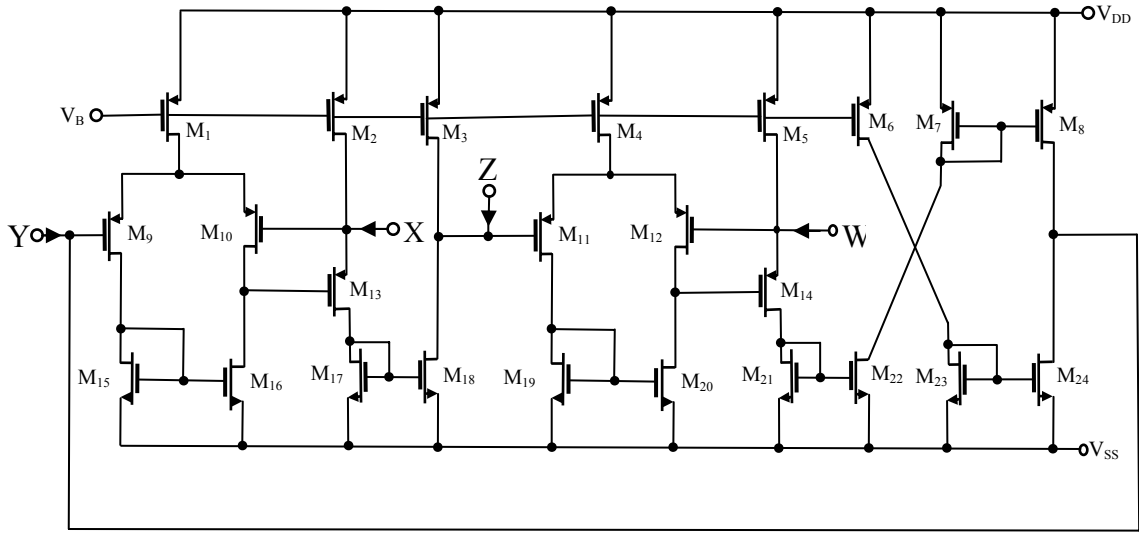


Figure 3.11. Developed internal structure of the MCFOA using CMOS transistors

Assuming that the output resistances of the transistors M_9 , M_{10} , M_{15} and M_{16} of the MCFOA in Figure 3.11 are equal to r_a and similarly, the output resistances of the transistors M_{11} , M_{12} , M_{19} and M_{20} of the MCFOA are equal to r_b thus the resistances seen at terminals Y, Z, X and W are respectively calculated as

$$R_y = \frac{r_{o8}r_{o24}}{r_{o8} + r_{o24}} \quad (3.39)$$

$$R_z = \frac{r_{o3}r_{o18}}{r_{o3} + r_{o18}} \quad (3.40)$$

$$R_x = \left(\frac{r_{o13} + \frac{r_{o17}}{1 + g_{m17}r_{o17}}}{1 + r_{o13}g_{m13} \left(1 + \frac{r_a}{2} g_{m10} \right)} \right) \parallel r_{o2} \cong \frac{2}{g_{m10}g_{m13}r_a} \quad (3.41)$$

$$R_w = \left(\frac{r_{o14} + \frac{r_{o21}}{1 + g_{m21}r_{o21}}}{1 + r_{o14}g_{m14} \left(1 + \frac{r_b}{2} g_{m12} \right)} \right) \parallel r_{o5} \cong \frac{2}{g_{m12}g_{m14}r_b} \quad (3.42)$$

where r_{oi} and g_{mi} are the output resistances and transconductances of the i -th CMOS transistor, respectively.

The noise equivalent circuit of the MCFOA whose X and Y terminals are input terminals and other terminals are output terminals, useful for the derivation of the noise model of any conveyors, is given in Figure 3.12.

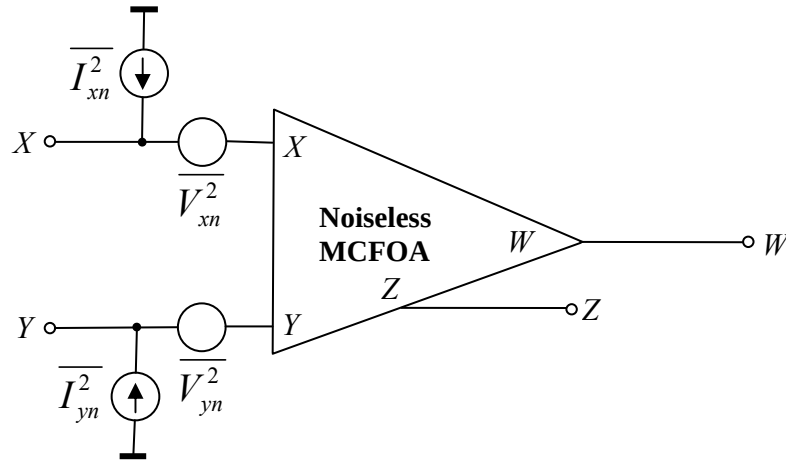


Figure 3.12. Equivalent noise model of the MCFOA

The power spectral densities of the model components (including only dominant terms) are

$$\overline{I_{nx}^2} = 4KT\gamma(g_{m2} + g_{m13}) \quad (3.43)$$

$$\overline{V_{nx}^2} = 4KT\gamma\left(\frac{g_{m10} + g_{m16}}{g_{m10}^2}\right) \quad (3.44)$$

$$\overline{I_{ny}^2} = 4KT\gamma(g_{m8} + g_{m24}) \quad (3.45)$$

$$\overline{V_{ny}^2} = 4KT\gamma\left(\frac{g_{m9} + g_{m15}}{g_{m9}^2}\right) \quad (3.46)$$

Here, $K = 1.38 \cdot 10^{-23}$ J/K is the Boltzman constant, T is the temperature in Kelvin and γ is a coefficient that equals to about 2.5 in some $0.25 \mu\text{m}$ MOS devices.

3.4.2. Simulator Circuits Using the Proposed MCFOA

The proposed circuits using single MCFOA are shown in Figures 3.13 and 3.14.

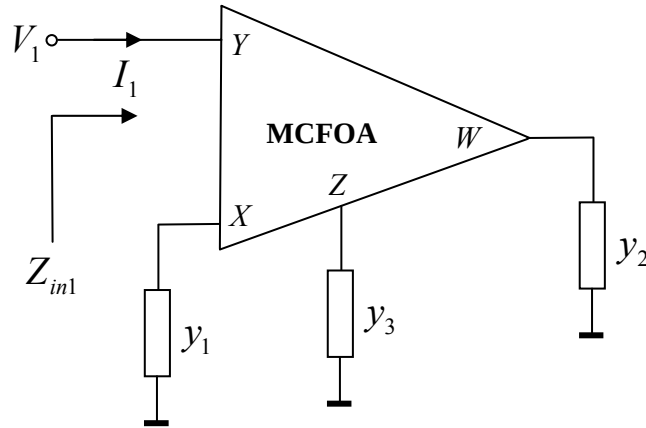


Figure 3.13. Proposed first circuit (Y-terminal input)

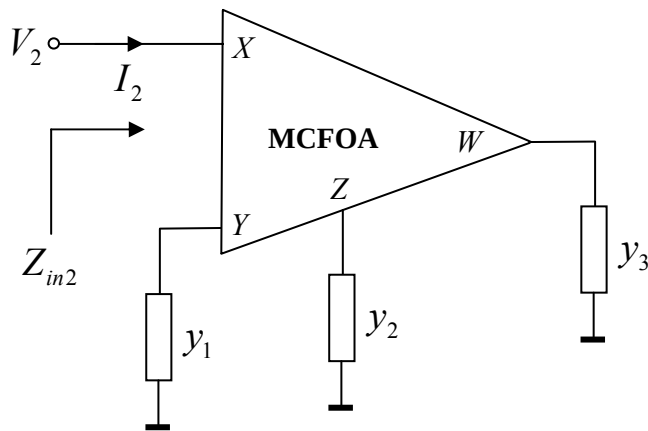


Figure 3.14. Proposed second circuit (X-terminal input)

Straightforward analysis of these networks gives the following input admittances:

$$Y_{in1} = \frac{1}{Z_{in1}} = \frac{I_1}{V_1} = \frac{y_1 y_2}{y_3} \alpha_1 \alpha_2 \beta_1 \beta_2 \quad (3.47)$$

and

$$Y_{in2} = \frac{1}{Z_{in2}} = \frac{I_2}{V_2} = \frac{y_1 y_2}{y_3} \frac{1}{\alpha_1 \alpha_2 \beta_1 \beta_2} \quad (3.48)$$

for the circuits of Figures 3.13 and 3.14, respectively.

It is obvious that using the two simulators in Figures 3.13 and 3.14 employing identical MCFOA, six different inductor simulators without non-ideal gain effects can be obtained.

- i)** the second simulator Y_{in2} is connected instead of y_1 of the first simulator Y_{in1} .
- ii)** the second simulator is connected instead of y_2 of the first simulator.
- iii)** identical simulator is connected instead of y_3 of the first simulator.
- iv)** the first simulator Y_{in1} is connected instead of y_1 of the second simulator Y_{in2} .
- v)** the first simulator Y_{in1} is connected instead of y_2 of the second simulator.
- vi)** identical simulator is connected instead of y_3 of the second simulator.

It is seen from equations (3.47) and (3.48) that both circuits have the same input admittances in ideal case ($\alpha_1 = \alpha_2 = \beta_1 = \beta_2 = 1$). By selecting various passive components for y_1 , y_2 and y_3 in the proposed circuit, one can obtain an inductor simulator, capacitor multiplier and an FDNR as follows:

- a)** If $y_1 = G_1$, $y_2 = G_2$ and $y_3 = sC_3$ are chosen, an inductor simulator is obtained as

$$Z_{in1} = Z_{in2} = sL_{eq} = \frac{sC_3}{G_1 G_2} \quad (3.49)$$

where $L_{eq} = C_3 / (G_1 G_2)$.

- b)** If $y_1 = sC_1$, $y_2 = G_2$ and $y_3 = G_3$ are chosen, a capacitance multiplier is realized by

$$Z_{in1} = Z_{in2} = \frac{1}{sC_{eq}} = \frac{G_3}{sC_1 G_2} \quad (3.50)$$

Here, $C_{eq} = C_1 G_2 / G_3$.

- c)** If $y_1 = sC_1$, $y_2 = sC_2$ and $y_3 = G_3$ are chosen, an FDNR is implemented as follows:

$$Z_{in1} = Z_{in2} = \frac{1}{s^2 D_{eq}} = \frac{G_3}{s^2 C_1 C_2} \quad (3.51)$$

where $D_{eq} = C_1 C_2 / G_3$.

If only resistors and no capacitors for a circuit are connected in series to the X and W terminals of the MCFOA, this circuit can be operated at high frequencies [82]. Hence, the first proposed circuit (Z_{in1}) can work at higher frequencies for the inductance simulator choice. Also, the second circuit (Z_{in2}) can be used at higher frequencies for the FDNR selection.

Considering the parasitic elements of the MCFOA (R_x and R_w in series at terminals X and W, $R_y = 1/G_y$ and C_y in parallel at terminal Y, $R_z = 1/G_z$ and C_z in parallel at terminal Z), the input impedances of the circuits in Figures 3.13 and 3.14 can be found as:

$$Z_{in1} = \frac{V_1}{I_1} = \left(\frac{1}{G_y + sC_y} \right) // \left(\frac{y_3 + sC_z + G_z}{\left(\frac{y_1}{1 + R_x y_1} \right) \left(\frac{y_2}{1 + R_w y_2} \right)} \right) \quad (3.52)$$

$$Z_{in2} = \frac{V_2}{I_2} = R_x + \frac{\frac{y_3}{1 + R_w y_4}}{(y_1 + sC_y + G_y)(y_2 + sC_z + G_z)} \quad (3.53)$$

If $y_1 = G_1$, $y_2 = G_2$ and $y_3 = sC_3$ are chosen, the impedances in equations (3.52) and (3.53) behave like inductors with limits at low and high frequencies because of parasitic impedances. For example, the impedance in equation (3.52) has a limit at low frequencies due to G_z . Also, it has a limit at very high frequencies stemmed from $G_y + sC_y$. Similarly, the impedance in equation (3.53) has a limit at low frequencies due to R_x and a limit at high frequencies stemmed from R_w . Briefly, the impedance in equation (3.52) can be operated at higher frequencies than the impedance in equation (3.53) for the inductor simulator choice.

In the next section, voltage-mode and current-mode multifunction filters using a single MCFOA are going to be proposed. Also, signal limitations of the analog filters are going to be discussed briefly.

3.4.3. Multifunction Filters Using the Proposed MCFOA

The proposed MCFOA can be used easily to realize voltage-mode and current-mode multifunction filters.

3.4.3.1. Voltage-Mode Filter

A voltage-mode filter using only one MCFOA can be realized as shown in Figure 3.15. Routine analysis of the voltage-mode single input three outputs filter depicted in Figure 3.15, the following voltage-mode filter TFs can be obtained simultaneously:

$$\frac{V_{BP}}{V_{in}} = \frac{R_3}{R_1} \frac{s \frac{\omega_0}{Q}}{D_1(s)} \quad (3.54)$$

$$\frac{V_{HP}}{V_{in}} = \frac{s^2}{D_1(s)} \quad (3.55)$$

$$\frac{V_{NF}}{V_{in}} = \frac{s^2 + \omega_0^2}{D_1(s)} \quad (3.56)$$

where

$$D_1(s) = s^2 + s \frac{\omega_0}{Q} + \omega_0^2 \quad (3.57)$$

The angular resonance frequency (ω_0) and quality factor (Q) of the filter are found as

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_2 R_3}} \quad (3.58)$$

$$Q = \frac{1}{R_1} \sqrt{\frac{C_2 R_2 R_3}{C_1}} \quad (3.59)$$

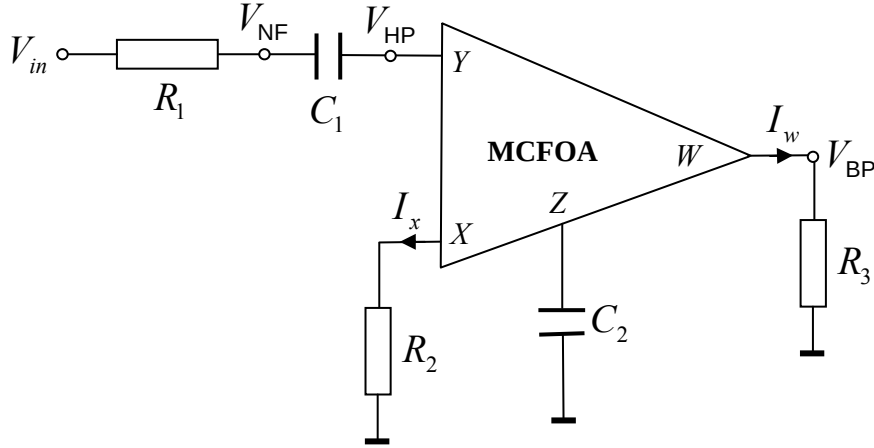


Figure 3.15. Developed voltage-mode filter

It is observed from equation (3.57) that the parameter ω_o can be adjusted by changing R_2 and R_3 . Note that the resistors R_2 and R_3 can be replaced by voltage-controlled grounded resistors [90] employing CMOS transistors. After adjusting ω_o , the parameter Q of the filter can be controlled via R_1 .

3.4.3.2. Current-Mode Filter

A current-mode filter can also be realized as depicted in Figure 3.16.

From the straightforward analysis of the current-mode single input three outputs filter depicted in Figure 3.16, the following current-mode filter TFs can be obtained simultaneously:

$$\frac{I_{LP}}{I_{in}} = \frac{\omega_o^2}{D_2(s)} \quad (3.60)$$

$$\frac{I_{BP}}{I_{in}} = \frac{s \frac{\omega_0}{Q}}{D_2(s)} \quad (3.61)$$

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{D_2(s)} \quad (3.62)$$

$$D_2(s) = s^2 + s \frac{\omega_0}{Q} + \omega_0^2 \quad (3.63)$$

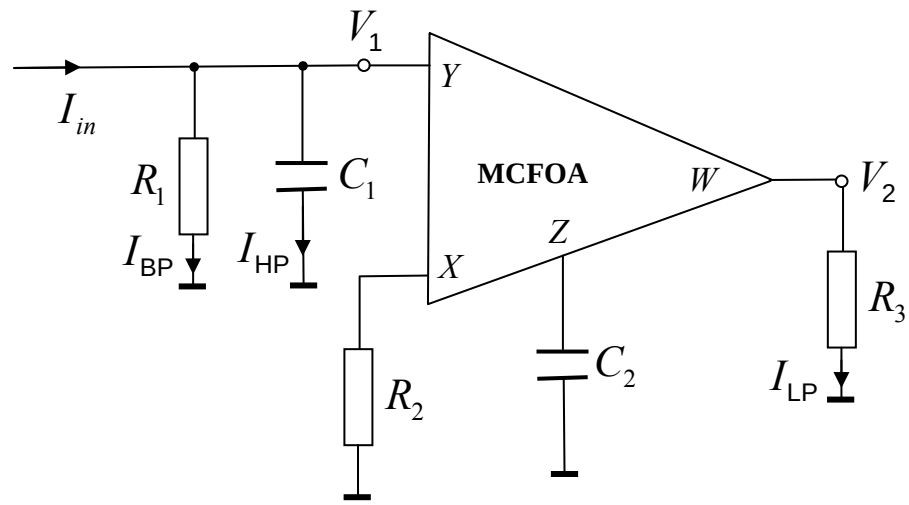


Figure 3.16. Proposed current-mode filter

The parameters ω_0 and Q for equations (3.60)-(3.63) are found to be as follows:

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_2 R_3}} \quad (3.64)$$

$$Q = R_1 \sqrt{\frac{C_1}{C_2 R_2 R_3}} \quad (3.65)$$

The filters in Figures 3.15 and 3.16 like all other filters in the literature have signal limitations due to restricted terminal voltages of the MCFOA and maximum allowable input currents of the MCFOA. In general, either current-mode or voltage-mode filters can be represented in the following filter TFs:

a) *Low-pass filter TF,*

$$H_{\text{LP}}(s) = K_{\text{LP}} \frac{\omega_0^2}{D(s)} \quad (3.66)$$

b) *Band-pass filter TF,*

$$H_{\text{BP}}(s) = K_{\text{BP}} \frac{s \frac{\omega_0}{Q}}{D(s)} \quad (3.67)$$

c) *High-pass filter TF,*

$$H_{\text{HP}}(s) = K_{\text{HP}} \frac{s^2}{D(s)} \quad (3.68)$$

d) *Notch filter TF,*

$$H_{\text{NF}}(s) = K_{\text{NF}} \frac{s^2 + \omega_0^2}{D(s)} \quad (3.69)$$

e) *All-pass filter TF,*

$$H_{\text{AP}}(s) = K_{\text{AP}} \frac{s^2 - s \frac{\omega_0}{Q} + \omega_0^2}{D(s)} \quad (3.70)$$

where $D(s)$ is given as

$$D(s) = s^2 + s \frac{\omega_0}{Q} + \omega_0^2 \quad (3.71)$$

The TFs in equations (3.66)-(3.70) at $\omega = \omega_0$ and replacing $j\omega$ by s convert

$$H_{\text{LP}} = -jK_{\text{LP}}Q \quad (3.72)$$

$$H_{\text{BP}} = K_{\text{BP}} \quad (3.73)$$

$$H_{\text{HP}} = jK_{\text{HP}}Q \quad (3.74)$$

$$H_{NF} = 0 \quad (3.75)$$

$$H_{AP} = K_{AP} \quad (3.76)$$

It is seen from equations (3.72) and (3.74), H_{LP} and H_{HP} at $\omega = \omega_0$ are proportional to Q . Therefore, Q may result in a limitation thus it cannot be chosen arbitrarily large. Otherwise, terminal voltages of the filter and/or terminal currents of the active device exceed the limit and distortion occurs.

The actual limitations depend on the specific MCFOA and circuit topology. However, for simplicity we assume that maximum terminal voltages of the X, Y, Z and W are equal to V_r called rated voltage. V_r can be expressed as $V_r = \min\{|V_{r-}| \leq |V_{SS}|, V_{r+} \leq V_{DD}\}$ in which V_{SS} and V_{DD} are negative and positive DC power supply voltages of the circuit, respectively. Also, it is assumed that the MCFOA can operate without significant distortion.

It is important to note that all the circuits using active devices such as CFOAs and current conveyors suffer from parasitic and non-ideal gain effects, stability problems and signal limitations. The signal limitations of the voltage-mode filter in Figure 3.15 can be expressed as

$$\max\{|V_{HP}|, |V_{BP}|\} \leq V_r \quad (3.77)$$

$$|I_x| = \left| \frac{V_{HP}}{R_2} \right| \leq I_{x,\max} \quad (3.78)$$

$$|I_w| = \left| \frac{V_{BP}}{R_3} \right| \leq I_{w,\max} \quad (3.79)$$

where $I_{x,\max}$ and $I_{w,\max}$ are maximum allowable terminal current of the X and W terminals of the MCFOA, respectively.

Maximum value of V_{BP} and V_{HP} occur at ω_0 for high Q and they can be calculated as

$$\frac{V_{BP}}{V_{in}} = \frac{R_3}{R_1} \quad (3.80)$$

$$\frac{V_{HP}}{V_{in}} = jQ \quad (3.81)$$

Signal limitations of the current-mode filter in Figure 3.16 are given as

$$\max\{|V_1|, |V_2|\} \leq V_r \quad (3.82)$$

$$|I_x| = \left| \frac{V_1}{R_2} \right| \leq I_{x,max} \quad (3.83)$$

$$|I_w| = \left| \frac{V_2}{R_3} \right| \leq I_{w,max} \quad (3.84)$$

Similarly, maximum values of V_1 and V_2 at ω_0 for high Q are calculated as

$$V_1 = R_1 I_{in} \quad (3.85)$$

$$V_2 = QR_3 I_{in} \quad (3.86)$$

It is observed from equations (3.82) to (3.86) that signal limitations of the current-mode and voltage-mode filters employing these active devices mainly depend on the passive element values and power supply voltages of the circuit besides maximum allowable terminal currents of the active devices.

The results obtained in this section can be generalized to other active devices and circuits.

3.4.4. Simulation Results

Simulations based on $0.25\mu m$ TSMC CMOS technology with power supply voltages $V_{DD} = -V_{SS} = 1.5\text{ V}$ and $V_B = 0.763\text{ V}$ are performed. The parasitic elements of the proposed MCFOA using SPICE program are obtained as $R_x = R_w = 0.514\text{ k}\Omega$, $R_y = 84.47\text{ k}\Omega$, $R_z = 97.763\text{ k}\Omega$, $C_y = 4.44\text{ fF}$ and $C_z = 2.69\text{ fF}$ but R_x and R_w can be reduced by increasing the aspect ratios of the M_{13} and M_{14} of the MCFOA in Figure 3.11, respectively. If we increase the aspect ratio of the M_{13} ten times, R_x becomes 97Ω . The internal structure of the MCFOA using CMOS transistors as declared before is depicted in

Figure 3.11. The dimensions of the MOS transistors used in the construction of the MCFOA in Figure 3.11 are given in Table 3.4.

Table 3.4. Dimensions of the CMOS transistors used in the MCFOA in Figure 3.11

PMOS Transistors	$W(\mu m) / L(\mu m)$
M ₁ , M ₄ and M ₉ , M ₁₀ , M ₁₁ and M ₁₂	1.0/0.25
M ₂ , M ₃ , M ₅ , M ₆ , M ₇ and M ₈	2.0/0.25
M ₁₃ and M ₁₄	4.0/0.25
NMOS Transistors	$W(\mu m) / L(\mu m)$
M ₁₅ , M ₁₆ , M ₁₇ , M ₁₈ , M ₁₉ , M ₂₀ , M ₂₁ , M ₂₂ , M ₂₃ and M ₂₄	0.5/0.25

The voltage gains V_x/V_y and V_w/V_z and current gains I_z/I_x and I_y/I_w are depicted in Figures 3.17 and 3.18, respectively. The passive elements $R_1 + R_x = R_2 + R_w = 1k\Omega$ and $C_3 = 0.1nF$ are selected for the circuit in Figure 3.13 to obtain $L_{eq1} = 0.1mH$.

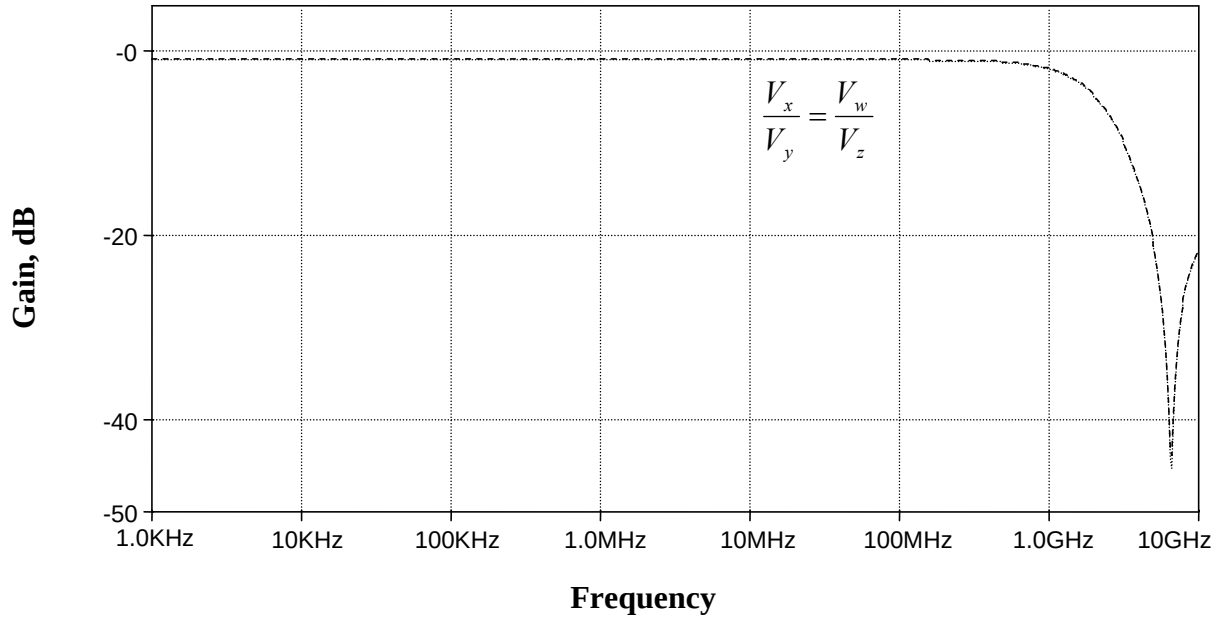


Figure 3.17. Frequency response of the voltage gains

Also, the layout of the MCFOA in Figure 3.11 based on $0.25\mu\text{m}$ CMOS technology using MAGIC program is shown in Figure 3.19. The area of the layout in Figure 3.19 is approximately $26.76\mu\text{m}^2$.

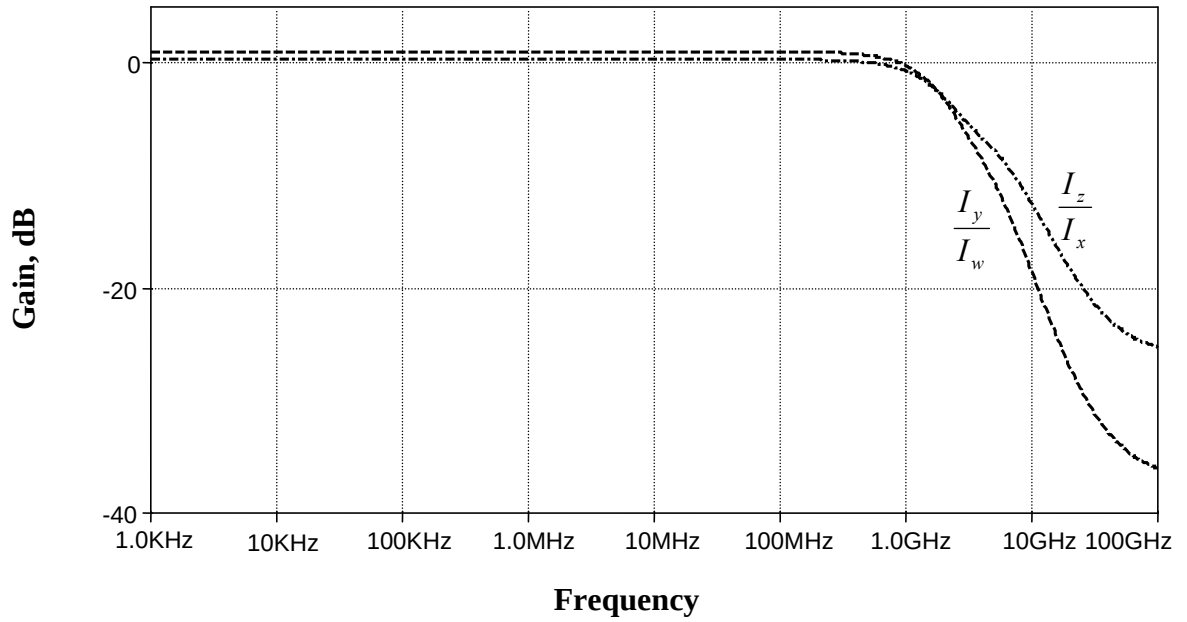


Figure 3.18. Frequency response of the current gains

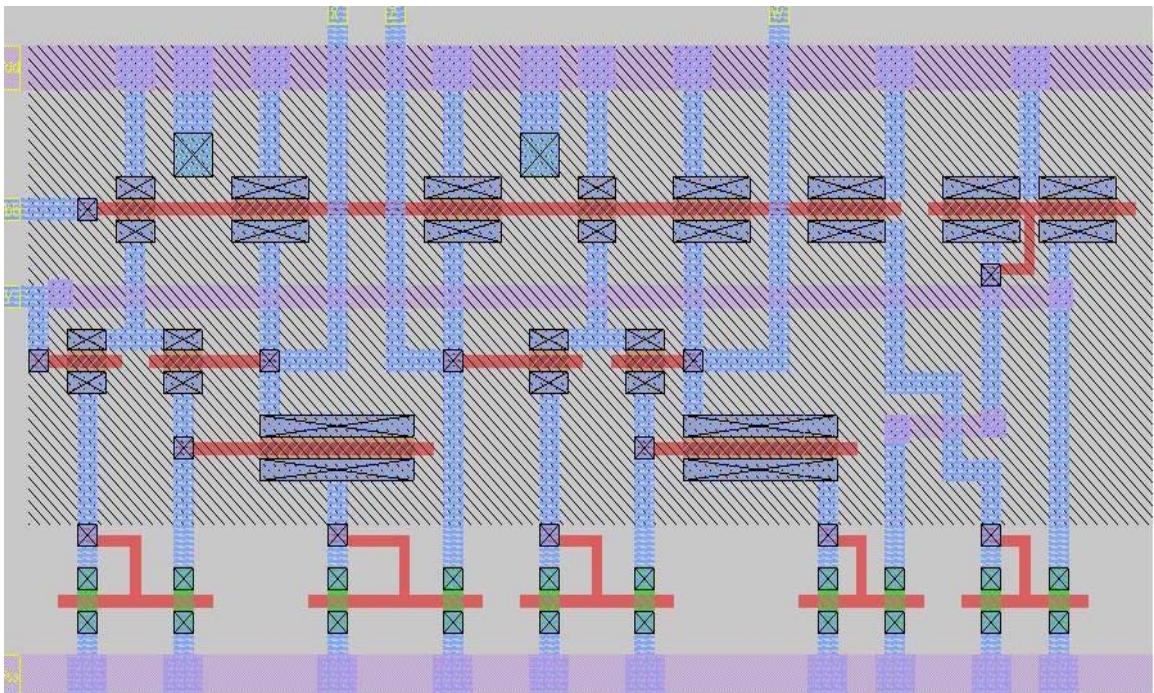


Figure 3.19. Layout of the MCFOA in Figure 3.11

To illustrate the time domain performance of the circuit in Figure 3.13 using above passive element values, a triangular input current I_{in} with 0.02mA peak-to-peak value at $f=1$ MHz is applied to the proposed inductance. We obtain a square wave output voltage V_{out} as depicted in Figure 3.20. Also, ideal and simulated phase and magnitude responses of the impedance of the inductor are shown in Figure 3.21.

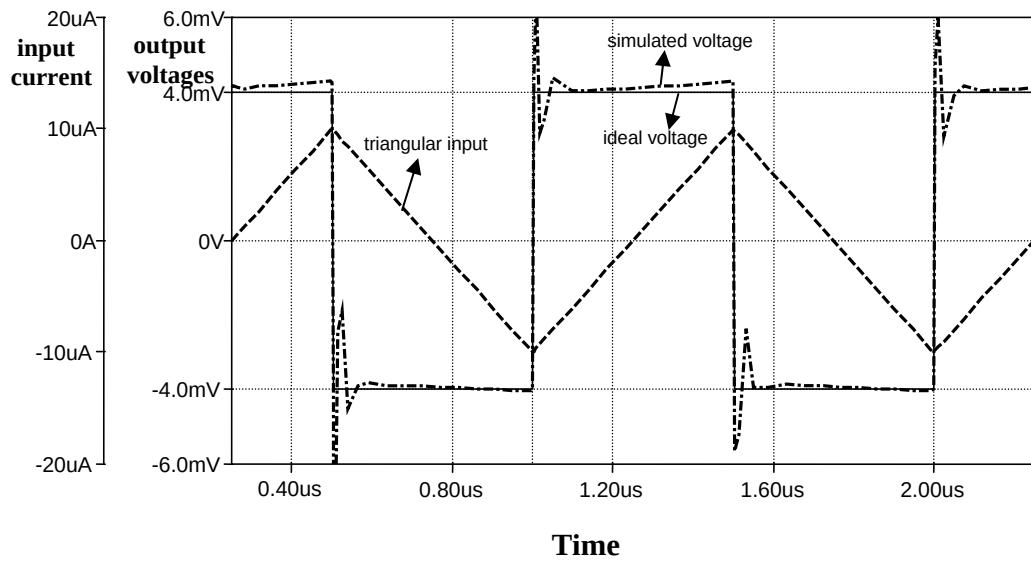


Figure 3.20. Time domain performance of the inductor realized with circuit in Figure 3.13

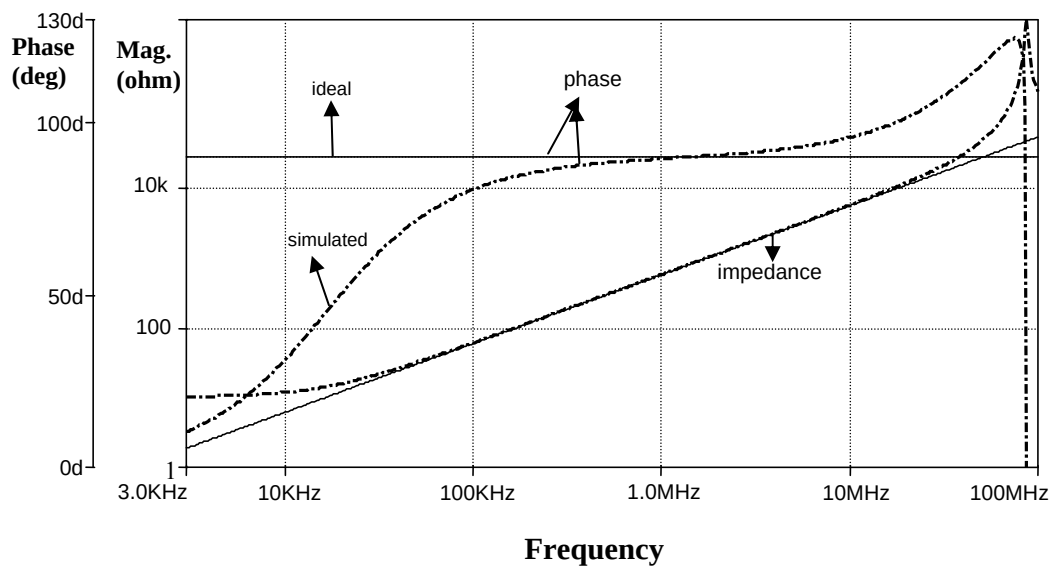


Figure 3.21. Phase and magnitude of the inductance impedance of the circuit in Figure 3.13

3.4.5. Experimental Results

The voltage-mode and current-mode filters given in Figures 3.15 and 3.16 are constructed using commercially available active devices, AD844s. The MCFOA is realized using three AD844s as shown Figure 3.22.

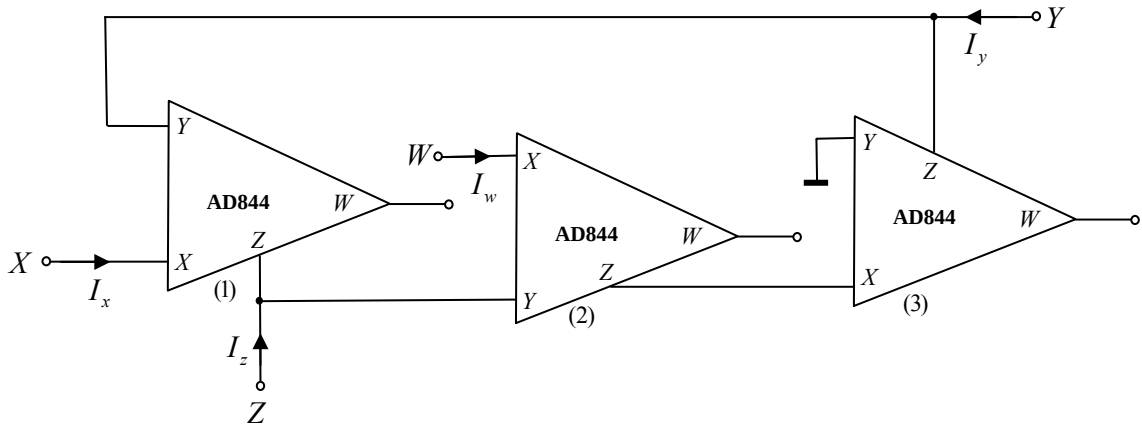


Figure 3.22. MCFOA construction using commercially available active devices

The passive elements $R_1 = R_2 = 1\text{k}\Omega$ (Also, $R_3 = 1\text{k}\Omega$ for the voltage mode filter) and $C_1 = C_2 = 1\text{nF}$ are selected. Both of the ideal and experimental filter responses of the presented circuits in Figures 3.15 and 3.16 are given in Figures 3.23 and 3.24, respectively.

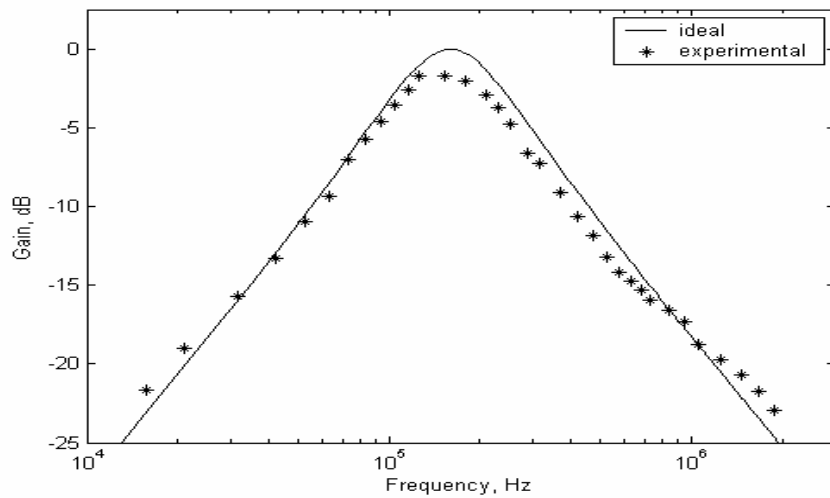


Figure 3.23. Ideal and experimental responses of the circuit in Figure 3.15 using the structure in Figure 3.22

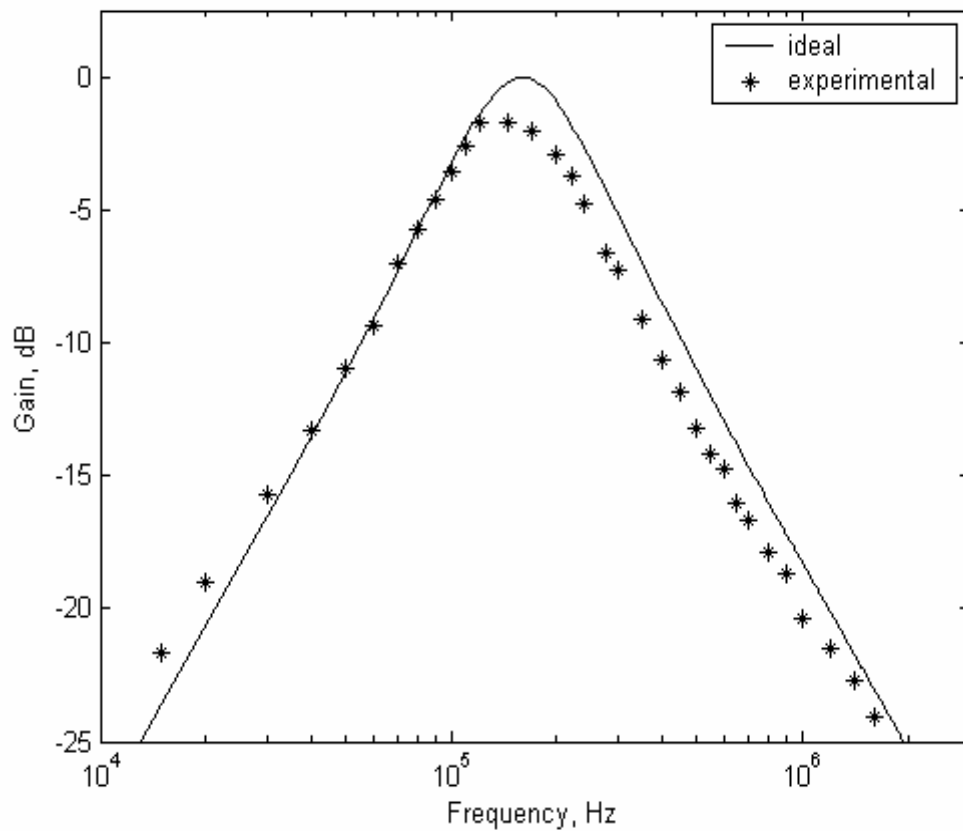


Figure 3.24. Ideal and experimental responses of the circuit in Figure 3.16 using the structure in Figure 3.22

The discrepancy between ideal and experimental responses mainly stems from the parasitic impedance and non-ideal gain effects of the AD844s and actual values of the resistors and capacitors.

In this chapter, after giving high frequency restrictions of the inductor simulators when applied input is a current source, a novel four port MCFOA and new circuits such as inductor simulators and current and voltage-mode filters are developed.

Six inductor simulator configurations with reduced non-ideal gain effects are also designed besides signal limitations of the analog filters are investigated shortly. Some useful simulated and experimental results as well as layout of the new MCFOA are given to clarify the theory.

In the next chapter, parasitic impedance effects on the performance of current-mode analog filters are investigated in great detail. Some second-order and high-order analog filters are going to be given as alternatives from the parasitic impedance effects point of views.

4. PARASITIC IMPEDANCE EFFECTS ON THE PERFORMANCE OF THE ANALOG FILTERS

In all analog filters, the designer must take attention on parasitic impedance effects. This is also valid for CCII/CCCII based analog filters. Second-generation current conveyors (CCIIs) and CCCIIs have parasitic resistances at the X and Z terminals and parasitic capacitances at the Y and Z terminals. These parasitic impedances cause additional poles or zeroes in the transfer functions of the filters, which are effective at low and high frequencies. The parasitic resistances in series with the capacitors connected to the X terminals of the CCIIs/CCCIIs affect the performance of the analog filter at high frequencies. The other limitation factors on the high-frequency performance of the CCII/CCCII based analog filters are parasitic capacitances at ports Z and Y of the conveyors. Furthermore, the parasitic resistances at port Z of the conveyors affect the low frequency performance of the analog filter.

In this chapter, parasitic impedance effects at high frequencies are explained by using two second-order current-mode analog filters. Several novel current-mode and voltage-mode analog filters with reduced parasitic impedance effects are also given as examples. These filters can operate at high frequencies since they have no capacitors connected in series to the X terminals of the conveyors.

4.1. Description of the Proposed Current-Mode Analog Filters

In this section, two new second-order current-mode analog filters, employing CCCIIs, are given to study their parasitic impedance effects on their performance.

The first second-order current-mode filter is shown in Figure 4.1. The biasing current of the first current controlled conveyor I_{o1} is chosen sufficiently large to ignore the effect of R_{x1} . The other conveyors have the X terminal parasitic resistances R_{xk} ($k = 2, 3, 4$).

Routine analysis of the circuit in Figure 4.1 gives the following TFs:

$$\frac{I_{lp1}}{I_{in1}} = \frac{R_{x2}\alpha_3\alpha_4\beta_3\beta_4}{D_1(s)} \quad (4.1)$$

$$\frac{I_{bp1}}{I_{in1}} = -\frac{sC_2R_{x3}R_{x4}\alpha_2}{D_1(s)} \quad (4.2)$$

$$\frac{I_{hp1}}{I_{in1}} = \frac{s^2C_1C_2R_{x2}R_{x3}R_{x4}\alpha_1\beta_1}{D_1(s)} \quad (4.3)$$

where $D_1(s)$ is found to be

$$D_1(s) = s^2C_1C_2R_{x2}R_{x3}R_{x4}\beta_1\gamma_1 + sC_2R_{x3}R_{x4} + R_{x2}\alpha_3\beta_3\beta_4\gamma_4 \quad (4.4)$$

In equations (4.1) - (4.4), α_k ($k=1,\dots,4$), γ_n ($n=1, \dots, 4$) are current gains and β_k are voltage gains of the corresponding CCCIIs, which are in the form of multipliers in each term of the TFs. Therefore, if variable-gain current conveyors [6] are employed, α and γ can be used to adjust each term of the TFs in equations (4.1) - (4.4) or compensate the errors in their values.

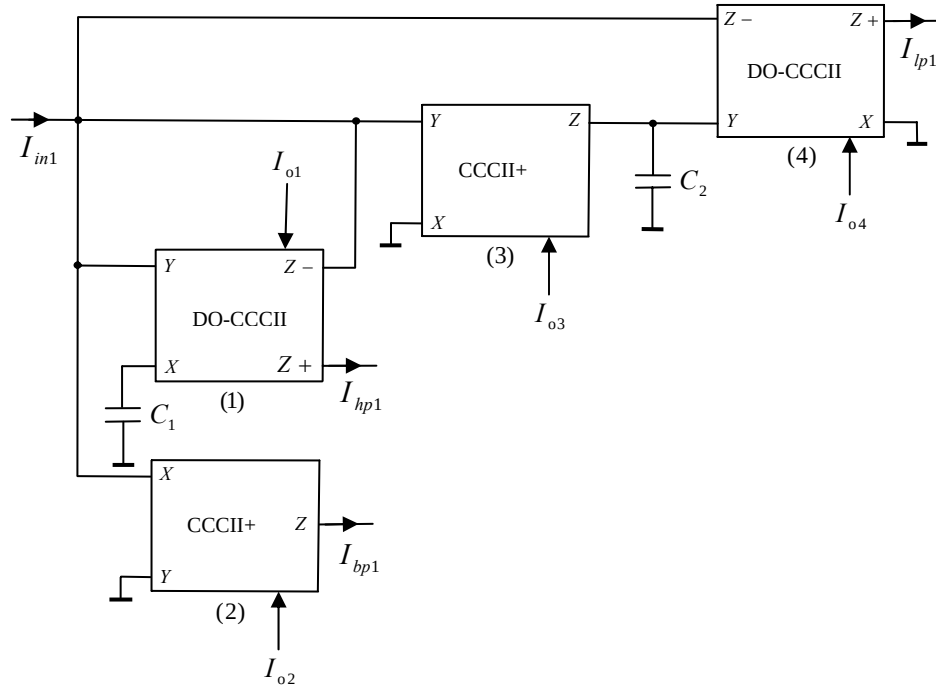


Figure 4.1. The first proposed second-order current-mode filter using current controlled conveyors and grounded capacitors

The interconnection of the relevant output currents in equations (4.1) - (4.3) yields to the notch and all-pass responses as

$$I_{notch1} = I_{lp1} + I_{hp1} \quad (4.5)$$

$$I_{all-pass1} = I_{lp1} + I_{bp1} + I_{hp1} \quad (4.6)$$

The parameters ω_{o1} and Q_1 for the proposed filter are calculated as

$$\omega_{o1} = \sqrt{\frac{\alpha_3 \beta_3 \beta_4 \gamma_4}{C_1 C_2 R_{x3} R_{x4} \beta_1 \gamma_1}} \quad (4.7)$$

$$Q_1 = R_{x2} \sqrt{\frac{C_1 \alpha_3 \beta_1 \beta_3 \beta_4 \gamma_1 \gamma_4}{C_2 R_{x3} R_{x4}}} \quad (4.8)$$

Note that the parameter Q_1 in equation (4.8) can be tuned by changing R_{x2} without disturbing the parameter ω_{o1} .

The second proposed current-mode filter with sufficiently large I_{o1} is shown in Figure 4.2.

Routine analysis of the circuit in Figure 4.2 gives the following filter TFs:

$$\frac{I_{lp2}}{I_{in2}} = \frac{R_{x2} \alpha_3 \alpha_4 \beta_3 \beta_4}{D_2(s)} \quad (4.9)$$

$$\frac{I_{bp2}}{I_{in2}} = -\frac{s C_2 R_{x3} (R_{x4} + R_{x5}) \alpha_2}{D_2(s)} \quad (4.10)$$

$$\frac{I_{hp2}}{I_{in2}} = \frac{s^2 C_2 C_3 R_{x2} R_{x3} (R_{x4} + R_{x5}) \alpha_1 \beta_1}{D_2(s)} \quad (4.11)$$

where $D_2(s)$ is found to be

$$D_2(s) = s^2 C_1 C_2 R_{x2} R_{x3} (R_{x4} + R_{x5}) + s C_2 R_{x3} (R_{x4} + R_{x5}) + R_{x2} \alpha_3 \alpha_5 \beta_3 \beta_4 \quad (4.12)$$

By interconnecting of the relevant output currents in (4.9) - (4.11) and taking $C_3 = C_1$, the notch and all-pass filter responses can be realized as

$$I_{notch2} = I_{lp2} + I_{hp2} \quad (4.13)$$

$$I_{all-pass2} = I_{lp2} + I_{bp2} + I_{hp2} \quad (4.14)$$

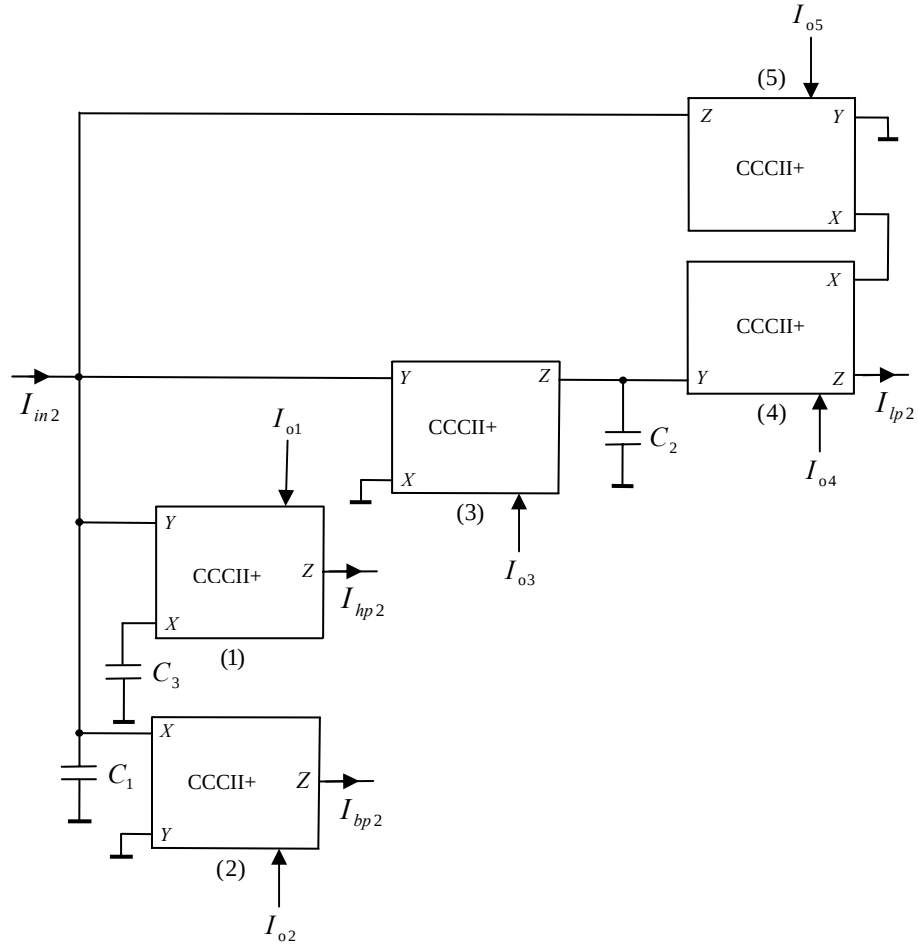


Figure 4.2. The second proposed filter employing only plus-type current controlled conveyors

The parameters ω_{o2} and Q_2 for this filter are found as

$$\omega_{o2} = \sqrt{\frac{\alpha_3 \alpha_5 \beta_3 \beta_4}{C_1 C_2 R_{x3} (R_{x4} + R_{x5})}} \quad (4.15)$$

$$Q_2 = R_{x2} \sqrt{\frac{C_1 \alpha_3 \alpha_5 \beta_3 \beta_4}{C_2 R_{x3} (R_{x4} + R_{x5})}} \quad (4.16)$$

The second proposed filter employs only CCCII+s thus AD844s with resistors can be used for its realization.

4.2. Parasitic Resistance Effects

The parasitic resistors and capacitors of a CCCII+ are shown in Figure 4.3. Similarly, a CCII+ has the same parasitic components. If only resistors and no capacitors are connected in series to the X terminals of the CCIIs / CCCII, the circuit can be operated at higher frequencies [82]. Regarding this, the frequency responses of the filters shown in Figures 4.1 and 4.2 are limited by the dominant poles $\omega_p = 1/(C_1 R_{x1})$ and $\omega_p = 1/(C_3 R_{x1})$, respectively. Therefore, more accurate transfer functions of the first proposed filter can be found by replacing the admittance sC_1 in equations (4.1) – (4.3) with the admittance $sC_1/(1+sC_1R_{x1})$. By replacing s with $j\omega$ in $sC_1/(1+sC_1R_{x1})$, the frequency domain equivalent admittance, becomes $j\omega C_1/(1+j\omega C_1 R_{x1})$.

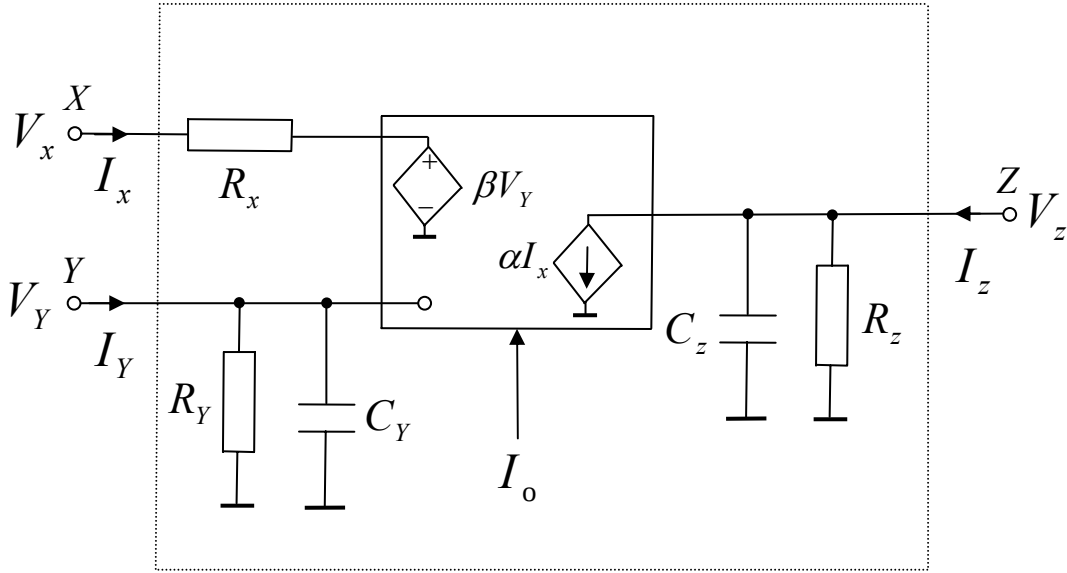


Figure 4.3. Parasitic resistances and capacitances of a CCCII+

Here, three cases can be considered.

(i) $1 + j\omega C_1 R_{x1} \cong 1$ for $\omega C_1 R_{x1} \leq 0.1$ thus we can ignore the parasitic resistance effect.

In this case, the maximum frequency for ideal operation can be given by

$$f_{\max} = \frac{0.1}{2\pi C_1 R_{x1}} \quad (4.17)$$

- (ii)** $1 + j\omega C_1 R_{x1} \cong j\omega C_1 R_{x1}$ for $\omega C_1 R_{x1} \geq 10$. In this case, $j\omega C_1 / (1 + j\omega C_1 R_{x1}) \cong 1/R_{x1}$ and the order of the filter is reduced by one.
- (iii)** $1 + j\omega C_1 R_{x1}$ remains without simplification for $0.1 < \omega C_1 R_{x1} < 10$ or in the frequency range $0.1/(2\pi C_1 R_{x1}) \leq f \leq 10/(2\pi C_1 R_{x1})$. Then extra terms appear in the TFs of the filter responses.

As shown in Figure 4.3, the CCII_s / CCCII_s have parasitic capacitances at their Y and Z terminals and resistances at their Z terminals. It should be mentioned that the parasitic resistance at Y terminal is very high and can be neglected. If external resistors are connected to the Y and Z terminals of the CCII_s / CCCII_s extra poles appear in the transfer functions, which limit the high frequency operation of the filter. In this section, X terminal parasitic resistance effects on the performance of the filters are under investigation in detail.

For the first proposed filter to operate at high frequencies the value of C_1 must be chosen sufficiently small and/or R_{x1} must be reduced by using larger biasing current. Taking R_{x1} into account, the equations (4.1)-(4.3) with $\alpha = \beta = \gamma = 1$ becomes

$$\frac{I_{lp1}}{I_{in1}} = \frac{R_{x2}}{\Delta_1(s)} \quad (4.18)$$

$$\frac{I_{bp1}}{I_{in1}} = -\frac{sC_2 R_{x3} R_{x4}}{\Delta_1(s)} \quad (4.19)$$

$$\frac{I_{hp1}}{I_{in1}} = \frac{\frac{s^2 C_1 C_2 R_{x2} R_{x3} R_{x4}}{1 + sC_1 R_{x1}}}{\Delta_1(s)} \quad (4.20)$$

where

$$\Delta_1(s) = \frac{s^2 C_1 C_2 R_{x2} R_{x3} R_{x4}}{1 + sC_1 R_{x1}} + sC_2 R_{x3} R_{x4} + R_{x2} \quad (4.21)$$

For $\omega \geq 10/(C_1 R_{x1})$ and replacing $j\omega$ for s , the TFs in equations (4.18) – (4.20) can be approximated as

$$\frac{I_{lp1}}{I_{in1}} = \frac{R_{x2}}{\hat{\Delta}_1(j\omega)} \quad (4.22)$$

$$\frac{I_{bp1}}{I_{in1}} = -\frac{j\omega C_2 R_{x3} R_{x4}}{\hat{\Delta}_1(j\omega)} \quad (4.23)$$

$$\frac{I_{hp1}}{I_{in1}} = \frac{j\omega \frac{C_2 R_{x2} R_{x3} R_{x4}}{R_{x1}}}{\hat{\Delta}_1(j\omega)} \quad (4.24)$$

where

$$\hat{\Delta}_1(j\omega) = j\omega C_2 R_{x3} R_{x4} \left(\frac{R_{x2}}{R_{x1}} + 1 \right) + R_{x2} \quad (4.25)$$

From equation (4.22) through equation (4.24) it can be realized that for the frequencies grater than $\omega \geq 10/(C_1 R_{x1})$ the filter exhibits first-order characteristics for all responses.

Defining $f_\beta = 1/(2\pi C_1 R_{x1})$, the filter operates well up to the frequency $f = 0.1f_\beta$. For instance, considering practical passive element values of $C_1 = 100\text{pF}$ and $R_{x1} = 10\Omega$ for the proposed filter, it should exhibit good performance up to 15.915 MHz.

Note that in the analysis above, we assumed that the poles and zeros of the current and voltage gains are at much higher frequencies.

The second proposed filter in Figure 4.2 has one dominant pole due to the parasitic resistance R_{x1} , which affects its high frequency performance. Thus, high frequency performance of the high-pass, notch and all-pass responses is limited by this pole. In equation (4.11), replacing sC_3 with $sC_3/(1+sC_3 R_{x1})$ gives the high frequency transfer functions of the filter. Moreover, low-pass and band-pass responses are not affected from

this parasitic resistance effects. Similarly, taking R_{x1} into account, the equations (4.9)-(4.11) with $\alpha = \beta = 1$ becomes

$$\frac{I_{lp2}}{I_{in2}} = \frac{R_{x2}}{\Delta_2(s)} \quad (4.26)$$

$$\frac{I_{bp2}}{I_{in2}} = -\frac{sC_2R_{x3}(R_{x4} + R_{x5})}{\Delta_2(s)} \quad (4.27)$$

$$\frac{I_{hp2}}{I_{in2}} = \frac{s^2 \frac{C_3}{1 + sC_3R_{x1}} C_2R_{x2}R_{x3}(R_{x4} + R_{x5})}{\Delta_2(s)} \quad (4.28)$$

where $\Delta_2(s)$ is found to be

$$\Delta_2(s) = s^2 C_1 C_2 R_{x2} R_{x3} (R_{x4} + R_{x5}) + s C_2 R_{x3} (R_{x4} + R_{x5}) + R_{x2} \quad (4.29)$$

The TFs in equations (4.26) – (4.28) for $\omega \geq 10/(C_3 R_{x1})$ and replacing $j\omega$ for s , can be approximated as

$$\frac{I_{lp2}}{I_{in2}} = \frac{R_{x2}}{\hat{\Delta}_2(j\omega)} \quad (4.30)$$

$$\frac{I_{bp2}}{I_{in2}} = -\frac{j\omega C_2 R_{x3} (R_{x4} + R_{x5})}{\hat{\Delta}_2(j\omega)} \quad (4.31)$$

$$\frac{I_{hp2}}{I_{in2}} = \frac{j\omega \frac{C_2 R_{x2} R_{x3} (R_{x4} + R_{x5})}{R_{x1}}}{\hat{\Delta}_2(j\omega)} \quad (4.32)$$

where $\hat{\Delta}_2(j\omega)$ is found to be

$$\hat{\Delta}_2(j\omega) = (j\omega)^2 C_1 C_2 R_{x2} R_{x3} (R_{x4} + R_{x5}) + (j\omega) C_2 R_{x3} (R_{x4} + R_{x5}) + R_{x2} \quad (4.33)$$

Note that the second-order low-pass and band-pass responses in equations (4.30) and (4.31) remain unchanged but the second-order high-pass response in equation (4.32) becomes a standard second-order band-pass response in the vicinity of ω_o for $\omega \geq 10/(C_3 R_{x1})$.

The high frequency limitations mainly stem from three reasons:

- (i) If a capacitor is connected in series to the X terminal of the CCII/CCCII, the useful frequency range due to this capacitor and the X terminal parasitic resistance is defined by $f \leq 0.1f_{pr}$, where f_{pr} is considered as the dominant pole due to the parasitic resistors.
- (ii) If a resistor is connected to the Z terminal of the CCII/CCCII, the useful frequency range of the filter is limited by the resistor and parasitic capacitors at Z terminal of the conveyor and can be defined by $f \leq 0.1f_{pc}$, where f_{pc} is assumed as the dominant pole due to parasitic capacitors and parallel resistors in Z terminals.
- (iii) Due to the frequency dependent non-ideal voltage and current gains of the CCII/CCCII, the useful frequency range is defined by $f \leq 0.1f_{ni}$ where f_{ni} is considered as the dominant pole due to non-ideal gains.

As a result, to obtain ideal responses as close as possible to the ideal response, the frequency range of operation should be selected as

$$f \leq f_H = 0.1 \times \min\{f_{pr}, f_{pc}, f_{ni}\} \quad (4.34)$$

Here, it is assumed that one of the limits is dominant at high frequencies.

It should be mentioned that if a grounded capacitor C is connected to the Z terminal of a CCII/CCCII, there is a limitation at low frequencies due to the parasitic resistance R_z in parallel at the Z terminal. Therefore, in the frequency domain, the admittance at the Z terminal is expressed as $j\omega C + 1/R_z$. For $\omega \geq 10/(CR_z)$, $j\omega C + 1/R_z \cong j\omega C$. Hence, the frequency range at low frequencies is calculated as

$$f \geq \frac{0.1}{2\pi} \frac{1}{CR_z} = f_L \quad (4.35)$$

For example, the capacitor C_2 in Figure 4.1 is in parallel with a parasitic resistance R_{z3} (the Z terminal parasitic resistance of the third CCCII). Then, the frequency range for the filter in Figure 4.1 at low frequencies is $f \geq 0.1/(2\pi C_2 R_{z3})$. As a result, the useful

$$I_{BP} = -\frac{sC_2R_{x3}}{D(s)}I_{in} \quad (4.37)$$

$$I_{HP} = \frac{s^2C_1C_2R_{x2}R_{x3}}{D(s)}I_{in} \quad (4.38)$$

where, $D(s) = s^2C_1C_2R_{x2}R_{x3} + sC_2R_{x3} + 1$. The all-pass and notch responses can also be obtained as $I_{AP} = I_{HP} + I_{BP} + I_{LP}$ and $I_{NF} = I_{HP} + I_{LP}$, respectively. Also the proposed filter in Figure 4.4 can be used to construct a high-order filter as shown in Figure 4.5. The high-order filter in Figure 4.5 has the following low-pass and high-pass responses:

$$I_{lp} = \frac{1}{\Delta(s)}I_{in} \quad (4.39)$$

$$I_{hp} = \frac{s^n \left(\prod_{i=1}^n (C_i R_{x(i+1)}) \right)}{\Delta(s)}I_{in} \quad (4.40)$$

where,

$$\Delta(s) = \sum_{j=1}^n \left(s^j \left(\prod_{i=1}^j (C_{n-i+1} R_{x(n-i+2)}) \right) \right) + 1 \quad (4.41)$$

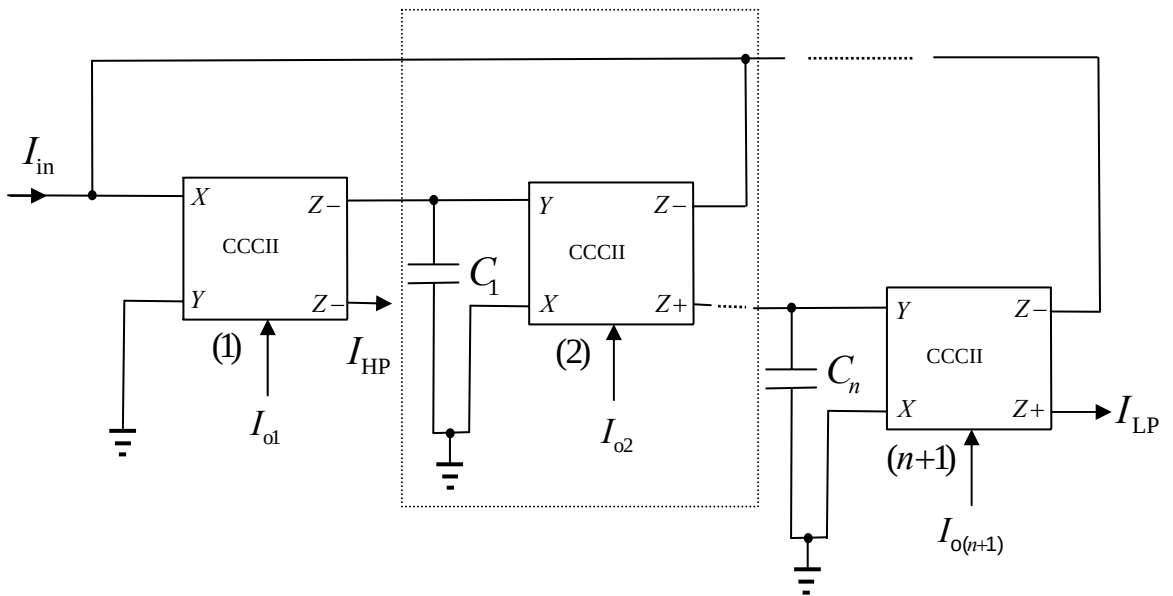


Figure 4.5. Proposed high-order filter derived from the filter shown in Figure 4.4

4.3.1.1. Simulation Results

The proposed filter in Figure 4.4 is simulated using SPICE program. The dual output CCCII (DO-CCCI) has been simulated using the schematic implementation in Figure 2.18. The following settings have been selected to obtain the low-pass, band-pass and high-pass responses at the resonance frequency of $f_o = 318.3 \text{ kHz}$ and quality factor of $Q = 1$: $I_{o1} = I_{o2} = I_{o3} = 13 \mu\text{A}$ ($R_{x1} = R_{x2} = R_{x3} = 1 \text{ k}\Omega$) and $C_1 = C_2 = 0.5 \text{ nF}$. The ideal (theoretical) and simulated low-pass and high-pass responses of the filter are shown in Figure 4.6. Also, ideal and simulated band-pass and notch characteristics are depicted in Figure 4.7.

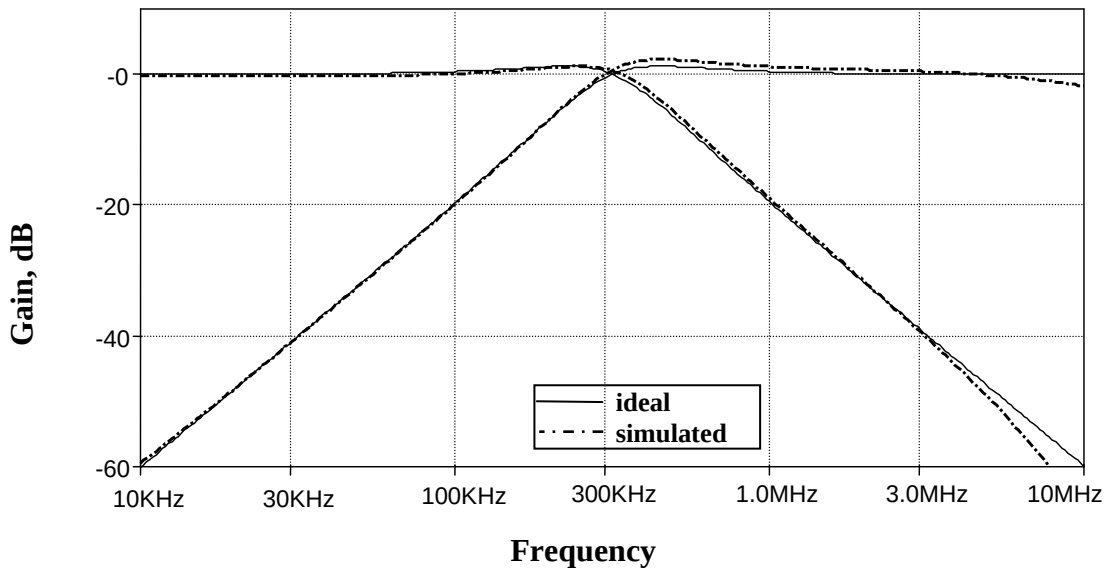


Figure 4.6. Theoretical and simulated low-pass and high-pass responses of the filter given in Figure 4.4

Furthermore, both of the theoretical and simulated phase and magnitude responses of the all-pass filter are given in Figure 4.8.

The large signal behavior of the circuit in Figure 4.4 is tested with investigation of the dependence of the output harmonic distortion for the band-pass response on the amplitude of the sinusoidal input signal at 318.3 kHz.

The results are given in Table 4.1. The total power dissipation of the filter is found to be 1.64mW.

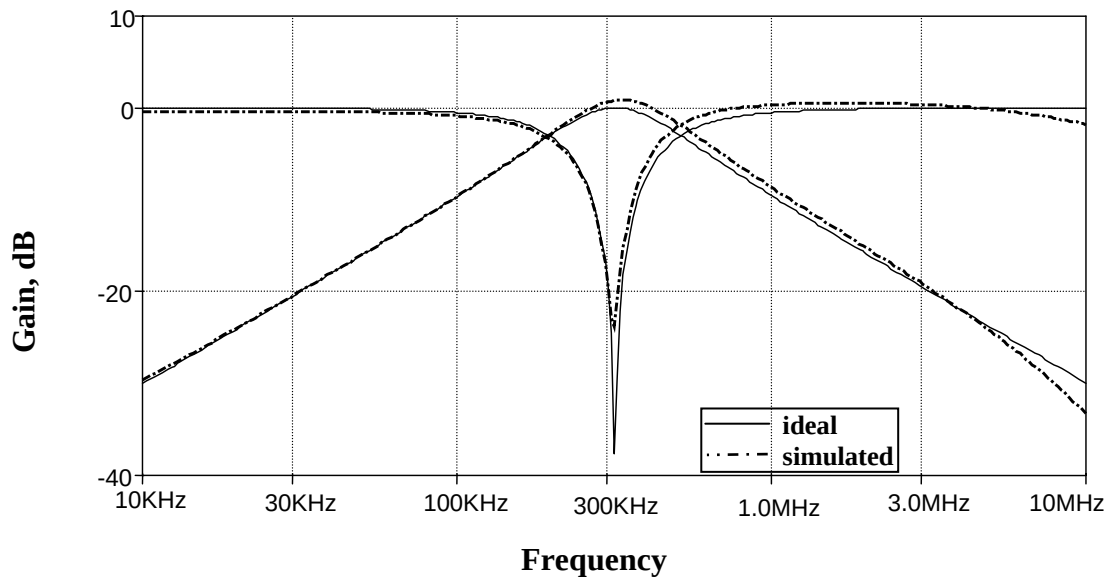


Figure 4.7. Ideal and simulated band-pass and notch responses of the filter in Figure 4.4

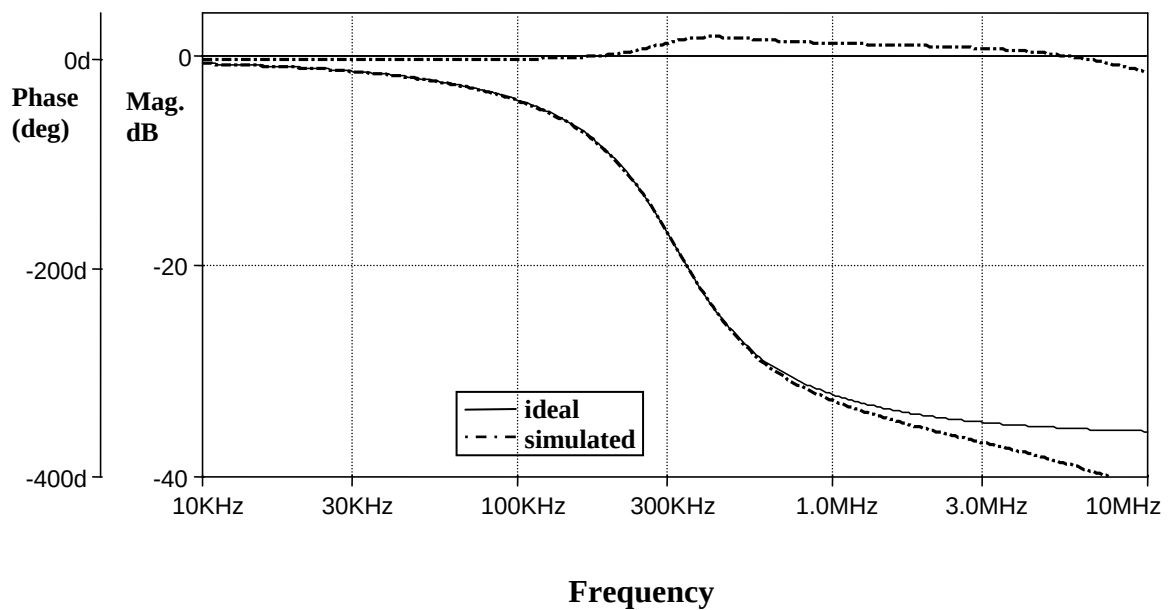


Figure 4.8. Ideal and simulated phase and magnitude responses of the all-pass filter

Straightforward analysis of the high-order filter in Figure 4.9 gives the following low-pass filter TF:

$$\frac{I_{LP}}{I_{in}} = \frac{1}{\sum_{j=1}^n \left(s^j \left(\prod_{i=1}^j (C_{n-i+1} R_{(n-i+1)}) \right) \right) + 1} \quad (4.42)$$

Also, if non-ideal gains are taken into account, the third-order TF in equation (4.42) turns to

$$\frac{I_{LP}}{I_{in}} = \frac{\alpha_1 \alpha_3 \alpha_5 \beta_2 \beta_5}{s^3 C_1 C_2 C_3 R_1 R_2 R_3 + s^2 C_2 C_3 R_2 R_3 + s C_3 R_3 \alpha_1 \alpha_2 \beta_2 + \alpha_1 \alpha_3 \alpha_4 \beta_2 \beta_5} \quad (4.43)$$

Similarly, $C_1 = C_2 = C_3 = 1\text{nF}$, $R_1 = 0.5\text{k}\Omega$, $R_2 = 1\text{k}\Omega$ and $R_3 = 2\text{k}\Omega$ are chosen to obtain a third-order Butterworth filter from the circuit in Figure 4.9 with $f_o = 159.15\text{ kHz}$. Both ideal and experimental frequency domain responses for the third-order filter are given in Figure 4.10. Furthermore, both experimental input and output currents of the third-order filter are shown in Figure 4.11. The input current is 1mA.

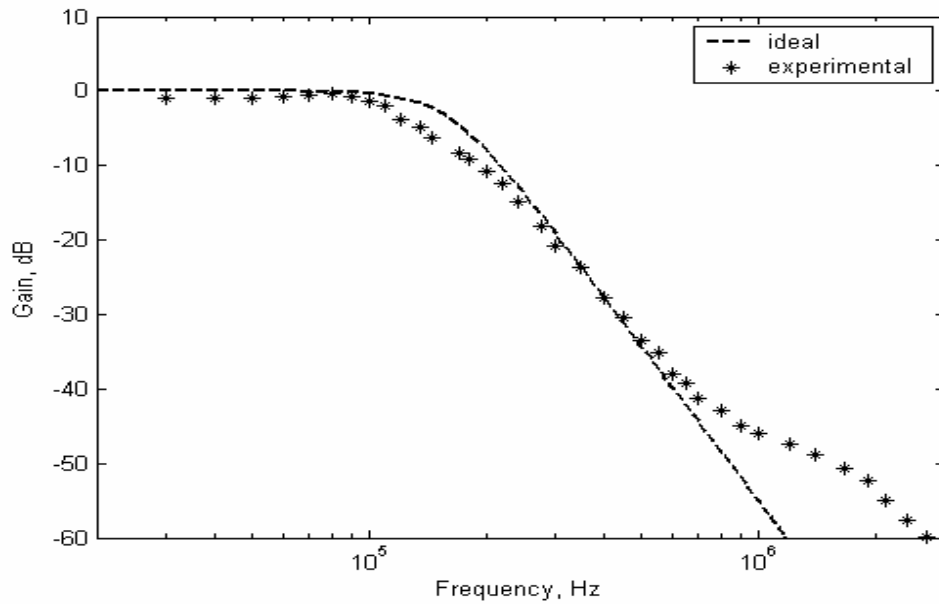


Figure 4.10. Ideal and experimental third-order low-pass Butterworth responses of the filter in Figure 4.9

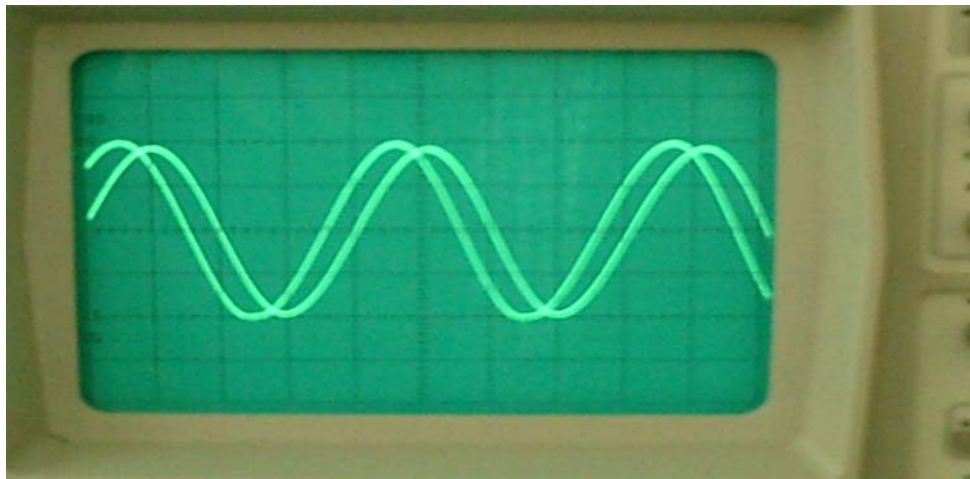


Figure 4.11. Time domain input signal and output response of the filter in Figure 4.9 for 1mA input current (vertical scale: 0.5mA/division, horizontal scale: 2 μ s/division)

4.3.3. A Unified Simple Double-Mode Universal Analog Filter/ Inductance Simulator

A versatile circuit in Figure 4.12 for analog filtering applications is proposed as a third alternative filter.

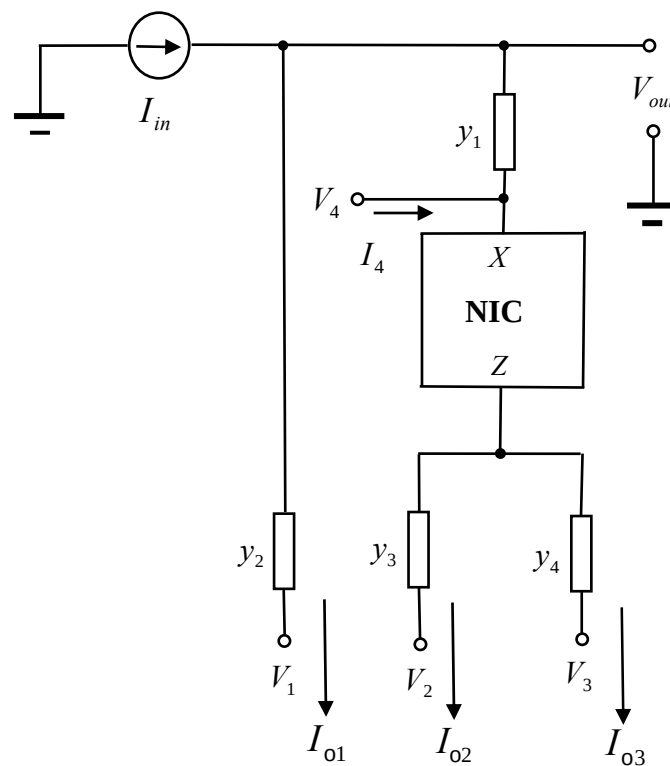


Figure 4.12. The proposed multi-purpose topology

The developed structure with appropriate component and input port selection also gives four kinds of lossy grounded inductors. This is the first circuit that provides both of the current-mode and voltage-mode standard universal filter responses as well as synthetic inductors from the same topology. The introduced circuit uses a minimum number of active and passive components both for analog filters and synthetic inductors. Nevertheless, the presented network needs only a single resistor value matching.

4.3.3.1. The Proposed Filter

Using standard notation, as an active device, the negative impedance converter (NIC) can be characterized as follows:

$$\begin{bmatrix} V_x \\ I_z \end{bmatrix} = \begin{bmatrix} \beta & 0 \\ 0 & \alpha \end{bmatrix} \begin{bmatrix} V_z \\ I_x \end{bmatrix} \quad (4.44)$$

Here, α and β are the frequency dependent non-ideal current and voltage gains (ideally equal to unity), respectively. Current convention is such that both of the currents of the NIC flow into it.

4.3.3.2. Current-Mode Filter

If $V_1 = V_2 = V_3 = 0$ and $y_1 = y_4$ are chosen where V_4 is open circuit, with straightforward analysis of the circuit in Figure 4.12, the following universal current-mode filter transfer functions are obtained:

$$\frac{I_{o1}}{I_{in}} = \frac{y_2 y_3}{D_i(s)} \quad (4.45)$$

$$\frac{I_{o2}}{I_{in}} = -\frac{y_1 y_3}{D_i(s)} \quad (4.46)$$

$$\frac{I_{o3}}{I_{in}} = -\frac{y_1^2}{D_i(s)} \quad (4.47)$$

where

$$D_i(s) = y_2 y_3 + y_1 y_3 + y_1^2 \quad (4.48)$$

If $y_1 = 1/R_1 = 1/R$, $y_2 = sC_2$, $y_3 = sC_3$ and $y_4 = 1/R_4 = 1/R$ are taken, $D_i(s)$ in equation (4.48) becomes

$$D_i(s) = s^2 C_2 C_3 + \frac{sC_3}{R} + \frac{1}{R^2} \quad (4.49)$$

Therefore, high-pass I_{o1} , band-pass I_{o2} and low-pass I_{o3} currents are obtained from the presented circuit. Also, either notch (I_{notch}) or all-pass ($I_{all-pass}$) filter response can be obtained by using extra current followers and connecting the relevant output currents as $I_{notch} = I_{o1} - I_{o3}$ and $I_{all-pass} = I_{o1} + I_{o2} - I_{o3}$. Moreover, if non-ideal gains are taken into account and matching constraints are not considered, $D_i(s)$ in equation (4.49) converts

$$D_n(s) = s^2 C_2 C_3 + \frac{sC_3}{R_1} + sC_2 \left(\frac{1}{R_4} - \alpha\beta \frac{1}{R_1} \right) + \frac{1}{R_1 R_4} \quad (4.50)$$

The parameters angular resonance frequency ω_0 and quality factor Q of the filter for $\alpha = \beta = 1$ and $R_1 = R_4 = R$ are calculated as

$$\omega_0 = \frac{1}{R} \sqrt{\frac{1}{C_2 C_3}} \quad (4.51)$$

$$Q = \sqrt{\frac{C_2}{C_3}} \quad (4.52)$$

It is observed from equations (4.51) and (4.52) that ω_0 and Q can be chosen arbitrarily. Also, passive component sensitivities are no more than unity in magnitudes.

4.3.3.3. Voltage-Mode Filter

If $I_{in} = 0$ and $y_1 = y_4$, $y_1 = 1/R_1 = 1/R$, $y_2 = sC_2$, $y_3 = sC_3$ and $y_4 = 1/R_4 = 1/R$ are taken where V_4 is open circuit, with routine analysis of the circuit in Figure 4.12, the output voltage V_{out} is given as

$$V_{out} = \frac{V_1 s^2 C_2 C_3 + V_2 \frac{s C_3}{R} + V_3 \frac{1}{R^2}}{D(s)} \quad (4.53)$$

Here, $D(s)$ is identical to $D_i(s)$ in (4.49) and if non-ideal gains and no matching condition are taken into account, $D(s)$ is identical to $D_n(s)$ in (4.50).

The output voltage V_{out} in equation (4.53) can be expressed for various applied input signals as

For $V_1 = V_{in}$ and $V_2 = V_3 = 0$, a high-pass analog filter response V_{hp} can be realized.

For $V_2 = V_{in}$ and $V_1 = V_3 = 0$, a band-pass analog filter response V_{bp} can be realized.

For $V_3 = V_{in}$ and $V_1 = V_2 = 0$, a low-pass analog filter response V_{lp} can be realized.

For $V_1 = V_3 = V_{in}$ and $V_2 = 0$, a notch analog filter response V_{notch} can be realized.

For $V_1 = -V_2 = V_3 = V_{in}$, an all-pass analog filter response $V_{all-pass}$ can be realized.

4.3.3.4. Lossy Inductors

Using the structure in Figure 4.12, lossy simulated inductors can also be implemented.

4.3.3.4.1. Positive Inductor with a Series Positive Resistor

If $I_{in} = 0$, $V_1 = V_3 = 0$, $y_3 = \infty$ and $y_1 = y_4$ are chosen and V_2 is taken as input where V_4 is open circuit, the impedance of the network becomes as

$$Z_{in2} = \frac{V_2}{-I_{o2}} = \frac{1}{y_1} + \frac{y_2}{y_1^2} \quad (4.54)$$

Also, for $y_1 = y_4 = 1/R$ and $y_2 = sC$, Z_{in2} in equation (4.54) becomes $Z_{in2} = sCR^2 + R$.

In some applications and for sufficiently high frequencies, this inductor can be used instead of a lossless inductor.

4.3.3.4.2. Negative Inductor with a Series Negative Resistor

If $I_{in} = 0$, $V_1 = V_2 = V_3 = 0$, $y_3 = 0$ and $y_1 = y_4$ are chosen and V_4 is taken as input, the impedance of the network is calculated as

$$Z_{in4} = \frac{V_4}{I_4} = -\frac{1}{y_1} - \frac{y_2}{y_1^2} \quad (4.55)$$

Also, for $y_1 = y_4 = 1/R$ and $y_2 = sC$, Z_{in4} in equation (4.55) becomes $Z_{in4} = -sCR^2 - R$.

4.3.3.4.3. Positive Inductor with a Parallel Positive Resistor

If $I_{in} = 0$, $V_2 = V_3 = 0$, $y_2 = \infty$ and $y_1 = y_4$ are chosen and V_1 is taken as input where V_4 is open circuit, the admittance of the network becomes as in the following:

$$Y_{in1} = \frac{-I_{o1}}{V_1} = y_1 + \frac{y_1^2}{y_3} \quad (4.56)$$

Also, for $y_1 = y_4 = 1/R$ and $y_3 = sC$, Y_{in1} in equation (4.56) is found to be

$$Y_{in1} = \frac{1}{R} + \frac{1}{sCR^2} \quad (4.57)$$

Hence, this topology can be used instead of a lossless simulated inductor at sufficiently low frequencies.

4.3.3.4.4. Negative Inductor with a Parallel Negative Resistor

If $I_{in} = 0$, $V_1 = 0$, $y_2 = \infty$ and $y_1 = y_4$ are chosen and $V_{in} = V_2 = V_3$ is taken as input where V_4 is open circuit, the admittance of the network is computed as

$$Y_{in23} = \frac{-I_{o2} - I_{o3}}{V_{in}} = -y_1 - \frac{y_1^2}{y_3} \quad (4.58)$$

Also, for $y_1 = y_4 = 1/R$ and $y_3 = sC$, Y_{in23} in equation (4.58) is found to be

$$Y_{in23} = -\frac{1}{R} - \frac{1}{sCR^2} \quad (4.59)$$

It is seen from Figure 4.12 that both of the positive lossy inductors employ a grounded capacitor so they can easily be realized in fully integrated circuit (IC) technology. Also, only a resistive element and no capacitors are connected in series to the X terminal of the NIC, so the proposed circuit can be operated at higher frequencies [82].

4.3.3.5. Simulation Results for the Current-Mode Filter

The proposed circuit with $V_1 = V_2 = V_3 = 0$ and $y_1 = y_4$ is constructed to obtain a current-mode filter. The filter is realized by using an AD844 with $\pm 15V$ DC power supply. The passive components are selected for the current-mode filter as $R_1 = R_4 = 1k\Omega$ and $C_2 = C_3 = 0.1nF$ to obtain $f_o = 1.59MHz$ and $Q = 1$. The simulation results shown in Figure 4.13 quite agree with the theoretical ones as expected, but the discrepancy between them mainly stems from the non-ideal gain and parasitic impedance effects of the AD844.

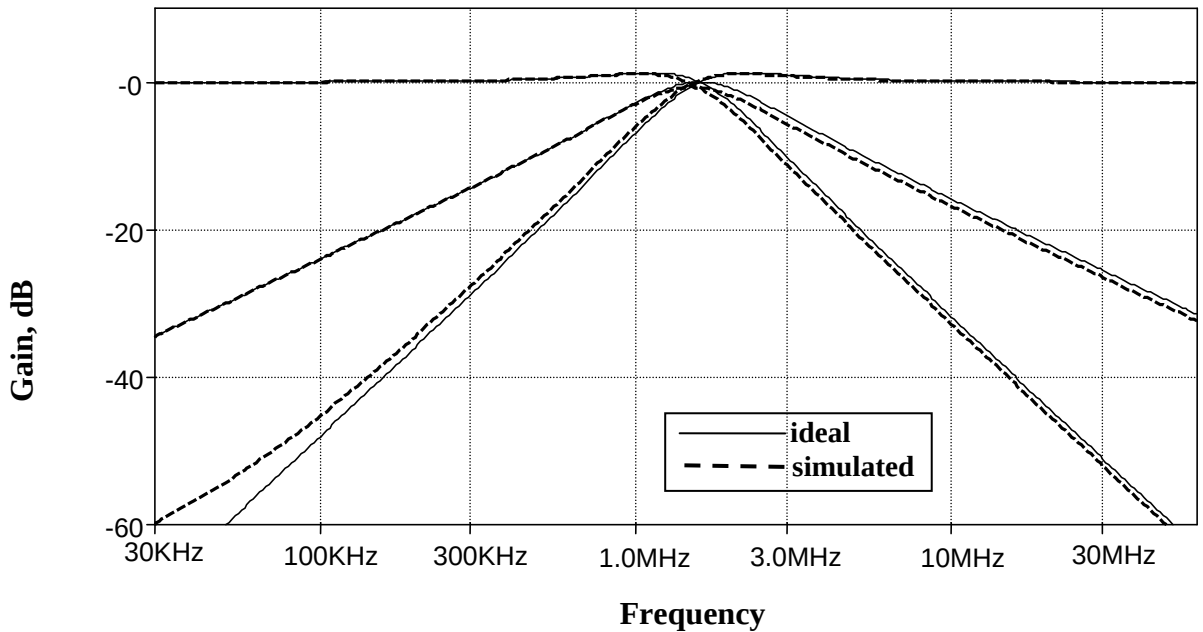


Figure 4.13. Ideal and simulated current-mode low-pass, band-pass and high-pass filter responses of the circuit in Figure 4.12

4.3.4. Fully Integrable Universal Current-Mode Filter with Specific Application of the CFOA

In this section, a current-mode universal filter using a single modified current-feedback operational amplifier (MCFOA) and only grounded passive elements is introduced. The proposed filter can simultaneously realize low-pass, band-pass and notch filter responses, and can also realize high-pass and all-pass filter responses with interconnection of the relevant output currents. This filter offers orthogonal control of angular resonance frequency (ω_o) and quality factor (Q), and has low active and passive component sensitivities.

4.3.4.1. Description of the New Seven Port Active Device

The Modified Current Feedback Operational Amplifier (MCFOA) is a seven-port device, and can be represented by the following matrix equation:

$$\begin{bmatrix} I_{z1} \\ I_y \\ V_x \\ V_w \\ I_{z2} \\ I_{z3} \\ I_{z4} \end{bmatrix} = \begin{bmatrix} \alpha_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\alpha_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \beta_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \beta_2 & 0 & 0 & 0 \\ \alpha_3 & 0 & 0 & 0 & 0 & 0 & 0 \\ \alpha_4 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha_5 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ I_w \\ V_y \\ V_{z1} \\ V_{z2} \\ V_{z3} \\ V_{z4} \end{bmatrix} \quad (4.60)$$

Current convention is such that all currents flow into the MCFOA. The frequency dependent non-ideal current gains α_j ($j = 1, 2, 3, 4, 5$) and voltage gains β_i ($i = 1, 2$) are ideally equal to unity. It is observed from equation (4.60) that the proposed MCFOA is a bit different from the CFOA.

(i) The MCFOA has extra three high output impedance terminals, Z_2 , Z_3 and Z_4 .

(ii) The MCFOA has the equation $I_y = -I_w$ but the CFOA has the equation $I_y = 0$.

4.3.4.2. Description of the New Analog Filter

Using the above MCFOA, a novel filter can be realized. Routine analysis of the filter in Figure 4.14 with $R_1 = R_2 = R$ gives the following filter transfer functions (TFs):

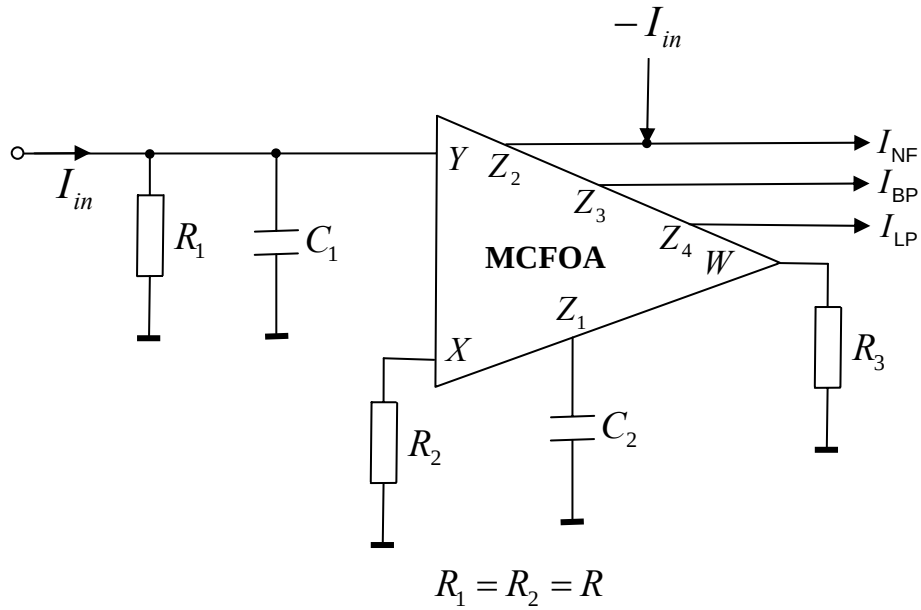


Figure 4.14. A universal current-mode filter, simultaneously realizing low-pass, band-pass and notch filter responses

$$\frac{I_{LP}}{I_{in}} = \frac{\omega_o^2}{D(s)} \quad (4.61)$$

$$\frac{I_{BP}}{I_{in}} = \frac{s \frac{\omega_o}{Q}}{D(s)} \quad (4.62)$$

$$\frac{I_{NF}}{I_{in}} = -\frac{s^2 + \omega_o^2}{D(s)} \quad (4.63)$$

where the denominator $D(s)$ and parameters ω_o and Q in equations (4.61) – (4.63) are found to be

$$D(s) = s^2 + s \frac{\omega_0}{Q} + \omega_0^2 \quad (4.64)$$

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R R_3}} \quad (4.65)$$

$$Q = \sqrt{\frac{C_1 R}{C_2 R_3}} \quad (4.66)$$

Interconnection of the relevant output currents, high-pass filter response ($I_{HP} = I_{LP} + I_{NF}$) and all-pass filter response ($I_{AP} = I_{BP} + I_{NF}$) can also be obtained.

If non-ideal gains are considered, TFs in equations (4.61)–(4.63) convert

$$\frac{I_{LP}}{I_{in}} = \frac{\alpha_1 \alpha_5 \beta_1 \beta_2}{\Delta(s)} \quad (4.67)$$

$$\frac{I_{BP}}{I_{in}} = \frac{s C_2 R_3 \alpha_4 \beta_1}{\Delta(s)} \quad (4.68)$$

$$\frac{I_{NF}}{I_{in}} = -\frac{s^2 C_1 C_2 R R_3 + s C_2 R_3 (1 - \alpha_3 \beta_1) + \alpha_1 \alpha_2 \beta_1 \beta_2}{\Delta(s)} \quad (4.69)$$

Here, $\Delta(s) = s^2 C_1 C_2 R R_3 + s C_2 R_3 + \alpha_1 \alpha_2 \beta_1 \beta_2$. Both of the parameters ω_0 and Q can be selected arbitrarily without disturbing the other parameter by choosing suitable passive components. Also, all of the active and passive element sensitivities of ω_0 and Q are no more than unity in magnitude.

4.3.4.3. Implementation and Simulations of the Proposed Filter

The internal structure of the new seven port MCFOA circuit is given in Figure 4.15. The circuit is designed using $0.35\mu m$ TSMC CMOS technology. The transistor model parameters are given in Table 4.2. Simulations are performed using the given device parameters. The dimensions of the MOS transistors are given in Table 4.3. The passive elements $R_1 = R_2 = R_3 = 1k\Omega$ and $C_1 = C_2 = 0.1nF$ are selected for the proposed filter to obtain $Q = 1$ and $f_0 = 1.59MHz$.

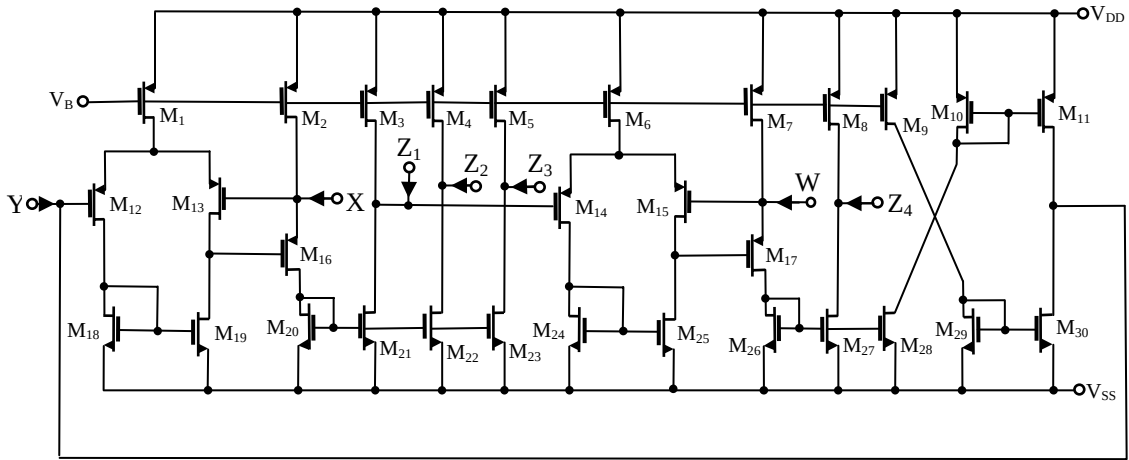


Figure 4.15. Internal structure of the developed MCFOA using CMOS transistors

Table 4.2. The 0.35 μm TSMC CMOS process parameters

.MODEL NT NMOS (LEVEL=3 TOX=7.9E-9 NSUB=1E17 GAMMA=0.5827871 + PHI=0.7 VTO=0.5445549 DELTA=0 UO=436.256147 ETA=0 THETA=0.1749684 + KP=2.055786E-4 VMAX= 8.309444E4 KAPPA=0.2574081 RSH=0.0559398 + NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11 WD=7.046724E-8 CGDO=2.82E-10 + CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3 PB=0.9758533 MJ=0.3448504 + CJSW=3.777852E-10 MJSW=0.3508721)
.MODEL PT PMOS (LEVEL=3 TOX=7.9E-9 NSUB=1E17 GAMMA=0.4083894 + PHI=0.7 VTO=-0.7140674 DELTA=0 UO=212.2319801 ETA=9.999762E-4 + THETA= 0.2020774 KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5 + RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD=5.000001E-13 WD=1.24987E-7 + CGDO=3.09E-10 CGSO=3.09E-10 CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 + MJ=0.5 CJSW=4.813504E-10 MJSW=0.5)

Table 4.3. Dimensions of the CMOS transistors used in the implementation of the MCFOA

PMOS Transistors	$W(\mu\text{m}) / L(\mu\text{m})$
M ₁ , M ₆ , M ₁₂ , M ₁₃ , M ₁₄ and M ₁₅	1.4/0.35
M ₂ , M ₃ , M ₄ , M ₅ , M ₇ , M ₈ , M ₉ , M ₁₀ and M ₁₁	2.8/0.35
M ₁₆ and M ₁₇	5.6/0.35
NMOS Transistors	$W(\mu\text{m}) / L(\mu\text{m})$
M ₁₈ , M ₁₉ , M ₂₀ , M ₂₁ , M ₂₂ , M ₂₃ , M ₂₄ , M ₂₅ , M ₂₆ , M ₂₇ , M ₂₈ , M ₂₉ and M ₃₀	0.7/0.35

It is observed that the simulated low-pass, band-pass and high-pass filter responses shown in Figure 4.16 agree quite well with the ideal ones.

Also, both of the nominal and worst-case simulations for the low-pass, band-pass and notch filter responses are shown in Figure 4.17.

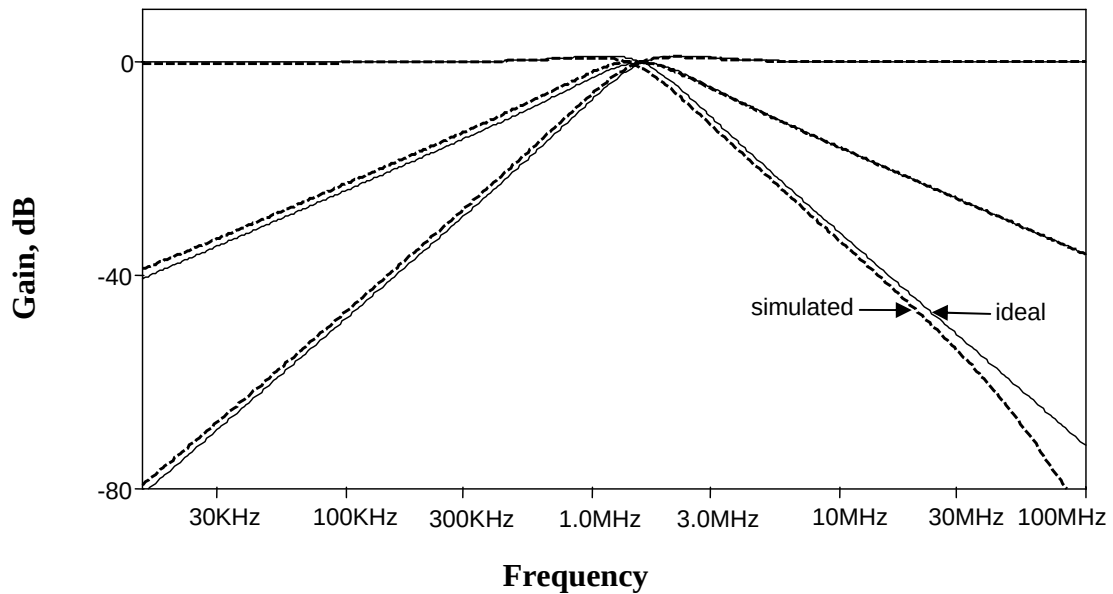


Figure 4.16. Frequency domain performance of the proposed filter

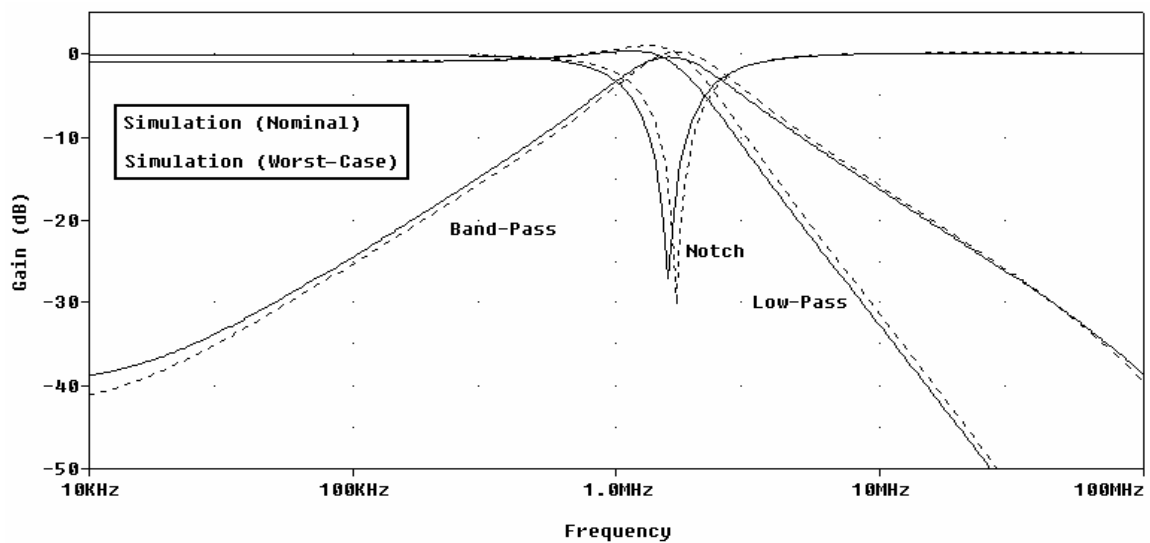


Figure 4.17. Nominal and worst-case simulated low-pass, band-pass and notch responses of the filter in Figure 4.14

On the other hand, the difference between ideal and simulated filter responses mainly stems from the parasitic impedance and non-ideal gain effects of the MCFOA.

4.3.5. Voltage-Mode Filters

A second-order electronically tunable voltage-mode filter is shown in Figure 4.18. It consists of a negative-type second-generation current conveyor and a voltage buffer.

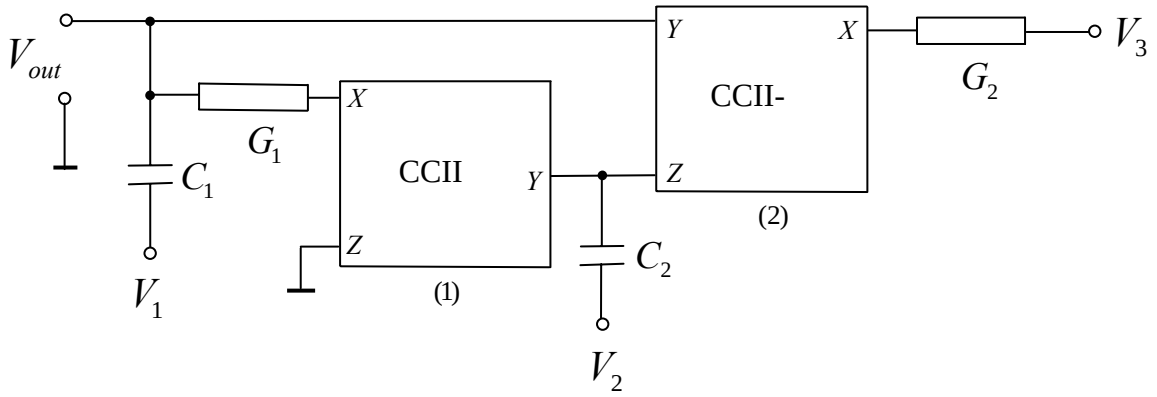


Figure 4.18. The proposed universal voltage-mode filter employing a single CCII- and a voltage buffer

Routine analysis of the circuit in Figure 4.18 gives the following output voltage:

$$V_{out} = \frac{s^2 C_1 C_2 V_1 + s C_2 G_1 \beta_1 V_2 + G_1 G_2 \alpha_2 \beta_1 V_3}{s^2 C_1 C_2 + s C_2 G_1 + G_1 G_2 \alpha_2 \beta_1 \beta_2} \quad (4.70)$$

Note that both of the resistors in circuit of Figure 4.18 are connected in series to the X port of the CCII-. Therefore by employing CCCIIs instead of the CCII-, the resistors in the circuit can be removed, resulting in an active-C filter (without using external resistors). Specialization of the numerator in equation (4.70) gives the following voltage-mode filter TFs:

- 1) $V_2 = V_3 = 0$ and $V_1 = V_{in}$ are taken for high-pass TF
- 2) $V_1 = V_2 = 0$ and $V_3 = V_{in}$ are taken for low-pass TF

- 3) $V_1 = V_3 = 0$ and $V_2 = V_{in}$ are taken for band-pass TF
- 4) $V_1 = V_3 = V_{in}$ and $V_2 = -V_{in}$ are taken for all-pass TF
- 5) $V_2 = 0$ and $V_1 = V_3 = V_{in}$ is taken for notch TF

Therefore, the parameters ω_0 and Q of this filter are computed as

$$\omega_0 = \sqrt{\frac{G_1 G_2 \alpha_2 \beta_1 \beta_2}{C_1 C_2}} \quad (4.71)$$

$$Q = \sqrt{\frac{C_1 G_2 \alpha_2 \beta_1 \beta_2}{C_2 G_1}} \quad (4.72)$$

From equations (4.71) and (4.72), it can be seen that ω_0 and Q can be adjusted by changing G_1 and G_2 . Also all active and passive element sensitivities of ω_0 and Q are equal to 0.5 in magnitude. So the proposed filters exhibit low active and passive sensitivities.

The second proposed circuit is shown in Figure 4.19. It consists of two resistors (one connected in series to the X terminal), two capacitors and only one CCII-. The analysis of the circuit gives the following output voltage:

$$V_{out} = \frac{s^2 C_1 C_2 V_1 + s C_1 G_1 V_1 + s C_2 G_1 V_2 + G_1 G_2 V_3}{s^2 C_1 C_2 + s(C_1 + C_2)G_1 + G_1 G_2} \quad (4.73)$$

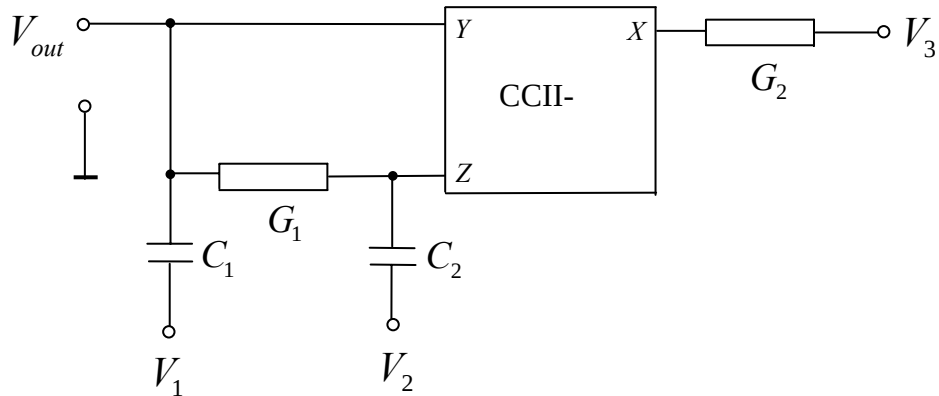


Figure 4.19. The proposed another second-order voltage-mode analog filter

Specialization of the numerator in equation (4.73) yields the following voltage-mode filter transfer functions (TFs):

- 1) $V_3 = 0$, $V_1 = V_{in}$ and $V_2 = -C_1 V_{in} / C_2$ are chosen for high pass TF
- 2) $V_1 = V_2 = 0$ and $V_3 = V_{in}$ are chosen for low-pass TF
- 3) $V_1 = V_3 = 0$ and $V_2 = (C_1 + C_2) V_{in} / C_2$ are chosen for band-pass TF
- 4) $V_1 = V_3 = V_{in}$ and $V_2 = -(2C_1 + C_2) V_{in} / C_2$ are chosen for all-pass TF
- 5) $V_1 = V_3 = V_{in}$ and $V_2 = -C_1 V_{in} / C_2$ are chosen for notch TF

As a result, ω_o and Q of the filter are given by

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \quad (4.74)$$

$$Q = \frac{1}{(C_1 + C_2)} \sqrt{\frac{C_1 C_2 G_2}{G_1}} \quad (4.75)$$

From equations (4.74) and (4.75) it can be seen that ω_o and Q can arbitrarily be adjustable. It means that ω_o can be adjusted without disturbing the Q by changing G_1 and G_2 simultaneously keeping G_2/G_1 constant for fixed capacitor values.

Passive element sensitivities of ω_o and Q in equations (4.74) and (4.75) are calculated as follows:

$$S_{G_1, G_2}^{\omega} = 0.5 \quad S_{C_1, C_2}^{\omega} = -0.5 \quad S_{G_1}^Q = -0.5 \quad S_{G_2}^Q = 0.5 \quad (4.76)$$

$$S_{C_1}^Q = 0.5 - C_1 / (C_1 + C_2) \quad S_{C_2}^Q = 0.5 - C_2 / (C_1 + C_2) \quad (4.77)$$

Note that all the passive element sensitivities are low. Also, $S_{C_1}^Q = S_{C_2}^Q = 0$ for $C_1 = C_2$. If a negative-type second-generation current controlled conveyor (CCCII-) is employed instead of the CCII- for this filter, $G_x = 1/R_x$ replaces for G_2 . Therefore, the parameters ω_o and Q can be adjusted electronically.

If α and β are taken into account, the output voltage in equation (4.73) becomes

$$V_{out} = \frac{s^2 C_1 C_2 V_1 + s C_1 G_1 V_1 + s C_2 G_1 V_2 + \alpha G_1 G_2 V_3}{s^2 C_1 C_2 + s(C_1 + C_2)G_1 + \alpha \beta G_1 G_2} \quad (4.78)$$

Therefore, ω_o and Q are computed as

$$\omega_o = \sqrt{\frac{\alpha \beta G_1 G_2}{C_1 C_2}} \quad (4.79)$$

$$Q = \frac{1}{(C_1 + C_2)} \sqrt{\frac{\alpha \beta C_1 C_2 G_2}{G_1}} \quad (4.80)$$

Note that all passive element sensitivities of ω_o and Q remain with no change as given before, and all of the active sensitivities of ω_o and Q are equal to 0.5.

The simulations are performed for the voltage-mode filter of Figure 4.19 to exhibit its performance. The CCII- is simulated using the schematic implementations shown in Figure 4.20 with DC symmetrical power supply voltages ± 1.5 V and bias voltages $V_B = 0.5$ V and $V_C = -0.5$ V.

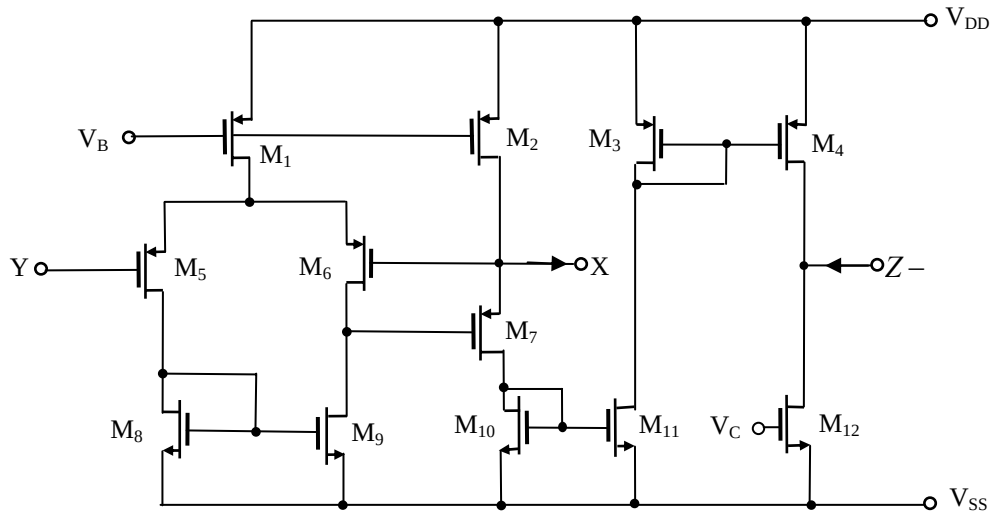


Figure 4.20. Internal structure of the CCII-

Figure 4.21 shows both the ideal and simulated low-pass and high-pass responses of the presented filter in Figure 4.19.

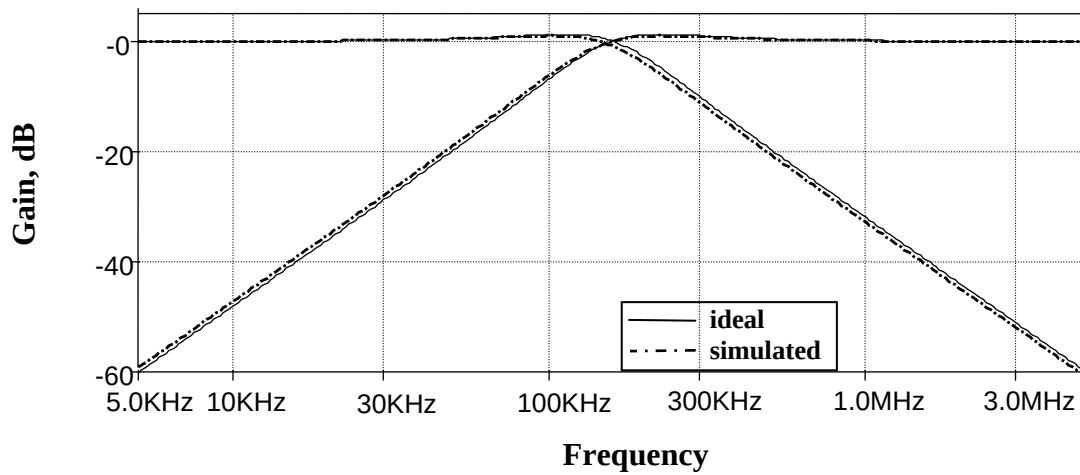


Figure 4.21. Ideal and simulated low-pass and high-pass responses of the filter in Figure 4.19

The ideal and simulated band-pass and notch responses are depicted in Figure 4.22. Also both ideal and simulated phase and magnitude responses of the all-pass filter are shown in Figure 4.23. The all-pass filter has 180° phase shift at $f_o = 159.15$ kHz.

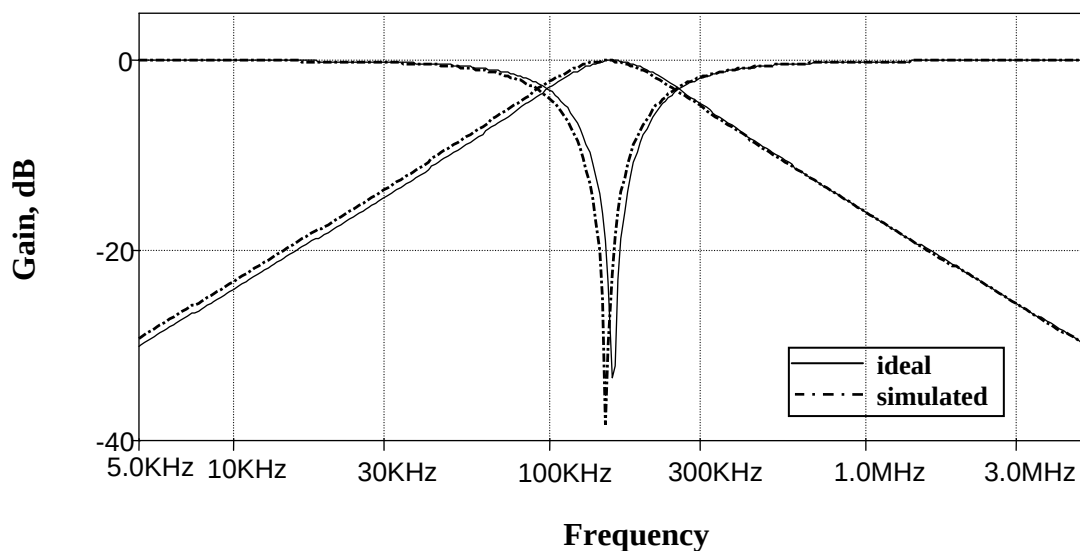


Figure 4.22. Ideal and simulated band-pass and notch responses of the filter in Figure 4.19

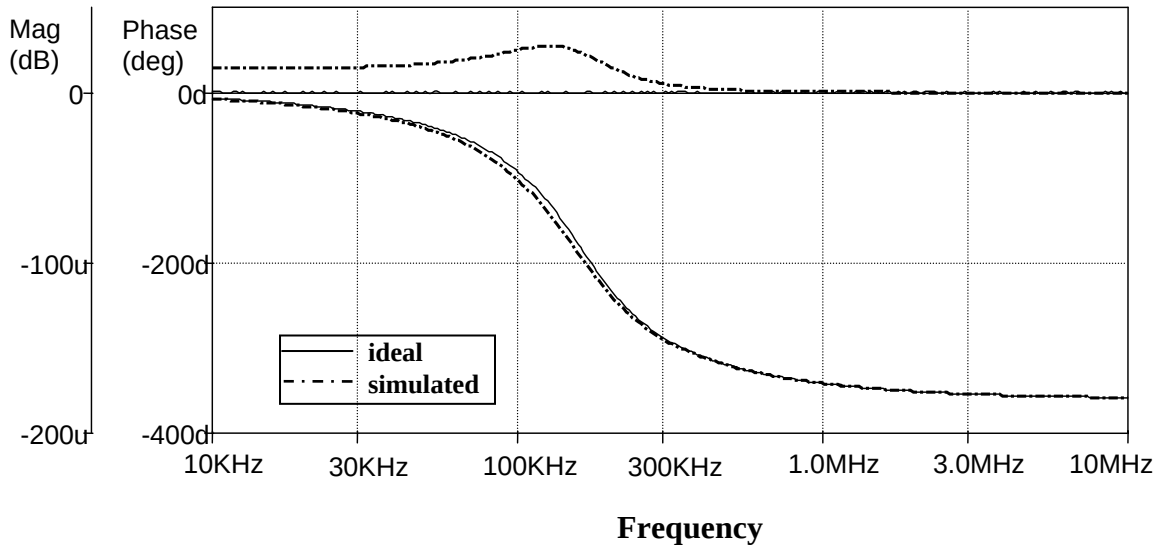


Figure 4.23. Ideal and simulated phase and magnitude of the all-pass response of the filter in Figure 4.19

From Figures 4.21-4.23, it can be seen that the simulation results agree well with the theoretical results.

The simulations are based on $0.35\mu\text{m}$ TSMC CMOS technology with parameters given in Table 4.3. The dimensions of the MOS transistors are given in Table 4.4. The passive elements are selected as: $G_1 = 0.5\text{mS}$, $G_2 = 2\text{mS}$ and $C_1 = C_2 = 1\text{nF}$ result in a natural frequency of $f_o = 159.15\text{ kHz}$ and $Q = 1$.

Table 4.4. Aspect ratio of the MOS transistors for the CCII- of Figure 4.20

PMOS Transistors	$W(\mu\text{m}) / L(\mu\text{m})$
M_1, M_5 and M_6	1.4/0.35
M_2, M_3 and M_4	2.8/0.35
M_7	5.6/0.35
NMOS Transistors	$W(\mu\text{m}) / L(\mu\text{m})$
M_8, M_9, M_{10}, M_{11} and M_{12}	0.7/0.35

Parasitic impedance effects on the performances of the current-mode filters have been discussed in the beginning of this chapter. A number of novel filters with reduced

parasitic impedances are proposed to solve the problems associated with the parasitic impedances.

In the next chapter, signal limitations of the analog filters stemmed from the restricted terminal voltages of the analog filters and maximum allowable terminal currents of the active devices are examined in detail.

5. SIGNAL LIMITATION IN ANALOG FILTERS

Due to the trend in the technology towards lower power supply voltages, the maximum amplitude of the signals processed in a filter is also decreasing. The aim in this chapter is to evaluate the limitations of the analog filters which are the results of terminal current limitations of the (CCII)s and limited power supply voltages resulting in restrictions in the selection of passive element values, operating frequency, applied input current, quality factor (Q) and gain constant (K) of the filter.

Contrary to the study of the limitations of the current conveyor based filters reported in [80] and [81], this thesis is focused on the limitations of the current conveyor based second-order filters due to quality factor and gain of the filter.

In this chapter, the signal limitation problems of the current-mode filters due to active element terminal currents and active element terminal voltages of the filters are investigated. The presented theory is applied to a given circuit example. Finally, the solutions to reduce the signal limitation problems of the filters are given.

5.1. Description of the Current-Mode Analog Filter Responses

In this section, signal limitations of filters are investigated by giving a universal current-mode filter example. A standard second-order current-mode filter has the following responses:

a) *Low-pass response,*

$$I_{lp} = K_1 \frac{\omega_o^2}{D(s)} I_{in} \quad (5.1)$$

b) *Band-pass response,*

$$I_{bp} = K_2 \frac{s \frac{\omega_o}{Q}}{D(s)} I_{in} \quad (5.2)$$

c) High-pass response,

$$I_{hp} = K_3 \frac{s^2}{D(s)} I_{in} \quad (5.3)$$

d) Notch response with $K_1 = K_3 = K_{NF}$,

$$I_{notch} = I_{lp} + I_{hp} = K_{NF} \frac{s^2 + \omega_0^2}{D(s)} I_{in} \quad (5.4)$$

e) All-pass response with $K_1 = K_2 = K_3 = K_{AP}$,

$$I_{all-pass} = I_{lp} - I_{bp} + I_{hp} = K_{AP} \frac{s^2 - s \frac{\omega_0}{Q} + \omega_0^2}{D(s)} I_{in} \quad (5.5)$$

where $D(s)$ is given as

$$D(s) = s^2 + s \frac{\omega_0}{Q} + \omega_0^2 \quad (5.6)$$

The actual physical implementations of equations (5.1)-(5.6) may employ various active devices including (CCII)s.

At $\omega = \omega_0$, the equations (5.1)-(5.6) in $j\omega$ domain convert

$$I_{lp} = -jK_1 Q I_{in} \quad (5.7)$$

$$I_{bp} = K_2 I_{in} \quad (5.8)$$

$$I_{hp} = jK_3 Q I_{in} \quad (5.9)$$

$$I_{notch} = 0 \quad (5.10)$$

$$I_{all-pass} = K_{AP} I_{in} \quad (5.11)$$

It is observed from equations (5.7) and (5.9) that the magnitudes of the low-pass and high-pass filter responses are proportional to Q at ω_0 .

The variations of an ideal low-pass filter response for $Q = 0.5, 1, 3$ and 10 at resonance frequency $f = 159.15$ kHz and $K = 1$ are given in Figure 5.1 to exhibit the effect of Q at ω_0 on the response of the filter.

A second-order current-mode universal filter employing k (CCII)s ($k \geq 1$), c capacitors ($c \geq 2$) and r resistors ($r \geq 2$) has k X-terminal currents, and these currents depend on passive element values and frequency.

In fact, the X-terminal current of each CCII in the circuit can be expressed as

$$I_{xj} = \Phi_j(R_1, R_2, \dots, R_r, C_1, C_2, \dots, C_c, f) I_{in} \quad (5.12)$$

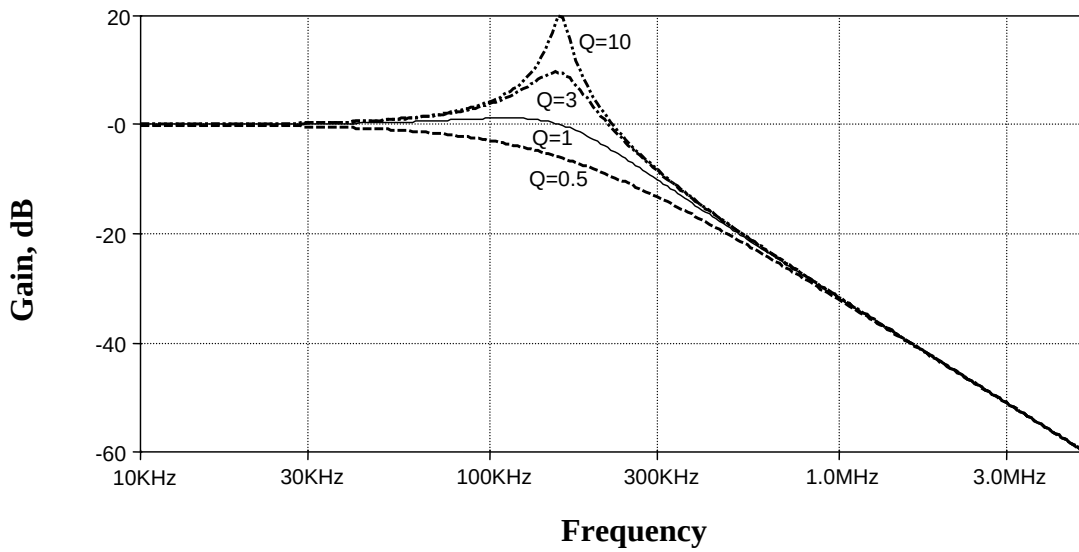


Figure 5.1. The variation of the low-pass response for $Q = 0.5, 1, 3$ and 10 at the resonance frequency of $f_0 = 159.15$ kHz and $K = 1$

where R and C denote resistors and capacitors used in the circuit and I_{xj} ($j = 1, 2, \dots, k$) represents the terminal current of the j th current conveyor.

On the other hand, the current signal limitation of the CCII is given as

$$|I_{xj}| \leq I_M \quad (5.13)$$

where I_M is the maximum allowable terminal current of the (CCII)s.

Also, a universal filter may have extra m current conveyors ($m = l-3$) in which the i -th current conveyor of the filter ($i = 4, 5, \dots, l$) has generally the following current:

$$I_i = \frac{K_{1i}s^2 + K_{2i}s\frac{\omega_o}{Q} + K_{3i}\omega_o^2}{D(s)} I_{in} \quad (5.14)$$

In equation (5.14), K_{ni} ($n = 1, 2, 3$) are real numbers.

Hence, the following restriction for the current in a filter can be given by:

$$\max\left\{|I_{lp}|, |I_{bp}|, |I_{hp}|, |I_{notch}|, |I_{all-pass}|, |I_1|, |I_2|, \dots, |I_m|\right\} \leq I_M \quad (5.15)$$

A current-mode filter has also active element terminal voltages denoted as critical nodes the following functions:

$$V_v = \varphi_v(R_1, R_2, \dots, R_r, C_1, C_2, \dots, C_c, f) I_{in} \quad (5.16)$$

Here, v represents the v -th critical node of the filter. It is important to note that the critical node voltages are limited by the symmetrical power supply voltage given by

$$V_{SS} \leq V_{rv-} \leq V_v \leq V_{rv+} \leq V_{DD} \quad (5.17)$$

Here, V_{rv-} is the minimum possible and V_{rv+} is the maximum possible terminal voltage where CCII can operate without significant distortion.

5.2. Applications of the Presented Theory

A new universal filter is designed and given in Figure 5.2, to test the theory. This filter employs only grounded capacitors and CCII's (four CCII+ and one CCII-), and can be constructed with commercially available active devices AD844s which have maximum allowable X terminal current of $I_M = 5\text{mA}$ and maximum power supply voltage of $V_{DD\text{max}} = 18\text{V}$.

Routine analysis of the circuit in Figure 5.2 gives the following responses:

$$I_{hp} = k_1 \frac{s^2 C_1 C_2 R_1 R_2}{D(s)} I_{in} = I_{x1} \quad (5.18)$$

$$I_{bp} = k_2 \frac{sC_2 R_2}{D(s)} I_{in} = I_{x2} = I_{x4} \quad (5.19)$$

$$I_{lp} = k_3 \frac{1}{D(s)} I_{in} = I_{x5} \quad (5.20)$$

$$I_O = -\frac{1 + sC_2 R_2}{D(s)} I_{in} = I_{x3} \quad (5.21)$$

where $D(s) = s^2 C_1 C_2 R_1 R_2 + sC_2 R_2 + 1$, $k_1 = -C_3 / C_1$, $k_2 = R_1 / R_2$ and $k_3 = -R_1 / R_3$.

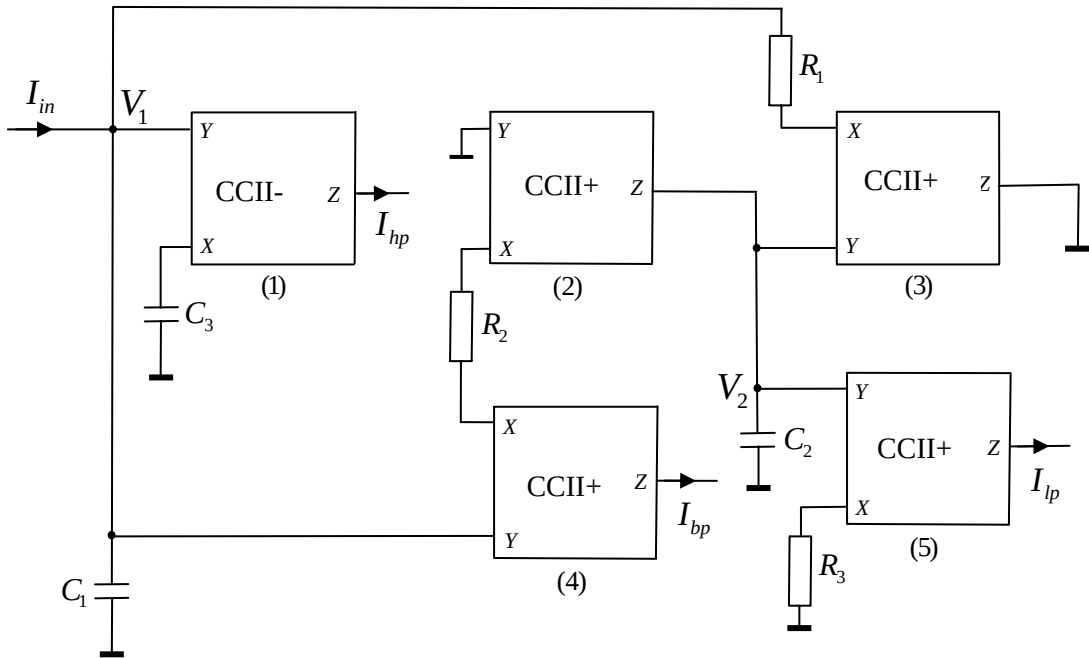


Figure 5.2. A universal current-mode filter example given to exhibit its signal limitations

Note that for $k_1 = -k_2 = k_3 = -1$ and interconnection of the relevant output currents, notch and all-pass responses are also obtained.

$$I_{notch} = I_{lp} + I_{hp} \quad (5.22)$$

$$I_{all-pass} = I_{lp} + I_{bp} + I_{hp} \quad (5.23)$$

The parameters ω_0 and Q of the filter example are found to be

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}} \quad (5.24)$$

$$Q = \sqrt{\frac{C_1 R_1}{C_2 R_2}} \quad (5.25)$$

The magnitudes of the X terminal currents of the filter in Figure 5.2 at $\omega = \omega_o$ are calculated as

$$|I_{x1}| = Q|k_1 I_{in}| \quad (5.26)$$

$$|I_{x2}| = |I_{x4}| = |k_2 I_{in}| \quad (5.27)$$

$$|I_{x3}| = \sqrt{Q^2 + 1}|I_{in}| \quad (5.28)$$

$$|I_{x5}| = Q|k_3 I_{in}| \quad (5.29)$$

Therefore, the input current range of the filter in Figure 5.2 for high Q is computed as

$$I_{in} \leq \min \left\{ \frac{1}{|k_1|Q}, \frac{1}{|k_2|}, \frac{1}{|k_3|Q}, \frac{1}{\sqrt{Q^2 + 1}} \right\} \times 5\text{mA} = I_{inC \max} \quad (5.30)$$

Here, $I_{inC \max}$ is the limit due to maximum allowable terminal currents of the CCIIs of the filter.

The critical node voltages V_1 and V_2 of the filter in Figure 5.2 is calculated as follows:

$$V_1 = \frac{sC_2 R_1 R_2}{s^2 C_1 C_2 R_1 R_2 + sC_2 R_2 + 1} I_{in} \quad (5.31)$$

$$V_2 = -\frac{V_1}{sC_2 R_2} \quad (5.32)$$

In $j\omega$ domain, the magnitudes of the node voltages in equations (5.31) and (5.32) $\omega = \omega_o$ become

$$|V_1| = R_1 |I_{in}| \quad (5.33)$$

$$|V_2| = \frac{R_1}{\omega_0 C_2 R_2} |I_{in}| = QR_1 |I_{in}| \quad (5.34)$$

As a result, considering $V_k (k = 1, 2) \leq V_r$, the following terminal current limitations must be satisfied:

$$|I_{in}| \leq \min \left\{ \frac{V_r}{R_1}, \frac{V_r}{QR_1} \right\} = I_{inV \max} \quad (5.35)$$

where $I_{inV \max}$ is the limit due to terminal voltages of the active element of the filter.

Hence, the following inequality must be satisfied for proper operation of the filter:

$$|I_{in}| \leq \min \{ I_{inC \max}, I_{inV \max} \} \quad (5.36)$$

It is observed from equation (5.36) that the input current I_{in} of the filter is limited in a range. This range can be called as input dynamic range of the filter.

It is important to note that all of the resistors of the filter in Figure 5.2 are connected in series to the X terminals of the (CCII)s thus plus-type second-generation current controlled conveyors (CCCII)s can be replaced for the (CCII)s to obtain electronic tunability [7].

It is difficult to adjust the capacitor values in IC processs but resistive components can be made variable by employing (CCCII)s. In the other word, replacing (CCCII)s for the (CCII)s, the intrinsic resistors R_{xi} ($i = 1, 2, 3, 4, 5$) at the X terminals of the (CCCII)s which can be tuned electronically instead of resistors R_1 , R_2 and R_3 in Figure 5.2.

The current-mode universal filter in Figure 5.2 is simulated with SPICE to exhibit its performance in Figure 5.3. The filter is also constructed experimentally using AD844 ICs of analog devices with DC supply voltages equal to $\pm 15V$. The passive components are selected as $C_1 = C_2 = C_3 = 1nF$ and $R_1 = R_2 = R_3 = 1k\Omega$ to obtain $f_o = 159.15 kHz$ and $Q = 1$. Experimental results of the band-pass response of the filter are shown in Figure 5.4.

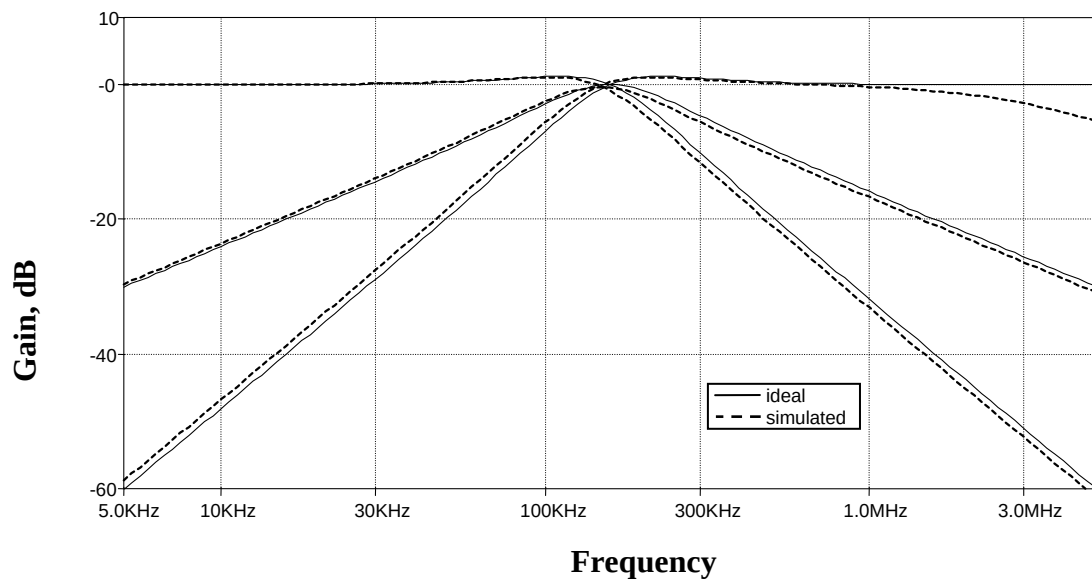


Figure 5.3. Ideal and simulated low-pass, band-pass and high-pass responses of the proposed filter example

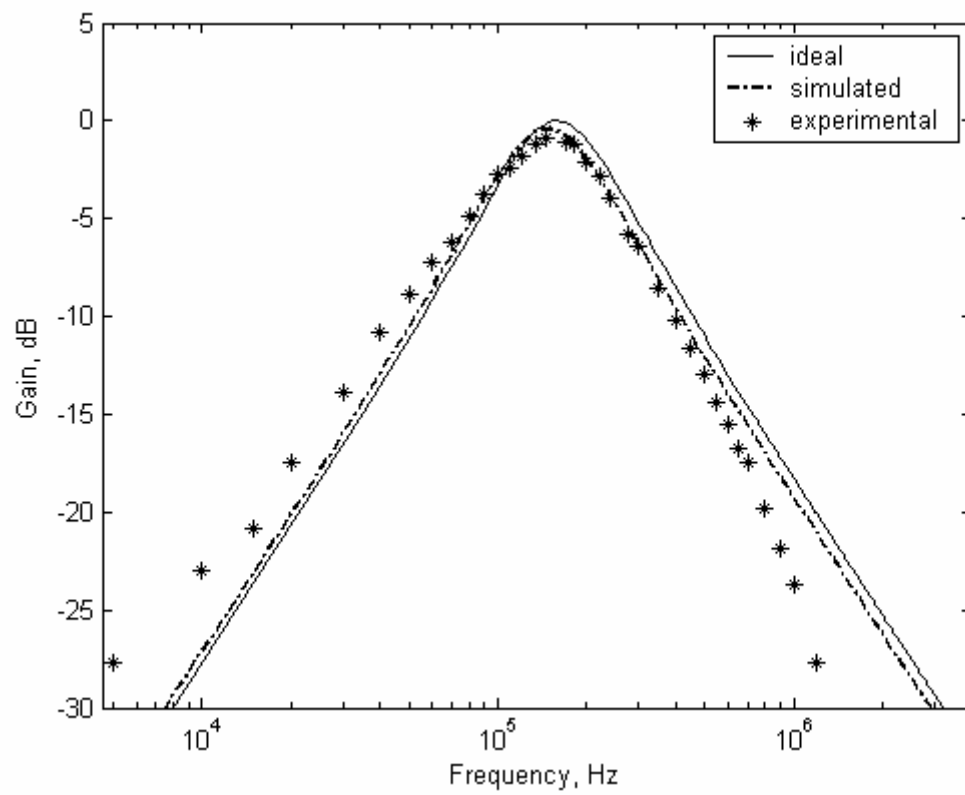


Figure 5.4. Ideal, simulated and experimental band-pass responses of the introduced filter

The ideal and simulated low-pass, band-pass and high-pass responses presented in Figure 5.3 confirm the workability of the current-mode filter.

The ideal and simulated time domain responses of the terminal voltage V_2 of the proposed filter in Figure 5.2 are shown in Figure 5.5 where 2.5 mA peak sinusoidal input current is applied to the proposed filter. As seen from Figure 5.5, since the rated voltage of the proposed filter is about 12 V. The terminal voltage V_2 cannot exceed 12 V.

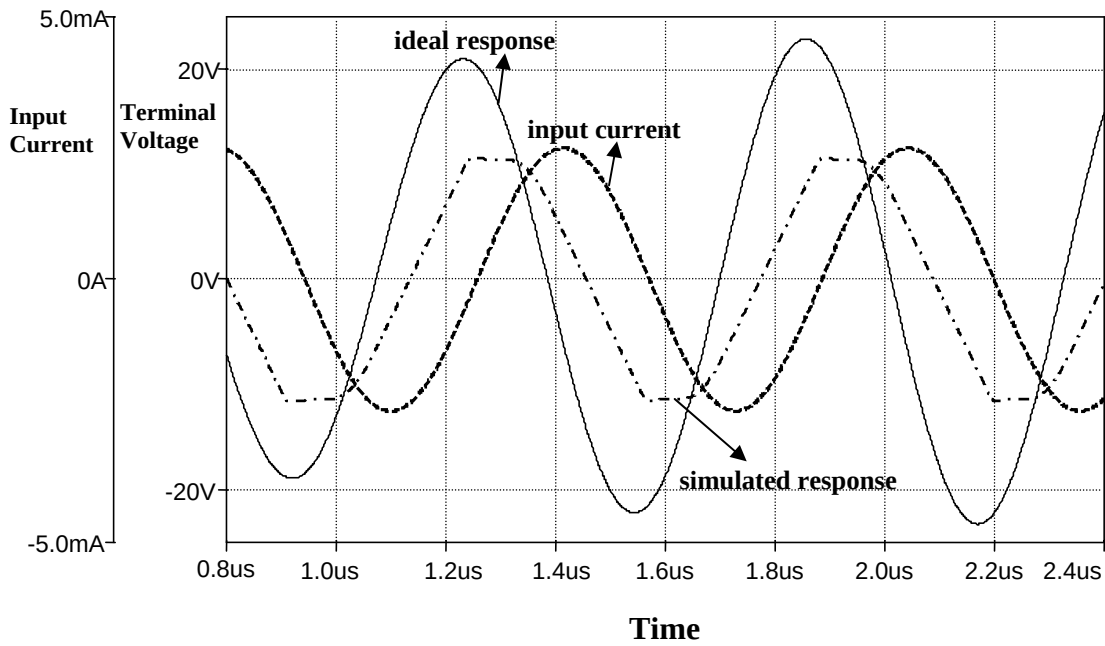


Figure 5.5. Ideal and simulated time domain responses of the terminal voltage V_2 of the proposed filter in Figure 5.2

In Figure 5.5, the passive components are selected as $C_1 = C_2 = 0.1 \text{ nF}$ and $R_1 = 3 \text{ k}\Omega$, $R_2 = 0.3 \text{ k}\Omega$ and $R_3 = 1 \text{ k}\Omega$ to obtain $Q = 3.16$ and $f_o = 1.67 \text{ MHz}$.

5.3. Design Example for the Signal Limitation of the Filter

The parameters ω_o and Q of the filter example in Figure 5.2 are chosen as

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}} = 10^6 \text{ rad/s} \quad (5.37)$$

$$Q = \sqrt{\frac{C_1 R_1}{C_2 R_2}} = 2 \quad (5.38)$$

Hence,

$$C_1 R_1 = 2 \times 10^{-6} \text{ s} \quad (5.39)$$

$$C_2 R_2 = 0.5 \times 10^{-6} \text{ s} \quad (5.40)$$

5.3.1. Limitation from the X Terminal Currents

Equation (5.30) turns to

$$|I_{in}| \leq \min \left\{ \frac{1}{QR_1/R_3}, \frac{1}{R_1/R_2}, \frac{1}{QC_3/C_1}, \frac{1}{\sqrt{Q^2+1}} \right\} I_M = I_{inC \max} \quad (5.41)$$

It is observed from the last term of equation in (5.41) that the maximum value of $I_{inC \max}$ is $I_M / \sqrt{5} = 0.447 I_M$.

Using equations (5.39), (5.40) and (5.41), the following inequalities can be obtained:

$$\frac{R_1}{R_2} \leq 2.23 \Rightarrow R_2 \geq 0.447 R_1 \quad (5.42)$$

$$\frac{2R_1}{R_3} \leq 2.23 \Rightarrow R_3 \geq 0.894 R_1 \quad (5.43)$$

$$C_1 = \frac{2 \times 10^{-6}}{R_1} \text{ F} \quad (5.44)$$

$$C_2 = \frac{0.5 \times 10^{-6}}{R_2} \quad (5.45)$$

$$\frac{2C_3}{C_1} \leq 2.23 \Rightarrow C_3 \leq 1.115 C_1 \quad (5.46)$$

where maximum value of $I_{in} = 2.23 \text{ mA}$ as explained above.

5.3.2. Limitation from the Terminal Voltages

The equation (5.35) can be rewritten as

$$I_{in} \leq \min \left\{ \frac{V_r \cong 12V}{R_1}, \frac{V_r \cong 12V}{2R_1} \right\} = I_{inV \max} \quad (5.47)$$

Consequently, the range of R_1 using (5.47) is found to be

$$R_1 \leq 2.683k\Omega \quad (5.48)$$

In the worst case, $R_1 = 2.683k\Omega$. Therefore, the values of the other passive elements in equation (5.42)-(5.46) are calculated as follows:

$$R_2 \geq 1.2k\Omega \quad (5.49)$$

$$R_3 \geq 2.4k\Omega \quad (5.50)$$

$$C_1 \geq 0.745nF \quad (5.51)$$

$$C_2 \leq 0.416nF \quad (5.52)$$

$$C_3 \leq 0.833nF \quad (5.53)$$

In this section, we proposed a passive element selection method for maximum dynamic range. The given constraints for the passive components of the filter in Figure 5.2 are due to signal limitations of an analog filter. Also, constraints of the passive components of the analog filter stemmed from the stability problems should be taken into account.

In the next chapter, stability problems of the analog filters due to frequency dependent non-ideal gains, using a single pole model, are investigated in detail.

6. STABILITY PROBLEMS IN ANALOG FILTERS

In this chapter, four current-mode analog filters, three of them being universal, employing CCCIs/ CCII are investigated with respect to their stabilities in detail. The presented method can be applied to all the second-order current-mode filters employing active devices.

A theoretical study on the stability of high frequency CFOA integrator is given in [86] in which the current-mirror pole frequency is much greater than the transimpedance pole of the active device and there are other poles at high frequencies. Considering all of the poles of the active devices for stability analysis for a circuit employing active components such as CCs, CCCIs, OAs *etc.* would be more realistic. Nevertheless, for simplicity, a single pole model will only be taken into account for each current gain of the CCCIs. Moreover, the voltage gain pole frequency is assumed to be at a much higher frequency and its effect can be ignored.

The results in this chapter should not be used to make a binary decision on the stabilities of the corresponding circuits. However, the analysis gives a rough idea about the stability performance. Taking more poles and possible zeros may change the stability decision. In fact, an unstable circuit with a single pole model can behave as stable and vice versa.

6.1. Description of the Developed Analog Filters

Two universal current-mode analog filters employing only CCCIs are introduced in this section to make the stability problems of the filters understandable. Straightforward analysis of the circuit in Figure 6.1 gives the following filter TFs:

$$\frac{I_{LP}}{I_{in}} = \frac{1}{D(s)} \quad (6.1)$$

$$\frac{I_{BP}}{I_{in}} = -\frac{sC_2R_{x2}}{D(s)} \quad (6.2)$$

$$\frac{I_{HP}}{I_{in}} = \frac{s^2 C_1 C_2 R_{x1} R_{x2}}{D(s)} \quad (6.3)$$

where $D(s)$ is given as

$$D(s) = s^2 C_1 C_2 R_{x1} R_{x2} + s C_2 R_{x2} + 1 \quad (6.4)$$

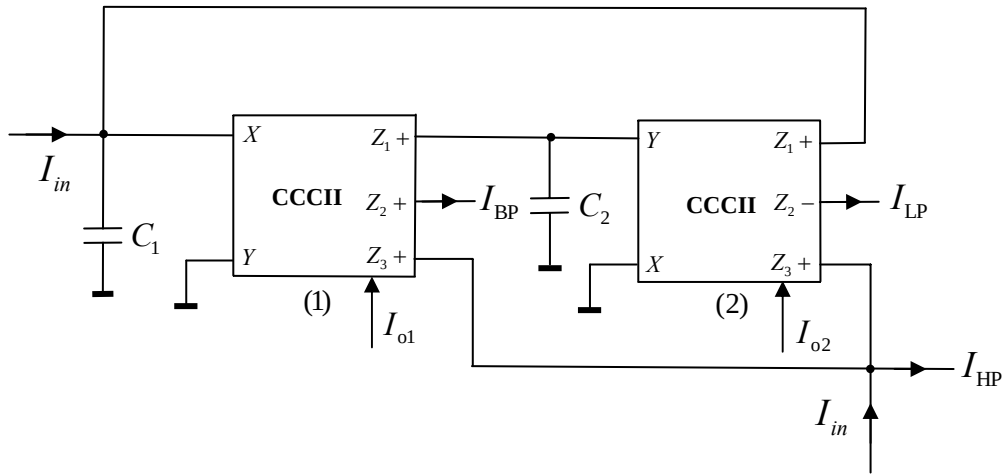


Figure 6.1. The first proposed filter employing only grounded capacitors

If the current gain α is considered, the filter TFs and their denominator $D(s)$ in equation (6.4) convert to

$$\frac{I_{LP}}{I_{in}} = \frac{\alpha_{11} \alpha_{22}}{D(s)} \quad (6.5)$$

$$\frac{I_{BP}}{I_{in}} = -\frac{s C_2 R_{x2} \alpha_{12}}{D(s)} \quad (6.6)$$

$$\frac{I_{HP}}{I_{in}} = \frac{s^2 C_1 C_2 R_{x1} R_{x2} + s C_2 R_{x2} (1 - \alpha_{13}) + \alpha_{11} (\alpha_{21} - \alpha_{23})}{D(s)} \quad (6.7)$$

$$D(s) = s^2 C_1 C_2 R_{x1} R_{x2} + s C_2 R_{x2} + \alpha_{11} \alpha_{21} \quad (6.8)$$

Here, for α_{ij} ($i = 1, 2$) represents the i th CCCII and ($j = 1, 2, 3$) exhibits the j th Z terminal.

Note that notch ($I_{LP} + I_{HP}$) and all-pass ($I_{LP} + I_{BP} + I_{HP}$) filter responses can also be obtained with interconnection of the relevant output currents.

The parameters ω_0 and Q for equation (6.8) are calculated as

$$\omega_0 = \sqrt{\frac{\alpha_{11}\alpha_{21}}{C_1C_2R_{x1}R_{x2}}} \quad (6.9)$$

$$Q = \sqrt{\frac{C_1R_{x1}\alpha_{11}\alpha_{21}}{C_2R_{x2}}} \quad (6.10)$$

Note that all of the active and passive component sensitivities in equations (6.9) and (6.10) equal to 0.5 in magnitudes.

Routine analysis of the filter in Figure 6.2 derived from the filter in Figure 6.1 with $R_{x3} = R_{x1}/2$ gives the following filter TFs:

$$H_{A1}(s) = \frac{I_{LP}}{I_{in}} = -\frac{\omega_0^2 \alpha_{12} \alpha_{22}}{D_n(s)} \quad (6.11)$$

$$H_{A2}(s) = \frac{I_{BP}}{I_{in}} = 2 \frac{s \frac{\omega_0}{Q} \alpha_{31}}{D_n(s)} \quad (6.12)$$

$$H_{A3}(s) = \frac{I_{HP}}{I_{in}} = \frac{s^2 + s \frac{\omega_0}{Q} (1 - \alpha_{13}) + \omega_0^2 \alpha_{12} (\alpha_{21} - \alpha_{23})}{D_n(s)} \quad (6.13)$$

$$H_{A4}(s) = \frac{I_{NF}}{I_{in}} = \frac{s^2 + s \frac{\omega_0}{Q} (1 - \alpha_{11}) + \omega_0^2 \alpha_{12} \alpha_{21}}{D_n(s)} \quad (6.14)$$

$$H_{A5}(s) = \frac{I_{AP}}{I_{in}} = -\frac{s^2 - s \frac{\omega_0}{Q} (2\alpha_{32} - 1) + \omega_0^2 \alpha_{12} \alpha_{21}}{D_n(s)} \quad (6.15)$$

where $H_{Ai}(s)$ for $i = 1, 2, 3, 4, 5$ corresponds to low-pass, band-pass, high-pass, notch and all-pass analog filter TFs, respectively.

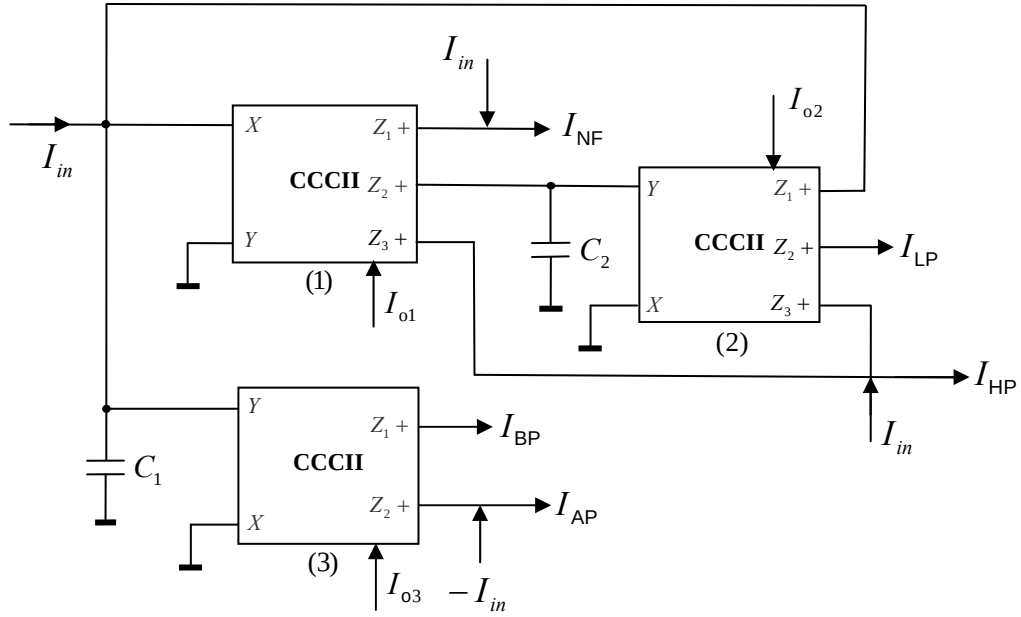


Figure 6.2. The second presented filter derived from the filter in Figure 6.1 for simultaneously realizing low-pass, band-pass, high-pass, notch and all-pass filter responses

Here, the denominator $D_n(s)$ for the filter in Figure 6.2 are calculated as

$$D_n(s) = s^2 + s \frac{\omega_o}{Q} + \omega_o^2 \alpha_{12} \alpha_{21} \quad (6.16)$$

It is important to note that the denominators of the filters in Figures 6.1 and 6.2 are equivalent.

6.2. Stability Problems of the Proposed Filters

If a coefficient of the denominator of a filter is negative, the filter has a stability problem. The denominator of the filter proposed in [49] is given as follows:

$$D_n(s) = s^2 C_1 C_2 R_1 R_2 + s C_2 (R_2 \alpha_4 \beta_4 + R_1 (1 - \beta_3)) + \alpha_4 \beta_3 \beta_4 \quad (6.17)$$

It can be observed that the equation in (6.17) may have stability problem for

$$\beta_3 > 1 + R_2 \alpha_4 \beta_4 / R_1 \quad (6.18)$$

As a result, the ratio of R_2 / R_1 must be chosen carefully to obtain stable filter responses. It is assumed that $\alpha_4 = 1 + \varepsilon_1$, $\beta_3 = 1 + \varepsilon_2$, $\beta_4 = 1 + \varepsilon_3$ where ε_i ($i = 1, 2, 3$) is assumed to be

$$|\varepsilon_i| \leq 0.1 \quad (6.19)$$

In the worst case, $\alpha_4 = 0.9$, $\beta_3 = 1.1$ and $\beta_4 = 0.9$ thus $R_2 / R_1 \geq 0.124$ must be satisfied for stable filter responses.

In general, the denominator similar to equation (6.17) can be written as follows:

$$D_n(s) = s^2 + s\left(\frac{\omega_{\text{on}}}{Q_n} - n_o\right) + \omega_{\text{on}}^2 \quad (6.20)$$

Here,

$$\omega_{\text{on}}^2 = \alpha_4 \beta_3 \beta_4 / C_1 C_2 R_1 R_2 \quad (6.21)$$

$$\omega_{\text{on}} / Q_n = (R_2 \alpha_4 \beta_4 + R_1) / C_1 R_1 R_2 \quad (6.22)$$

$$n_o = \beta_3 / C_1 R_2 \quad (6.23)$$

The additional term n_o in equation (6.23) comes due to non-ideal voltage gain β_3 . $D_n(s)$ in equation (6.20) can also be expressed as

$$D_n(s) = s^2 + s \frac{\omega_{\text{on}}}{Q_{\text{new}}} + \omega_{\text{on}}^2 \quad (6.24)$$

where $Q_{\text{new}} = Q_n \omega_{\text{on}} / (\omega_{\text{on}} - n_o Q_n)$. If Q_{new} is negative or $\omega_{\text{on}} < n_o Q_n$, the filter exhibits unstable responses.

The well-known methods to test the stability of the filter characteristics are Routh's stability criterion [94]. To apply the stability test, a single pole model for each current gain,

$\alpha_{11} = \alpha_1 = \alpha_{10} / (1 + \tau_1 s)$ and $\alpha_{21} = \alpha_2 = \alpha_{20} / (1 + \tau_2 s)$, is replaced for $D(s)$ in equation (6.8). Here, the poles depending on the fabrication of the device $\omega_{\alpha 1} = 1/\tau_1$ and $\omega_{\alpha 2} = 1/\tau_2$ correspond to α_1 and α_2 , respectively. Also, α_{10} and α_{20} are in the vicinity of unity, and are the DC current gains of α_1 and α_2 , respectively. On the other hand, in reality, each current gain has k zeros and l poles. Therefore, a current gain can be represented by

$$\alpha(s) = \alpha_0 \frac{\prod_{i=1}^k (1 + \tau_{zi} s)}{\prod_{i=1}^l (1 + \tau_{pi} s)} \quad (6.25)$$

Here, k and l are integer numbers besides $l \geq k$. Specifically, for $k=0$ and $l=0$, the corresponding numerator and denominator are taken unity, respectively.

However, we use a single pole model for each current gain to simplify the stability analysis. Therefore, $\alpha(s)$ in equation (6.25) converts

$$\alpha(s) = \frac{\alpha_0}{1 + \tau s} \quad (6.26)$$

Also, $D(s)$ in equation (6.8) turns to

$$D(s) = s^2 C_1 C_2 R_{x1} R_{x2} + s C_2 R_{x2} + \frac{\alpha_{10}}{1 + \tau_1 s} \cdot \frac{\alpha_{20}}{1 + \tau_2 s} \quad (6.27)$$

Therefore, $D(s) = 0$ in equation (6.27) converts

$$\{(1 + \tau_1 s)(1 + \tau_2 s)\} \left\{ s^2 + s \frac{\omega_0}{Q} \right\} + \omega_0^2 \alpha_{10} \alpha_{20} = 0 \quad (6.28)$$

We assume identical conveyors such that $\tau_1 = \tau_2 = \tau$ and $\alpha_{10} = \alpha_{20} = \alpha_0$.

Routh's stability criterion can be applied to $a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0 = 0$ in equation (6.28) as follows:

$$\begin{cases} s^4 & a_4 & a_2 & a_0 \\ s^3 & a_3 & a_1 & \\ s^2 & b & a_0 & \\ s^1 & c & & \\ s^0 & a_0 & & \end{cases} \quad (6.29)$$

Here,

$$a_4 = \tau^2 \quad (6.30)$$

$$a_3 = 2\tau + \frac{\omega_0}{Q} \tau^2 \quad (6.31)$$

$$a_2 = 1 + \frac{\omega_0}{Q} 2\tau \quad (6.32)$$

$$a_1 = \frac{\omega_0}{Q} \quad (6.33)$$

$$a_0 = \omega_0^2 \alpha_0^2 \quad (6.34)$$

It is known that the terms b and c in equation (6.29) must be positive real numbers for stable filter responses. Therefore,

$$b = \frac{a_2 a_3 - a_1 a_4}{a_3} > 0 \quad (6.35)$$

$$c = \frac{a_1 b - a_0 a_3}{b} > 0 \quad (6.36)$$

6.3. Further Example for Stability Analysis

Now we consider the circuit in Figure 6.3, for this circuit, the parameters ω_0 and Q are given by

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_{x1} R_{x2}}} \quad (6.37)$$

$$Q = \sqrt{\frac{C_1 R_{x1}}{C_2 R_{x2}}} \quad (6.38)$$

It is important to note that the parameters in equations (6.37) and (6.38) can be chosen arbitrarily in an IC process by changing only bias currents externally for fixed valued capacitors.

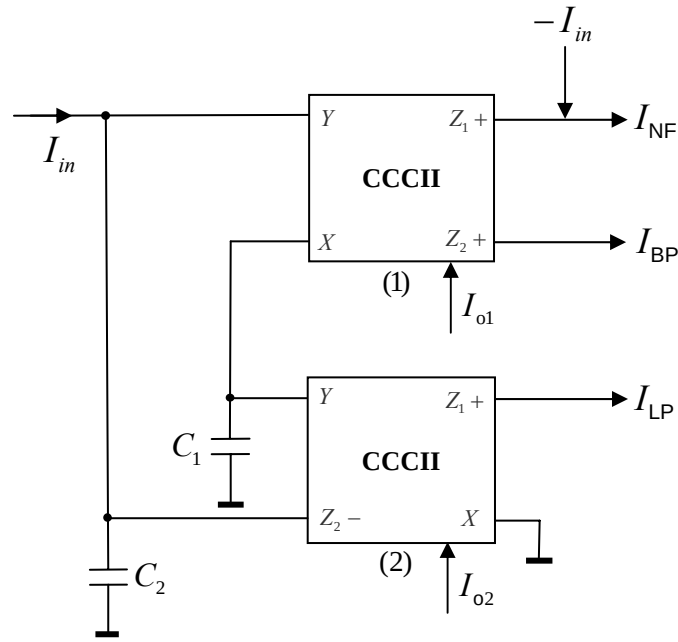


Figure 6.3. The third developed filter employing only grounded capacitors

If non-ideal current gains are taken into account, the TFs of the filter in Figure 6.3 using the parameters ω_o and Q in equations (6.37) and (6.38) turn to

$$\frac{I_{LP}}{I_{in}} = \frac{\omega_o^2 \alpha_{21}}{\Delta(s)} \quad (6.39)$$

$$\frac{I_{BP}}{I_{in}} = \frac{C_1}{C_2} \frac{s \frac{\omega_o}{Q} \alpha_{12}}{\Delta(s)} \quad (6.40)$$

$$\frac{I_{NF}}{I_{in}} = - \frac{s^2 + s \frac{\omega_o}{Q} \left(1 - \frac{C_1}{C_2} \alpha_{11} \right) + \omega_o^2 \alpha_{22}}{\Delta(s)} \quad (6.41)$$

Here,

$$\Delta(s) = s^2 + s \frac{\omega_o}{Q} + \omega_o^2 \alpha_{22} \quad (6.42)$$

If $C_1 = C_2$ is chosen, the following universal filter responses can be obtained with interconnection of the relevant output currents in addition to low-pass, band-pass and notch responses.

High-pass response ($I_{HP} = I_{LP} + I_{NF}$) can be realized.

All-pass response ($I_{AP} = I_{BP} + I_{NF}$) can be realized.

Taking $\Delta(s) = 0$ in equation (6.42) and replacing a single pole model for $\alpha_{22} = \alpha_o / (1 + s\tau)$ gives the following equation:

$$s^3 \tau + s^2 \left(1 + \tau \frac{\omega_o}{Q} \right) + s \frac{\omega_o}{Q} + \omega_o^2 \alpha_o = 0 \quad (6.43)$$

The pole $\omega_\alpha = 1/\tau$ depending on the fabrication of the device can be called -3dB cut-off frequency of the α_{22} . Routh's stability criterion [94] can be applied to equation (6.43) to test the stability of the proposed filter. Hence,

$$\begin{aligned} s^3 &\Rightarrow \tau & \frac{\omega_o}{Q} \\ s^2 &\Rightarrow 1 + \tau \frac{\omega_o}{Q} & \omega_o^2 \alpha_o \\ s^1 &\Rightarrow \frac{\omega_o}{Q} + \left(\frac{\omega_o}{Q} \right)^2 \tau - \omega_o^2 \alpha_o \tau > 0 \\ s^0 &\Rightarrow \omega_o^2 \alpha_o \end{aligned}$$

It is obvious that all values of $\tau = 1/\omega_\alpha$, $1 + \omega_o \tau / Q$ and $\omega_o^2 \alpha_o$ are all greater than zero thus $\omega_o Q (\alpha_o - 1/Q^2) < 1/\tau = \omega_\alpha$ must be chosen for stable filter responses. In other words, for $Q \leq 1/\sqrt{\alpha_o}$ the filter can always realize stable filter responses. Otherwise, for $Q \gg 1$, ω_α must be greater than $\omega_o Q$ for stable filter responses.

In general, using a single pole model, the denominator $D(s)$ of a second-order filter using CCCIs due to frequency dependent current gains can be written as follows:

$$D(s) = s^2 \sum_{j=1}^a \left(\prod_{i=1}^n \left(\frac{\pm \alpha_{oij}}{1 + \tau_i s} \right) \right) + s \frac{\omega_o}{Q} \sum_{j=1}^b \left(\prod_{i=n+1}^{n+m} \left(\frac{\pm \alpha_{oij}}{1 + \tau_i s} \right) \right) + \omega_o^2 \sum_{j=1}^c \left(\prod_{i=n+m+1}^{n+m+r} \left(\frac{\pm \alpha_{oij}}{1 + \tau_i s} \right) \right) \quad (6.44)$$

Hence, as explained before $-\alpha_{oij}$ ($i = 1, 2, \dots, n+m+r$) may cause stability problems. Also, it is assumed that $a \geq 1$, $b \geq 1$, $c \geq 1$, $n \geq 1$, $m \geq 1$ and $r \geq 1$ otherwise the terms are taken unity as follows:

$$\sum_{j=1}^a \left(\prod_{i=1}^n \left(\frac{\pm \alpha_{oij}}{1 + \tau_i s} \right) \right) = 1 \quad (6.45)$$

$$\frac{\omega_o}{Q} \sum_{j=1}^b \left(\prod_{i=n+1}^{n+m} \left(\frac{\pm \alpha_{oij}}{1 + \tau_i s} \right) \right) = 1 \quad (4.46)$$

$$\sum_{j=1}^c \left(\prod_{i=n+m+1}^{n+m+r} \left(\frac{\pm \alpha_{oij}}{1 + \tau_i s} \right) \right) \quad (4.47)$$

Also, the order k of this filter as known is $k = 2 + \max\{n, m, r\}$. Also, equation (6.44) can be expressed as

$$D(s) = a_k s^k + a_{k-1} s^{k-1} + \dots + a_1 s + a_0 \quad (6.48)$$

Using MATLAB program, the stable and unstable regions of the first developed filter with respect to two combinations of three parameters k , α_o and Q are depicted in Figures 6.4 – 6.6 in which $k = \omega_{\alpha i} / \omega_o = 1/(\tau \omega_o)$, $\alpha_{10} = \alpha_{20} = \alpha_o$, $\omega_{\alpha 1} = \omega_{\alpha 2} = \omega_\alpha$ or $\tau_1 = \tau_2 = \tau$ and $\omega_o = 5 \times 10^5$ rad/s are chosen.

Note that ω_o and Q values put restriction on possible element selection C_1 , C_2 , R_{x1} and R_{x2} .

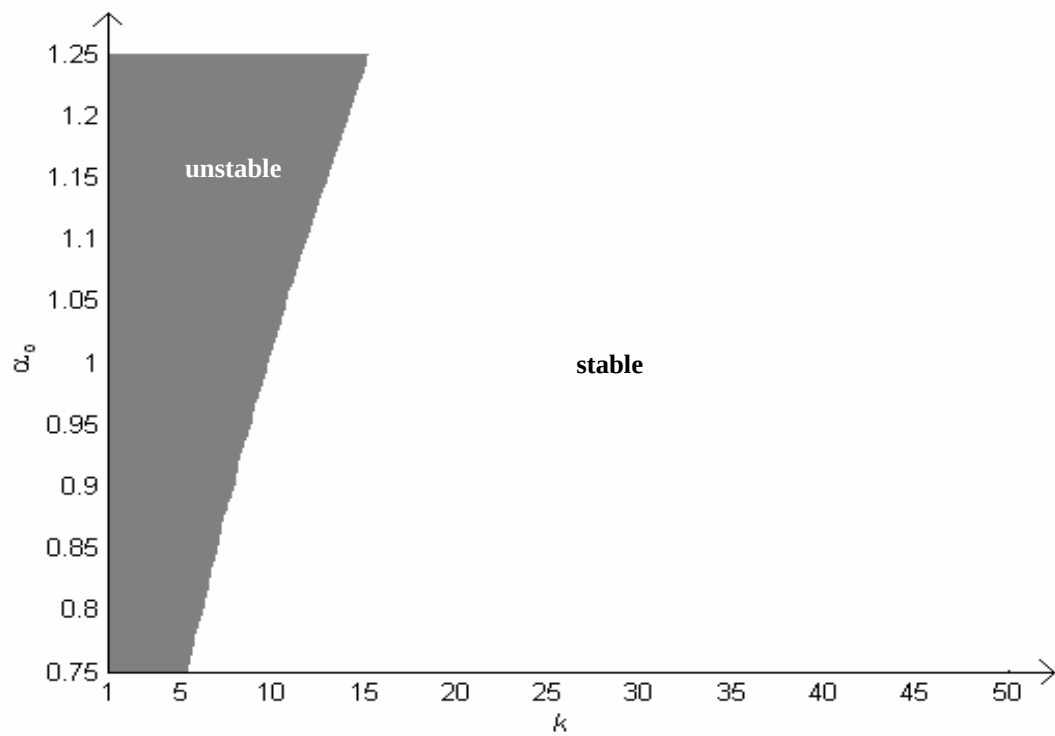


Figure 6.4. Stable region with respect to variations of k and α_0 where $Q=5$

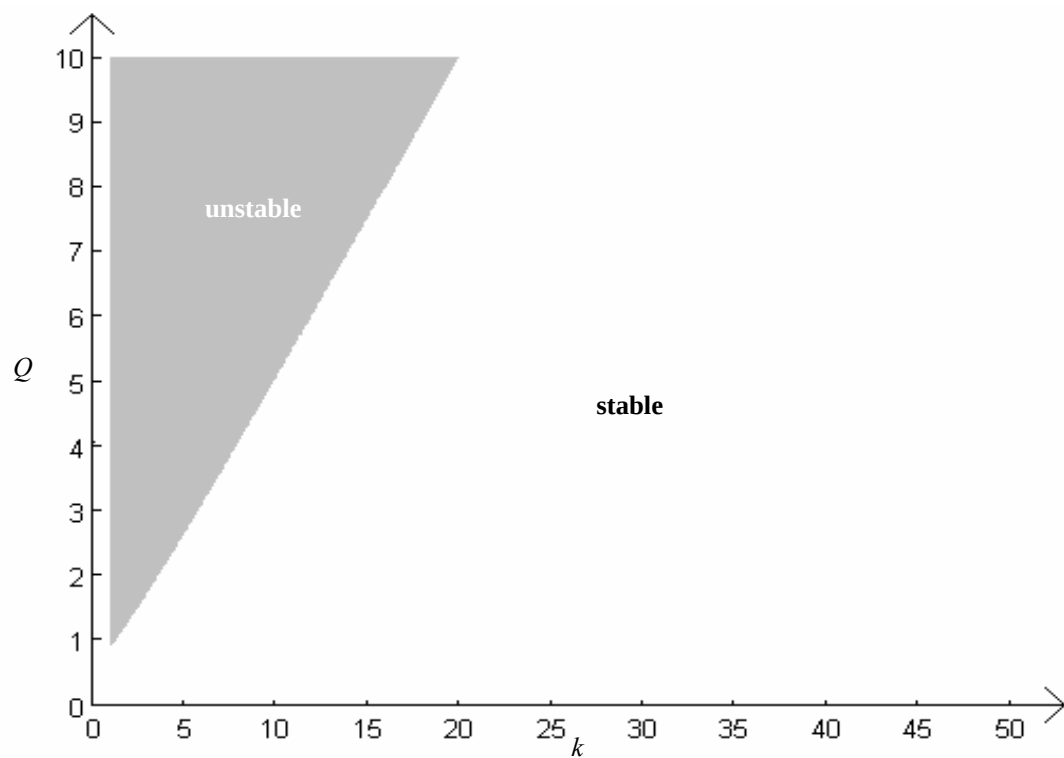


Figure 6.5. Stable region with respect to variations of k and Q where $\alpha_0=1$

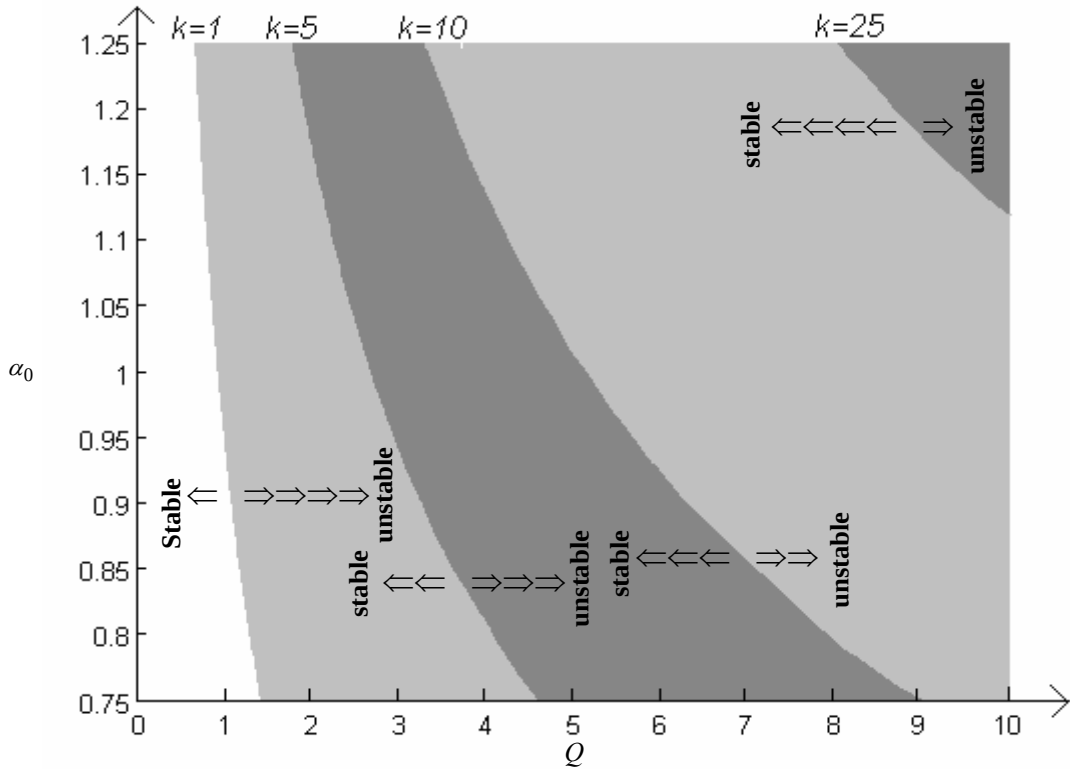


Figure 6.6. Stable region with respect to variations of Q and α_0 where $k = 1, 5, 10$ and 25

From Figure 6.4, assuming a straight line between the stable and unstable regions, a linear relation could be given as $k > 20\alpha_0 - 10$ in order to satisfy stability.

From Figure 6.5, the stable and unstable regions are nearly separated with a line and the linear relation could be written as $k > 2Q$ to provide stability.

From Figure 6.6, for the given intervals, the relationship among k , Q and α_0 that define the stable regions seems to be highly non-linear. For simplicity, by taking a linear relationship, it may be approximated as $k > 4\alpha_0 Q - 2Q$ for stability.

In summary, using Routh's stability criterion, the $D(s) = 0$ in equation (6.45) is tested with respect to the parameters α_0 , k and Q . It is observed from Figures 6.4-6.6 that the larger k and the smaller α_0 and Q , the more stable filter responses can be obtained. Also, it can be concluded that (from Figures 6.4 and 6.5) that for $\alpha_0 \leq 0.5$, the filter is always stable without regarding the values of k and Q . Nonetheless, for $\alpha_0 = 0.5$ and $Q =$

10, one should select $k > 5$ instead of $k > 0$ due non-linearity. One should chose $k > 20$ for $\alpha_0 = 1$ and $Q = 10$.

6.4. Stability Analysis Using Bode Plot

A filter TF can be represented by

$$T(s) = \frac{G(s)}{1 + G(s)H(s)} = K \frac{a_e s^e + a_{e-1} s^{e-1} + \dots + a_1 s + a_0}{b_f s^f + b_{f-1} s^{f-1} + \dots + b_1 s + b_0} \quad (6.49)$$

where $e \leq f$.

$G(s)H(s)$, $G(s)$ and $H(s)$ in equation (6.49) can be found as

$$G(s)H(s) = \frac{b_0}{b_f s^f + b_{f-1} s^{f-1} + \dots + b_2 s^2 + b_1 s} \quad (6.50)$$

$$G(s) = K \frac{a_e s^e + a_{e-1} s^{e-1} + \dots + a_1 s + a_0}{b_f s^e + b_{f-1} s^{f-1} + \dots + b_2 s^2 + b_1 s} \quad (6.51)$$

$$H(s) = \frac{1}{K} \frac{b_0}{a_e s^e + a_{e-1} s^{e-1} + \dots + a_1 s + a_0} \quad (6.52)$$

The stability of the TF of the simple circuit in Figure 6.7 is tested by applying Bode stability analysis [94] on $G(s)H(s)$ in equation (6.50) with simultaneously drawing magnitude and phase responses of $G(s)H(s)$ and taking $\tau_\alpha = \tau_\beta = \tau_\gamma = \tau$ for simplicity.

Straightforward analysis of the filter in Figure 6.7 using a single pole model gives the following filter TF:

$$\frac{I_{LP}}{I_{in}} = \frac{\frac{\alpha_o}{1 + s\tau}}{s^2 C_1 C_2 R_1 R_2 + s(C_1 + C_2)R_2 + \frac{\beta_o}{1 + s\tau} \frac{\gamma_o}{1 + s\tau}} \quad (6.53)$$

Note that the DO-CCII in Figure 6.7 has $I_{z+} = \alpha I_x$, $I_{z-} = -\gamma I_x$, $I_y = 0$ and $V_x = \beta V_y$.

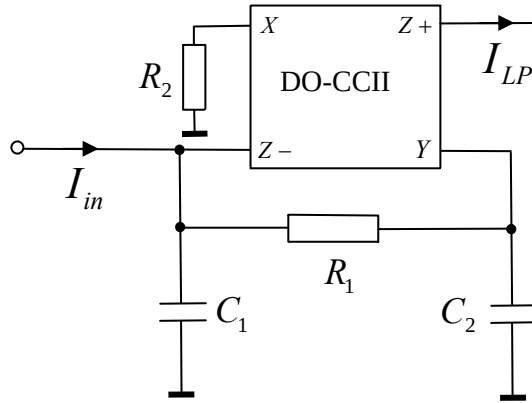


Figure 6.7. The filter employing a minimum number of elements with high output impedance low-pass response

The denominator of (6.53) can be rewritten as

$$D(s) = \left(s^2 C_1 C_2 R_1 R_2 + s(C_1 + C_2)R_2 + \frac{\beta_o}{1 + s\tau} \frac{\gamma_o}{1 + s\tau} \right) = 0 \quad (6.54)$$

Thus, using (6.54), the following polynomial can be obtained:

$$P(s) = (1 + s\tau)^2 (s^2 C_1 C_2 R_1 R_2 + s(C_1 + C_2)R_2) + \beta_o \gamma_o = 0 \quad (6.55)$$

As a result, $P(s)$ in (6.55) converts

$$P(s) = a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_o = 0 \quad (6.56)$$

Here,

$$\left. \begin{aligned} a_4 &= \tau^2 C_1 C_2 R_1 R_2 \\ a_3 &= \tau^2 R_2 (C_1 + C_2) + 2\tau C_1 C_2 R_1 R_2 \\ a_2 &= 2\tau R_2 (C_1 + C_2) + C_1 C_2 R_1 R_2 \\ a_1 &= R_2 (C_1 + C_2) \\ a_o &= \beta_o \gamma_o \end{aligned} \right\} \quad (6.57)$$

Hence, $G(s)H(s)$ is found as

$$G(s)H(s) = \frac{a_0}{s(a_4s^3 + a_3s^2 + a_2s + a_1)} \quad (6.58)$$

where a_i ($i = 0, 1, \dots, 4$) is given in equation (6.56).

If Bode stability criterion [94] is applied to $H(s)G(s)$, the stability of the circuit in equation (6.56) can be determined.

The gain and phase margins are calculated for different values of R_iC_i ($i = 1, 2$ and for simplicity $C_1R_1 = C_2R_2$) and τ and are given in Figures 6.8 and 6.9, respectively. By evaluating the given gain and phase margin values, the stable and unstable regions are determined as shown in Figure 6.10. The system is stable in the right side of the line.

It is seen that the system is stable for larger values of R_iC_i and smaller values of τ . The stability regions in Figure 6.10 give us an insight on how to choose the system parameters.

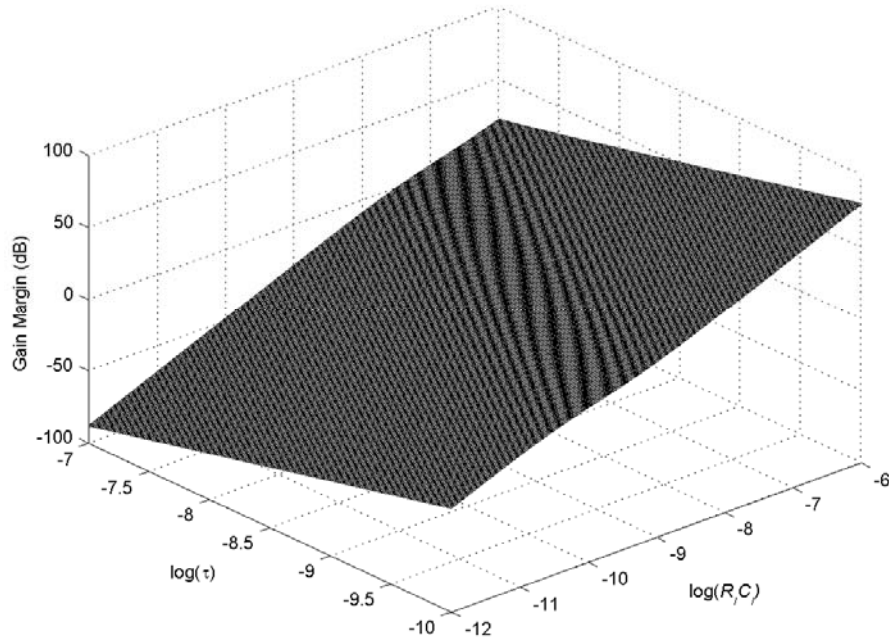


Figure 6.8. Gain margins

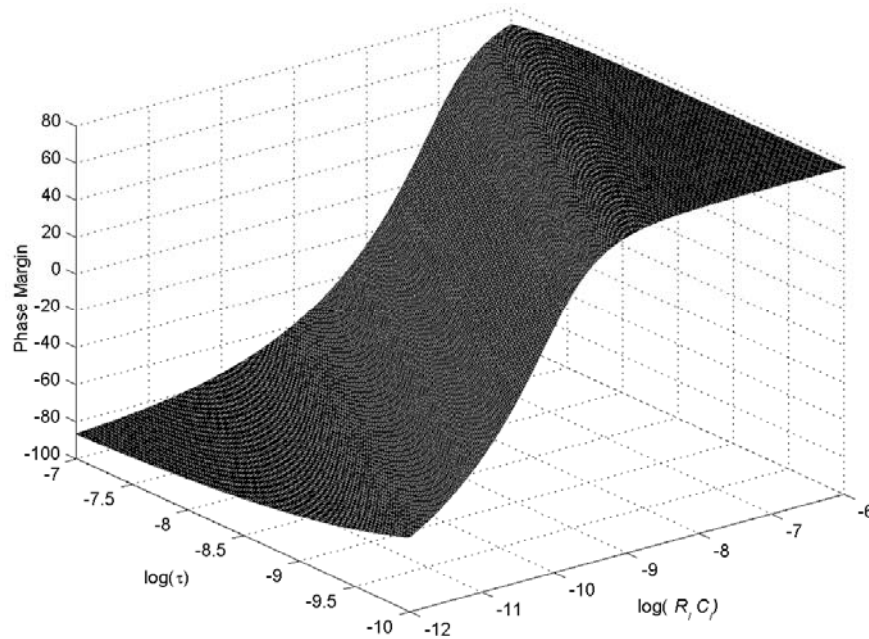


Figure 6.9. Phase margins

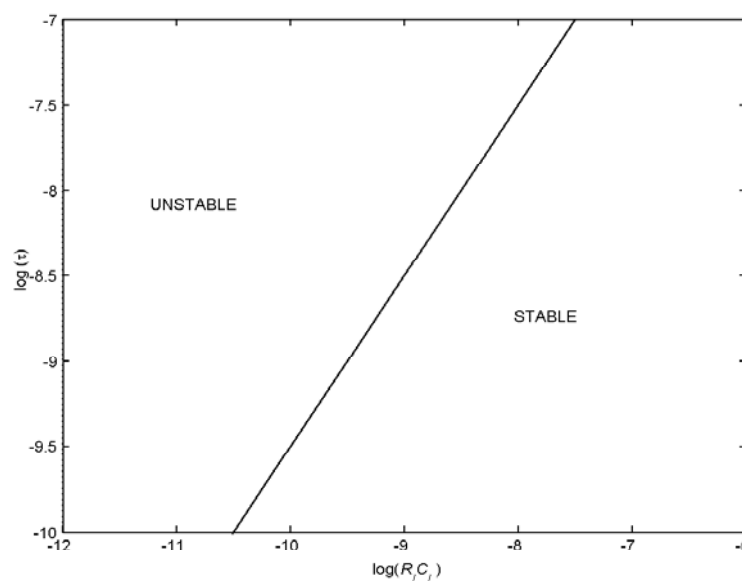


Figure 6.10. Stability regions

In general, we are not only interested in the systems that are stable, but also the systems that have a certain degree of stability. An important insight for the stability of the closed-loop system can be achieved by analyzing the gain and phase margins of the system. For this purpose, $R_1C_1 = R_2C_2 = 10^{-6}$ s is chosen and Bode plots are given for different values of $\tau = 10^{-7}$, 10^{-8} , 10^{-9} and 0 s as in Figure 6.11.

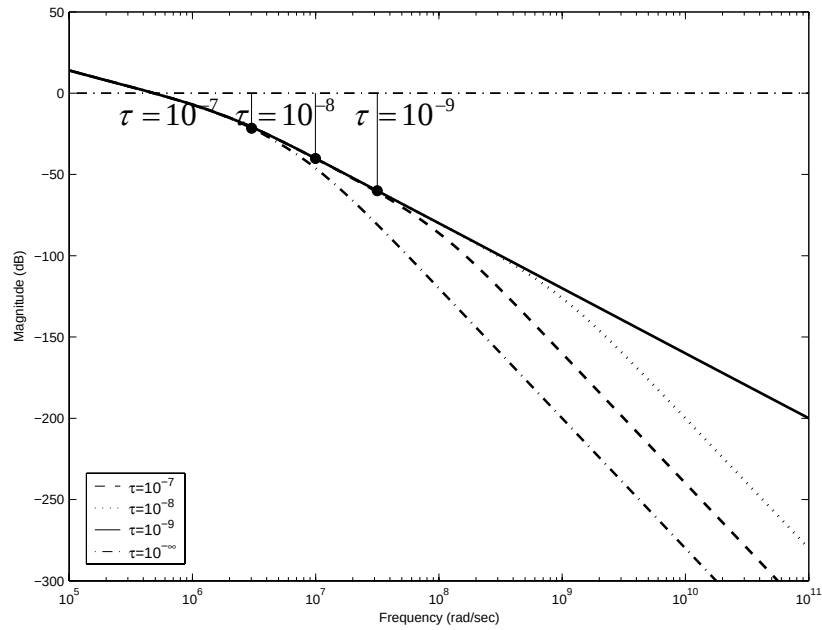


Figure 6.11. Bode magnitude plot

The phase crossover frequencies calculated as $\omega_{pc}=3.02 \times 10^6$, 9.95×10^6 , 3.16×10^7 and $+\infty$ rad/s for $\tau = 10^{-7}$, 10^{-8} , 10^{-9} and 0 s, respectively. For the ideal case, $\tau = 0$ s, the gain margin is infinite in decibel, which means that the value of the loop gain can be theoretically increased to infinity before instability occurs. Also, the phase plot is given in Figure 6.12.

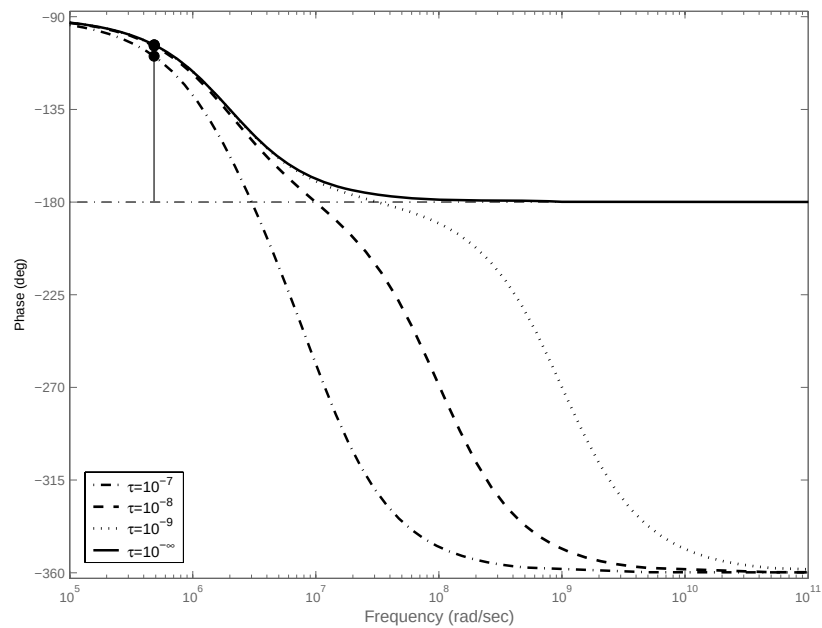


Figure 6.12. Bode phase plot

The gain crossover frequencies are $\omega_{gc} = 4.85 \times 10^5$ rad/s for all τ values. The gain and phase margin values increase as the value of τ decreases. Thus, the system is relatively more stable for smaller τ values.

In this chapter, an approach for the evaluation of stability of the filters is presented. The given theory can be applied to other filters to obtain an understanding of stability properties of a given topology. The results are therefore expected to be useful as a guide for the selection of passive components, cut-off frequencies of the active device and other parameters of the filter. However, the results should not be used as a final decision for the stability since a dominant pole approach is followed and higher order poles/ zeros as well as parasitic poles/ zeros are not taken into account.

VII. CONCLUSIONS

Current conveyors are widely used to design analog circuits as an alternative to operational amplifier.

In this thesis, restrictions of the current conveyors are shown on analog filter circuits and inductance simulator examples that are building blocks for analog signal processing systems.

The non-idealities directly affect the design constraints. In general, for a given topology, the engineer has theoretically many degrees of freedom to select the passive element values but non-ideality limitations may restrict the selection set.

Parasitic impedances and the poles of the transfer function are one of the important causes for the non-ideal behavior.

The work done in this thesis can be summarized as follows:

In this thesis, several analog filter topologies and synthetic inductors are analyzed in terms of current conveyor restrictions and their advantages and disadvantages are comparatively shown. Guidelines are given to evaluate and compare performance parameters of the designed circuits.

A new method for evaluation and comparison of the terminal current limitations of simulated inductors are given. Five simulated inductors are compared and the results are given in tabular form. It is found that some topologies are superior to others. The presented method can be used to evaluate other inductance simulators as well.

Certain modifications are made on the classical current conveyor and some new modified current conveyors and current feedback op-amps are presented. Some experiments carried out to test the functionality of several other given circuits. Some new topologies with these novel elements are also presented.

It is observed that a suitable set of passive element values must be chosen for a specific circuit to overcome signal swing limitations of the internal nodes. It is illustrated how to choose this specific set.

The effects of parasitic impedances are extensively studied and it is found that Z and Y terminal parasitic resistances are reduced dramatically by using the parasitic impedance compensation technique shown in the thesis. From this part, several important conclusions are derived and explained in the text.

Graphical illustrations are given to help the circuit designer, for passive element selection and to prevent instability due to parasitic poles.

The approach (the proposed and derived methods) in the thesis can be applied to the designs with active elements other than current conveyors as long as simple and accurate models for these active elements are available. The circuit designer can therefore optimize circuit parameters and improve the design.

It is concluded that;

- We observed that the CCII/CCCII based filters and inductor simulators exhibit good performances at high frequencies if only resistors but no capacitors are connected in series to the X terminals of the CCII/CCCII. This is in agreement with the literature.
- The designer should avoid of using resistors connected to the Y and/or Z terminals of the CCII/ CCCII for proper high frequency operation.
- The use of capacitors at Z terminal of the conveyors affects the low-frequency performance of the filter or simulated inductor.
- A suitable set of passive element values should be chosen for a specific circuit to overcome signal swing limitations of the internal nodes.

- If the cut-off frequencies of the non-ideal gains of the active devices are larger, the circuit has better stability condition thus analog circuit designer should try to increase the value of the cut-off frequencies.
- Especially, the effects of the Z and Y terminal parasitic resistances are reduced dramatically by using the parasitic impedance compensation technique presented in this thesis.

From this part, the following important conclusions can be derived:

- (i) The Z and Y terminal parasitic resistance reduction method is very useful when the capacitor connected to the Z/ Y terminal is grounded. Furthermore, a circuit employing grounded capacitors at the Z/ Y terminal is easy to implement in IC technology.
 - (ii) The developed parasitic impedance compensation method can be applied to the floating inductor simulators and analog filters as well as other current conveyor based circuits efficiently.
 - (iii) Nevertheless, as explained in this thesis, one should be very careful for reducing the Z and Y terminal parasitic resistance effects of an inductor simulator otherwise the inductor has a stability problem.
- Some new circuits are developed to solve the parasitic impedance effects of the conveyors.
- All of the proposed novel inductor simulators and analog filters have at least one of the following important features:
- (i) They occupy less area because of using reduced number of active and passive components, which is important from VLSI implementation point of view.
 - (ii) They have only resistive components but no capacitors are connected in series to the X terminals of the current conveyors, thus they can be tuned electronically by employing current controlled current conveyors, and operated at higher frequencies.

(iii) They employ only grounded capacitors, and need no critical component matching constraints so they are very suitable for IC implementation.

- It is expected that the methods derived and the results obtained in this thesis will be useful for analog circuit designers when they evaluate and compare similar circuits in the literature.
- For the analyzed circuits, experimental, simulated and theoretical results are shown to be in good agreement. Nevertheless, the discrepancy among them mainly stems from the non-ideal gain and parasitic impedance effects of the active devices as explained in the text.

In the future studies,

Quite a large number of other current conveyor circuits such as current-mode and voltage-mode PI, PD and PID controllers, synthetic transformers, full-wave rectifiers, chaotic oscillators, immittance function simulators and capacitance multipliers are available in the literature. The presented methods can easily be applied to these circuits for performance comparison and as a help to the designer for performance improvement.

Due to the lower voltage designs in the future, signal limitation problem can be expected to be a dominating problem. This problem seems to be solved by the new emerging log-domain concept in the future.

APPENDIX A: MATHEMATICAL FORMULAS FOR GROUNDED INDUCTOR SIMULATORS

For a set of previously published inductor simulators in [14] and [19]-[22] employing a minimum number of passive elements R_1 , R_2 and C , without passive element matching constraints, the following calculations can be performed:

$$I_{in} = \frac{\pm V_2}{R_i} \quad (\text{A.1})$$

$$\pm V_2 sC = \frac{V_{in}}{R_j} \quad (\text{A.2})$$

Therefore,

$$V_{in} = sCR_1R_2I_{in} = sL_{eq}I_{in} \quad (\text{A.3})$$

where $L_{eq} = CR_1R_2$, $i = 1, 2$ and $j = 1, 2$ as well as $i \neq j$. Here, V_{in} and I_{in} are the input voltage and current of the inductor simulator, respectively. Moreover, V_2 is the internal node voltage of the simulated inductors.

It is important to note that this grounded inductor simulator has two nodes with voltages V_{in} and V_2 besides ground.

If the input is a voltage source, the terminal voltage V_2 can be expressed as follows:

$$V_2 = \mp \frac{1}{sCR_j} V_{in} \quad (\text{A.4})$$

If the input is a current source, the terminal voltages V_{in} and V_2 can be expressed by

$$V_{in} = sCR_1R_2I_{in} \quad (\text{A.5})$$

$$V_2 = \mp R_l I_{in} \quad (\text{A.6})$$

APPENDIX B: DESCRIPTION OF A COMPLEX NUMBER

A complex number Z can be represented as $Z = A + j B$ in which A is real part and B is imaginary part of Z . The magnitude of Z is given as following:

$$|Z| = \sqrt{A^2 + B^2}$$

if $B \geq 5A$, $|Z| \cong B$ within less than 2% error.

if $A \geq 5B$, $|Z| \cong A$ within less than 2% error.

Similarly,

if $B \geq 10A$, $|Z| \cong B$ within less than 0.5% error.

if $A \geq 10B$, $|Z| \cong A$ within less than 0.5% error.

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