FIELD PROGRAMMABLE ANALOG ARRAY DESIGN FOR BIOMEDICAL APPLICATIONS

by

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ABSTRACT

FIELD PROGRAMMABLE ANALOG ARRAY DESIGN FOR BIOMEDICAL APPLICATIONS

The acquisition and processing of biomedical signals are important steps for clinical applications and academic research. Clinical applications involves diagnosis of diseases and also control of the prothesis or functional electrical stimulation systems. On the other hand, in academical researches biomedical signals must be collected for generating data sets. For both of these two applications, most of the time data capturing device needs to get data from the patient or subject for a long period of time or multiple electrodes need to get data at the same time as long as the patient or subject carries on his/her daily life. In such cases mobile medical devices become important. To capture and process the medical signals, analog front-end circuits and analog processing circuits need to be implemented. Medical signals are the signals which have low amplitude and low frequency body signals. Capturing biomedical signals on a living tissue is highly noise sensitive. Because of these reasons, implementation and validation of these type of circuits are harder and more time consuming. Biomedical signals are usually processed using analog circuits such as instrumentation amplifiers, filters, RMS converters or rectified average value converters. The design of such traditional circuits, however, especially during the validation phase, is time consuming. To reduce the time required for analog design, programmable devices become important. As a result, analog circuits can be designed to be programmable in a pre-defined limited operation range. In this study, main building blocks such as Low Noise Amplifier, Filters, Analog to Digital Converter, Switch Logic and Programming Logic have build. Pre-layout and post-layout simulations of these main building blocks have done. By using these building blocks, CAB structures have designed by considering the general requirements of a biomedical signal processing.

ÖZET

BİYOMEDİKAL UYGULAMALAR İÇİN ALAN PROGRAMLANABİLİR ANALOG DİZİ TASARIMI

Biyomedikal sinyalleri yakalamak ve işlemek klinik uygulamalar ve akademik araştırmalar için önemli adımlardır. Klinik uygulamalar, hastalıkların teşhisini ve işlevsel elektrikli uyarı sistemlerinin kontrolünü içermektedir. Diğer taraftan, akademik araştırmalarda veri setleri oluşturabilmek için biyomedikal sinyallerin toplanması gerekmektedir. Çoğu zaman bu uygulamaların her ikisi için de, hasta veya denek günlük hayatına devam ederken çok sayıda elektrod yardımıyla uzun süre veri toplanması gerekmektedir. Böyle durumlarda, taşınabilir ve insan sağlığına yan etkisi bulunmayan tıbbi cihazların kullanımı önem kazanmaktadır. Tıbbi sinyalleri elde etmek ve işlemek için, analog uç devrelerinin ve analog işleme devrelerinin uygulanması gerekmektedir. Tıbbi sinyaller, düşük genlikli ve düşük frekanslı vücut sinyalleridir. Canlı bir dokudan biyomedikal sinyaller elde etmek gürültüye oldukça hassastır. Bu nedenlerden ötürü, bu tür devrelerin tasarlanması ve gerçeklenmesi zor ve zaman alıcıdır. Biyomedikal sinyaller genellikle yükselticiler, filtreler, RMS dönüştürücüler veya doğrultulmuş ortalama değer dönüştürücüler gibi analog devreler kullanılarak işlenmektedir. Ancak bunlar gibi yaygın devrelerin tasarımı, özellikle gerçekleme aşamasında, zaman alcıdır. Analog tasarıma harcanan zamanı azaltmak için, programlanabilir cihazlar önem kazanmaktadır. Bu sebeplerden dolayı, analog devreler önceden tanımlanmış sınırlı bir işlem aralığında programlanabilir olacak şekilde tasarlanabilir. Bu çalışmada, Düşük Gürültülü Yükseltici, Filtreler, Analog-Sayısal Dönüştürücü, Anahtarlama Devreleri ve Programlama Devreleri gibi ana yapı blokları tasarlanmıştır. Bu ana blokların serim öncesi ve sonrası benzetimleri yapılmıştır. Bu yapı blokları kullanılarak biyomedikal sinyal işlemenin genel gereklilikleri göz önünde bulundurularak CAB yapısı tasarlanmıştır.

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C_{ox}	Gate oxide capacitance
F	Noise factor
k	Boltzmann's constant
°K	Degrees in Kelvin
L	Gate length
Q	Quality factor
W	Gate width
δ	Gate noise coefficient

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating current
DR	Dynamic range
FET	Field effect transistor
LNA	Low noise amplifier
MOS	Metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transistor
NF	Noise figure
SNR	Signal to noise ratio

1. INTRODUCTION

In real world, all events happen in continuous time. Analog circuits are very important in electronic systems. Analog circuits are used in the communication between digital circuits and external environment. Furthermore analog circuits realize some processes such as filtration, multiplication, integral etc. in a smaller area, faster and by consuming less amount of energy than digital circuits within a specific resolution range. On the other hand, when comparing to their analog equivalences, digital circuits are more flexible and their design process is easier.

There are some drawbacks of designing by discrete components or integrated circuits level in rapidly developing and changing technology world. With programmable logic devices, designers use inexpensive software tools to quickly develop, simulate, and test their designs. Then, a design can be quickly programmed into a device, and immediately tested in a live circuit. There are no NRE costs and the final design is completed much faster than that of a custom, fixed logic device. Another key benefit of using programmable devices is that during the design phase customers can change the circuitry as often as they want until the design operates to their satisfaction. That's because programmable devices are based on re-writable memory technology - to change the design, the device is simply reprogrammed. Once the design is final, customers can go into immediate production by simply programming as many programmable devices as they need with the final software design file.

Since the field programmable gate arrays (*FPGA*) produced commercially, they found various application fields. Thanks to their structure that is suitable for real-time change and development on design, FPGAs dramatically reduced design costs and duration. This success of FPGAs became a motivating factor in the design of Field Programmable Analog Arrays (*FPAA*). FPAAs have gained importance in design and development of analog circuits which are generally used in input-output stages and filtration.

Limited design flexibility of analog circuits prevents FPAAs working with adequate performance in all frequency bands. For this reason, FPAAs should be designed as suitable to work in specific ranges of frequency band.

In this study, some analog blocks required for designing low power FPAA architectures -especially for medical applications- like; low and very low frequency filters, tunable amplifications stages, programmable analog to digital converters (ADC), switch network elements and digital programming structure with pre and post-layout simulations are given.

2. LOW NOISE AMPLIFIER (*LNA*)

LNA is the block where the signals with low amplitude captured from analog world via probes are amplified before filtration and the other blocks. In this amplification process, undesired noise signals are also amplified in addition to the desired signals. Moreover, this amplifier block also adds some noise to the signal because of its structure. The block design is targeted to minimize the noise added to amplified signal.

Widely used biomedical signals are given in Table 3.1. The operating characteristic should satisfy to the operating frequency range and amplitude given in Table 3.1 by consuming low power. Due to electrochemical effects at the electrode-tissue interface, dc offsets of 1-2 V are common across differential recording electrodes [1]. These 1-2V DC offsets should be eliminated by the capacitors that are placed at the input stage. Regarding that the body signals captured by the probes are at the level of microvolts, noise should be kept below this level. LNA architecture that is designed by considering these limitations are given in Figure 2.1 was first described in [2].

Mid-band gain of the circuit given in Figure 2.1 is stated by

$$A_m = \frac{C_1}{C_2}. \tag{2.1}$$

For the condition that $C_1, C_L >> C_2$ bandwidth of the circuit can be stated as,

$$BW = \frac{g_m}{A_m C_L}, \tag{2.2}$$

where g_m is the transconductance of the OTA (*Operational Transconductance Amplifier*).

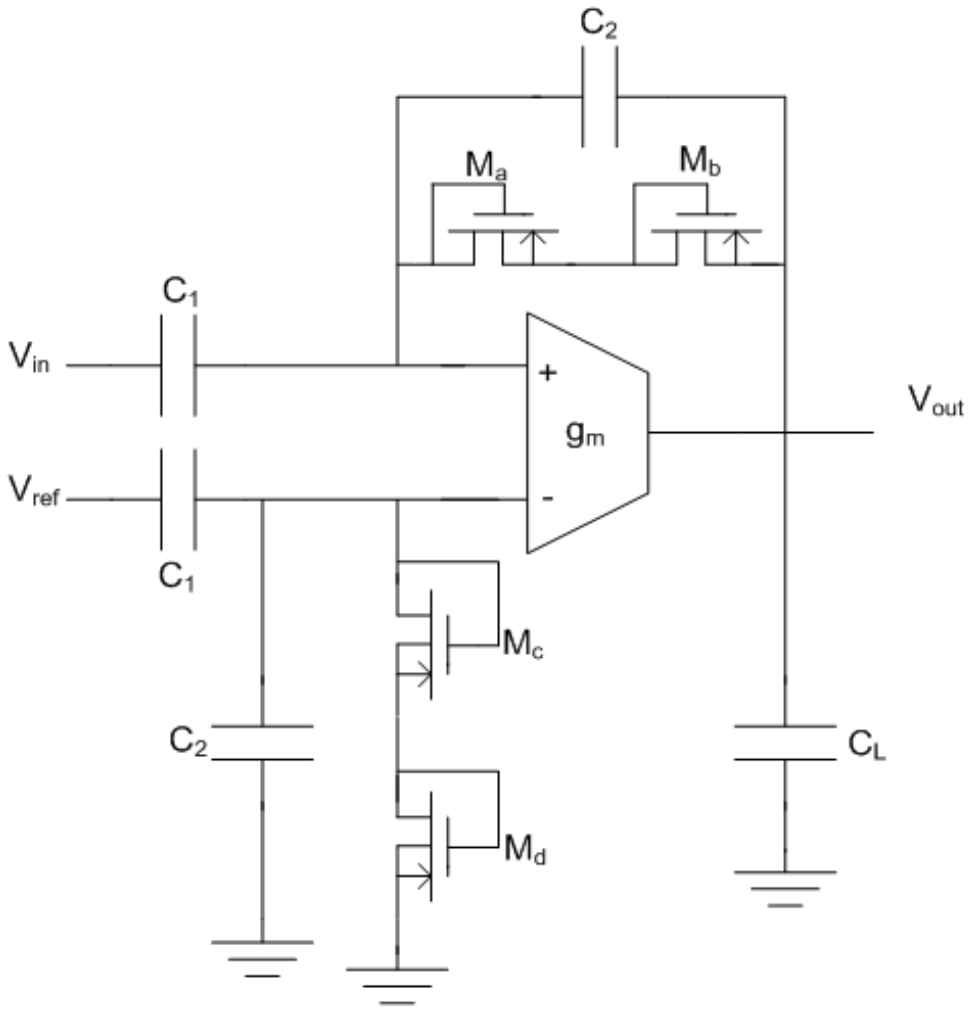

Figure 2.1. Schematic of LNA design.

2.1. Architecture

2.1.1. MOS Bipolar Elements

Transistors $M_a - M_d$ are MOS-bipolar devices acting as pseudoresistors. With negative Vgs , each device functions as diode connected PMOS transistor. With positive Vgs, the parasitic source-well-drain p-n-p bipolar junction transistor (BJT) is activated, and the device acts as a diode-connected BJT [3].

The reason behind series connection of the transistors is to reduce the distortion for large output signals. As we consider the resistance value of the diode connected

transistors “r”, the low cut-off frequency can be stated as,

$$W_L = \frac{1}{2rC_2}. \tag{2.3}$$

2.1.2. Low Noise Low Power OTA Design For LNA

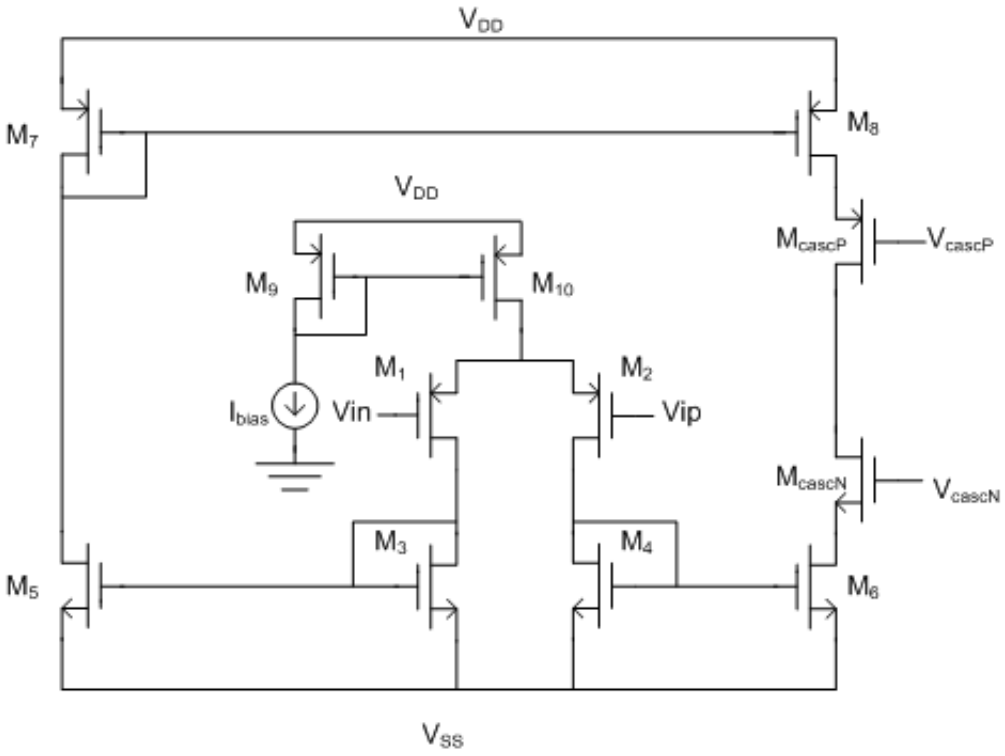

Figure 2.2. Schematic of OTA used in LNA.

The bias currents and voltages were generated by standard circuits. I_bias is set to 400nA so feeding devices $M_1 - M_8$ drain currents of 200nA. For these current ratings each device may operate in weak, moderate and strong inversion depending on W/L ratio. For each device, I_s is given by,

$$I_s = 2\mu \frac{(C_{ox}U_T^2)}{\kappa} \frac{W}{L}, \tag{2.4}$$

where U_T is the thermal voltage $\kappa T/q$, and is the sub-threshold gate coupling coefficient.

Note that U_T has a typical value of 0.7 and is equivalent to *1/n*, where denotes the reciprocal of the change in surface potential for a change in gate-to-body voltage [4].

The inversion coefficient *(I_C)* for each transistor may then be calculated as the ratio of drain current to the moderate inversion characteristic current, as follows;

$$I_C = \frac{I_D}{I_S}. \tag{2.5}$$

A device having $I_C > 10$ operates in strong inversion region and has a transconductance proportional to the square root of drain current. A device having $I_C < 0.1$ operates in the weak inversion *(sub-threshold)* region and has a transconductance proportional to drain current. For the devices operating in moderate inversion ($10 > I_C > 0.1$), both strong and weak inversion expressions overestimate transconductance [5].

For all regions g_m can be estimated as;

$$g_m \approx \frac{I_d}{U_T} \frac{2}{1 + \sqrt{1 + 4I_C}}. \tag{2.6}$$

And, the input-referred thermal noise power is;

$$(V^2_{ni,thermal}) = [\frac{16T}{3g_{m1}}(1 + \frac{2g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}})]\Delta f, \tag{2.7}$$

where $g_{m1} - g_{m7}$ is transconductance of the transistors $M_1 - M_7$ respectively.

Flicker noise, or *1/f* noise, is a major concern for a low-noise low-frequency circuit. We minimize the effects of flicker noise by using PMOS transistors as input devices and by using devices with large gate areas. Flicker noise in PMOS transistors is typically one to two orders of magnitude lower than flicker noise in NMOS transistors as long as V_{gs} does not greatly exceed the threshold voltage [5, 6] and flicker noise is inversely proportional to gate area. All transistors should be made as large as possible to minimize noise. However, as devices made larger, $C_3 - C_7$ are needed to be larger [7].

2.2. Noise Analysis

There is a tradeoff between power and noise. Since we are interested in minimizing noise within a limited power budget, below given formula should be analyzed. The noise efficiency factor *(NEF)* introduced in [8] quantifies this tradeoff;

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{U_T 4\kappa TBW}}, \tag{2.8}$$

where $V_{ni,rms}$ is the input-referred rms noise voltage, I_{tot} is the total amplifier supply current and BW is the amplifier bandwidth in Hertz.

By substituting the expression for thermal noise for $g_{m3}, g_{m7} << g_{m1}$ we find;

$$NEF = \sqrt{\frac{4I_{tot}}{3U_T g_{m1}}} = \sqrt{\frac{16}{3U_T}\frac{I_{D_1}}{g_{m1}}}, \tag{2.9}$$

where I_{D_1} and g_{m1} are the drain current through M_1 and transconductance respectively.

2.3. Simulation Results

2.3.1. Pre-Layout Simulation Results

Figure 2.3 gives the transient analysis of LNA, input and output signal waveforms top and bottom respectively. Input is 10uV and 20Hz sinusoidal.

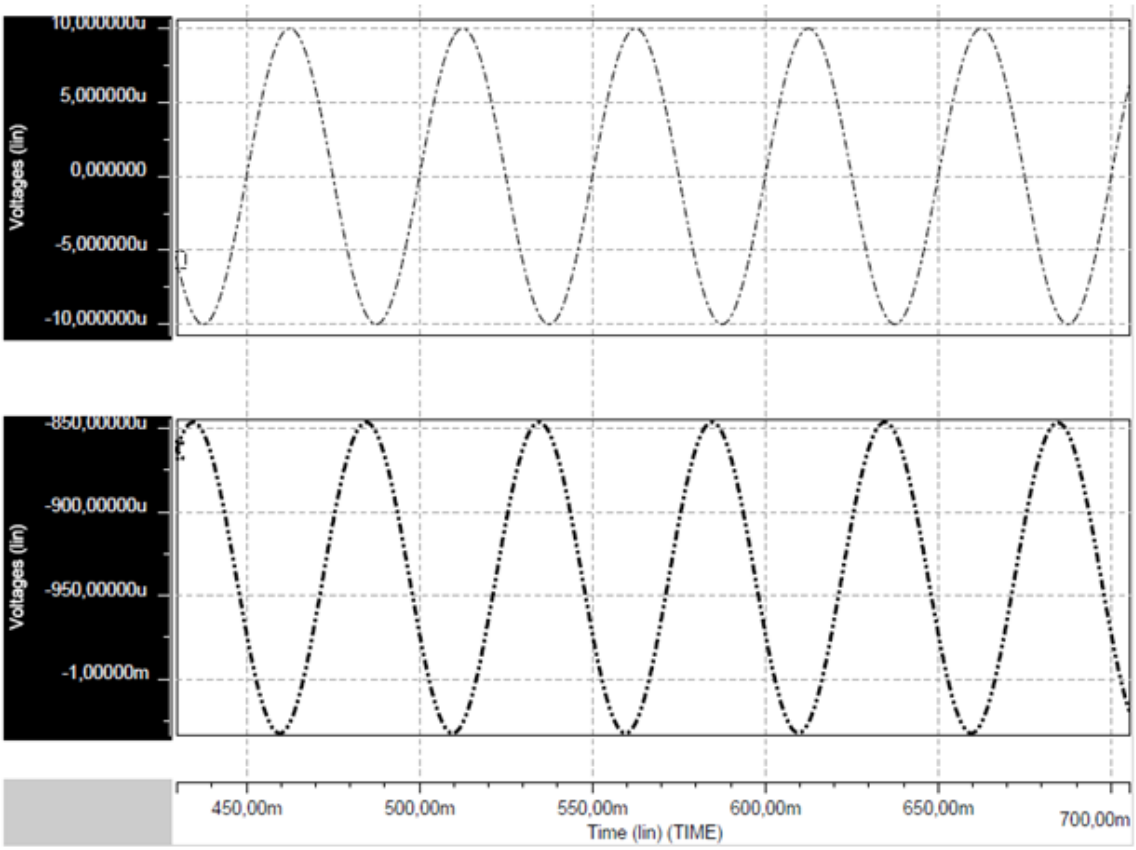

Figure 2.3. Input and output waveform of LNA as the gain is 10.

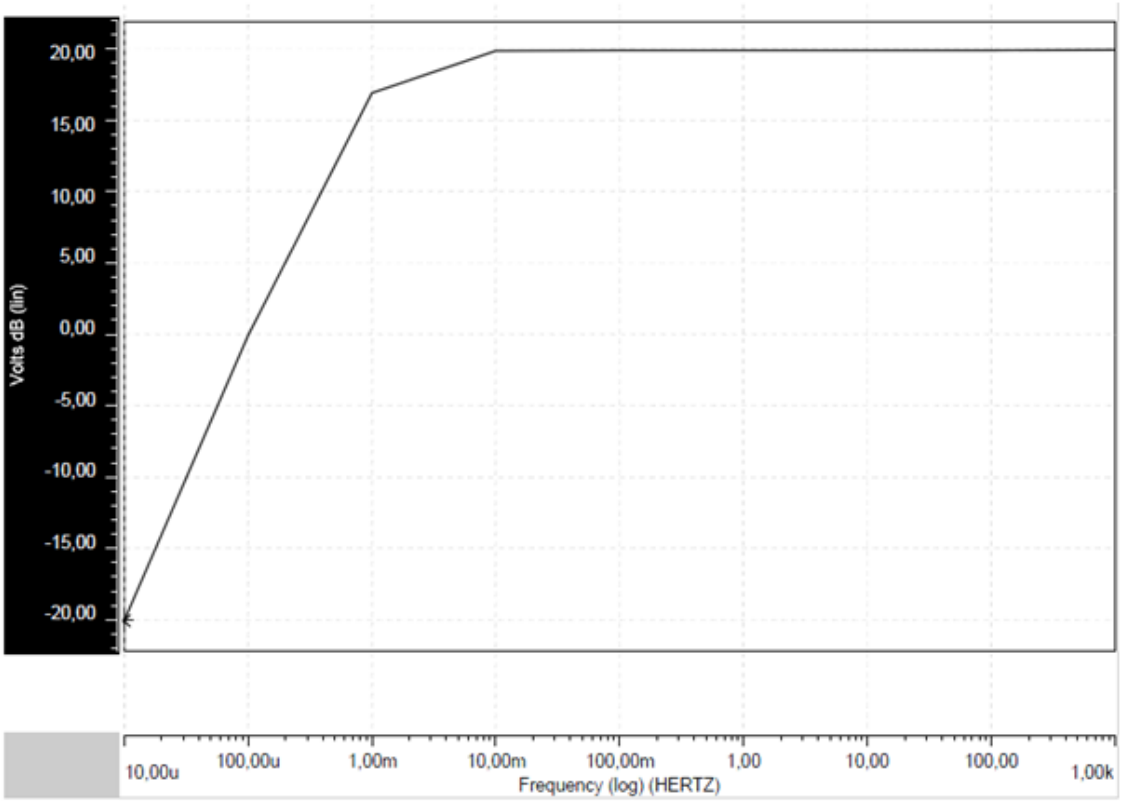

Figure 2.4. AC simulation output of LNA. Gain is 19.8db and low frequency cut-off is 10mV.

Figure 2.4 gives the AC analysis output waveform. Gain is 20dB for 10 mHz-1 kHz.

Figure 2.5 gives the AC analysis output waveform. Gain is 39.7dB for 100 mHz-1 kHz. By setting I_{bias} current as 400nA the value of g_m can be set as 2.3S. Average power consumption and average gain of the designed circuit for 1 mHz-1 kHz range is 1.5W and 39.7db respectively.

Table 2.1. Gain and noise ratings for targeting frequencies.

Frequency (Hz)	Gain (dB)	Noise (input-refered) $(V/\sqrt{Hz})$
0.1 m	1.97	940μ
1 m	19.3	94μ
10 m	85	9μ
100 m	94	954n
1	94	190n
10	94	166n
100	94.5	165n
1 k	96.6	166n
10 k	38	207n

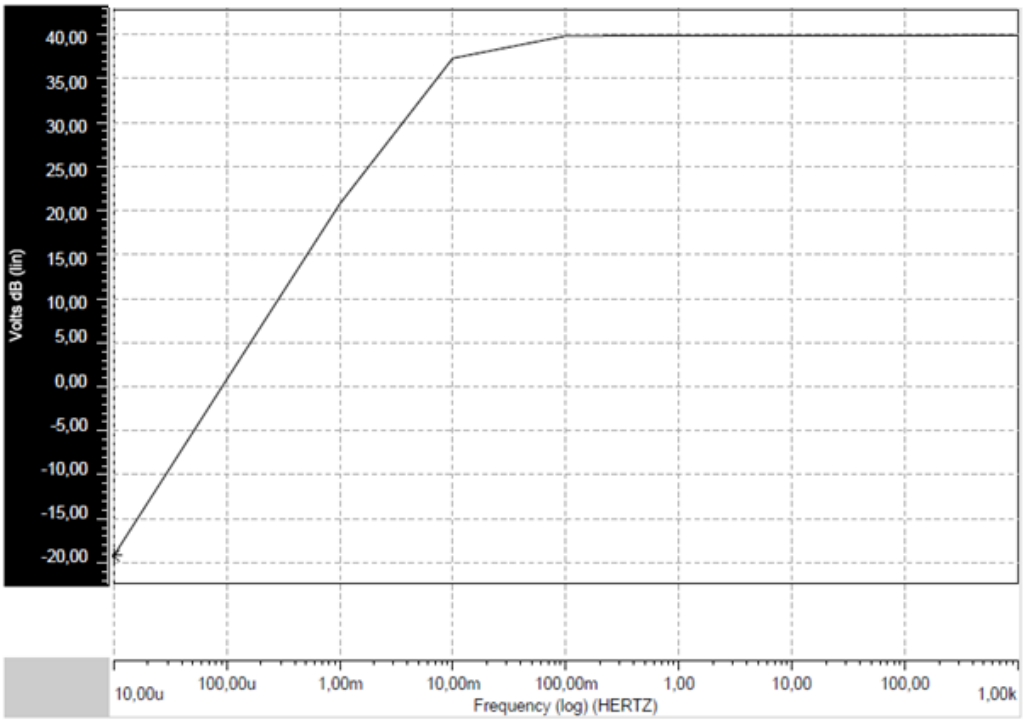

Figure 2.5. AC simulation output of LNA. Gain is 39.8db and low frequency cut-off is 50mHz.

2.3.2. Post-Layout Simulation Results

Layout for the Low Noise Amplifier has been generated and extracted for the simulations. In the layout phase, lines between the components and different layers cause parasitic effects. Layout extraction provides two types of netlist, netlist with parasitic effect and without parasitic effects. The two outputs have simulated and compared but the difference at the output between these two simulations are negligible.

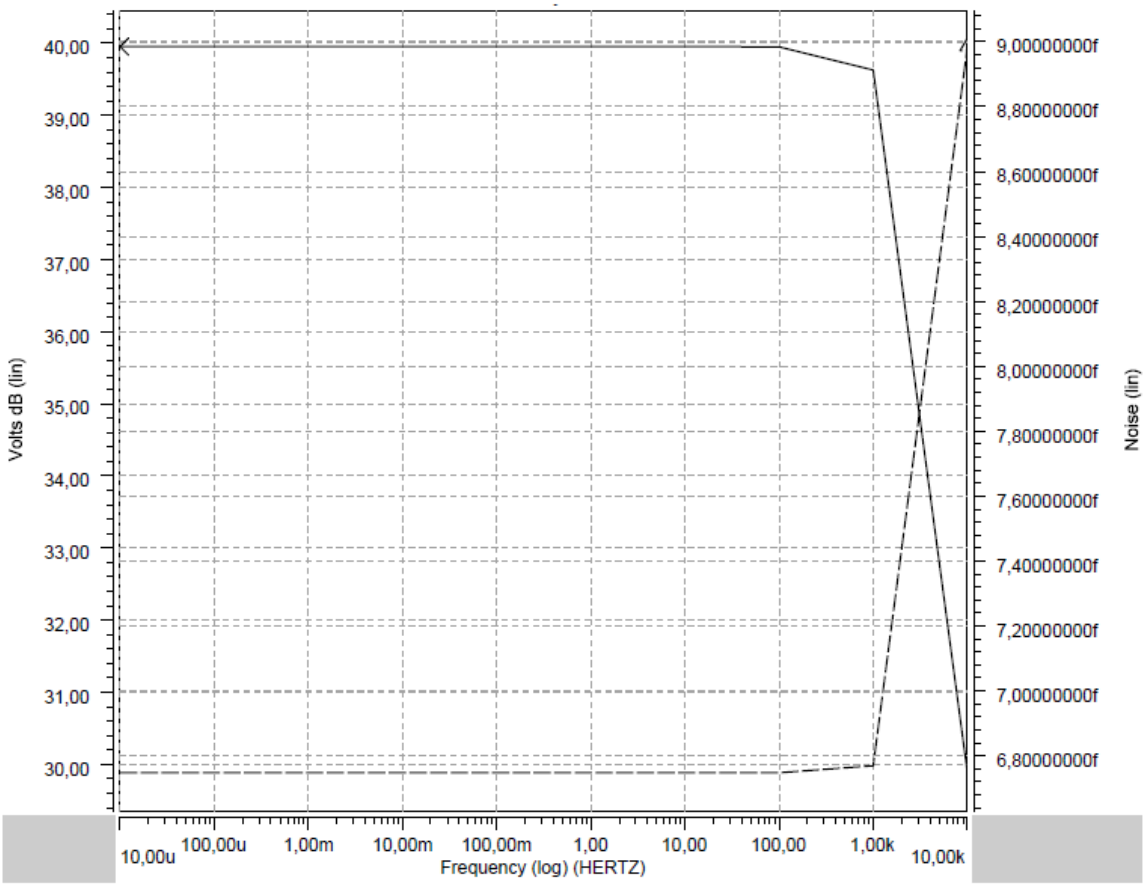

Figure 2.6. Post-layout AC simulation output of LNA. Gain is 39.8db.

Post-layout simulation output of the LNA design is given in Figure 2.6. The total power consumption of extracted LNA block is 9.317μW.

3. FILTERS

Filters are the electronic circuits which perform signal processing functions, specifically to remove unwanted frequency components from the signal, to enhance wanted ones, or both.

Filters can be classified by different specifications;

- Passive or Active,
- Analog or Digital,
- High-pass, low-pass, band-pass, band-reject or all-pass,
- Discrete-time or continuous-time,
- Linear or non-linear,
- Infinite or finite response.

For our targeted application, analog signals captured from outside world needs to be processed without any noise contribution as quantization error with low power consumption ratings. As long as we process analog signals, no time domain sampling is needed. On the other hand, targeted filter design needs to be configurable for realizing different filter types like low-pass, band-pass and so on for different frequencies.

As the target field of application of the design is processing biomedical signals, the operational frequency range is selected as the widely used frequencies in medical.

As it can be seen from the table, low frequency filter with low noise is obligatory for medical applications. On the other hand, one of the other design goals of the integrated circuit is making it portable; thus, low power consumption is considered among the priorities [9].

The two common filters are OTA based or OPAMP based filters.

Table 3.1. Frequency and amplitute ranges for ECG, EEG, EOG and EMG.

Signal	Frequency Range (Hz)	Amplitute Range (mV)
ECG	0.01 - 300	0.05 - 3
EEG	0.1 - 100	0.001 - 1
EOG	0.1 - 10	0.001 - 0.3
EMG	50 - 3000	0.001 - 100

The conventional operational amplifier (OPAMP) is used as the active device in the vast majority of the active filter literature. For design purposes, the assumption that the OPAMP is ideal $A_v = \infty$, $R_in = \infty$, $R_o = 0$ is generally made, and large amounts of feedback are used to make the filter gain essentially independent of the gain of the OPAMP. A host of practical filter designs have evolved following this approach. But, convenient voltage or current control schemes for externally adjusting the filter characteristics do not exist. At that point, OTA structures offer improvements in design simplicity and programmability when compared to OPAMP based structures as well as reduced component count.

Many of the basic OTA based structures use only OTAs and capacitors and, hence, are attractive for integration. Component count of these structures is often very low *(e.g., second-order bi-quad filters can be constructed with two OTAs and two capacitors)* when compared to *VCVS* designs. Convenient internal or external voltage or current control of filter characteristics is attainable with these designs [10].

3.1. Different OTA Architectures

To operating *OTA-C (Operational Transconductance Amplifier - Capacitor)* filter in low frequency requires low g_m OTAs (typically of the order of a few nA/V - pA/V) with linearity and/or realization of large capacitors on chip (typically of the order of a few pF) [11, 12]. By considering this, different design techniques for obtaining low transconductances are analyzed below.

3.1.1. Basic OTA

In this OTA design, there is a differential pair, M_1, M_2 and three current mirrors. As we consider $M_3 = M_4 = M_5 = M_6 = M_7 = M_8$, the G_m of the OTA is equals to G_m of M_1 and M_2.

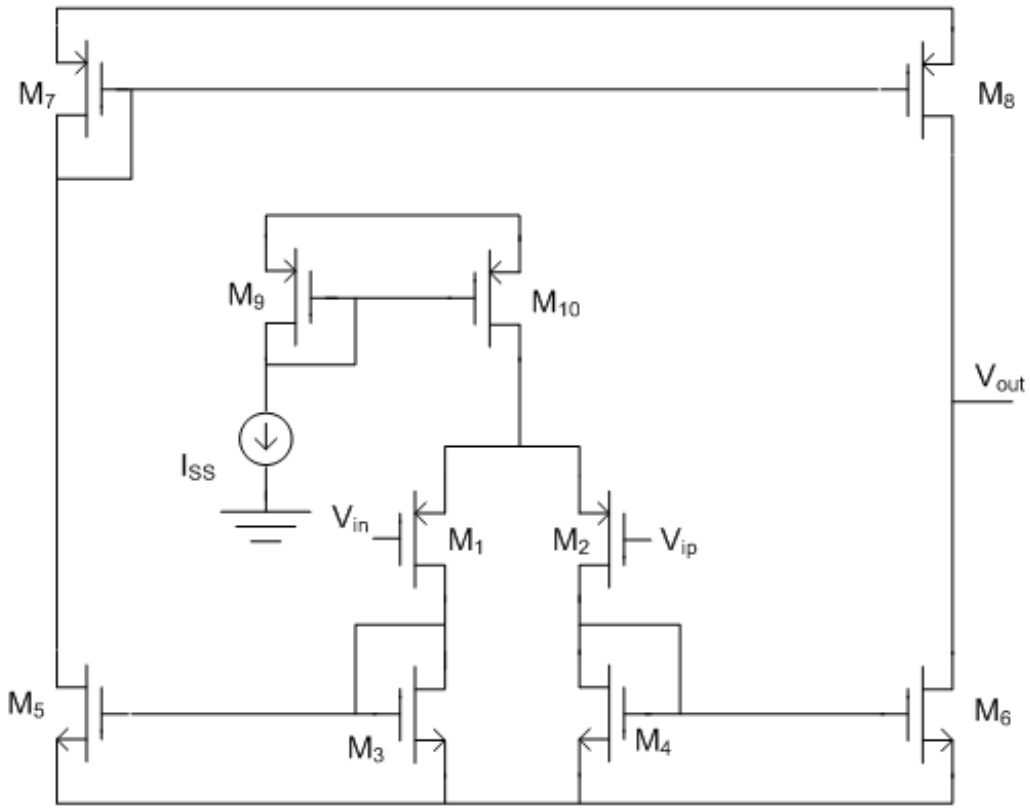

Figure 3.1. Schematic of basic OTA.

If we set W/L ratios of the transistors in the order of 0.001 or less, we can get very low transconductances in the order of pS [13].

3.1.2. OTA with Current Division and Source Degeneration (SD+CD)

This topology is given in [10, 14]. Given topology consists of two methods; current division and source degeneration. In Figure 3.2 current division idea is given. The

effective g_m is;

$$G_{meff} = \frac{g_{mtot}}{M+1}, \tag{3.1}$$

where g_{mtot} is the total g_m of one pair. The bias current Iss is spitted by the factor 1 and M. The current flow over M becomes Iss/M+1. This reduces the effective transconductance by the factor M+1. Source degeneration principle is given in Figure 3.3. If we write the equation for g_m;

$$G_m = \frac{g_{m_{M_{1,2}}}}{1 + g_{m_{M_{1,2}}} R}, \tag{3.2}$$

which gives an effective transconductance reduction by the factor (1+g_mR).

$$G_m = \frac{g_{m_{Mc}}}{M+1}, \tag{3.3}$$

$$G_m = \frac{g_m}{1 + g_m R}. \tag{3.4}$$

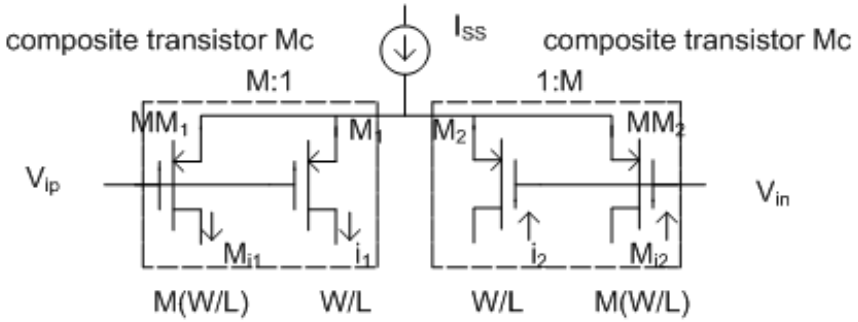

Figure 3.2. Transconductance reduction technique: current splitting.

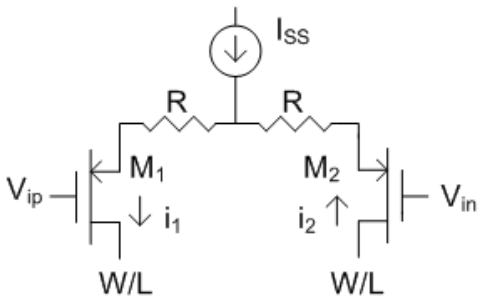

Figure 3.3. Transconductance reduction technique: source degeneration.

The schematic for the OTA which includes the previously explained current division and source degeneration technique is given in Figure 3.4. Small signal analyses give overall g_m as;

$$G_m = \left(\frac{g_{m,M_{1,2}}}{1 + \frac{(M+1)g_{m,M_{1,2}}}{g_{0_{M_{14}}}}}\right), \tag{3.5}$$

$$M = \frac{g_{m_{MM_1}}}{g_{m_{M_1}}}, \tag{3.6}$$

$$g_{0_{M_{14}}} = \eta\mu C_{ox}\frac{W_{M_{14}}}{L_{M_{14}}}(V_{SG_{M_{14}}} - |V_{TP}|) = \eta\mu C_{ox}\frac{W_{M_{14}}}{L_{M_{14}}}\sqrt{\frac{2I_{SS}}{\eta\mu C_{ox}}\frac{L_{16}}{W_{16}}}, \tag{3.7}$$

where g_m and $g_o = 1/R$ are respectively the transconductance and output conductance of the MOS transistor. G_m is dependent to $g_{o_{M14}}$, which is controlled by the bias current Iss. The transistors *M14 and M15* are working in the triode region. So, they act as source degeneration resistors and and implement source degeneration. *M3, M16, M17 and M18* are used to control the VSG of *M14, M15* and thus, their resistance. *MM1 and MM2* drive a significant portion of the bias current to the Vss, thus reducing G_m by the factor *(1+M)* to implement current division. As we mentioned above, to get low g_m values we have to lower the current flowing. But maintaining very small currents are not easy and not easy to control. On the other hand, from the layout perspective it

is not easy to match the transistors with very long lengths. To sum up, we use current division to get low g_m values.

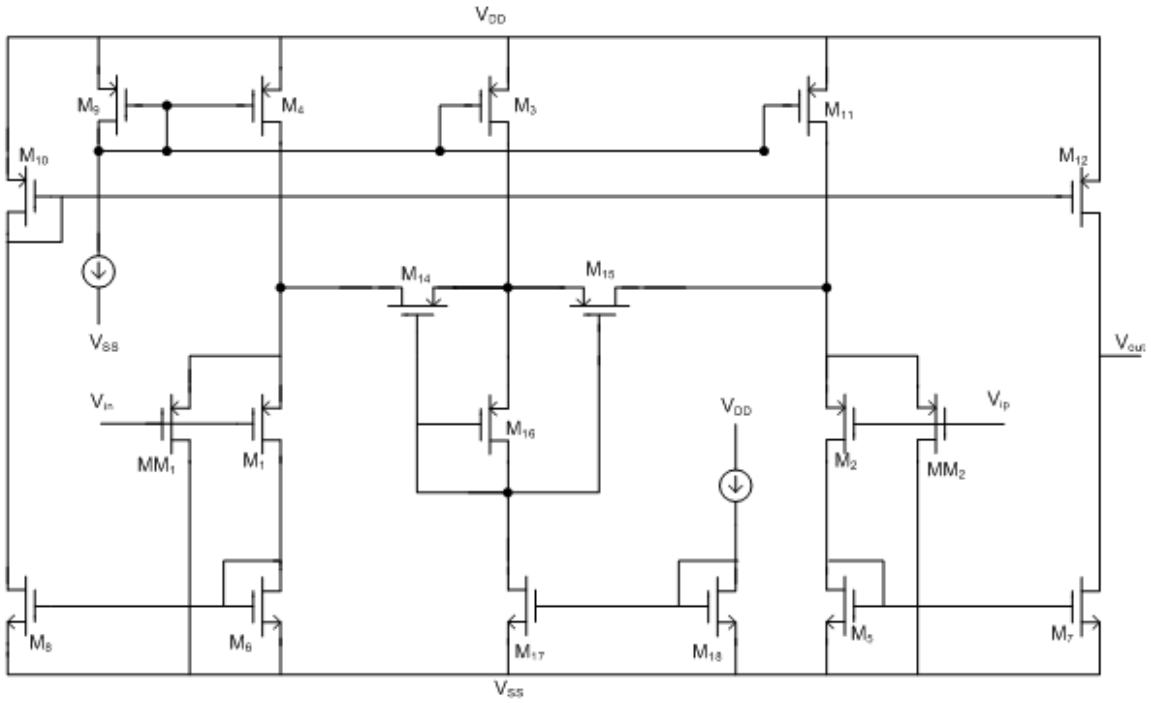

Figure 3.4. Schematic of OTA with current division and source degeneration.

3.1.3. OTA with Floating Gate (FG + CD)

The topology of Floating Gate OTA is given in Figure 3.5 [15, 16]. The transistors of the input stage are floating gate capacitors. As the nature of floating gate structure, voltage division occurs at the input capacitors.

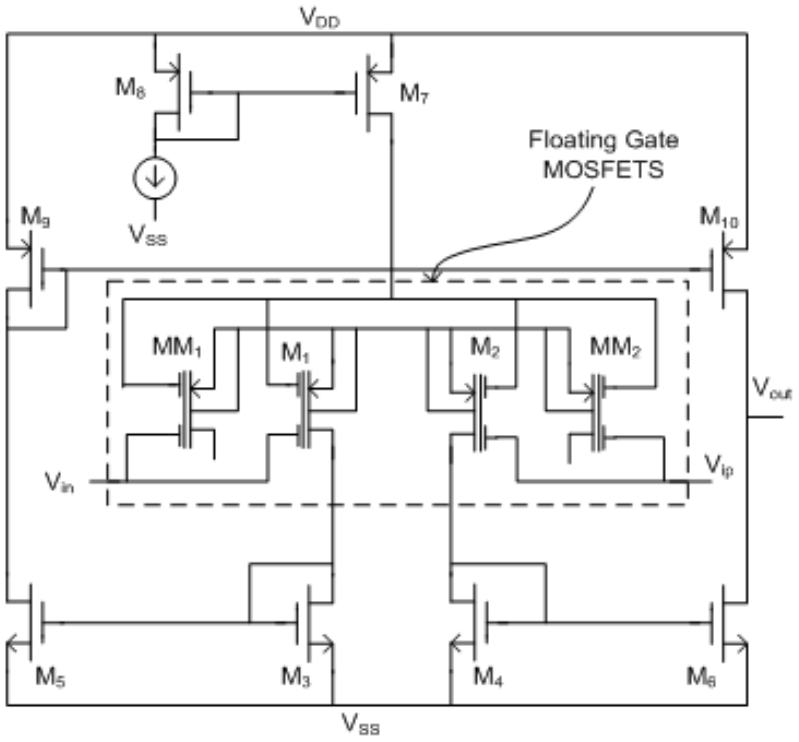

Figure 3.5. Schematic of OTA with current division and floating gate.

In addition to this, current division is applied. If we assume the parasitic capacitance negligible, in terms of model parameters total g_m of the circuit is given by [16],

$$G_m \cong (\frac{C_A}{C_A + C_B}) g_{m_{FG_1}} = (\frac{C_A}{C_A + C_B})(\frac{I_{SS}}{\varphi_1 n(1 + \sqrt{1 + i_{f_{M1}}})})(\frac{1}{M+1}), \tag{3.8}$$

where C_A is the capacitance coupling at input A to floating gate, C_B is the capacitance coupling at input B to floating gate, $g_{m_{FG1}}$ is the transconductance of the floating gate transistor M_1. For proper input voltage scaling, C_A and C_B should be significantly larger than the total parasitic capacitance seen at the floating gate. A good compromise would be to make C_A and C_B around 5-10 times this parasitic capacitance.

3.1.4. Bulk Driven OTA (BD+CD)

In this topology given in the Figure 3.6 is Bulk Driven OTA [17, 18]. The input of the circuit is bulk rather than the gate as in usual. Typically, g_m of the bulk driven

topology is approximately smaller than the half of the usual ones. But this circuit is very process dependent. G_m of the circuit in terms of model parameters is given by,

$$G_m = (\frac{\gamma_0}{2\sqrt{2\varphi_{FB} + |V_{BS}|}})g_{m_{M1}} = (\frac{\gamma_0}{2\sqrt{2\varphi_{FB} + |V_{BS}|}})(\frac{I_{SS}}{\varphi_1 n(1 + \sqrt{1 + i_{f_{M1}}})})(\frac{1}{M+1}), \tag{3.9}$$

where γ_0 is the body effect parameter (typically 0.7V), *FB* is the bulk *Fermi Potential* (typically 0.35V) and $g_{m_{M1}}$ is the gate transconductance.

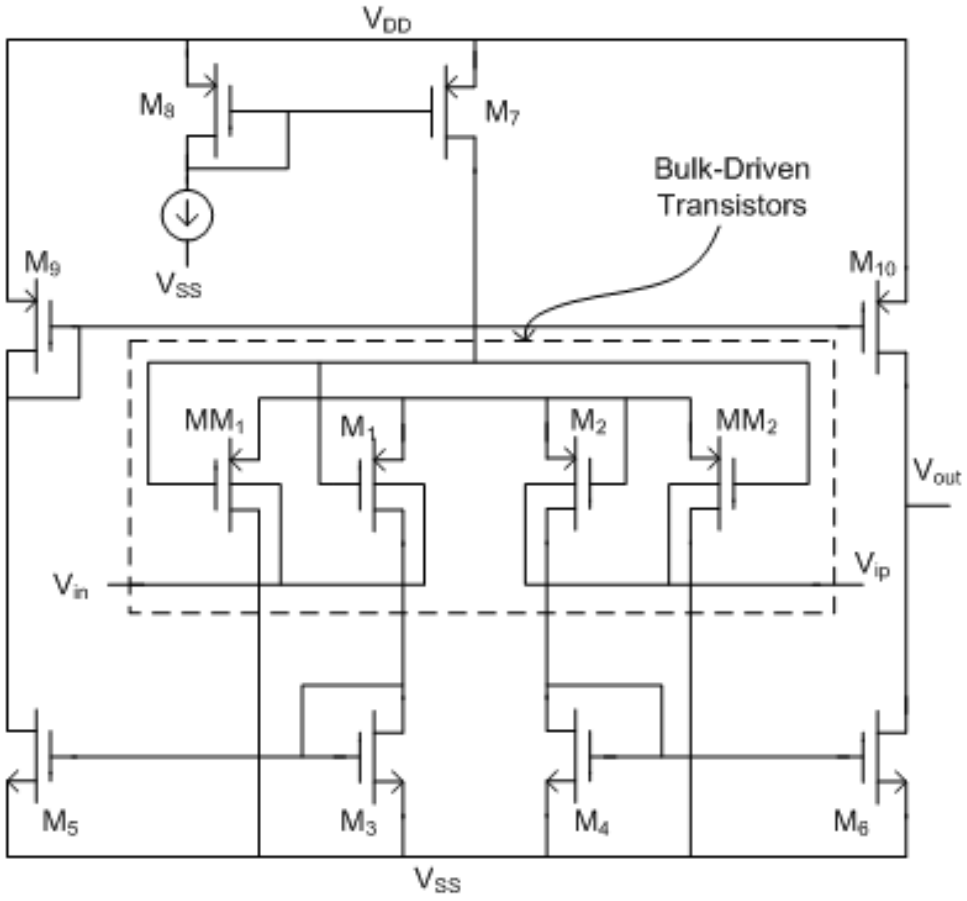

Figure 3.6. Schematic OTA with bulk driven topology.

From the layout point of view, one of the drawback is the bulk driven transistors need to be isolated in separate wells. Another drawback is the finite input impedance of the OTA.

3.2. Designed OTA Architectures

As a result of literature study, current division and source degeneration OTAs were preferred because of their performance and ease of implementation both in design and layout, in GmC filter structures for low frequency applications. The components of the designed filter blocks are programmable capacitor arrays and OTAs.

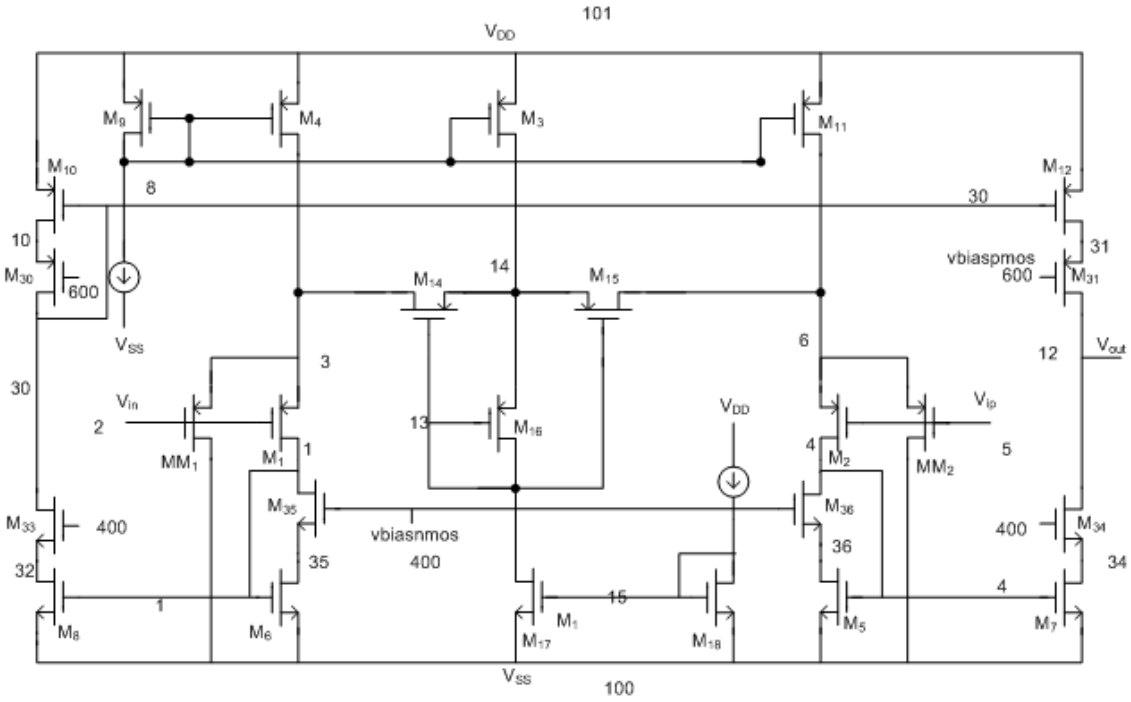

Figure 3.7. Schematic of active region OTA design with SD+CD.

In order to use wafer as feasible as possible, g_m values reduced as much as possible. OTAs, working in cut-off region and active region, have g_m values as 90pS and 12nS respectively.

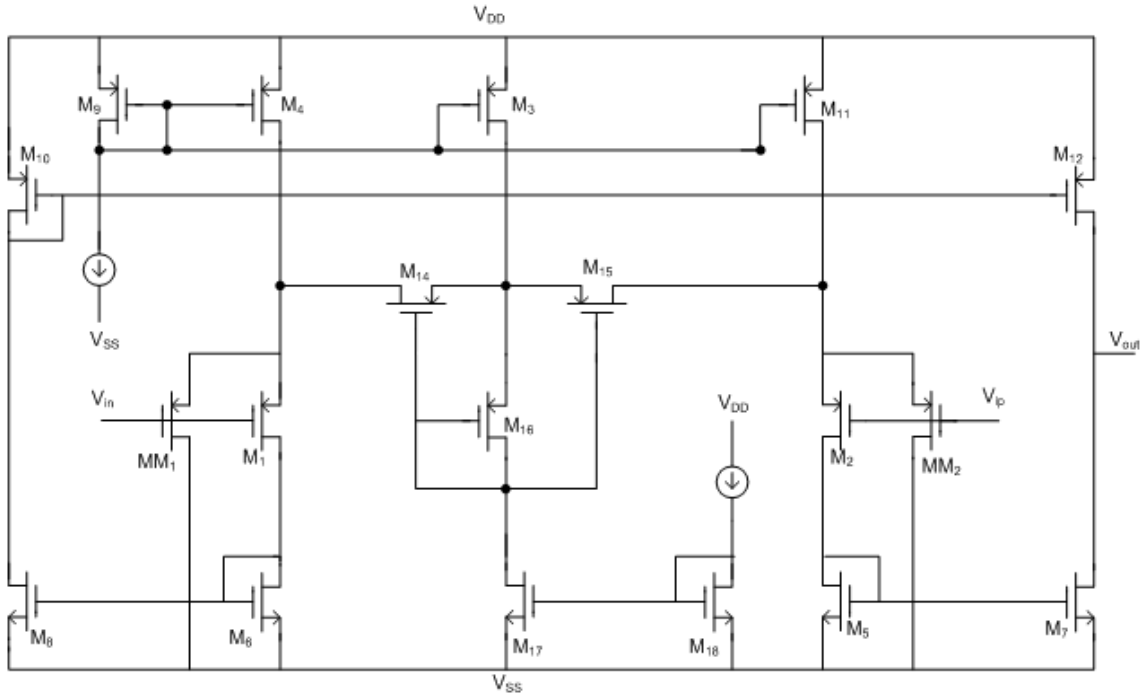

Figure 3.8. Schematic of sub-threshold region OTA design with SD+CD.

3.3. Simulation Results of Designed OTA-C Filters

3.3.1. Pre-Layout Simulation Results

In Figure 3.11, LNA and a biquad filter is connected cascaded. And generated system has a bandpass characteristic between 0.1 Hz and 10 Hz. ECG signal from, MIT medical signal database is applied to the input. Input and output signal is given in Figure 3.12.

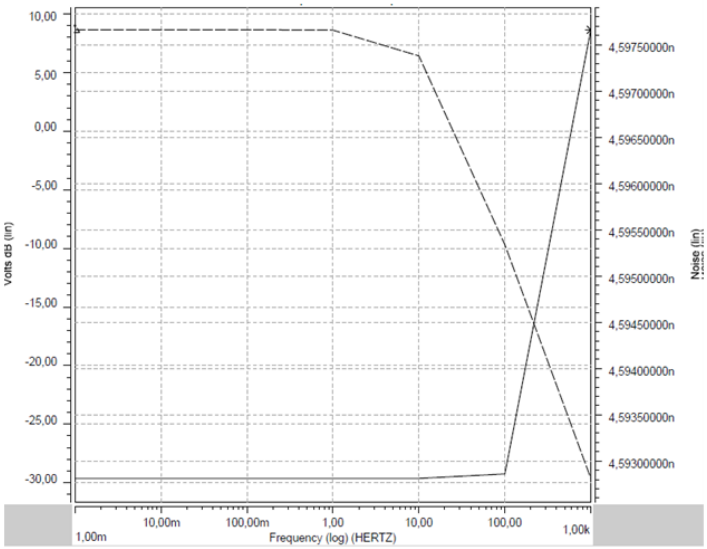

Figure 3.9. AC simulation output of a biquad lowpass filter configuration by using sub-OTA with fc = 5Hz. Gain of the filter and noise versus logarithmic scale frequency.

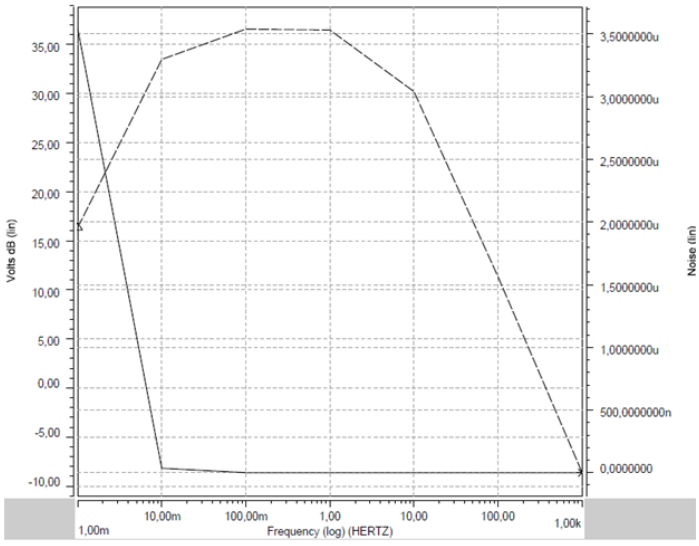

Figure 3.10. Low-noise amplifier together with biquad lowpass filter (by using sub-OTA) with fc = 5Hz is given. Gain of the system and noise versus logarithmic scale frequency is given.

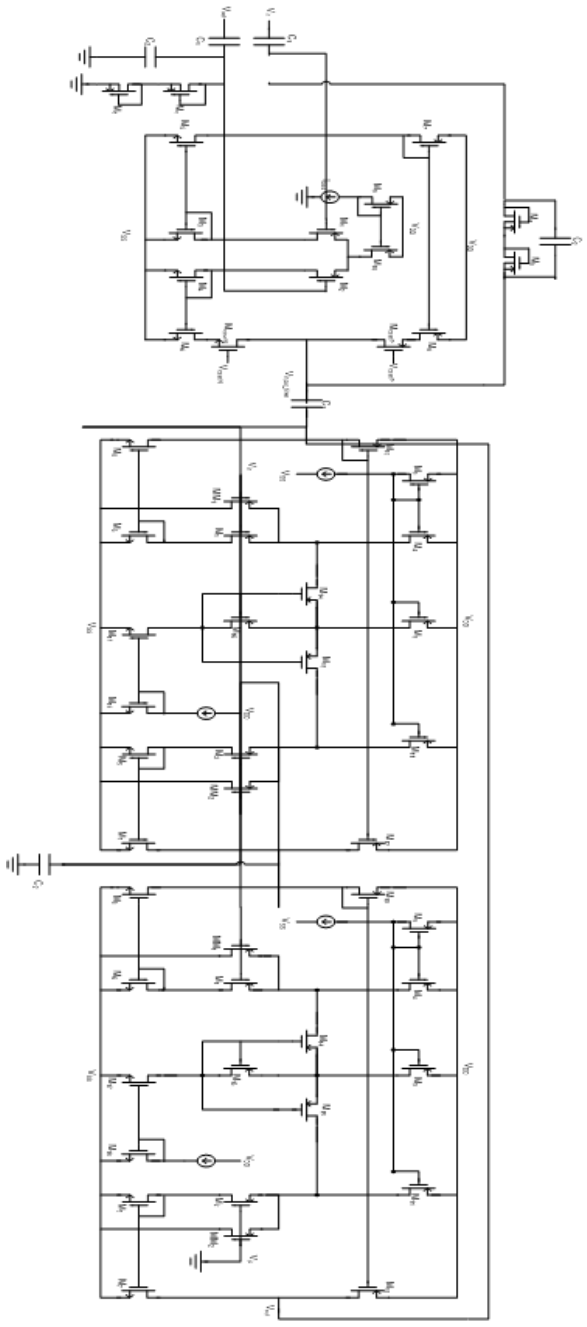

Figure 3.11. Circuit schematic of lowpass biquad configuration with an LNA at the input stage.

In Figure 3.11, LNA and a biquad filter is connected cascaded. And generated system has a bandpass characteristic between 0.1 Hz and 10 Hz. ECG signal from, MIT medical signal database is applied to the input. Input and output signal is given in Figure 3.12.

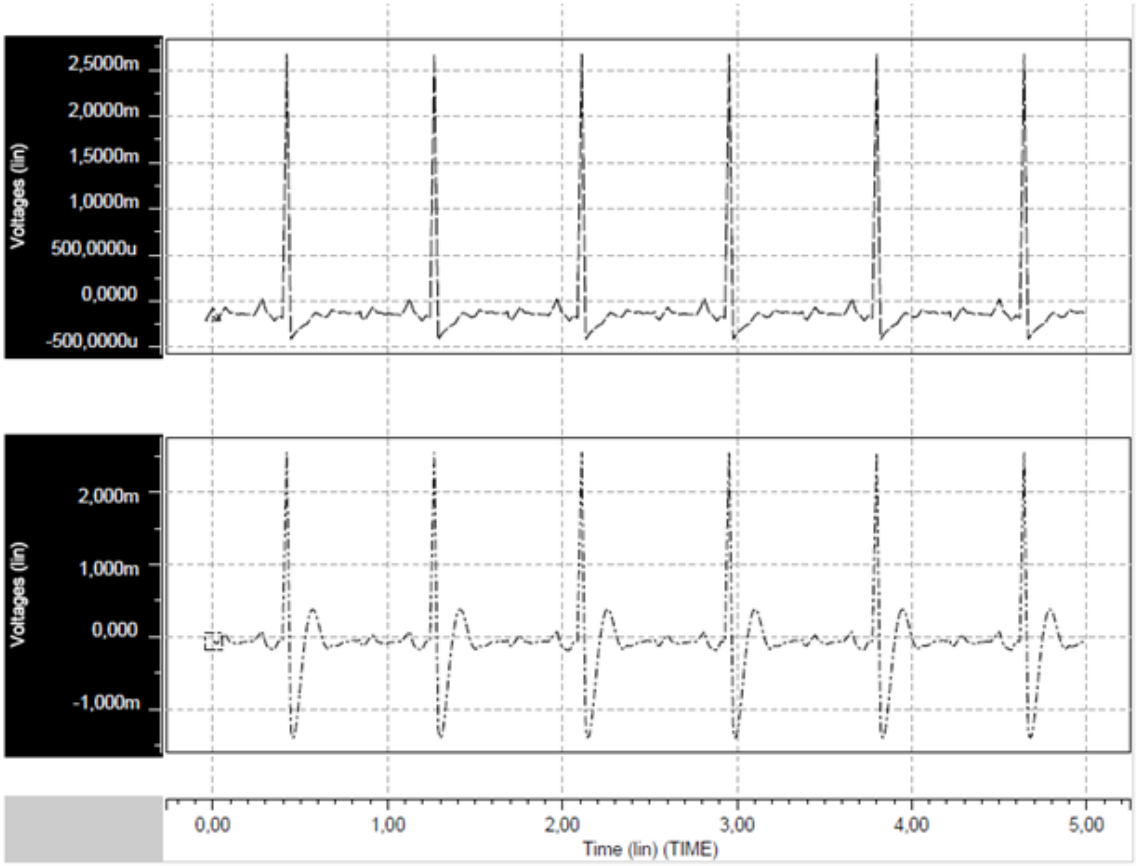

Figure 3.12. Input and output waveform of an examplar ECG signal.

Matrices for circuit structure required for the design of desired G_mC filters were acquired by selecting the degree of desired filter as Chebhsev, Butterworth or Bessel from MATLAB. These matrixes were converted to G_mC filter structure and by this way desired filters were acquired through selecting required OTA and capacitor arrays from programming network.

3.3.2. Post-Layout Simulation Results

Layout for the OTAs and Filter structures have been generated and extracted for the simulations. In the layout phase, lines between the components and different layers cause parasitic effects. Layout extraction provides two types of netlist, netlist with parasitic effect and without parasitic effects. The two outputs have simulated and compared but the difference at the output between these two simulations are negligible.

Post-layout simulation output of the Active Region OTA layout and design are given in Figure 3.13 and Figure 2.6 respectively.

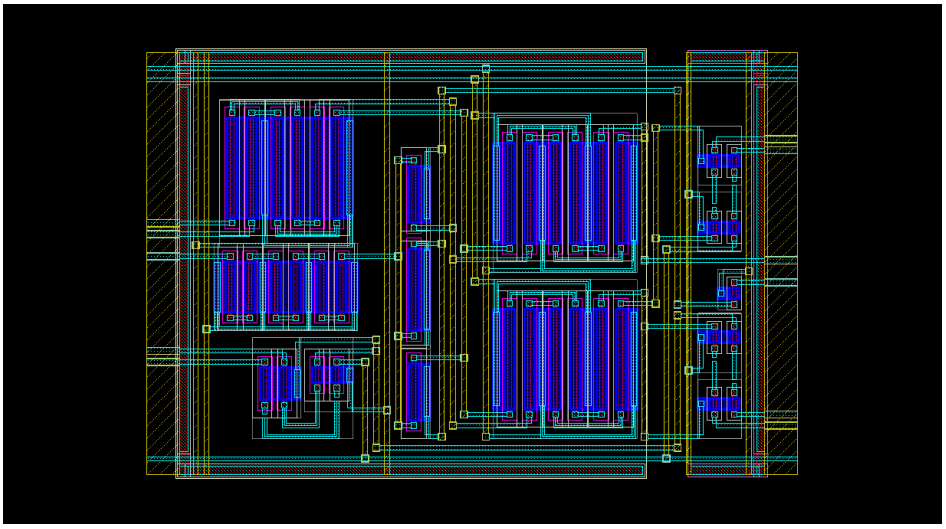

Figure 3.13. Layout of active region OTA design.

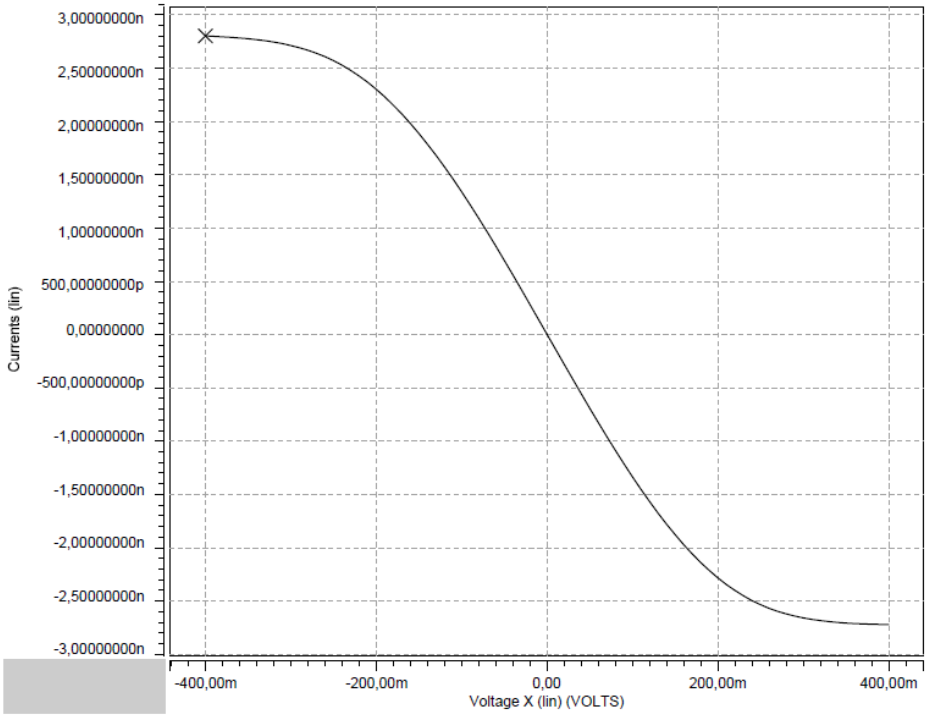

Figure 3.14. Post-layout simulation output of active region OTA design.

Post-layout simulation output of the Cut-off Region OTA layout and design are given in Figure 3.15 and Figure 2.6 respectively.

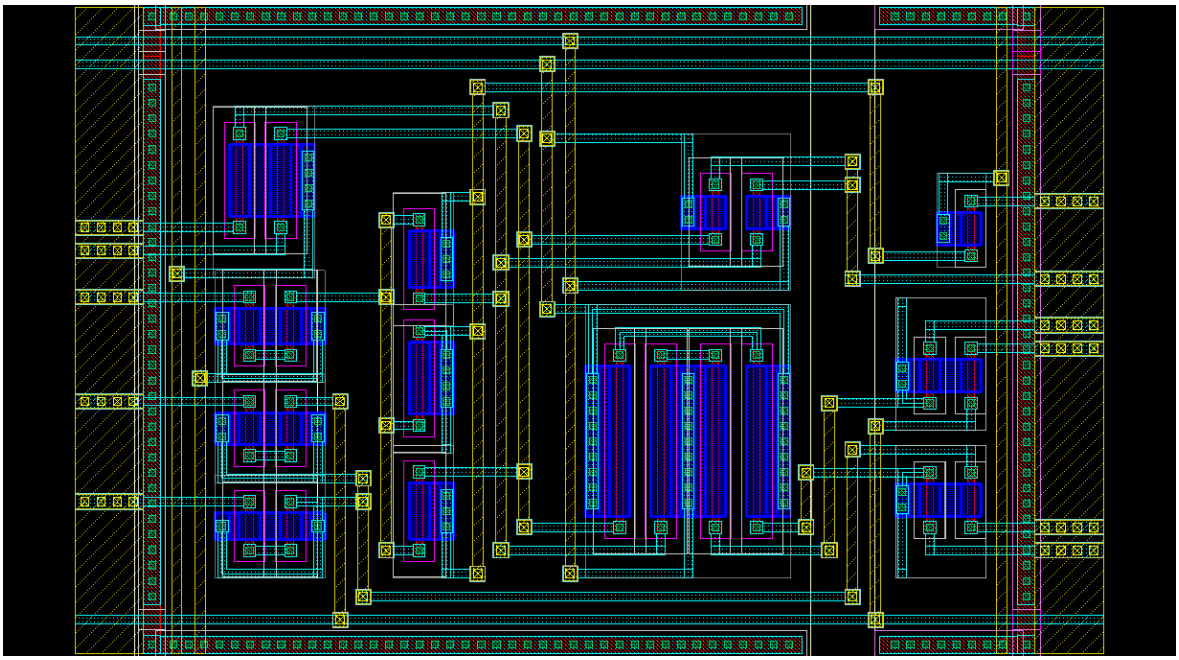

Figure 3.15. Layout of Cut-off Region OTA Design.

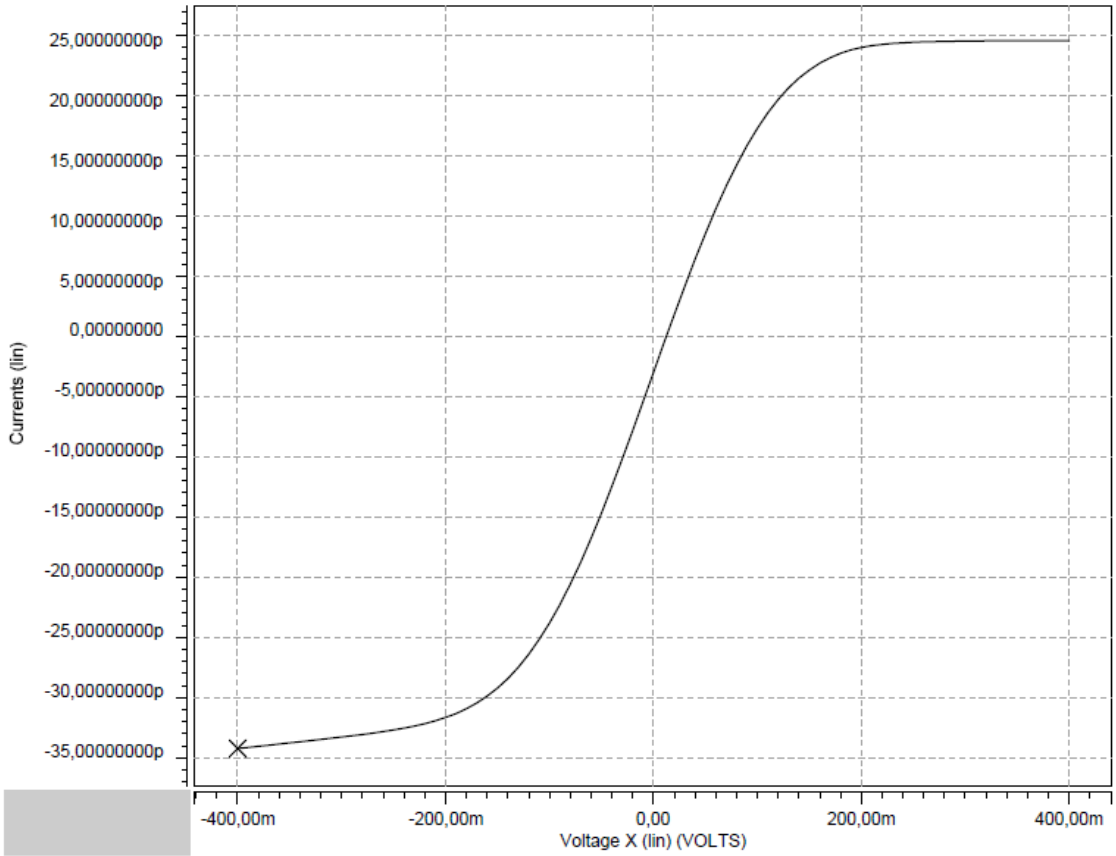

Figure 3.16. Post-layout simulation output of cut-off region OTA design.

In Figure 3.17 post-layout AC simulation output of a bandpass filter together with LNA at the input stage with 10Hz center frequency is given. The total power consumption of the system is 9.321μW.

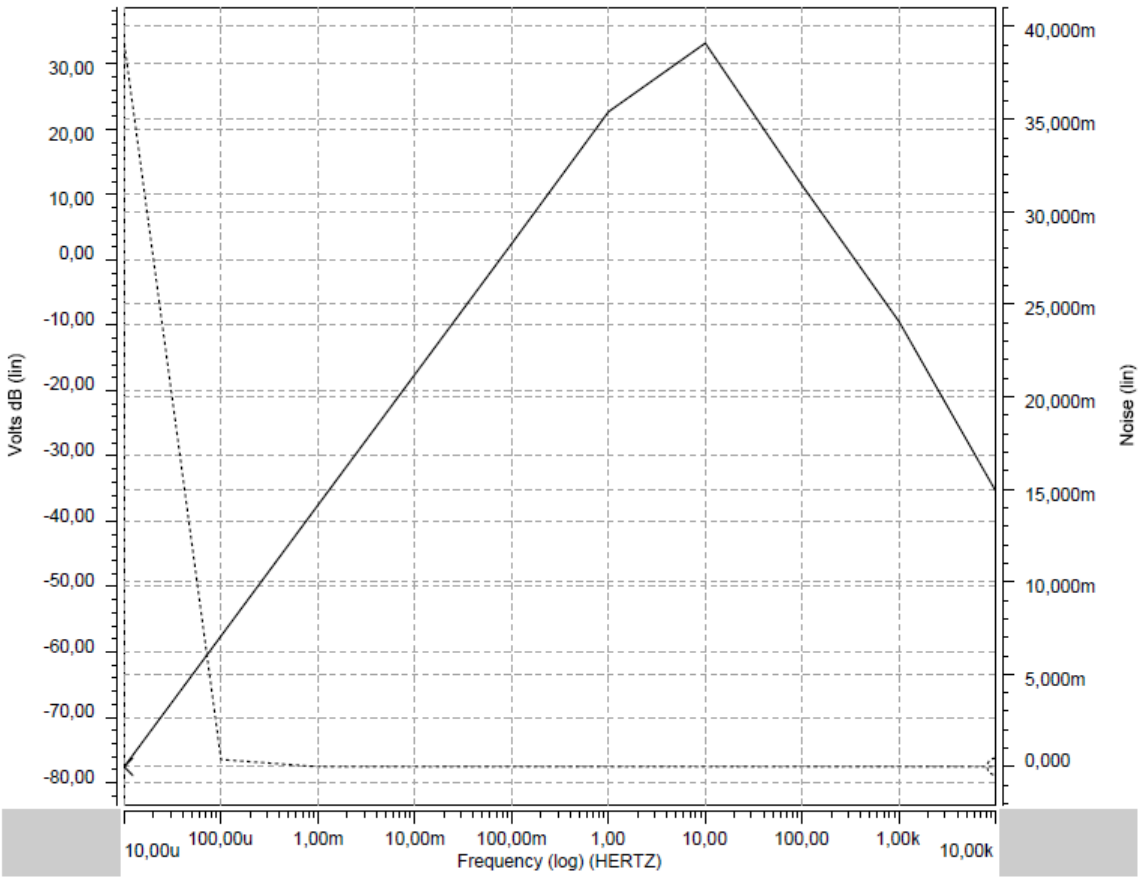

Figure 3.17. Post-layout AC simulation output of LNA input stage plus bandpass filter with 10Hz center frequency.

In Figure 3.18 post-layout transient simulation output of the bandpass filter with bandpass characteristic between 1Hz and 10Hz is given. The schematic of the simulated circuit is given in Figure 3.11. The total power consumption of the exemplar system is 7.254μW.

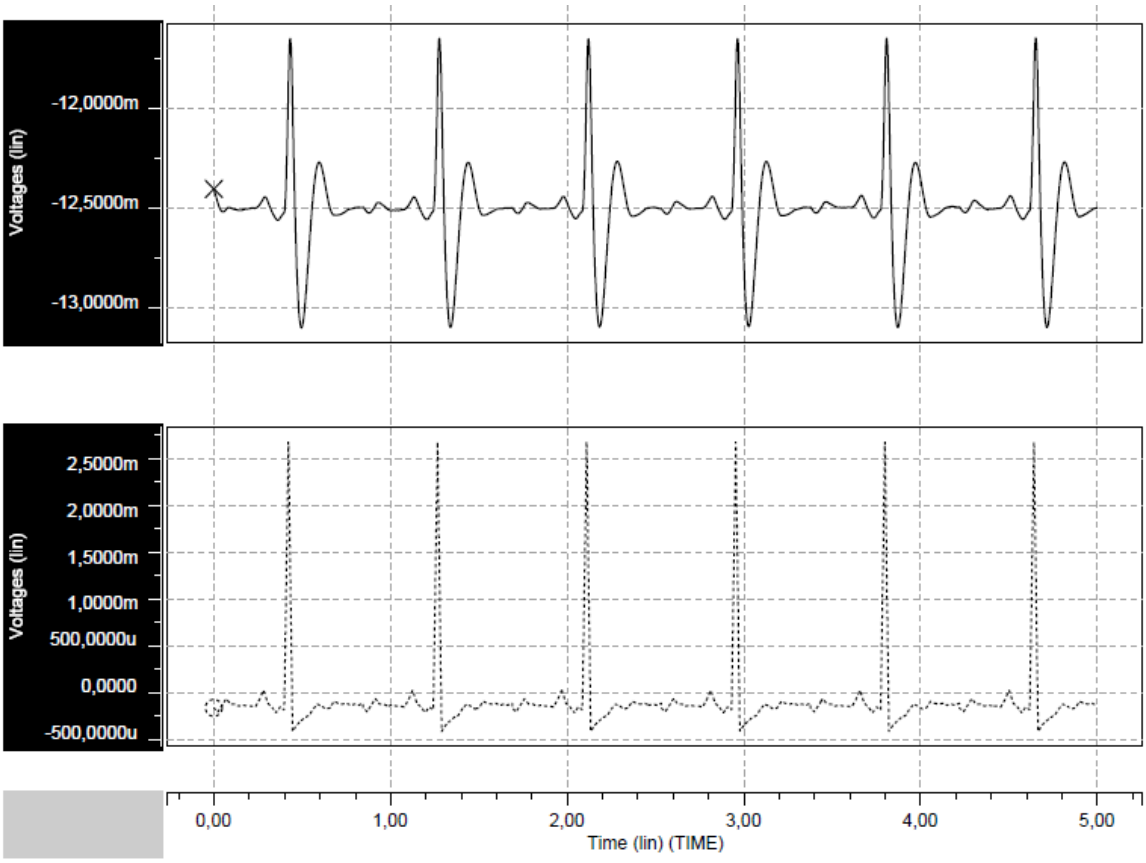

Figure 3.18. Post-layout AC simulation output of LNA input stage plus bandpass filter with 10Hz center frequency.

4. ANALOG TO DIGITAL CONVERTER

An analog to digital converter (abbreviated *ADC*, *A/D* or *A to D*) is a device which converts a continuous quantity to a discrete time digital representation. The reverse operation is performed by a digital to analog converter (*DAC*).

Typically, an ADC is an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. The digital output may use different coding schemes.

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The values are usually stored electronically in binary form, so the resolution is usually expressed in bits. In consequence, the number of discrete values available, or levels, is a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from -128 to 127 (i.e. signed integer), depending on the application.

There is large variety of ADC architectures in literature. We can classify them as follows [19];

4.1. ADC Architectures

- Comparator (1 bit ADC)
- High Speed ADC Architectures
  - (i) Flash Converters (*Paralel ADCs*),
  - (ii) Successive Approximation ADCs,
  - (iii) Sub-ranging Error Corrected and Pipelined ADCs,
  - (iv) Serial Bit-Per-Stage Binary and Gray Coded(Folding) ADCs and so on,
  - (v) Charge Run-Down ADC,
  - (vi) Ramp Run-Up ADC,

(vii) Tracking ADC,

(viii) Voltage to Frequency Converters (*VFCs*) combined with Frequency Counter,

(ix) Dual Slope/Multislope ADCs,

(x) Optical Converters,

(xi) Resolver to Digital Converters (*RDCs*),

- Sigma-Delta ADC.

4.2. Successive Approximation ADC

The successive approximation ADC is by far the most popular architecture for data-acquisition applications, especially when multiple channels require input multiplexing. The overall accuracy and linearity of the SAR ADC are determined primarily by the internal DAC's characteristics. Switched-capacitor (*or charge-redistribution*) DACs have become popular in newer CMOS-based SAR ADCs, as their accuracy and linearity are primarily determined by high-accuracy photolithography [20].

A Successive Approximation ADC uses a comparator and works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the charges induced by input and referenced voltage difference) until the best approximation is achieved.

For every step, charge induced on the capacitors updated by input voltage as initialization. In every clock cycle reference voltage is applied to capacitor array one by one, starting from MSB (which is the largest capacitor in the array). The comparator circuit compares the value on the common node of the capacitor array with ground (or another voltage reference). For example, if the input voltage is 0.8V and the reference voltage is 1V, in the first clock cycle 0.8V is compared with 0.5V (the reference divided by two. This is the output of the internal DAC when the input is a '1' followed by zeros), comparator takes the difference of this signals from capacitor array and compares this difference by ground. And, as the difference is greater than zero, comparator gives '1' to the output. This output is the input of the SAR logic. According to this comparison result, SAR keeps most significant bit (MSB) '1' and passes the next bit.

For the next step SAR applies “11” followed by zeros to the capacitor array selection pins. At this time, input node (which has charged in the initialization phase once) is compared to 0.75V. Again, the difference (0.8 -0.75 = 0.15) is compared with ground, and comparator gives ‘1’ to the SAR logic. SAR logic applies “111” followed by zeros to the capacitor array. This time, the difference $(0.8 - 0.875 = -0.075)$ is negative, so as the comparator compares this value by ground and gives ‘0’ to the output. SAR applies “1101” followed by zeros to the capacitor array. And this procedure loops until the SAR reaches the last bit. At the end of the step, SAR logic generates enable signal aligned with the data, and new input signal is sampled by the capacitor array as directed by SAR. As seen from the example, as the bit size increase the resolution increases, quantization errors decrease. This is also called bit-weighting conversion, and is similar to a binary search. The analogue value is rounded to the nearest binary value below. Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired. The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired plus initializing phase cycles.

4.2.1. Advantages of SAR ADC

- The principle behind SAR ADC is simple. It implements binary search algorithm.
- The power consumption of SAR topology is very small in compare to Pipelined and Sigma Delta Converters. Because, above mentioned topologies contain operational amplifiers. In compare to, basic comparators utilized in SAR, operational amplifiers consume more power.
- No pipeline delay (*latency*). In a pipelined ADC, the pipeline delay is a multiple of the sampling clock period. For low sampling frequencies, there will be a considerable latency. The SAR ADC can use an internal clock that is independent of (and - if desired - much faster than) the sampling clock; output codes can thus be delivered with a delay negligible with respect to the sampling clock period [20, 19].

4.2.2. SAR Topology

A SAR ADC has the following building blocks [20]:

- Sample-and-Hold Stage (S/H),
- Digital-to-Analog Converter (DAC),
- Comparator,
- Successive Approximation Register (SAR).

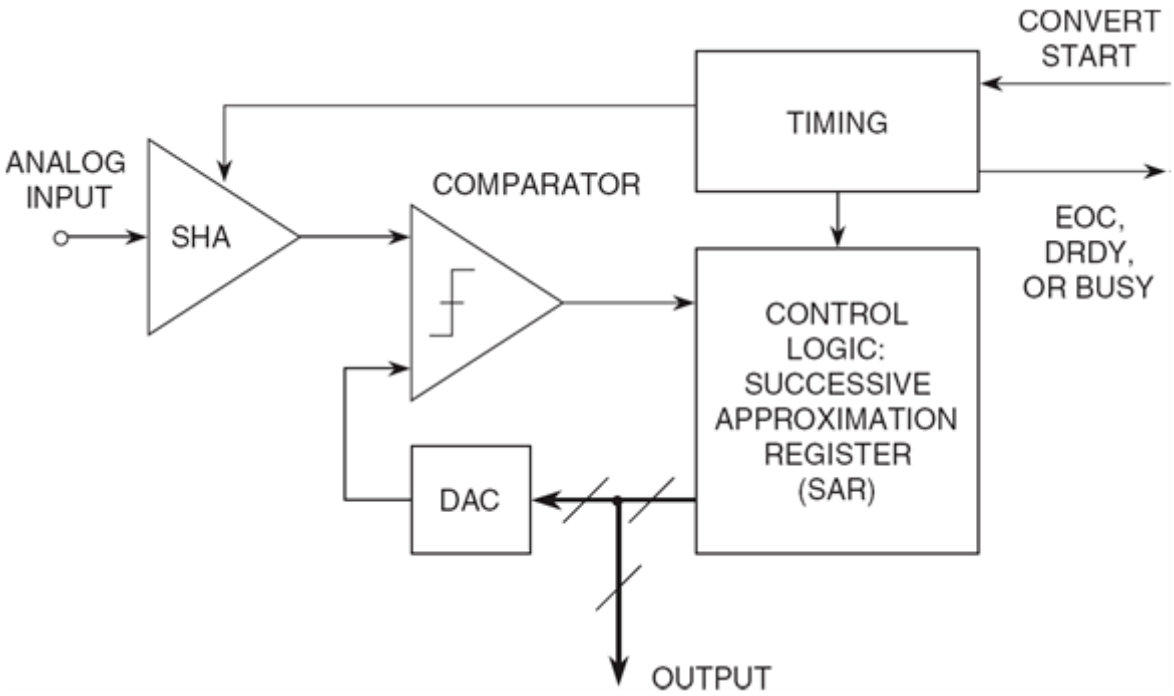

Figure 4.1. SAR ADC basic blocks and flow.

SAR ADCs can be classified according to the DAC they use. The Charge-Redistribution or Switched-Capacitor (SC) SAR ADC is by far the most popular one. It combines the S/H stage and the DAC in a single building block, a switched-capacitor array. Figure 4.2 shows a 3-bit SC SAR ADC with its binary-weighted parallel capacitor array [20, 19].

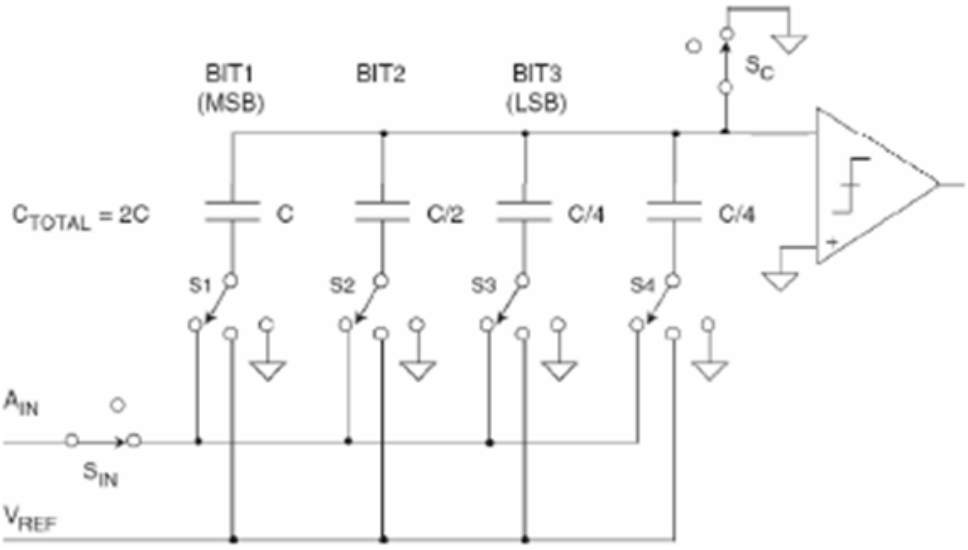

Figure 4.2. 3-bit switched capcitor SAR ADC with single-ended analog path.

The capacitor array serves as DAC and S/H stage at the same time. The SAR control logic, which is not shown here, controls the switches and takes the comparator's response as input.

4.3. Designed Architecture

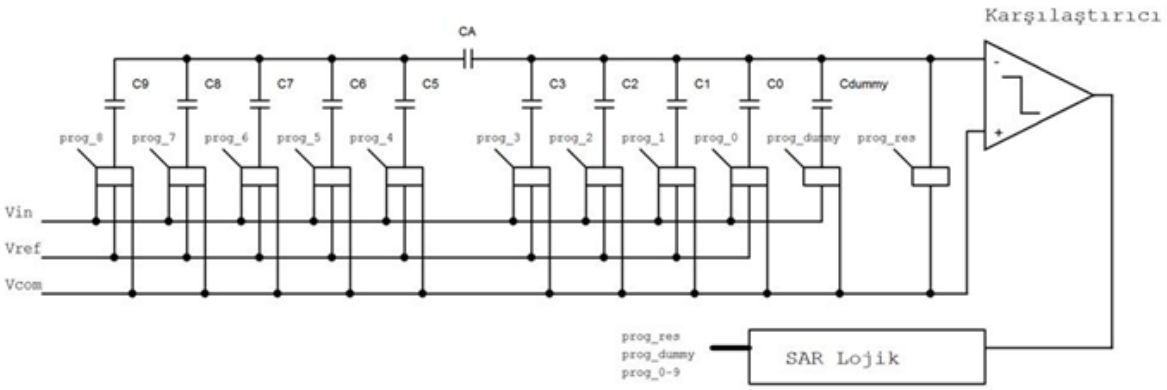

Figure 4.3. Designed ADC architecture.

Biomedical signals from the external world is required to be processed and stored for analyzing step by the person who is concerned. For many applications, these steps are realized in digital environments, especially on computers. This makes conversion of analog signals to digital equivalents very important.

As a topology, SAR (Successive Approximation Register) given in Figure 4.3 was used. For targeted application, an ADC working with 56 kHz oscillator was realized. It can be configured in order to work as 8 bit or 10 bit SAR ADC. The design specs are assumed as low frequency, low power consumption and small area.

In this structure given in Figure 4.3, data sample and hold operation is held by capacitor array. Control of the capacitor array is realized by SAR logic which is the digital part of the circuit. In the other words, SAR logic makes capacitor array working as DAC (*Digital to Analog Converter*) by selecting the line where the capacitors would connect and controlling conversion of digital signal to analog signal by producing control bit array.

4.3.1. Sample and Hold Circuit

In our design, we utilize Switched Capacitor topology as sample and hold operation, also for digital to analog conversion of the SAR Logic output. As we design ADC configurable for 8-10 bits resolution, realized circuits are given in Figure 4.6,

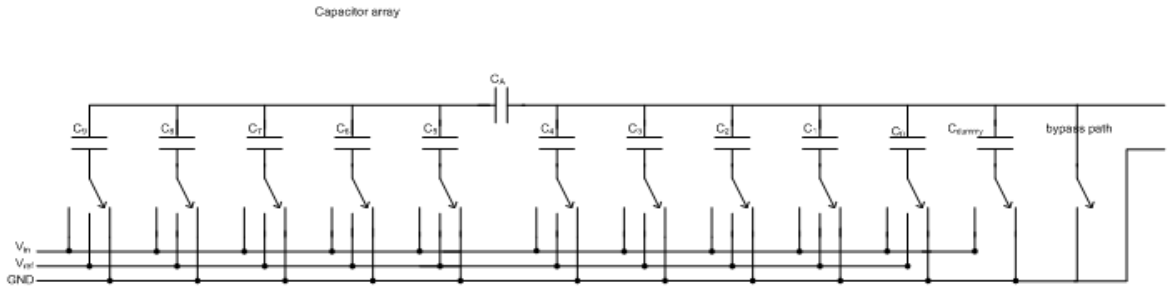

Figure 4.4. Schematic of sample and hold circuitry which also works as DAC.

4.3.2. Comparator

Designed comparator is given in Figure 4.5. For every comparison reset pin needs to be released, so as to align comparison output with SAR logic, falling edge of the clock signal used in SAR has utilized.

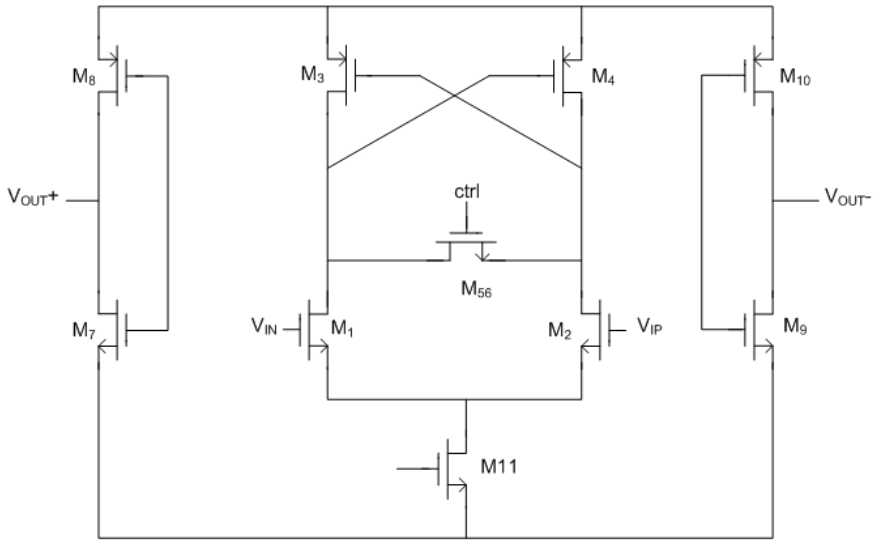

Figure 4.5. Schematic of comparator circuit.

In Figure 4.5, comparator circuit was given. Comparator makes comparison between potential stored on capacitor array and common mode. If the potential stored on the capacitor array is bigger than the common node, it will pull the output to ground, thus SAR logic decrement the bit array given to the capacitor array one. When the potential stored on the capacitor array is smaller than the common node, SAR logic increments the bit array applied to capacitor array one. Bit array which is the output of the SAR logic is at the same time, the converted digital output. Therefore, for every clock cycle a signal converted to digital from analog is acquired. Average total power consumption of analog blocks of ADC is 703nW.

4.3.3. SAR Logic

SAR Logic is coded in VHDL. It works with rising edge of the clock. Total latency for 10 bit configuration is 14 clock cycles, and for 8 bit configuration 12 clock cycles. Operational frequency dependents on Nyguist sampling rate criteria. As we use this design for processing biomedical signals which are assumed below 1 kHz, According to Nyguist criteria we have to sample data at 2 kHz (minimum). To guarantee, error free operation clock frequency of the circuit is selected as 56 kHz.

4.4. Simulation Results

Simulation results and performance measurements are given below;

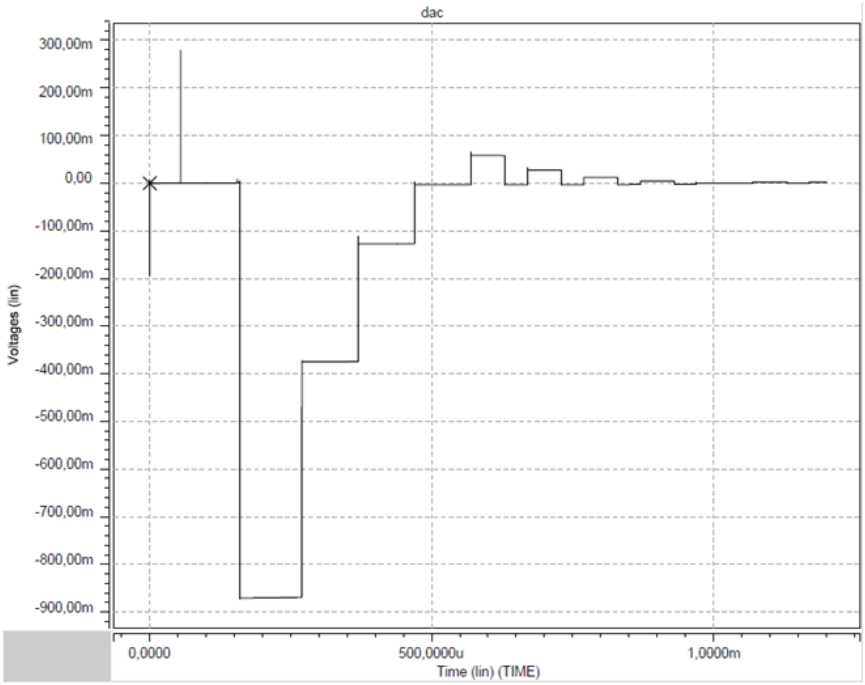

Figure 4.6. Comparator circuit that is cascaded with Sample and Hold (DAC) circuit, output response for 0.88 V input by 10 bit conversion configuration.

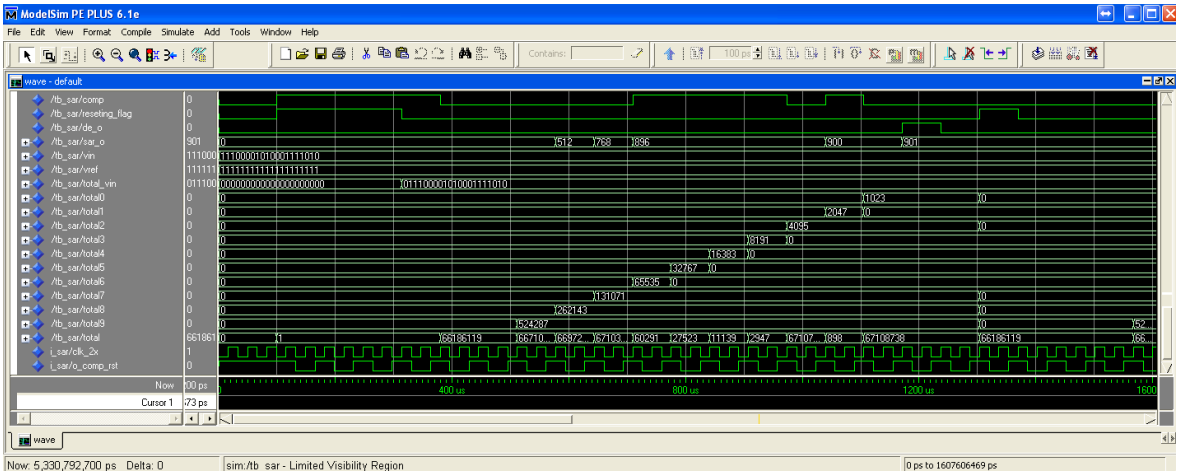

Figure 4.7. Simulation of SAR ADC by ModelSim. Analog part of the circuit is modeled in VHDL with more than 30 bits of accuracy.

5. PROGRAMMING LOGIC

Main processing blocks of the FPAA are low noise amplifiers, filters, analog to digital converters. For different applications each block must be configured. By configuring the blocks, the frequency operating range, gain, power consumption, filter types, digital conversion resolution and module bypass options can be altered.

As mentioned in the previous chapters, each block has been designed compatible with programmability, as a summary of previous chapters and the working principle of how to program the blocks;

Low noise amplifiers are the input stage of the FPAA. And low amplitude signals are amplified before filtration and the other blocks. The gain of this amplification stage should be tuned uniquely for the input signal type for correct operation. The gain of the LNA structure that we built can be changed by changing the G_m (transconductance) of the OTA used in LNA and changing the capacitor values connected to the LNA. G_m of the OTA is set by changing the bias current of the OTA. The bias current is controlled by the Bias Cell mentioned in Chapter 6. Also capacitor values connected to the LNA can be changed by the Switch Cell mentioned in Chapter 6. Programming logic sets the switch cell and bias cell for intented use of the LNA.

Filters are the part where unwanted frequency components of the signal is removed to enhance the wanted ones. Setting the filtering frequency range and the type of the filter can be set by programming logic. Firstly, to change the cut of frequency of the filter, programming logic should set the Bias Cell. The bias cell controls the bias current of the OTA and G_m value of can be set tot he required value. Secondly, filter type and filtering frequency should be set by programming the switch cell to select the required capacitor values for the filter.

5.1. Programming Circuit

Requirements of the design should be calculated by the user for the specific application and FPAA should be programmed. As mentioned above, in order to program the blocks, structure utilize switch cells. These switch cells must be set to the required value that is calculated for the application from outside world. To communicate with the outside world, there are some data transfer protocols. One of the most popular one, which is used almost all computer communications, is I2C.

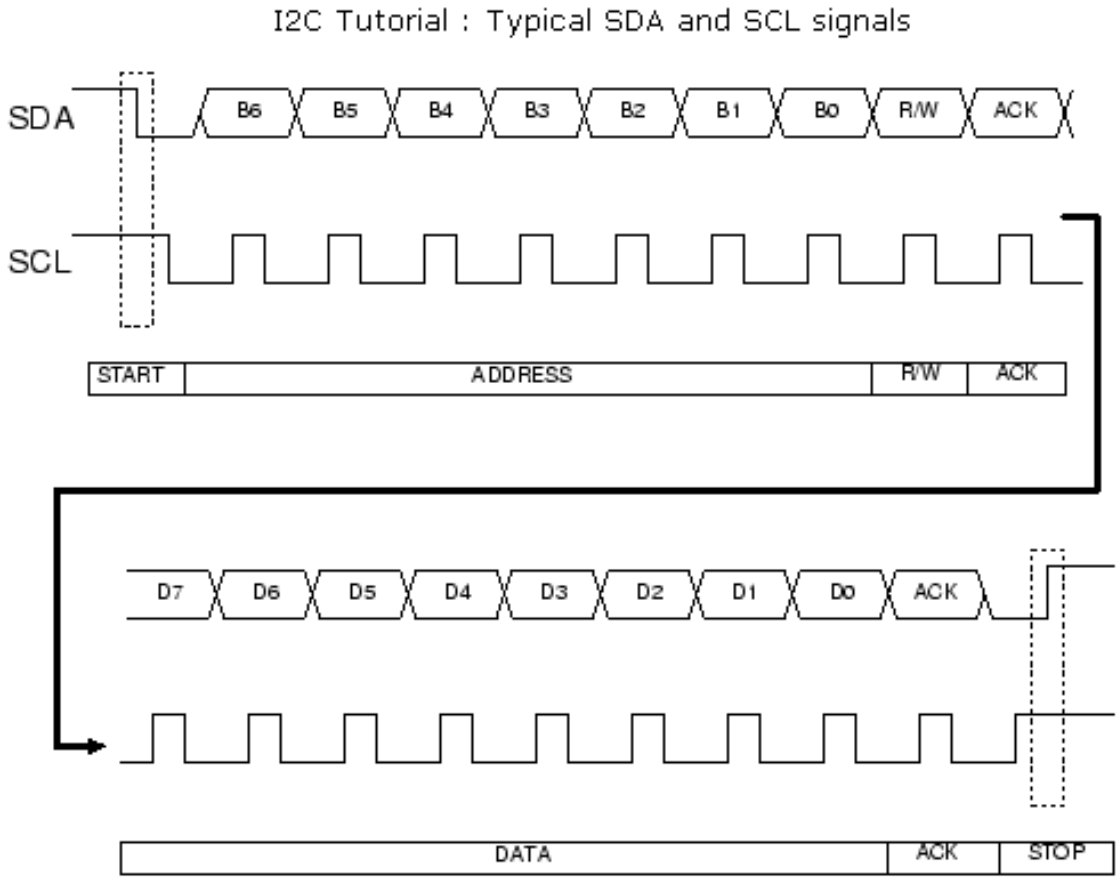

Figure 5.1. I2C signal flow.

I2C created by Philips Semiconductors and commonly written as (*I2C*) stands for Inter-Integrated Circuit and allows communication of data between I2C devices over two wires. It sends information serially using one line for data Serial Data (*SDA*) and one for clock Serial Clock (*SCL*). The Phillips I2C protocol defines the concept of master and slave devices. A master device is simply the device that is in charge of the

bus at the present time and this device controls the clock and generates START and STOP signals. Slaves simply listen to the bus and act on controls and data that they are sent. The master can send data to a slave or receive data from a slave - slaves do not transfer data between themselves. Standard clock speeds are 100kHz and 10kHz but the standard lets you use clock speeds from zero to 100kHz.

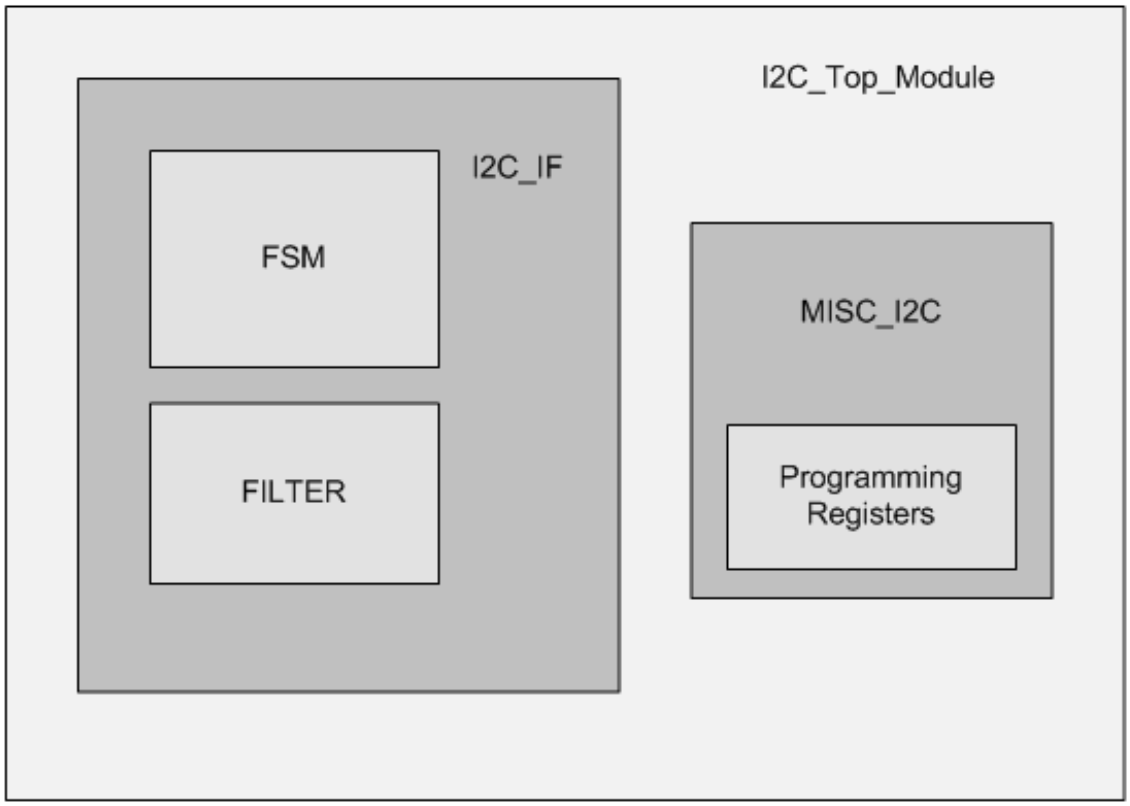

Figure 5.2. I2C modules.

FPAA utilizes I2C Slave Module for communication with outside world. This I2C module contains; I2C Input Filter; for safe sampling of the input I2C data, I2C FSM ; a finite state machine for data capturing, I2C IF ; for address and data decoding, I2C Misc Params ; to register the datas and addresses for transferring these data to switch boxes and I2C Top Module ; for wrapping the sub-modules and control the programming operation.

I2C module ,with programming control inside, is implemented in VHDL. And layout of the circuit is drawn in ICStudio. Layouts the the circuits is given below;

Figure 5.3. I2C input filter layout.

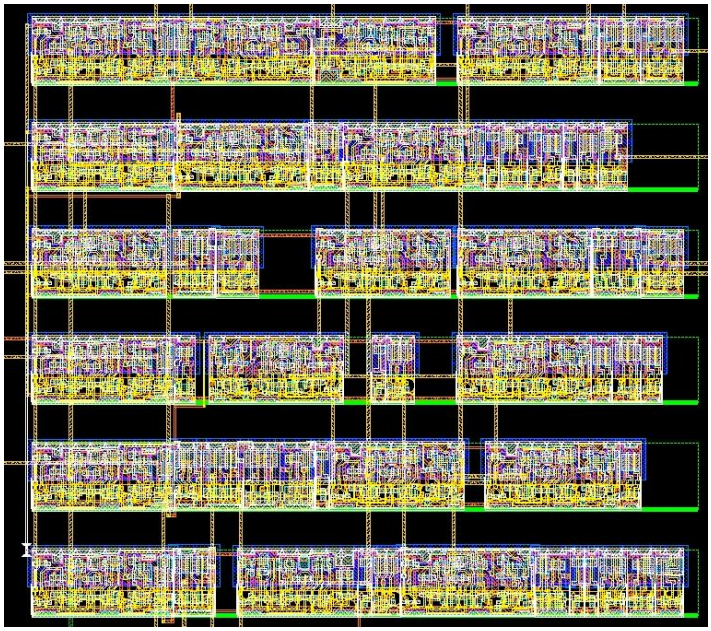

Figure 5.4. I2C FSM layout.

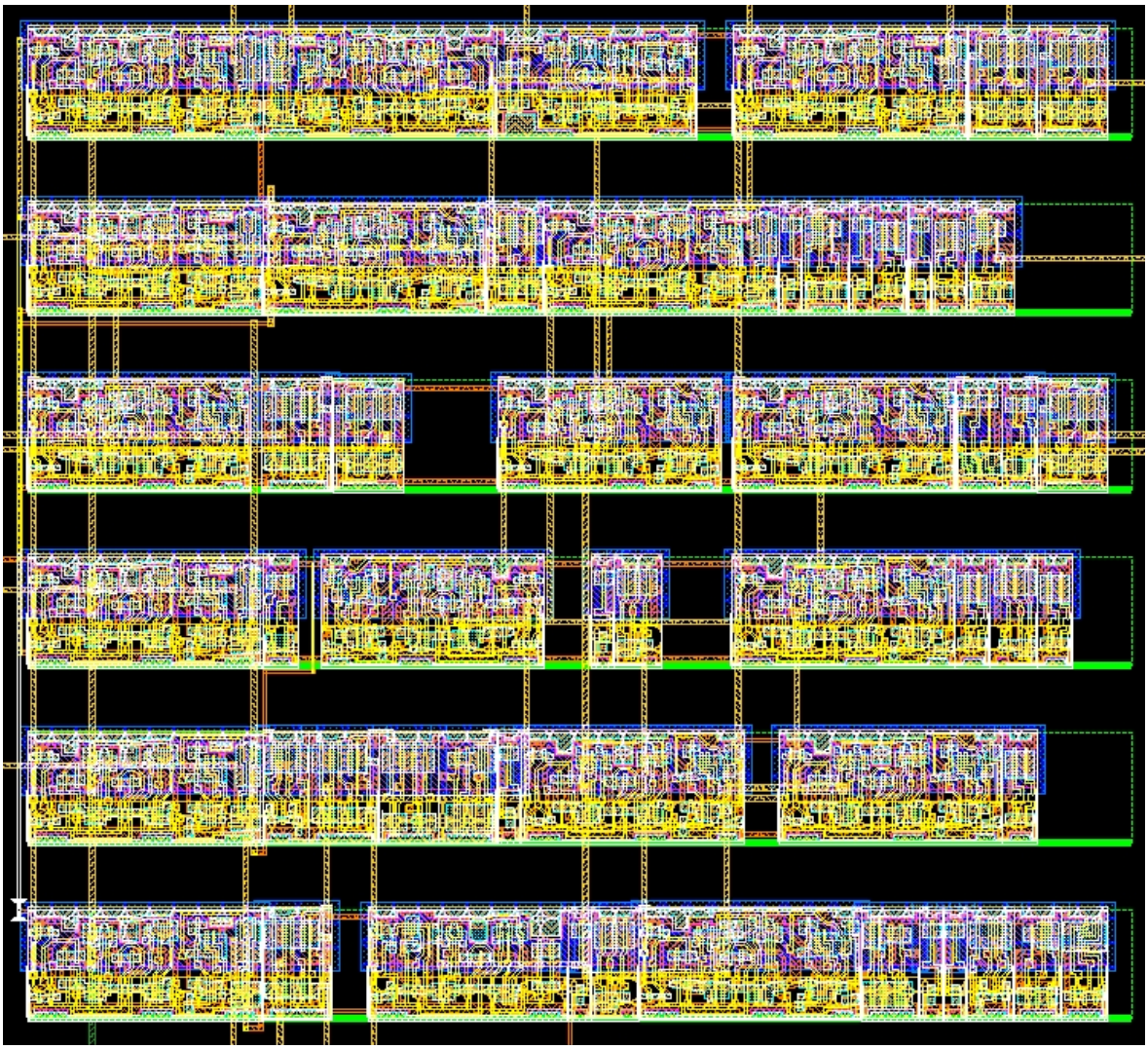

Figure 5.5. I2C interface layout.

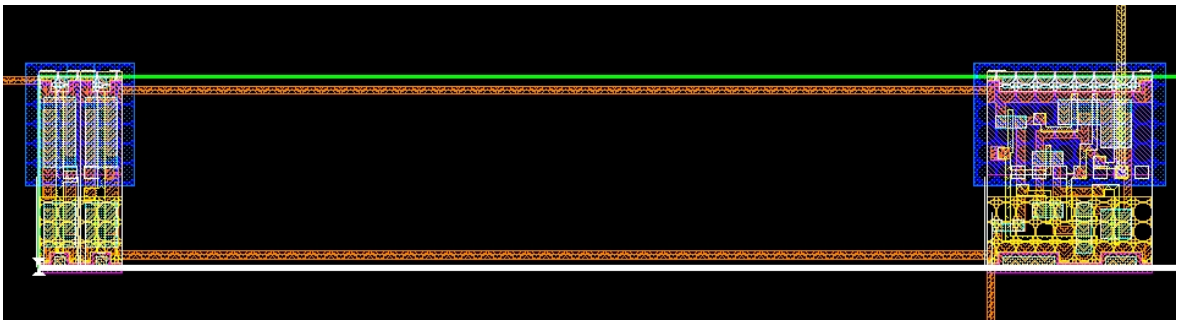

Figure 5.6. I2C top level layout.

6. MISCELLANEOUS BLOCKS

Besides the main blocks mentioned in previous chapters, there are two other building blocks. One of them is Switch Cell and the other one is Bias Cell. In Chapter 5, purposes of this modules in programming function and in Chapter 2, 3, 4 operating function have mentioned.

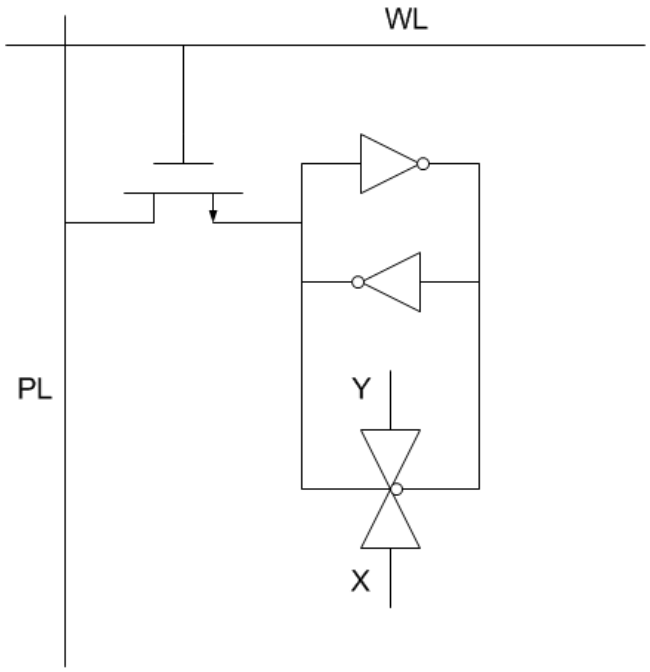

Figure 6.1. Schematic of switch.

6.1. Switch Cell

Switch Cell is the selectable(programmable) interconnection circuitry that is utilized all around the chip on the every interconnection point. Switch cell is a basic circuit and same as a SRAM cell. Circuit contains one driving NMOS, two inverters and one transmission gate shown in Figure 6.1. WL and PL in the figure are Word Line and Bit Line respectively also X and Y is the switching line.

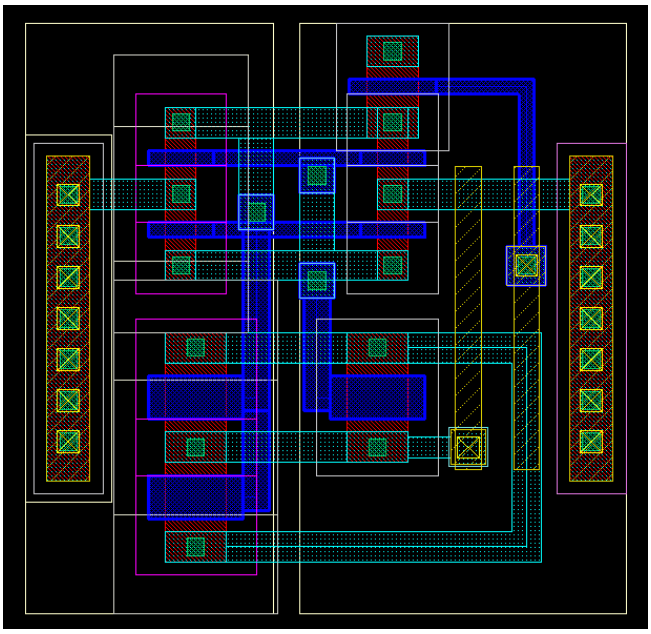

Figure 6.2. Layout of switch cell.

Layout of the designed switch cell is given in Figure 6.2. And the post-layout simulation result is given in Figure 6.3 below.

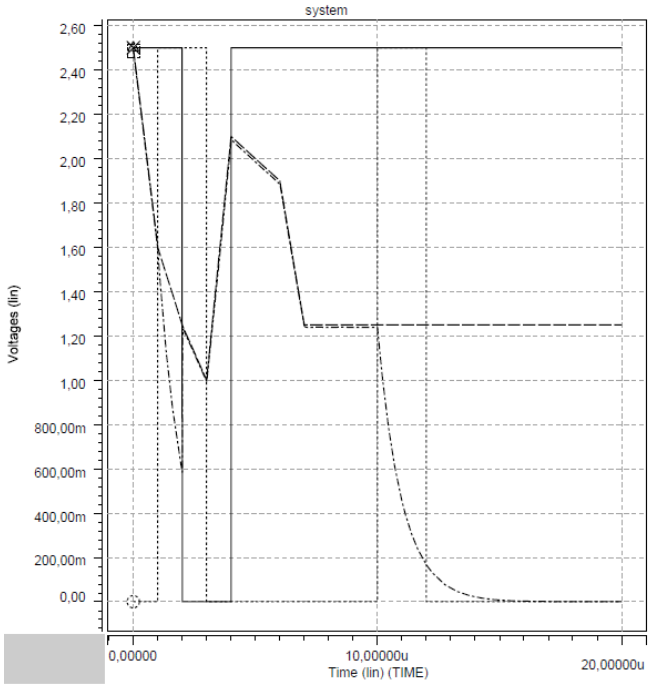

Figure 6.3. Post-layout simulation result of switch cell.

As seen on Figure 6.3, as the PL is on and WL is '1' switching X follows Y.

6.2. Bias Cell

Bias Cell is the selectable(programmable) bias current generation circuitry that is utilized all around the chip nearby every programmable block. Bias cell is a basic circuit and same as a current source. Circuit contains four transistors and three switch cell shown in Figure 6.4. Circuit working principle is basic current division. Current flowing from VDD to VSS is controlled by VINa and current over each PMOS is proportional to the width of the transistor. Programming logic controls the switch boxes. If the switch box is open current flows through it to the NMOS in the output stage. Output transistor is diode connected and gate of this transistor acts as VOUT which is the reference voltage for the programmable analog blocks.

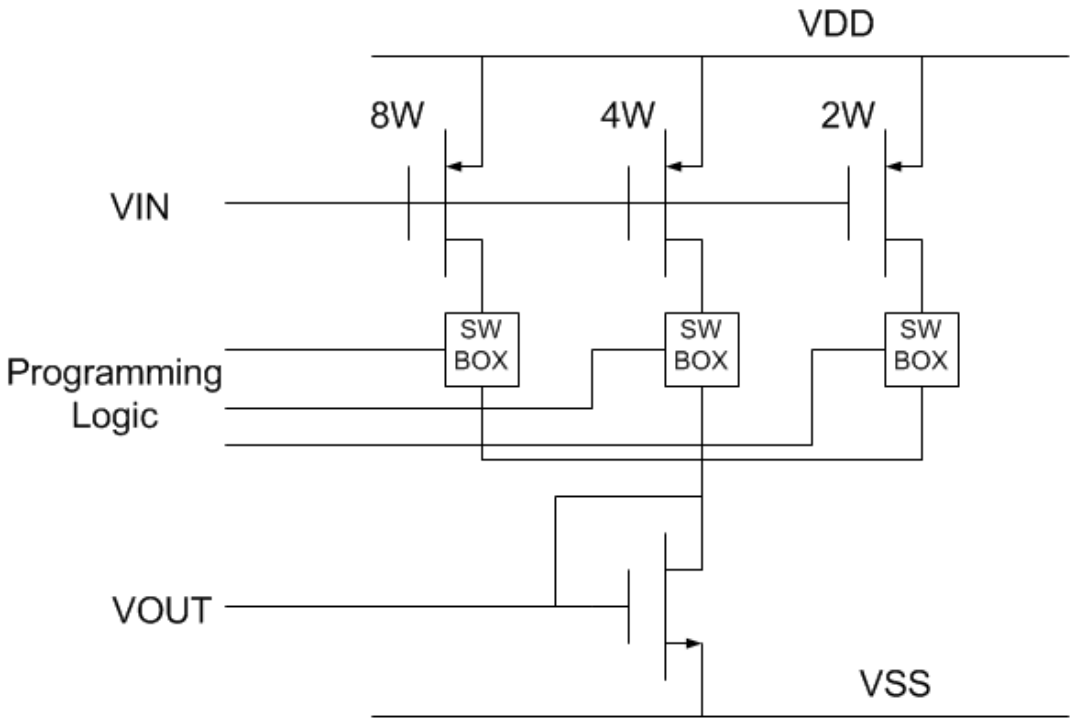

Figure 6.4. Schematic of bias cell.

Layout of the designed bias cell is given in Figure 6.5. And the post-layout simulation result is given in Figure 6.6 below.

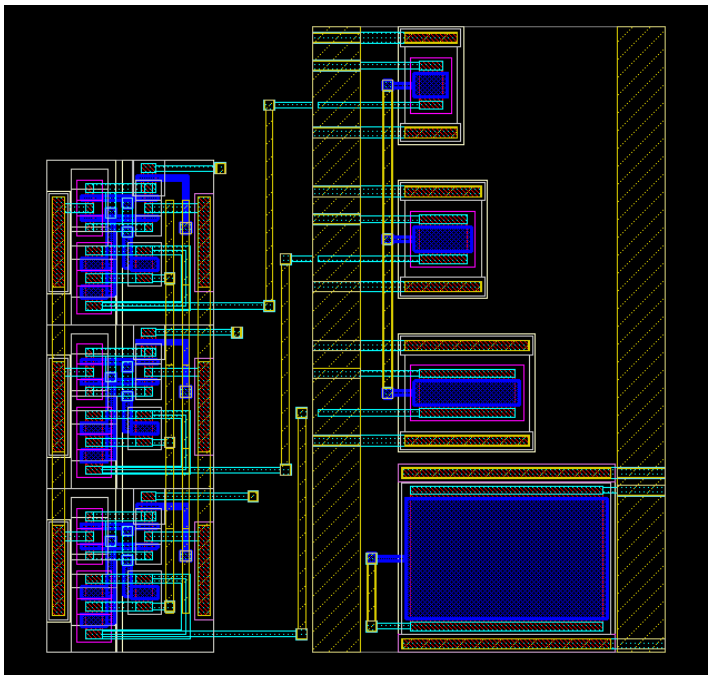

Figure 6.5. Layout of the bias cell.

As seen on Figure 6.6, voltage through the output transistor doubles as the switch cells becomes on, one by one.

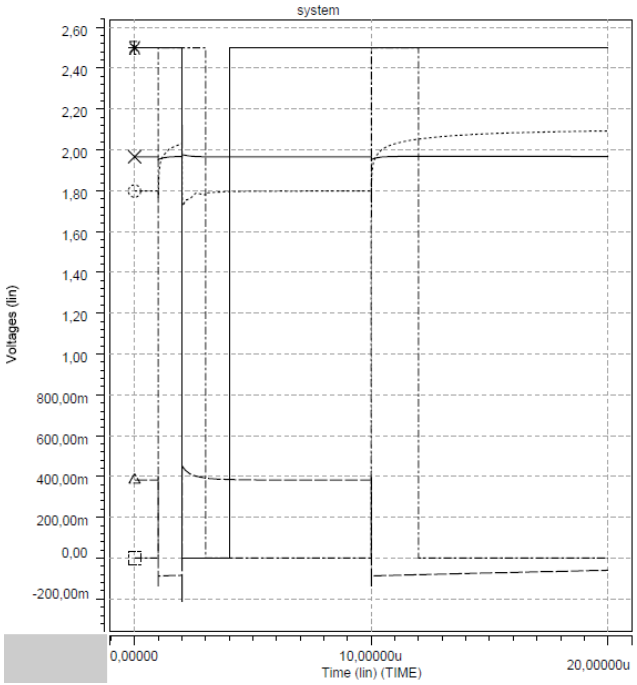

Figure 6.6. Post-layout simulation result of bias cell.

7. OVERVIEW OF THE DESIGNED FPAA STRUCTURE

The main blocks of the FPAA are Programmable Interconnection Network and Configurable Analog Blocks (CAB).

Interconnection network is a group of lines between the CABs to build the all possible connections. Switch cells mention in Chapter 6 take place in every connection point of this net to make the connections under control of programming logic mentioned in Chapter 5.

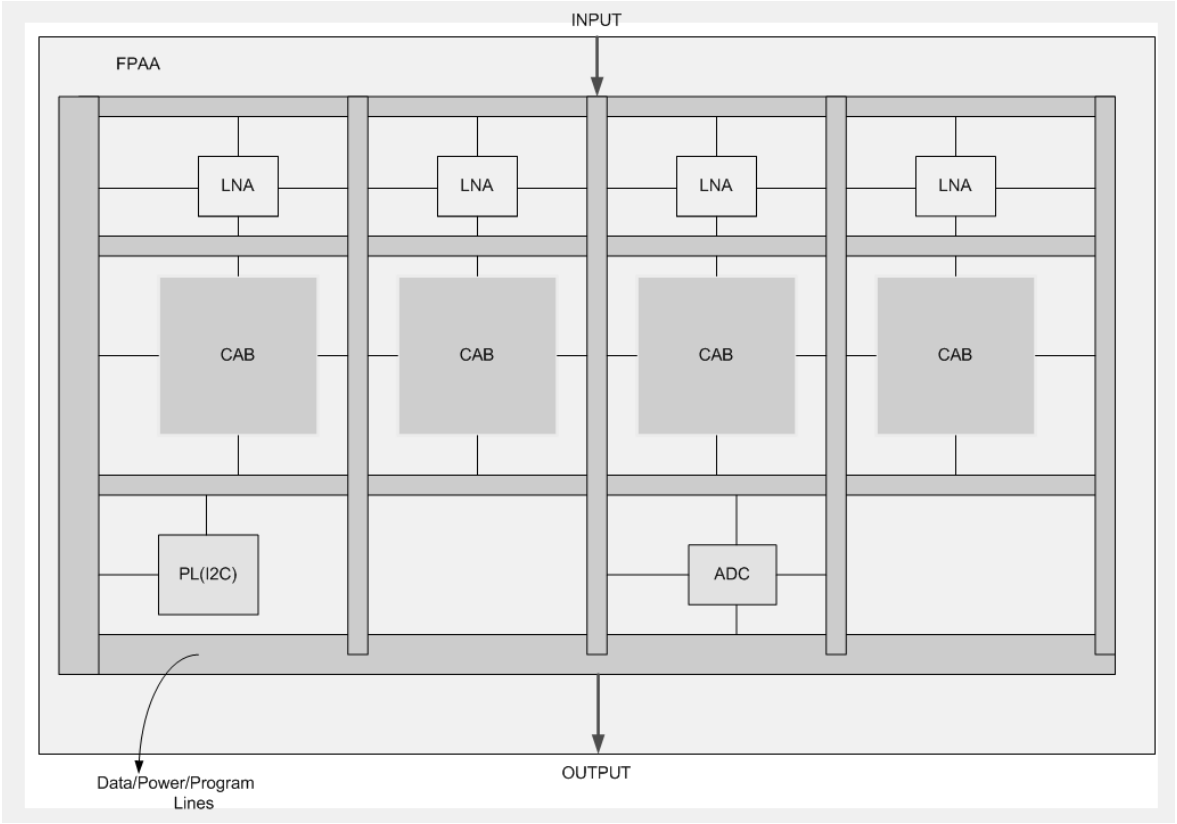

Figure 7.1. Structure of FPAA.

Figure 7.1, shows the top level view of our FPAA structure. Data/Power/Program Lines mentioned in the figure are the interconnection network. This network has switches at every connection point of every row and column. By the help of programming logic, required rows and columns can be connected. Programming logic

block is shown in the figure by PL(I2C). PL(I2C) also communicates with the outside world for programming operation by using I2C protocol.

Configurable analog blocks contain one or more basic building blocks such as amplifiers, integrators, filters, comparators and converters. The components of the CAB vary from FPAA to FPAA according to the needs of application field of the FPAA.

In our design, CAB contains OTAs and capacitors. By the combination of these blocks, required filter structures are constructed. Inside the CAB, the connection between the OTAs and the capacitors and also the selection capacitors and biasing of the OTAs are controlled and programmed through the interconnection network by the moderation of programming logic block.

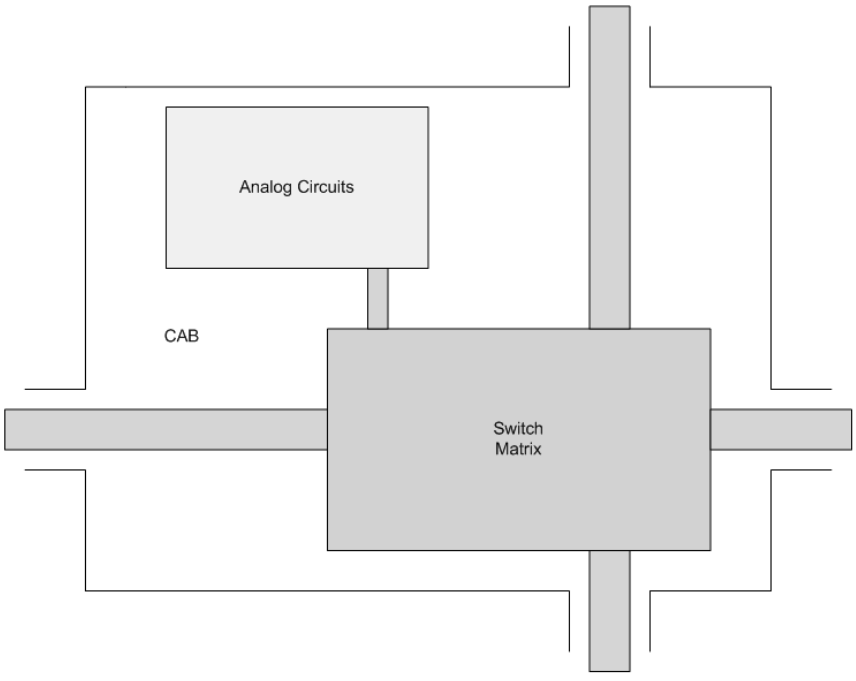

Figure 7.2. Structure of programming network inside the CAB.

Figure 7.2, shows the switch matrix connection with the analog circuits inside the CAB.

8. CONCLUSION AND FUTURE WORK

In this study, design of the blocks which could be used for Field Programmable Analog Array architecture, optimized for low frequency applications is presented. Besides the main aim that is designing a programmable structure for capturing and processing signals at low frequency, low noise and low power consumption can be said as the other main concerns.

As the output of this study, configurable LNA structure for different gains with low noise levels, programmable filters done by sub-threshold and active OTAs with selectable capacitor arrays and ADCs which can be selected as 2 different resolutions have been realized. As the biomedical applications have selected for target application, design was optimized for the signals which have frequency range 0.5Hz - 1kHz and amplitude range 1uV - 10mV.

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