NEW APPROACHES TO AUTOMATED ANALOG CIRCUIT DESIGN FOR ROBUSTNESS

by

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ABSTRACT

NEW APPROACHES TO AUTOMATED ANALOG CIRCUIT DESIGN FOR ROBUSTNESS

This thesis presents different simulation-based analog circuit synthesis methodologies to obtain robust circuit synthesis and their results. HSPICE is used as simulator and SACSES is used as general methodology for mentioned simulation based approach. Three distinct methods are acquired by making modifications in SACSES algorithm. All these three methodologies use sensitivity analyses which are done at some certain points in the process. In the first method, achieved sensitivity results are used for calculating new costs of every individual circuit. Second and third methods are based on respectively additive and multiplicative error terms whose boundaries are attained by sensitivity analyses. Said three methods are tested on different three circuit topologies and results are compared. Furthermore some changes are made on SACSES and the consequences are examined.

ÖZET

ANALOG GÜRBÜZ DEVRE TASARIM OTOMASYONU İÇİN YENİ YAKLAŞIMLAR

Bu tezde gürbüz devre tasarımı elde etmek amacıyla benzetim tabanlı yöntem dizileri ve bu yöntem dizilerinin sonuçlarına yer verilmektedir. Benzetim tabanlı yapıda, benzetici olarak HSPICE, genel yöntem dizisi olarak ise SACSES kullanılmaktadır. Gürbüz devre tasarımı amacıyla SACSES üzerinde çeşitli degişiklikler yapılarak üç adet yöntem elde edilmiştir. Kullanılan üç yöntem de süreç sırasında belirli noktalarda yapılan duyarlılık analizlerinin sonuçlarına dayanır. İlk yöntemde, elde edilen duyarlılık değerleri olası en kötü maliyeti hesaplamak için kullanılır. İkinci ve üçüncü yöntemlerde ise sırasıyla toplamsal ve çarpımsal hata terimleri için bir hedef belirlemek için kullanılarak farklı bir eniyileme metodu denenmiştir. Bahsedilen bu üç yöntem, üç ayrı devre üzerinde denenerek sonuçları alınmış ve karşılaştırılmıştır. Ayrıca SACSES üzerinde ufak degişiklikler yapılmış ve bu degişikliklerin sonuçları irdelenmiştir.

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LIST OF SYMBOLS

A_{V_T}	Technology Dependent Constant for Threshold Voltage
A_K	Technology Dependent Constant for Current Factor
b_i	Bad Limit for an Output
C_{av}	Average Cost
$C_{penalty}$	Penalty Cost
C_{perf}	Performance Cost
g_i	Good Limit for an Output
K	Current Factor
k_{sat}	Saturation Coefficient for Safety Margin in Biasing
k_{th}	Threshold Coefficient for Safety Margin in Biasing
L	Length of a Transistor
$p_{cut-off}$	Penalty for Cut-off Region
p_{triode}	Penalty for Triode Region
R_{out}	Output Resistance
T	Population Temperature
t_{ox}	Oxide Thickness
V_T	Threshold Voltage
W	Width of a Transistor
$w_{penalty}$	Penalty Weight
β	Current Factor
λ	The Number of Offsprings
μ	The Number of Parents
ε_{ox}	Electron Permittivity of Silicon Dioxide

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternative Current
BTS	Basic Two Stage
BW	Bandwidth
dB	Decibel
DC	Direct Current
DOE	Design of Experiments
DRC	Design Rule Check
EA	Evolutionary Algorithm
ES	Evolutionary Strategies
FC	Folded Cascode
FOM	Figure of Merit
GA	Genetic Algorithm
LVS	Layout Versus Schematic
OPAMP	Operational Amplifier
PM	Phase Margin
SA	Simulated Annealing
SACSES	Simulation Based Analog Circuit Synthesizer Using Evolutionary Strategies
SPICE	Simulation Program with Integrated Circuit Emphasis

1. INTRODUCTION

1.1. Analog Design Flow

With the invention of the transistor in 1947, and production of the integrated circuits, a new age has begun. Since then, electronic circuits have become an important part of our lives. They take place in various sectors such as communication, automotive, information, and many others. As these circuits get more versatile and harder to design, they tend to have more complex topologies and contain greater number of transistors. Thus, the workload and the time spent in the process of circuit design increases.

Design automation plays a major role in diminishing the amount of time spent in the circuit design process and removing the burden from electronic engineers. Unlike analog design, usage of automation has become very common in digital circuit design. However, since the world is analog, it is not feasible to eliminate the analog part of integrated circuit design. The analog design flow proposed in [1] contains system, circuit and layout level synthesis as shown in Figure 1.1.

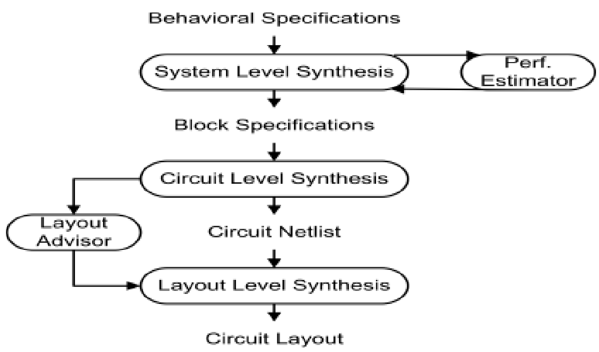

Figure 1.1. The analog design flow.

System level design is responsible for the bond between required specifications and the lower level blocks. Therefore, it should have information about block specifications used in the lower level and this information is obtained by a performance estimator.

In the layout level design, the schematic becomes ready to manufacture. This physical conversion is done via some layout synthesizers which use Design Rule Check (DRC) and Layout Versus Schematic (LVS) for verification.

Circuit level design constitutes the core of the analog design flow. In this stage, the circuit is sized to accomplish required specifications. While sizing a circuit, widths and lengths of transistors, values of reference currents, voltages, capacitors and resistances are arranged. This part is done by engineers who have an experience in analog circuit design and generally the process comprises a series of iterations conducted by an engineer to reach given criteria.

1.2. Optimization

Manual work mentioned above means a serious loss of time for the general design process. Moreover, a handmade design is open to many kinds of human errors. Consequently, an automated circuit design is far more reasonable considering design robustness and time management. However, even though optimization based synthesis is more preferable to knowledge based synthesis, a human centered process, guaranteeing a better performance in a shorter period, there are still some critical issues related to the optimization algorithm. Since the solution space to search is not smooth and can include many local optimum points, not to attain a global optimum point without sticking to a local solution is a significant problem to overcome. In other words, utilizing the right search algorithm with the right selection criteria is quite critical.

1.3. Robustness

Another important phenomenon to consider during design process is the degradation of performance due to variability and aging. A sized circuit, which satisfies the required goal according to simulations, may not ensure the same performance because of flaws induced by the fabrication which can be analyzed under the process variability and mismatch category [2]. In addition to the fact that performance of a circuit does not remain stable in time due to physical characteristics of the materials used in manufacturing the integrated circuit which is aging. Eventually, generating a robust circuit, the design process should be carried out considering all performance degrading factors which a circuit can encounter.

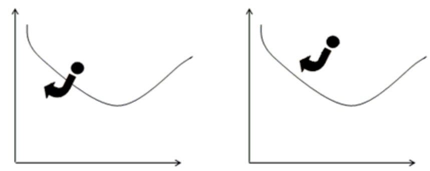

Figure 1.2. Performance degradation of a circuit due to variability and aging.

1.4. Objective of the Thesis

The objective of this thesis is making some improvements on a given automated simulation (HSPICE) based circuit synthesizer (SACSES) and to create three different methods by modifying SACSES considering the robustness of the circuits designed in terms of insensitivity to mismatches and process variations. Main contributions are listed below.

- The existing system, which is a simulation based automated design synthesizer which integrates SACSES with HSPICE, has been accelerated.
- In order to have a better performance, some changes have been made in selection system.
- Three new methodologies have been developed to design robust circuits consid-

ering variability issues.

The organization of this thesis is as follows:

Chapter 2 gives information related to previous studies which are the base optimization algorithm and its application on MATLAB. Moreover, a general knowledge about optimization methods to ensure robustness is presented.

Chapter 3 describes three different methodologies developed to design a robust circuit.

Chapter 4 presents simulation results of these three different methodologies on different topologies.

Chapter 5 concludes the thesis.

2. BACKGROUND

2.1. Background Information

Analog design synthesis can be examined under three main categories, namely knowledge based, equation based, and simulation based. Knowledge based synthesis is based on background knowledge and experience of the designer. For each topology, a different design solution is obtained by the designer. OASYS [3] and BLADES [4] can be given as examples for this kind of approach. Although the tools above are fast at synthesis, results are generally inaccurate. Topology dependence is another important disadvantage of knowledge based approach.

Analytic equations are used for circuit evaluation in equation based synthesis. Some examples for this kind of approach can be given as OPTIMAN [5] and AMGIE [6]. Even if this method is fairly fast for less complex topologies, growth in number of terms in the transfer function due to increasing complexity is an important problem. Some simplification methods can be used at the cost of decreasing accuracy. This handicap leads us to simulation based synthesis.

In simulation based synthesis, the circuit is evaluated with the aid of a circuit level simulator. Many simulation based tools use commercial simulators. For example, the tool described in [7] uses CADENCE Design Framework. HSPICE is used by GPOBCAD [8] and Eldo is used by the [9] with an algorithm-based optimizer. In this thesis, HSPICE is used because of its reliability.

Simulation based approach uses a SPICE netlist where the information about the transistors and all other elements in topology and their connections are present. Optimization algorithm is responsible for reaching the optimal solution deciding transistor dimensions and values of other components in the circuit. The search algorithm of the synthesizer is quite significant, because of the solution space to scan being rugged and vast.

A synthesizer starts from a randomly sized circuit and tries to find a general optimum point. Thus, a global search algorithm should be utilized. Evolutionary algorithms (EA) like genetic algorithms (GA) and evolutionary strategies (ES) and simulated annealing (SA) are the ones mostly in use for synthesis of analog circuits due to their global optimization property.

In simulated annealing, system processes points one by one at each step. In every selection, the algorithm decides between moving to a neighbor position or staying in a probabilistic manner. Using a temperature concept, accepting worse solutions other than the best ones is also possible. In this way sticking to local optima instead of searching for the global optima is prohibited. System guarantees best solution, however can take a very long time. Also, the behavior is highly dependent on the cooling schedule. That's why faster techniques such as very fast annealing [10] exist.

Unlike SA, genetic algorithms have the advantage of parallel searching. A generation of solutions is evaluated together instead of individually, which reduces the time spent significantly. The population of individuals is changed by recombination and mutation factors with the control of selection mechanism. Preventing the system from not converging due to over diversity or converging to a local optimum point is the main issue.

Evolutionary strategies can be seen as an extension to GA. Since transistor dimensions and the other values to be determined are continuous, ES can be very useful unlike GA. Self-adaptation of the design parameters, which can be used in continuous domains, is another feature of ES to utilize.

In this thesis, a combination of ES and SA is used [1]. Boltzman selection mechanism of SA is integrated with the selection stage of ES. At the beginning, the temperature is high, so that individuals worse than average are also welcomed. As the search proceeds, temperature gets lower and the system looks for the better individuals to reach the global optimum. Thus, focus and diversity are determined dynamically in the search process to prohibit sticking to a local optimum or not converging to an optimum point.

2.2. Optimization Algorithm

The algorithm which is used in this thesis is a modification of SACSES integrated with MATLAB using HSPICE as simulator. In this part, optimization algorithm of SACSES, will be described. The general flow of this synthesizer is given in Figure 2.1.

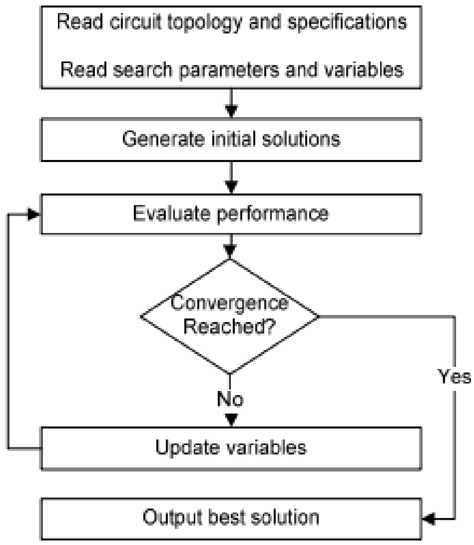

Figure 2.1. The general flow of this synthesizer.

The optimization algorithm tries to find the best solution considering determined desired goals from the circuit by changing the design parameters of the circuit which are dimensions of transistors, values of current, voltage sources, capacitors, inductors, and resistors. The sized circuit is sent to HSPICE, and AC and DC analyses are performed on the circuit. The outputs are read from HSPICE and evaluated in MATLAB by the algorithm to reach the global optimum point of the solution space [11].

Initially, circuit topology is read from the SPICE netlist. After that search parameters such as generation size, penalty weight and number of parents and offspring are read from the system. Initial values are obtained by the algorithm and the evaluation begins. Searching continues until the convergence criterion is ensured. In the

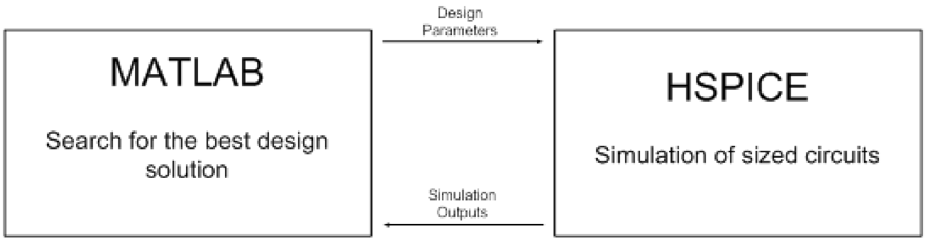

Figure 2.2. The connection between HSPICE and MATLAB.

process, generations and their coefficients are updated and evaluated in a loop.

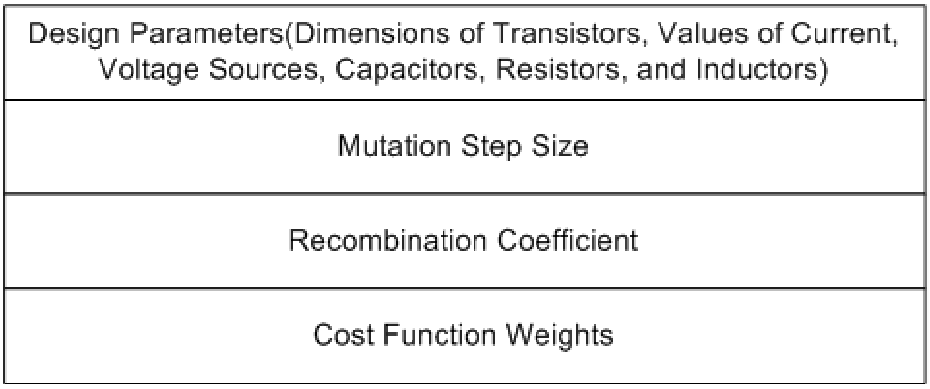

Figure 2.3. The content of an individual.

Measuring performance of individuals, a comparison metric should be determined. The cost value in the optimization algorithm provides that. Cost function can be separated to two parts; namely, performance cost and penalty cost.

$$C = C_{perf} + w_{penalty} C_{penalty} \tag{2.1}$$

C_{perf} is the total cost derived by the performance of evaluated individual considering the desired goal such as gain, power and area. It is calculated as given in the Equation 2.2.

$$C_{perf} = \sum_{i=1}^{n} + w_i \hat{f}_i^2 \tag{2.2}$$

w_i is weight of weight coefficient of every sub-objective, n is the number of performance objectives.

$$\hat{f}_i = \frac{g_i - f_i}{g_i - b_i}, \hat{f}_{i,min} = 0 \tag{2.3}$$

f_i is calculated for every sub-objective separately. g_i and b_i are respectively good and bad limits for performance specifications of every sub-objective.

$$W_{i+1_{BW}} = (W_{i_{BW}} * b_{i_{BW}})/result_{BW} \tag{2.4}$$

$$W_{i+1_{R_{out}}} = result_{R_{out}}/(W_{i_{R_{out}}} * b_{i_{R_{out}}}) \tag{2.5}$$

W_i represents for the current cost function weight whereas W_{i+1} is the next cost weight. BW stands for bandwidth and R_{out} stands for output resistance.

Cost function weights are updated for every generation using bad limits of output specifications. Updating equation alter according to the goal. If a better performance means higher output value for given goal such as BW, Equation 2.4 is applied. Equation 2.5 is applied for situations that a better performance means a lower output value for given goal such as R_{out}. Utilizing given weight updating operation, outputs which are moving away from desired goals have more priority for the algorithm. Even though the system seems to have a single objective utilizing a cost function measuring performance, owing to changing weight coefficients it behaves like a multi objective system.

$C_{penalty}$ is the cost term related to operation points of transistors. A transistor working in triode region may fulfill the specification requirements for AC conditions; however, in transient analysis there may be degradations in performance for bigger input amplitudes. That's why a penalty term is added to the cost function which increases as transistors are moving away from the specified working region.

$$p_{cut-off} = \sum_{i=1}^{m} p_{cut_i} = \sum_{i=1}^{m} \frac{k_{th}V_{th_i} - V_{gs_i}}{V_{th_i}}, p_{cut_i,min} = 0 \tag{2.6}$$

$$p_{triode} = \sum_{i=1}^{m} p_{triode_i} = \sum_{i=1}^{m} \frac{k_{sat}V_{dsat_i} - V_{ds_i}}{V_{dsat_i}}, p_{triode_i,min} = 0 \tag{2.7}$$

$$C_{penalty} = p_{cut-off} + p_{triode} \tag{2.8}$$

M is the number of biasing constraints, and coefficients k_{th} and k_{sat}, which are equal to unity in this work, are used as a safety margin.

As mentioned before SACSES algorithm uses a combination of ES and SA. Utilizing Metropolis criterion of SA at the selection mechanism with the self-adaptation feature of SA searching algorithm, system does not get stuck in a local optimum.

The utilized algorithm in this thesis can be shown as $(\mu + \lambda)$ ES where μ is the number of parents and λ is the number of offspring and the sum of parents and offspring gives the number of individuals in a generation. Outline of the algorithm is given in Figure 2.4.

Each individual consists of circuit variables such as dimensions of transistors, values of capacitors, resistors, inductors, and voltage and current sources placed in

$g \leftarrow 0$
$P_{\mu} \leftarrow P_{\mu 0}$
while *convergence not reached* **do**
  for $i = 1$ to $\lambda/2$ **do**
    $[I_{parent1}\ I_{parent2}] \leftarrow choose + (P_{\mu}, 2)$
    $[I_{\mu+i}\ I_{\mu+i+1}]_s \leftarrow recombine_s(I_{parent1},\ I_{parent2})$
    $[I_{\mu+i}\ I_{\mu+i+1}]_x \leftarrow recombine_x(I_{parent1},\ I_{parent2})$
  end for
  for $i = 1$ to $\mu + \lambda$ **do**
    if I_i *is selected for mutation* **then**
      $I_{i_s} \leftarrow mutate_s(I_i)$
      $I_{ix} \leftarrow mutate_x(I_i)$
    end if
    $I_{icost} \leftarrow evaluate(I_i)$
  end for
  $P_{\mu}^{g+1} \leftarrow select(P_{\mu+\lambda}^{g}, \mu)$
  $g \leftarrow g + 1$
  $T \leftarrow updatetemperature()$
end while
$output \leftarrow bestsolution$

Figure 2.4. ES Algorithm.

the topology. Besides, individual genes have their own algorithm parameters which are recombination, mutation, crossover coefficient, cost function weights and mutation step size.

At first the parents are generated randomly following the pre-determined boundaries. In the recombination process, two parents are chosen randomly, and using the recombination coefficient two offsprings are generated. In mutation part, which is a contribution of ES, individuals which are selected to mutate, are updated according to their standard deviation.

During evaluation, cost of every individual is calculated. In the selection, Metropolis criterion is used in a different manner than usual. After calculation of an average cost, C_{av}, using the generation cost matrix, randomly chosen individuals are competed with an imaginative individual whose cost is C_{av}. Winner individuals are selected for the next generation until their number is equal to the number of parents.

$$p(I_i) = 1/e^{C_i - C_{av/T}} \tag{2.9}$$

Population temperature, T, indicates the maturity of the search process. As the generations get closer to the desired value, temperature goes down. Searching for the optimum point continues until the maximum generation number is reached or improvements in the quality of the generations stop.

2.3. Output Estimation Techniques

During fabrication process, variations in the parameters of transistors occur due to defects in physical process of manufacturing. Dimensions, V_T (threshold voltage) and K (current factor) may differ from the desired value. A widely accepted model [12] for these variations is given in equation 12 where A_{V_T} and A_K are technology dependent constants.

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{W.L} \tag{2.10}$$

$$\sigma(\Delta\beta)\beta)^2 = \frac{A_\beta^2}{W.L} \tag{2.11}$$

Modifying SACSES in order to overcome these variations is the main goal of this study. In this way, modified algorithm gives us a robust circuit which means a circuit whose performance will be as desired even after the implementation.

To estimate variation in the output parameters, a sampling method should be chosen. Widely used techniques are Monte Carlo simulation, design of experiments (DOE) method, and sensitivity based variability estimation [13].

In Monte Carlo simulation, the design or the process is randomly simulated using stochastic probability of one or more random variables. Collective behavior of the outputs is observed. This method is the most exact method known for calculating the probability distribution for indefinite systems having indefinite inputs. Utilizing probabilistic distribution and properties of variables, system simulations are generated by sampling random variables.

There are many methods used for sampling such as simple random sampling [14] and descriptive sampling [15]. In simple random sampling method, sampling points are taken randomly from each distribution. Adequate number of samples has to be obtained to provide that each distribution is sampled completely.

Descriptive sampling is a method opposed for reducing the number of samples as well as number of simulations. In this technique, probability of each random variable is divided into fractions having equal probability and only one sample is taken from each fraction. Each row and column is sampled once in random order.

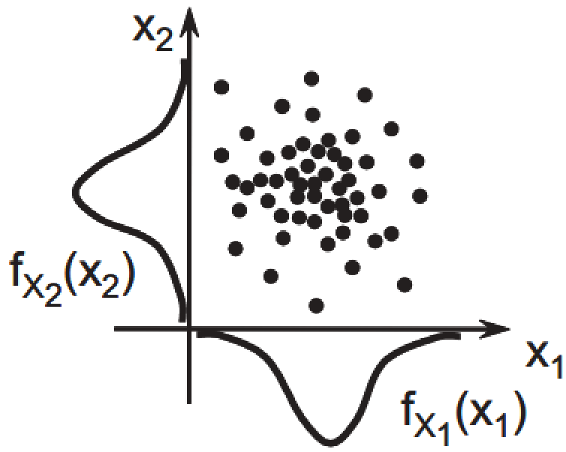

Figure 2.5. Simple random sampling.

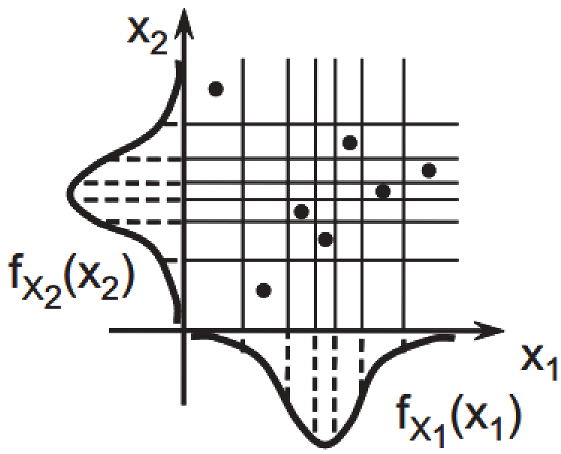

Figure 2.6. Descriptive sampling.

Although Monte Carlo simulation is fairly accurate, the computational load is high due to the large of number of simulations needed.

A second technique used for estimating variability of random variables is design of experiments method. In this method, a design matrix consisting of design variables is determined. Design variables are obtained not through probability distribution but utilizing some specified values or boundaries for variables. Thus, the result in this technique is based on ranges and the estimations may not be too accurate. The computational load in DOE depends on chosen variable levels and the design which is of interest. Usually DOE takes less time than Monte Carlo simulations. DOE can be useful in situations where the distributions of random variables are not exactly known.

The third approach to estimate variability is sensitivity based approach. In this method, unlike sampling points using distribution or some ranges, behavior of the responses is analyzed at specified values of random variables. There is a trade-off between the accuracy and the computation load and high order terms are generally neglected.

$$\sigma_Y = \sqrt{\sum_{i=1}^{n} \left(\frac{\partial Y}{\partial x_i}^2 (\sigma_{x_i})^2 \right)} \tag{2.12}$$

In equation 2.12, the standard deviation of $Y(x)$ is given where Y represents an output and X represents a random variable for the system under interest. N is the number of random variables in the system and σxi expresses the standard deviation of the $i-th$ random variable. Utilizing distribution knowledge, this method is more efficient than the Monte Carlo simulation and DOE. The main issue is the nonlinearity of the response behavior. It is critical to use sensitivity analysis, when the output characteristics are close to the linear region. In this thesis, sensitivity based approach will be used with some precautions to overcome the mentioned drawback.

3. ALGORITHMS

In this chapter, modifications to improve the algorithm of [11] will be presented before describing the robust algorithm technique which is the main subject of this thesis. After that, sensitivity based approach technique which is used for ensuring robustness will be described. In the end, three methods which use sensitivity analysis will be explained.

In first method, obtained output variations according to variations in random variables used in calculating the worst case cost value for every gene and the searching and selection mechanism is performed through these new costs.

In the second and third methods, an error term which is obtained from the sensitivity analysis executed is added to the desired values of output variables. While the outputs try to reach the given goals, error terms try to reach a given value. Desired value for the summed error terms is '0' in the second method and desired value for the multiplied error terms is '1' for the third method, both of which correspond to reducing the error.

3.1. Modifications on the Previous Study

- Automated design simulation time in [11] was given as approximately 15-16 minutes for all examples. Changing extensions of the command which calls HSPICE to run a simulation from MATLAB, now a simulation running for seventy generations lasts for 3-4 minutes. Breaking the simulation loops in case of frozen populations, design time is about 20-40 seconds.
- All the individuals in a population are listed in order considering their cost values. The genes having the best cost are stored with the values of their input and output variables. In this way, user can take the best design automatically instead of latest design simulator ran.
- In previous study, gain was processed in terms of dB unlike the other output

variables. Since the cost value is calculated by adding all the costs coming from outputs together, the mentioned difference in gain results in a problem for the algorithm which tries to converge to all goals equally. Thus, gain is converted to a linear ratio to ensure equilibrium in the cost function for all goals.

- Number of target outputs is increased. In the previous study, controlled outputs were gain, bandwidth, output resistance, power and area. Since phase margin is highly critical for an operational amplifier (OPAMP), phase margin is added to the goals in the new algorithm.
- The problem with calculating output resistance in the SPICE netlist is fixed. Output resistance is calculated using voltage and current values at the output node in the AC simulation for low frequency. Also, a conflict in the desired goals of output resistance is overcome.
- Topology dependent part which is responsible for updating cost function weights is removed to provide topology independence. In the new algorithm, cost function weights are updated in two ways: depending on the positions of outputs considering the desired goals and in case of a mutation.
- Freezing of a generation was determined using figure of merit (FOM) criteria in the previous study. Instead of using FOM, finalization of the simulation is managed by cost values of the generations. Each cost value in a generation is first ranked from low to high, then geometric mean of the first thirty individuals is calculated. If geometric mean value of the new generation is higher than the old generation with a specified ratio, program interprets the situation as a frozen population and terminates the simulation.

Out of the modifications mentioned above, some trials in the algorithm are carried out to compare the results with the original algorithm. These changes are explained below and all the results will be presented in fourth chapter.

- Understanding the ability to scan the solutions space of the given algorithm, number of individuals in a generation is increased. A simulation with sixty parents and forty offspring is performed.

- Different methods for updating the cost function weights are tested. In the previous study, cost function weights are only changed in a case of a mutation after first generation. Two methods will be tested to compare. In the first one, cost weights of parents after the first generation will remain same and the cost weights of offspring will be updated considering the distance of outputs to the desired goals in addition to mutation. In the second method, all individuals in a generation will be treated in the same way in terms of updating cost function weights.

3.2. Sensitivity Analysis

A sensitivity analysis is performed to estimate variances of outputs of a given design. Utilizing these values obtained from sensitivity analysis, one can estimate performance of a given design after manufacturing. Thus, a robust circuit design can be realized.

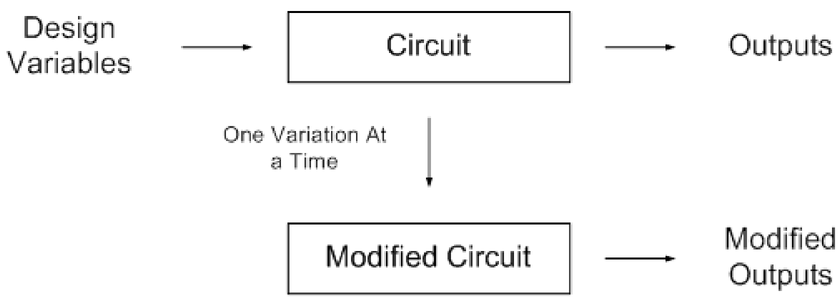

Figure 3.1. Block diagram for sensitivity analysis.

In this thesis, the input variables whose variances are of interest are width (W), length (L), oxide thickness (t_{ox}) and threshold voltage (V_T) of a transistor. Since oxide thickness is related to current factor as shown in Equation 3.1, variation in K can be used to calculate t_{ox} variation. Output variables whose variations to observe are gain, bandwidth, output resistance, phase margin, area, and power. The topologies, the sensitivity analysis and foregoing robust algorithm methods are performed on, are basic two stage (BTS) opamp and folded cascade opamp (FC OPAMP).

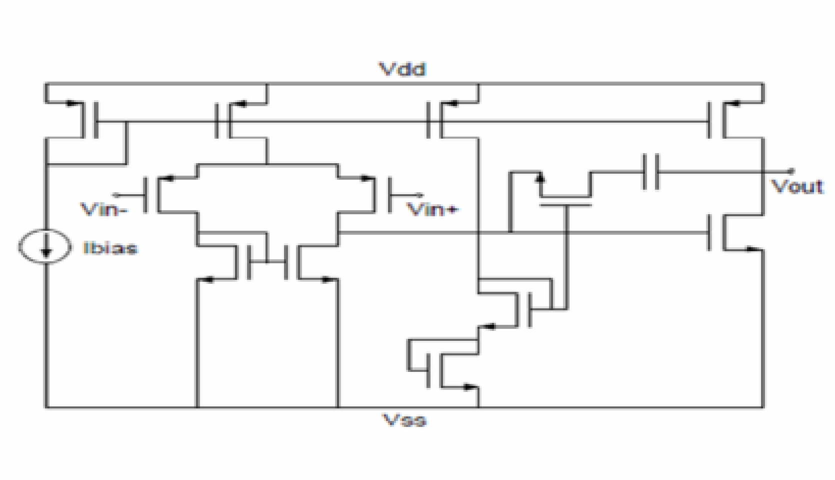

Figure 3.2. The circuit schematics of BTS OPAMP.

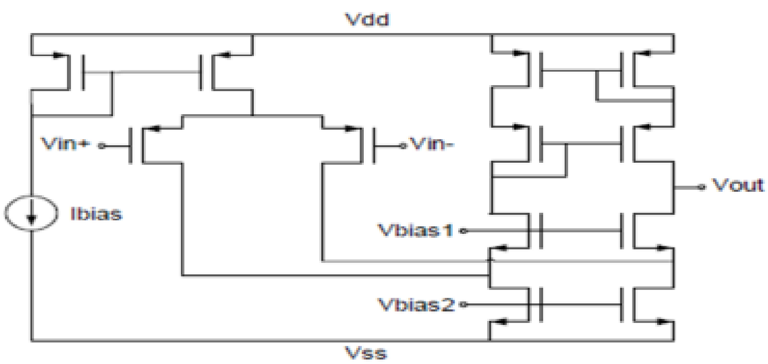

Figure 3.3. The circuit schematics of FC OPAMP.

The first step is to calculate the worst case variation values for given input variables for the technology used in the design. Worst case deviation for W and L in $0.18\mu m$ technology is $0.03\mu m$. We know that variations of V_T and β are inversely proportional to W and L values of a specified design. As mentioned before A_{V_T} and A_K are technology dependent coefficients. Using the values given in [16], we can take $A_{V_T} = 5mV\mu m$ and $A_K = 0.5\mu\mho\mu m$.

$$\beta = \mu.(\frac{\epsilon_{ox}}{t_{ox}}).\frac{W}{L} \tag{3.1}$$

Using Equation 3.1, Equation 3.2 can be derived. In this way, variation of t_{ox} can be calculated using variation of β.

$$t_{ox_2} = \frac{1}{\frac{1}{t_{ox_1}} + \frac{\Delta\beta}{\mu * \varepsilon_{ox}}} \tag{3.2}$$

In this way, calculating δW, δL, δV_t and δt_{ox} values for a specified sized design, an input worst case variation matrix is obtained. Since there are twelve transistors in both given schematics, a $48x1$ matrix is acquired. First task carried out by the sensitivity analysis is to constitute an output matrix, a $6x1$ matrix, with given design parameters considering six outputs whose behaviors are observed. After that, by changing only one input at a time using $48x1$ input variation matrix, modified output matrixes are attained. Taking the difference between modified output matrixes and the original output matrix, a $48x6$ deviation matrix is obtained. Each element in this matrix expresses how an output term reacts a change realized in an input variable.

Although these deviations occurring in the outputs may cancel each other, absolute values are taken to estimate a worst case situation. Changes fewer than five percent of the original output values are omitted and by adding all the deviation terms for an output, worst case output change is calculated.

$$\begin{bmatrix} \Delta BW \\ \Delta GAIN \\ \Delta ROUT \\ \Delta PM \\ \Delta POWER \\ \Delta AREA \end{bmatrix} = \begin{bmatrix} \Delta BW/\Delta W1 & \dots & \Delta BW/\Delta tox12 \\ \Delta GAIN/\Delta W1 & \dots & \Delta GAIN/\Delta tox12 \\ \Delta ROUT/\Delta W1 & \dots & \Delta ROUT/\Delta tox12 \\ \Delta PM/\Delta W1 & \dots & \Delta PM/\Delta tox12 \\ \Delta POWER/\Delta W1 & \dots & \Delta POWER/\Delta tox12 \\ \Delta AREA/\Delta W1 & \dots & \Delta AREA/\Delta tox12 \end{bmatrix} * \begin{bmatrix} \Delta W1 \\ \Delta W2 \\ \vdots \\ \Delta Vt8 \\ \vdots \\ \Delta tox12 \end{bmatrix}$$

Output Estimation Matrix Sensitivity Matrix Input Variation Matrix

6x1 6x48 48x1

Figure 3.4. Calculation of output estimation matrix.

Sensitivity analysis based approach may be more efficient than the other estimation methods; however, the operating point where the sensitivity analysis performed is highly critical due to the nonlinearity of the system. To overcome this drawback, points where the system acts linear or close to linear should be chosen. Besides, constructing a sensitivity matrix for every individual causes serious computational load and loss of time. Therefore, sensitivity analysis is performed not initially but at the final generations where the design solutions are close to an optimum point and each other. An individual representing its generation is chosen and the worst deviation terms obtained by this analysis is used for all the individuals in this generation. In this way, linearity is ensured with less computational load.

Using the values obtained from sensitivity analysis which is performed at the appropriate operating points of the system, a more robust circuit design is feasible. Methodologies, which are using sensitivity analysis, presented in this thesis are cost function based approach, additive error term based approach, and multiplicative error term based approach.

3.3. Cost Function Based Robust Design Methodology

The cost function based method utilizes output estimations acquired from sensitivity analysis at the evaluation stage of the search algorithm. The crucial part about the usage of obtained estimations is about the growth of the population.

The aim in using sensitivity analysis method for estimating the output distribution is to attain enough accuracy with a less computational load than Monte Carlo simulations. Besides performing sensitivity analysis at the operating points where the system is linear or close to linear is another concern.

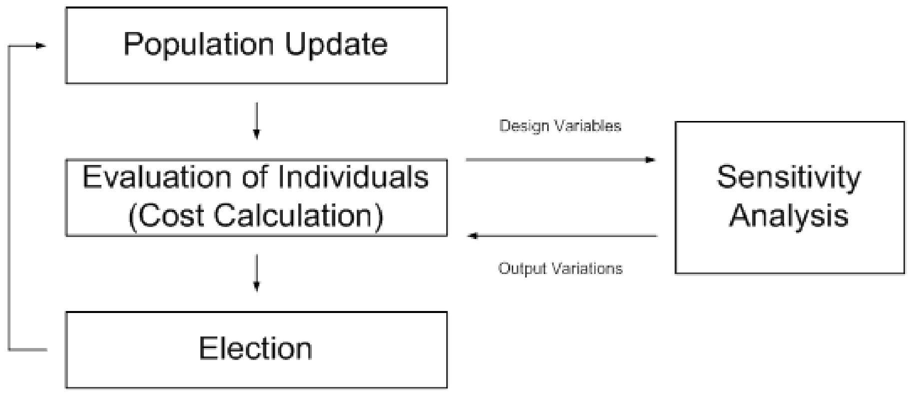

Figure 3.5. Block diagram for cost based method.

Considering mentioned challenges, sensitivity analysis is performed at the further generations of the populations where the individuals are close to each other. Waiting for more mature generations to execute the sensitivity analysis, using one individual to represent the whole generation is viable. In this way, smoother regions of the system are ensured and computational load to obtain accuracy is diminished.

In this method, since cost is the criterion for appraising individual design solutions, the operation point where the sensitivity analysis is performed initially is chosen considering the cost values of generations. Geometric mean of the cost of a generation stands for a maturity metric for the system. Algorithm starts to perform when the geometric mean of the costs of parents goes under a certain cost value determined dependent to system parameters. After the first execution of the sensitivity analysis, it is performed for every generation by choosing an individual from the parents.

Another essential issue about the usage of the outputs of the sensitivity analysis is that how these estimations are added to the cost value. Since the changes in Vt, tox, W, and L in all transistors are examined, there are twelve transistors and forty eight parameters for both BTS and FC OPAMP. After omitting the parameters which indicate a change at the output lower than five percent, all these estimations are added to obtain a worst case estimation even though some of them may cancel each other. In the end, a worst case estimation is acquired for every ouputs which are bandwidth, gain, phase margin, output resistance, area, and power.

$$C_{perf1_{BW}} = (g_{i_{BW}} - output_{BW} - \Delta BW_{WC})/(g_{i_{BW}} - b_{i_{BW}}) \tag{3.3}$$

$$C_{perf2_{BW}} = (g_{i_{BW}} - output_{BW} + \Delta BW_{WC})/(g_{i_{BW}} - b_{i_{BW}}) \tag{3.4}$$

Utilizing obtained outputs of sensitivity analysis, a worst case cost value is calculated. In order to do that, six worst case estimation values for each output are added to and subtracted from the sub-costs. An example is given above for bandwidth output. In this manner, the worst situation the system may go to is attained by using the higher cost value.

$$Cost = C_{perf_{BW}} + C_{perf_{Gain}} + C_{perf_{PM}} + C_{perf_{R_{out}}} + C_{perf_{Power}} + C_{perf_{Area}} \tag{3.5}$$

Adding all these sub-costs, worst case cost an individual can have is calculated. Performing election mechanism with updated calculated costs, searching for robust design solutions is ensured.

3.4. Additive Error Term Based Approach

This approach is based on error terms added to desired goals for outputs. Updating specifications the circuit design has to fulfill, another goal is created by error terms.

$$Bandwidth \longrightarrow BW_0 + E1$$

$$Gain \longrightarrow G_0 + E2$$

$$R_{out} \longrightarrow R_{out_0} + E3$$

$$PM \longrightarrow PM_0 + E4$$

$$Power \longrightarrow Power_0 + E5$$

$$Area \longrightarrow Area_0 + E6$$

$$(\frac{E1}{BW_0}) + (\frac{E2}{Gain_0}) + (\frac{E3}{R_{out_0}}) + (\frac{E4}{PM_0}) + (\frac{E5}{Power_0}) + (\frac{E6}{Area_0}) \longrightarrow E_{sub_0}$$

When all the outputs try to reach to their given goals, sum of error terms try to reach another goal determined by the user. In this way, system searches for an individual ensuring the updated goals.

Applying mentioned search algorithm for robustness, error terms added to desired output values are acquired from sensitivity analysis results. A safety margin for desired goals is constituted by utilizing worst case estimation values for outputs of the system as the error term to be added. Ratios of the worst case changes of outputs to the initial outputs of the system give another goal to reach for the sum of error terms.

Outputs try to reach to their updated goals which are a certain distance away from the required specifications for the system. In this way, sized circuits tend to

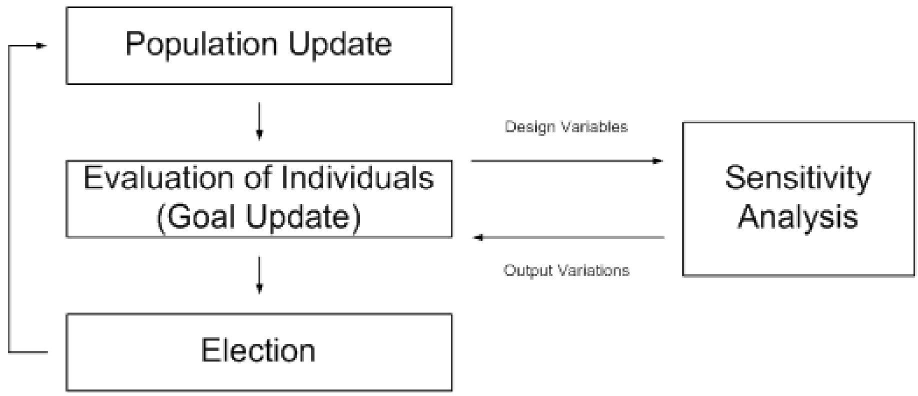

Figure 3.6. Block diagram for error term method.

match desired goals in spite of variations of input variables at manufacture process.

Goal obtained from sensitivity analysis results generates another sub-cost. This sub-cost is calculated using the outputs of every design solution and added to the general cost term with the aid of cost weights produced for each error term sub-cost. Election mechanism is done through these updated costs.

Choosing operation point when sensitivity analysis is performed depends on the same principal with other robust circuit design methods given in this thesis. First analysis is executed after waiting for creation of mature generations. After that point, analysis is performed repetitively for each generation.

3.5. Multiplicative Error Term Based Approach

In this approach, the connection with the sensitivity analysis and the general algorithm is same with the additive error term based approach. Error terms are obtained from sensitivity analysis results.

$$Bandwidth \longrightarrow BW_0 * E1$$

$$Gain \longrightarrow G_0 * E2$$

$$R_{out} \longrightarrow R_{out_0} * E3$$

$$PM \longrightarrow PM_0 * E4$$

$$Power \longrightarrow Power_0 * E5$$

$$Area \longrightarrow Area_0 * E6$$

$$E1 * E2 * E3 * E4 * E5 * E6 \longrightarrow E_{mul_0}$$

The difference from the previous approach is the usage of error terms. In this approach, updated desired goals are attained by multiplying the error terms with required specifications. The desired goal for error term is determined considering multiplication. Sub-cost calculated for these error terms are added to the general cost value and election is performed utilizing updated cost values.

Advantage of this approach to the additive term based method is the speed factor of multiplication compared to addition. Therefore, growth of population is expected to be at the earlier generations. The comparison of this method with the additive term based approach will be given in Results section.

4. RESULTS

In this chapter, initially simulation results for both BTS OPAMP and FC OPAMP will be given and improvements after the modifications done on the previous study will be examined. Then, results for different trials in the algorithm for BTS OPAMP will be given in a table and the outcome will be analyzed. Finally results for Cost Function Based Method, Additive and Multiplicative Error Term Based Approach will be given seperately. Their performances will be measured with the aid of Monte Carlo simulations in terms of robustness.

4.1. Simulation Results of BTS and FC OPAMP

A simulation with seventy generations for BTS and FC OPAMP is performed. Desired output specifications and simulation results are given below.

Table 4.1. Desired Output Targets for BTS OPAMP.

	BW	Gain	R_{out}	Power	Area
Good Limit	$10k$	5623	$50k$	$5m$	$30n$
Bad Limit	$9k$	5100	$55k$	$5.5m$	$33n$

Table 4.2. Desired Output Targets for FC OPAMP.

	BW	Gain	R_{out}	Power	Area
Good Limit	$10k$	316	$3M$	$3m$	$1n$
Bad Limit	$9k$	100	$5M$	$5.5m$	$6n$

It can be seen from the BTS OPAMP results given targets for chosen outputs are reached. Good limits for BW, R_{out}, power, and area are surpassed. Gain value obtained from the simulation is very close to the good limit. Simulation time is about four minutes.

A critical issue to consider while interpreting the simulation results is to under-

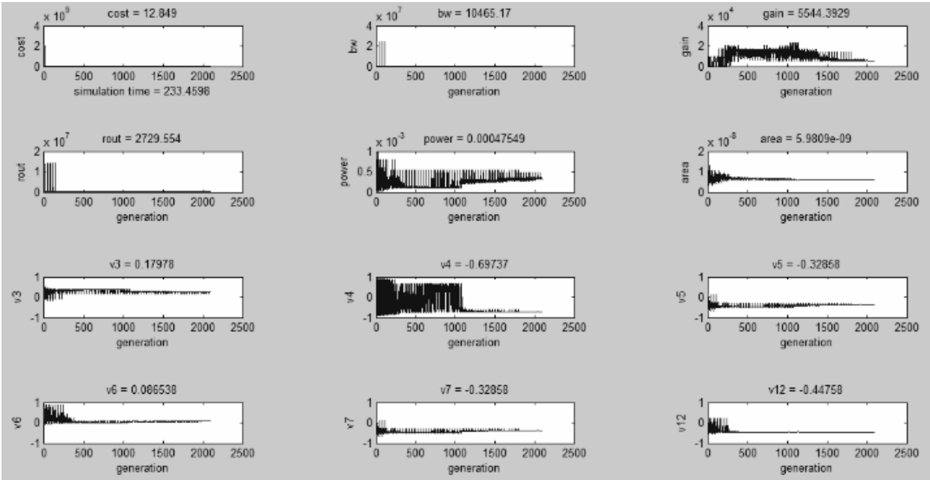

Figure 4.1. Simulation results for BTS OPAMP.

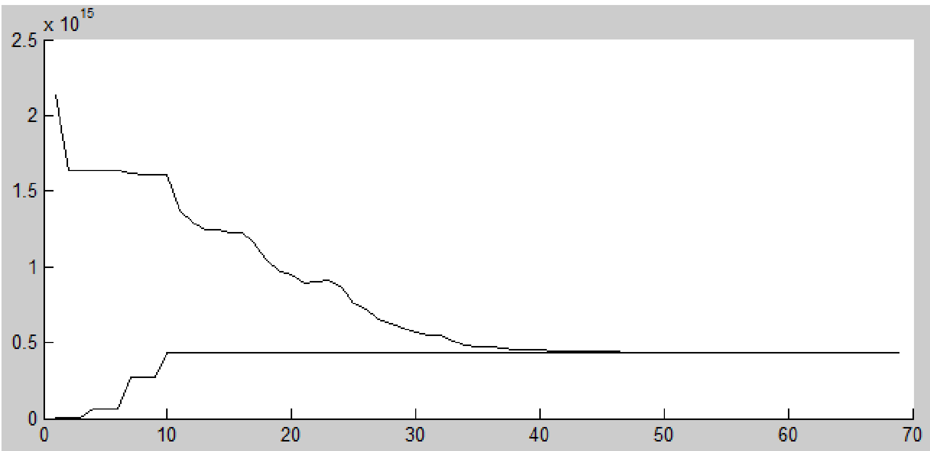

Figure 4.2. FOM values of first and last individuals.

stand the completely the cost function concept. Even though cost value is our main concern electing individuals from a generation, cost may not be suitable to realize the growth of the population due to constantly changing cost function weight coefficients. Thus, observing FOM behaviour of the population is a better way to comprehend the system. The individuals with the minimum and maximum FOM value of each generation is given in Figure 4.2.

FOM values of a generation are sorted to read the improvement of the population along generations. Since each generation means an advance in terms of a better solution, this development can be seen from the worst individual utilizing the FOM value. The reason why the individuals having the best FOM value get worse through generations, is the collective attitude of a generation. Important thing is the improvement of a generation in general.

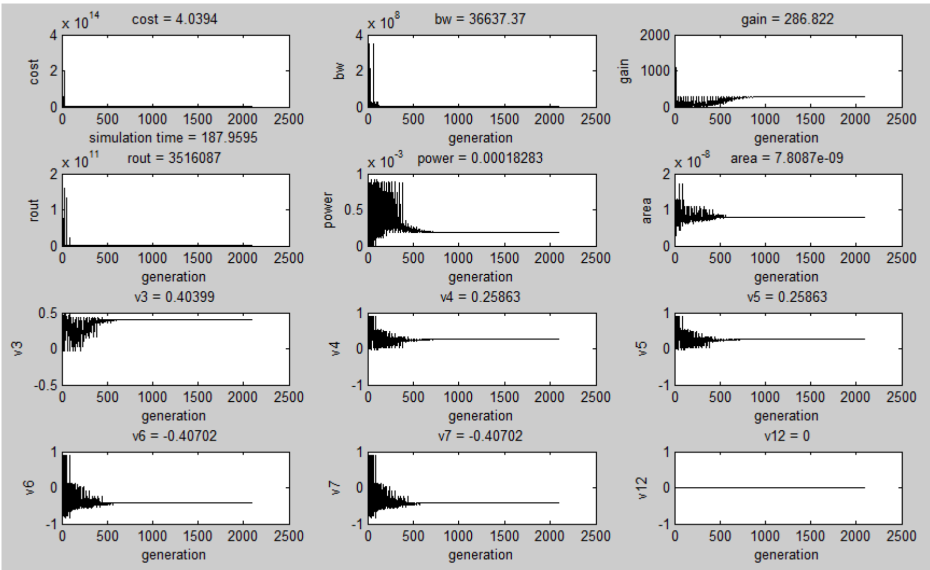

Figure 4.3. Simulation results for FC OPAMP.

FC OPAMP simulation results are compatible with the desired specifications for chosen outputs as it can be seen from Figure 4.3. The individuals having the worst FOM value of a generation improves with the growth of the population as expected.

Results from different trials are given below. In the first two lines, only cost

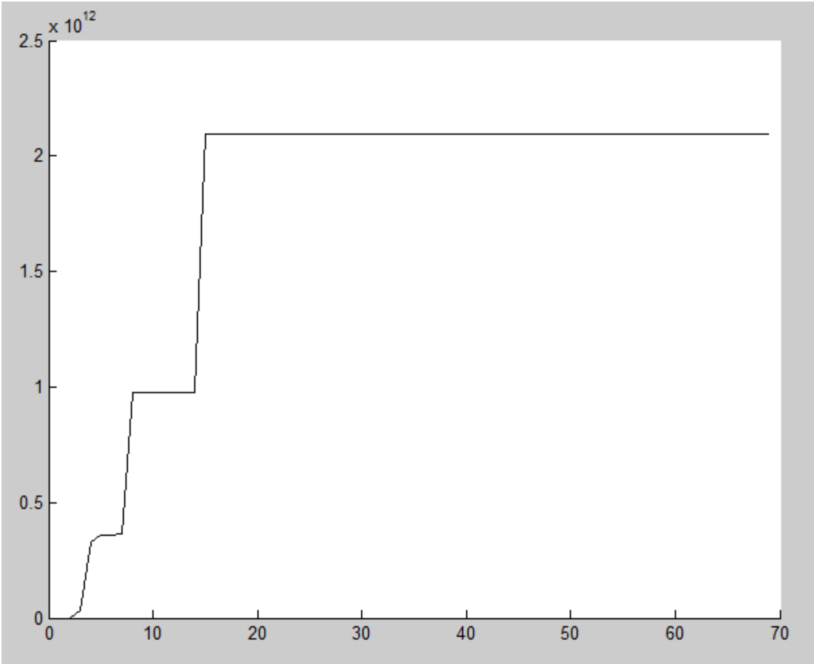

Figure 4.4. FOM graph for FC OPAMP.

function weight changing happens only in the first generation. In the third and fourth lines, algorithms includes the weight coefficient changing for offsprings of all generations. In the last two lines, all cost function weight coefficients are updated using the bad limit value given by the user. 30x20 represents 30 parents and 20 offsprings and 60x40 tells the algorithm utilizes 60 parents and 40 offsprings for every generation.

Table 4.3. Simulation Results for Various Trials in the Algorithm.

	Cost	BW	Gain	R_{out}	Power	Area	Time	FOM
30x20/Not Updated	18.43	29.3k	160.2	2.87k	0.25m	7.12n	29.1	0.89P
60x40/Not Updated	18.21	37.4k	165.6	2.12k	0.22m	6.62n	52.4	1.12P
30x20/μ Updated	19.25	71.1k	65.7	1.90k	0.43m	6.15n	18.6	0.20P
60x40/μ Updated	18.12	28.0k	36.4	1.41k	0.23m	6.90n	29.7	0.14P
30x20/All Updated	21.19	23.6k	108.6	1.73k	0.43m	7.34n	17.8	1.00P
60x40/All Updated	18.23	19.0k	112.1	1.68k	0.24m	8.38n	30.6	1.16P

As a general 60x40 algorithms have better results with the cost of time spent.

These algorithms search a wider space using 100 individuals for every generation and have a higher chance to find a better optimum point.

The cost weight coefficient updating is a considerable feature of this algorithm. As the outputs moving away from the desired goals, their importance goes up with the increasing cost weights. Thus, update operation prevents solutions from run away. With the guidance of these information, all updated algorithm is expected to give the better simulation results.

The algorithm which only updates offsprings displays a different behaviour than others. Since weights of parents are not updated, their cost function values remain same. As long as a better offspring is not created, first thirty individuals of the generation does not alter much along the generations. Search stick easily and the loop is broken at the early generations. The results of this part is not as expected due to failure of search mechanism. The results obtained are based on the random chance factor utilized at the first generation. The simulation time is shorter than it should be.

4.2. Simulation Results of Cost Function Based Method

The output specifications and simulation results for BTS OPAMP are given below.

Table 4.4. Desired Output Targets for BTS OPAMP.

	BW	Gain	R_{out}	PM	Power	Area
Good Limit	$20k$	310	$10k$	440	$3m$	$30n$
Bad Limit	$15k$	100	$22k$	430	$5.5m$	$40n$

It can be seen from the results, outputs of the circuit mostly match the requirements. However, surpassing given limits is not the main concern. Obtained sized circuit is tested using Monte Carlo simulations. Graphs represent 25 different samples for BW and R_{out}. In order to observe all outputs clearly, logarithm of results are

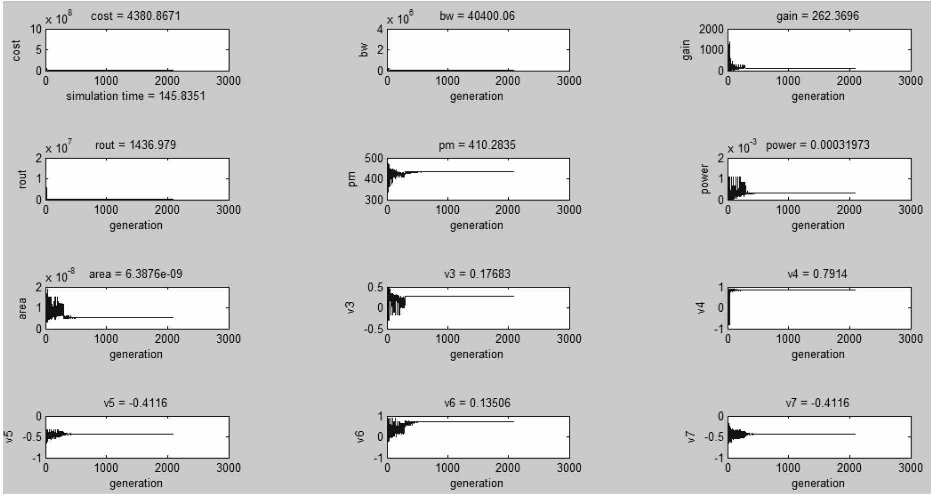

Figure 4.5. Simulation results for BTS OPAMP.

plotted.

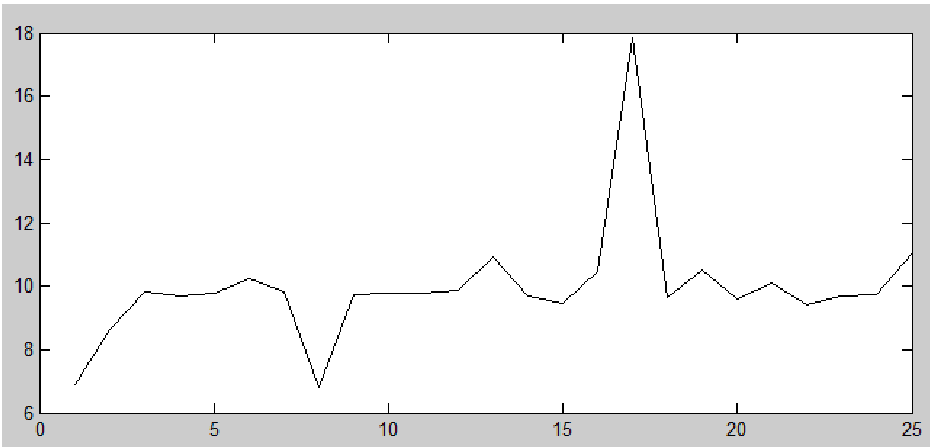

Figure 4.6. Monte Carlo results BW, BTS OPAMP.

Desired values for BW and R_{out} is respectively $20k$ and $10k$ which indicates 9.90 and 9.21 in logarithmic scale approximately. Even though the system seems safe considering BW, R_{out} results are highly volatile. The Monte Carlo results of BW and R_{out} for FC OPAMP is given below.

Targets for BW and R_{out} is 10.5 and 13.8 in logarithmic scale. Results better than target with a clear safety margin are obtained in terms of BW and R_{out}.

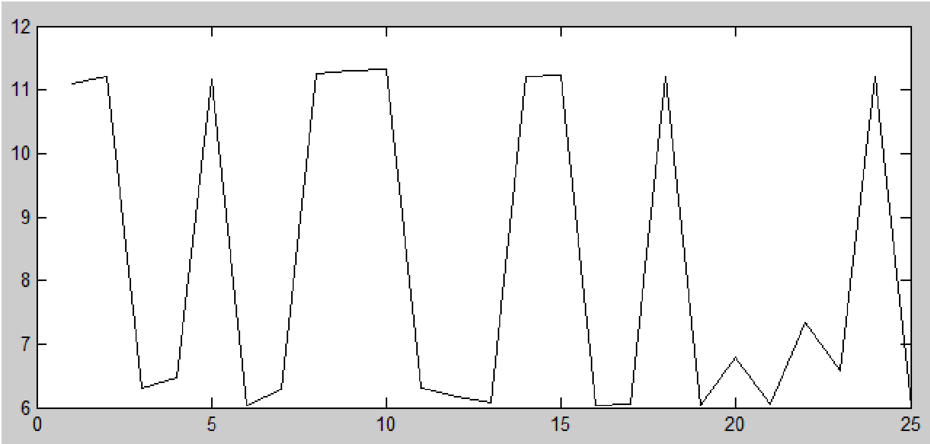

Figure 4.7. Monte Carlo results for R_{out}, BTS OPAMP.

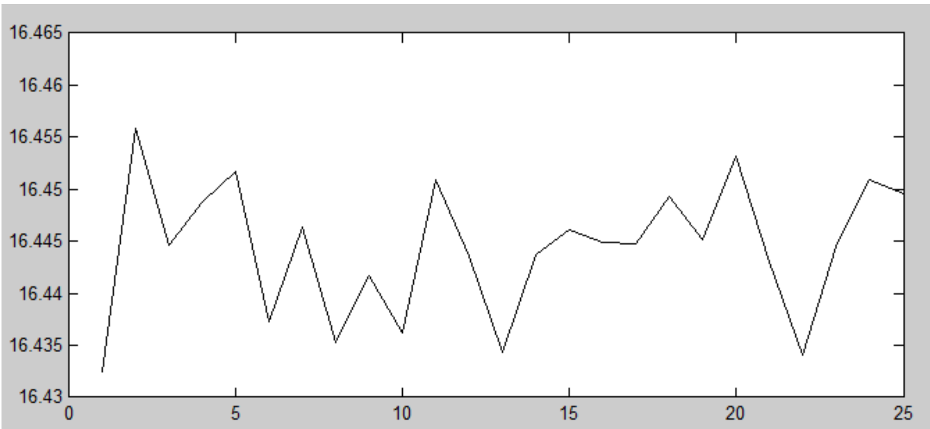

Figure 4.8. Monte Carlo results for BW, FC OPAMP.

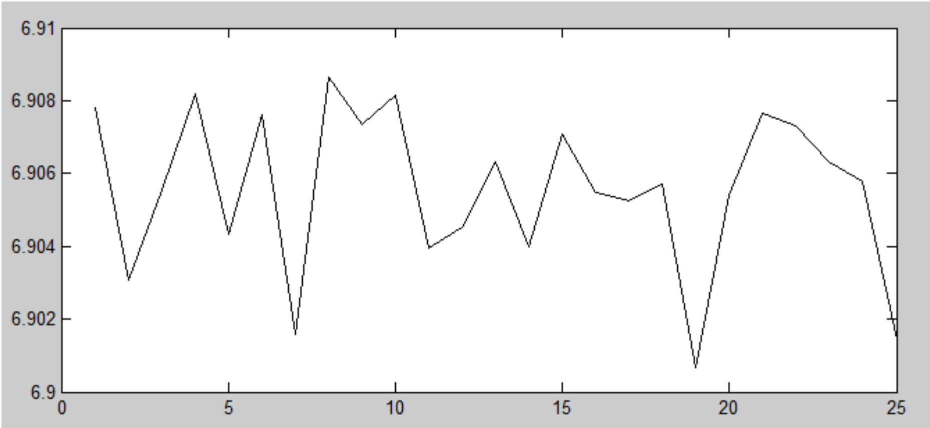

Figure 4.9. Monte Carlo results for R_{out}, FC OPAMP.

4.3. Simulation Results of Error Term Based Approach

Output specifications and results of Additive and Multiplicative Error Term Based Approach is given below.

Table 4.5. Results for Error Term Based Approaches.

	Goals	Error Added	Error Multiplied
Bandwidth	$> 20k$	$30.5k$	$20.2k$
Gain	> 310	679	547.6
R_{out}	$< 10k$	$1.69k$	$7.2k$
Power	$< 3m$	$0.41m$	$0.34m$
Area	$< 30n$	$9.6n$	$10.8k$
Time		$46s$	$43s$

Time results of these methods are considerably related to the number of generations of the population. The one converges faster than the other has less time value naturally. Considering the time and generation info obtained from simulations, Multiplicative Error Based Approach is faster than Additive Error Term Based Approach.

5. CONCLUSION

- A faster and more reliable algorithm is acquired than previous study owing to modifications done.

- Effects of updating weight coefficents and increasing the size of a generation is observed. Since changing weight coefficients of all individuals gives better results, new methods are built on update all search mechanism.

- Three different methods all using sensitivity analysis approach are opposed.

- Testing the sized circuits with Monte Carlo simulations, desired results could not be reached. The reason of failure is fairly related to the instability of search mechanism. System, despite using different concepts to overcome the danger of sticking with a local optimum, can not converge to a general optimum most of the time.

- Selection of target values is quite critical for a better optimization performance. Goals chosen not wisely directly causes an instability in system results.

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