DESIGN, SIMULATION AND CONSTRUCTION OF A WIRE CHAMBER ELECTRONICS

by

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ABSTRACT

DESIGN, SIMULATION AND CONSTRUCTION OF A WIRE CHAMBER ELECTRONICS

A Delay Wire Chamber (DWC) is a gaseous particle detector which enables detection of charged particles and their trajectories. They are preferred as they provide good position resolution inexpensively and due to their ease of use. The novel feature distinguishing it from other wire chambers is its readout electronics that allows reading and amplification of signals from tens of wires with a limited number of electronic components.

In this thesis, we present the basics of gaseous radiation detectors, describe the electronics of the DWC readout circuit, provide simulation results as well as the results from various implementations in hardware. The circuit is found to be sensitive to sources of noise and our attempts in improving its stability, as well as future directions of research are also presented.

ÖZET

TEL ODASI ELEKTRONİĞİNİN DİZAYNI, SİMÜLASYONU VE YAPISI

Gecikmeli Tel Odası (GeTO), yüklü parçacıkların varlığını ve yörüngelerini keşfetmeyi sağlayan gazlı bir parçacık algıcıdır. Bu algıçlar düşük maliyeti ve kullanım kolaylığı ve konum duyarlılığı sebebiyle tercih edilmektedirler. GeTO'yu diğer tel odalarından ayıran en önemli özelliği onun elektronik okuma devresi üzerinde yapılan değişikliklerdir; sinyalin yükseltme ve okumasını sınırlı sayıdaki elektronik bileşene sahip onlarca telden yapılmasını sağlar.

Bu tezde gazlı algıçların temel özelliklerinden başlayarak GeTO'nun elektronik okuma devresini detaylıca anlatıp, simülasyon ve laboratuvar çalışma sonuçları ile desteklemektir. Devre, çevresindeki gürültüden etkilenebilen hassas özelliklere sahiptir. Bizim amacımız, bunlardan kaynaklanan sorunları düzeltmek ve ileride yapılabilecek olası araştırmalar için de bir yön vermektir.

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LIST OF SYMBOLS

A_{CL}	Closed Loop Gain
A_{OL}	Open Loop Gain
C	Capacitance
L	Inductance
ns	Nanosecond
R	Resistance
R_{in}	Input Resistance
R_f	Feedback Resistance
V	SI Derived Unit of Voltage
V_{in}	Input Voltage
V_{out}	Output Voltage
β	Feedback Factor
Ω	SI Derived Unit of Electrical Resistance

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternative Current
BJT	Bipolar Junction Transistor
CERN	European Organization for Nuclear Research
CMRR	Common Mode Rejection Ratio
DC	Direct Current
DCR	Direct Current Resistance
DIP	Dual In-line Package
DWC	Delay Wire Chamber
FET	Field Effect Transistor
IC	Integrated Circuit
J-SMD	J-Bend Surface Mount Device
J1	Jag 1
J2	Jag 2
LTspice IV	Linear Technology SPICE IV
NPN	Negative-Positive-Negative
Op-amps	Operational Amplifiers
PCB	Printed Circuit Board
PSRR	Power Supply Rejection Ratio
SMD	Surface Mount Device
SPICE	Simulation Program with Integrated Circuit Emphasis
Tina-Ti	Toolkit for Interactive Network Analysis-Texas Instruments

1. INTRODUCTION

Fundamentals of gaseous detectors are based on Ernest Rutherford's studies. While pursuing the studies on the structure of the atom, he designed a tool [2] that could identify the traces of ionization in the gas. Since then, great progress has been made in gaseous detectors.

According to the intended usage, imaging capability, working range, size, scientists have constantly producing and improving the detectors. In the 1960s, especially in the high energy particle physics, it was needed to produce portable and fast working instruments.

In 1967, a new type of gaseous particle detector was invented by George Charpak at CERN, which served for these aims. He was the recipient of the 1992 Nobel Prize in Physics for this groundbreaking invention, which is called the Multi Wire Proportional Chamber. However, by the simplifications of this, a new generation detector was produced. A Delay Wire Chamber (DWC) is the simplified version of the MWPC by its easy handle read-out mechanism, portable size and reasonable cost.

When we have constructed the DWC in our laboratory we have encountered some deficiencies on the its electronic circuit. In this thesis, we present the problems and the solutions for its more effective work.

2. THE GASEOUS IONIZATION DETECTORS

Ionization detectors in particle physics enable the detection of the trajectory of particles, and also identify kinds of ionizing particles.

There are three main types of gaseous detectors: They are the ionization chamber, the proportional chamber and the Geiger-Müller counter. They have the same working principles but function in different voltage regimes.

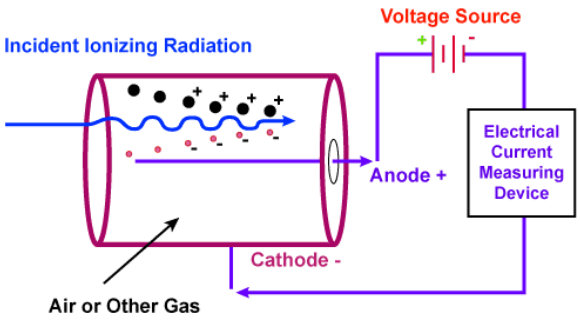


Figure 2.1. Schematics of a simple gaseous chamber[10].

Figure 2.1 shows the schematics of a simple gas chamber detector. When radiation (such as a charged particle) passes through the contained gas (or air), the gas molecules get ionized. With the help of a voltage applied between the anode and cathode electrodes (a wire and the conducting cylinder in the figure), ionized molecules move towards the opposite charged electrodes. The negatively charged electrons will be attracted by the anode, the positively charged ions will move to the cathode. When this process is completed a small current will reach the detector, and register as a signal. The size of the signal depends on the quantity of the collected radiation, as well as the accelerating voltage applied between the electrodes.

According to Figure 2.2, for very low values of the applied voltage, the collected number of electron-ion pairs is negligible. As the applied voltage is increased, this number increases, until we reach a plateau, which is called the ionization chamber

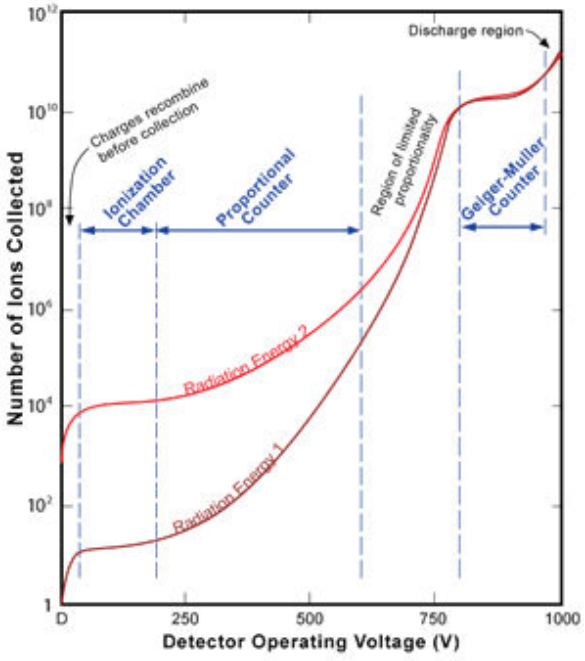


Figure 2.2. Voltage dependence of number of ions collected in a proportional counter. The cylinder shaped counter is generally filled with a proper noble gas [11].

regime. If the applied voltage is further increased, the electric field becomes so strong that the generated ions themselves become highly accelerated, and hence produce secondary ionization. This is called ionization avalanche. In this regime, the number of ions collected will be proportional to the applied voltage. This is the region of the proportional counter's working area. While the electric field increases the gain will increase, but after a voltage value this amplification will become non-linear. If the voltage is even further increased, at some point there will be saturation in the number of ions collected. This is the Geiger-Müller region.

2.1. The Multi Wire Proportional Chamber

A Multi Wire Proportional Chamber (MWPC) is a kind of proportional counter, which is generally used in order to determine the trajectory of the particles. Until 1970s optical detectors were commonly used to determine the trajectory of the particles, however, the MWPC opened up a new era in this field.

The MWPC consists of an anode plane, which consists of equally spaced Tungsten wires in the μm range, and two conducting parallel cathode planes. The anode wire plane is placed between the cathode planes. In anode plane, the separation between the wires is 2 mm, while the space between the anode and cathode planes is about 7 mm.[1] This configuration allows each anode wire to act as a single proportional counter. Moreover, the anode wire determines states the spatial resolution of the detector. In MWPC, spatial resolution is one half of the anode wires spacing, thereabout $\pm$1mm.

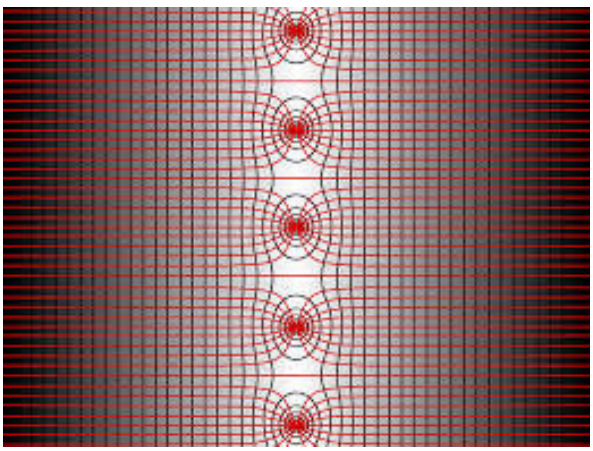


Figure 2.3. Electric field lines in a MWPC [14].

By applying high voltage (HV) to the cathode layers and grounding the anode wires, it is aimed to create an uniform electric field away from the wires, it can be seen in the Figure 2.3. This electric field acts on each wire a single cylindrical wire chamber and it is defined as:

$$E = \frac{V}{r \ln (b/a)} \tag{2.1}$$

In the Equation 2.1, V is the applied voltage value, r is the distance from the anode wire center, a is the anode wire radii, b is the cathode wire radii. By applied field, positive ions are attracted by cathodes and negatively charged electrons are accelerated towards the anode wires, and these electrons will create an avalanche. After a point, a negative signal will occur with a clear amplitude on the nearest anode wire. This is the basic working principle of a MWPC. In addition, by adding new layers of anode

wires aligned perpendicularly to the original anode wires, and using two detectors, two dimensional location determination is also possible.

While the MWPC was a great invention for its time as a position sensitive gaseous detector, further innovations were deemed necessary and a new generation of wire chambers was developed, namely the Delay Wire Chamber.

2.2. The Delay Wire Chamber

A Delay Wire Chamber (DWC) is a gaseous detector, a simplified and improved version of the MWPC. In the DWC, instead of using conducting plates as cathode layers, bronze-beryllium cathode wires, about μm range, are used perpendicularly to anode wires. This way, it becomes possible to observe the inside of the detector. Furthermore, the read out will be done from cathode wires instead of anode wires. Propagation delays are used between the cathode wires. While doing separate amplification in each anode wire in MWPC, by adding propagation delays between the cathode inputs and amplification section readout operation is became easier. Furthermore, DWC has a more user friendly design. While working with the MWPC it is not possible to see the inside of the chamber because of the cathode plates. Thus, if there occurs a problem because of anode wires, it can be very hard to investigate the cause of problem. Lastly, despite of its simplicity, the spatial resolution becomes better on auto-trigger facility than other proportional counters [4].

2.2.1. Working Principles of the Delay Wire Chamber

A Delay Wire Chamber works like its precedent Multi Wire Proportional Chamber, when the radiation passes through the gas in the chamber, ionization will be occur and this leads formation of negative and positive ion pairs. When the high voltage is applied between anode and cathode wire planes, ions will be attracted to opposite charged wires. At the around of the anode wires avalanche multiplication will occur. At which anode wire this avalanche is occurred, comparatively an image current will appear on the cathode wire. The incoming signal from the cathode wires are passed

through propagation delays before further amplification. When it reaches delays, goes into division; two equal signals in opposite ways on the delay, by this way a time difference is obtained. By measuring the delay time between the incoming signals from the propagation delays the coordinate of ionization can be determined. Perpendicularly adding another cathode and anode layers in the same chamber, bi-dimensional position determination can be possible.

2.3. Interaction of Charged Particles with Matter

For many of the applications of the DWC, the particles that will be tracked are muons, protons and heavy ions. When such radiation penetrates into a material, ionization or excitation occurs. Due to this, the particle transfers its energy and slows down along its route. The energy loss process is used to detect and extract the information about the passing particle.

2.3.1. Energy Loss of Heavy Charged Particles

While heavy charged particles travel through some material, their mean energy loss per distance can be computed by the stopping power of the material, which was firstly calculated by Bohr. The correct quantum mechanical calculation was done later and named the Bethe (or Bethe-Bloch in older texts) formula. The energy loss is, at least for primary ionization, proportional to the density of the absorbing material.

$$\left\langle -\frac{dE}{dx} \right\rangle = 2\pi N_a r_e^2 m_e c^2 \rho \frac{Z}{A} \frac{z^2}{\beta} \left[\ln \left(\frac{2m_e \gamma^2 v^2 W_{max}}{I^2} - 2\beta^2 - \delta - 2\frac{C}{Z} \right) \right] \tag{2.2}$$

with $2\pi N_a r_e^2 m_e c^2 = 0.1535$ MeVcm^2/g and

(i) r_e: classical electron radius

(ii) m_e: electron mass

(iii) N_a: Avogadro's number

(iv) I: mean excitation potential

(v) Z: atomic number of absorbing material
(vi) A: atomic weight of absorbing material
(vii) ρ: density of absorbing material
(viii) z: charge of incident particle in units of e
(ix) β: v/c of the incident particle
(x) γ: $1/\sqrt{1-\beta^2}$
(xi) δ: density correction
(xii) C: shell correction
(xiii) W_{max}: maximum energy transfer in a single collision

W_{max} depends on secondary collisions.

$$W_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2s\sqrt{1+\beta^2\gamma^2} + s^2} \tag{2.3}$$

where $s = m_e/M$ (M is mass of the particle), also if $M >> m_e$ then

$$W_{max} \simeq 2m_e c^2 \beta^2 \gamma^2 \tag{2.4}$$

Moreover, since I, the mean excitation potental, is the main parameter of the Bethe formula and is hard to calculate, the semi-empirical formulas have been used such as[2],

$$\frac{I}{Z} = 12 + \frac{7}{Z} eV \qquad Z < 13 \qquad and \qquad \frac{I}{Z} = 9.76 + 58.8 Z^{-1.19} eV \qquad Z \geq 13 \tag{2.5}$$

There are further corrections to the Bethe Formula, but they are hard to calculate for the system. People mostly use approximate results from Equation 2.2.

On the other hand, electrons and positrons undergo an additional energy loss when passing through a material named Bremsstrahlung because of their small mass in the region of the strong electric fields of atomic nuclei.

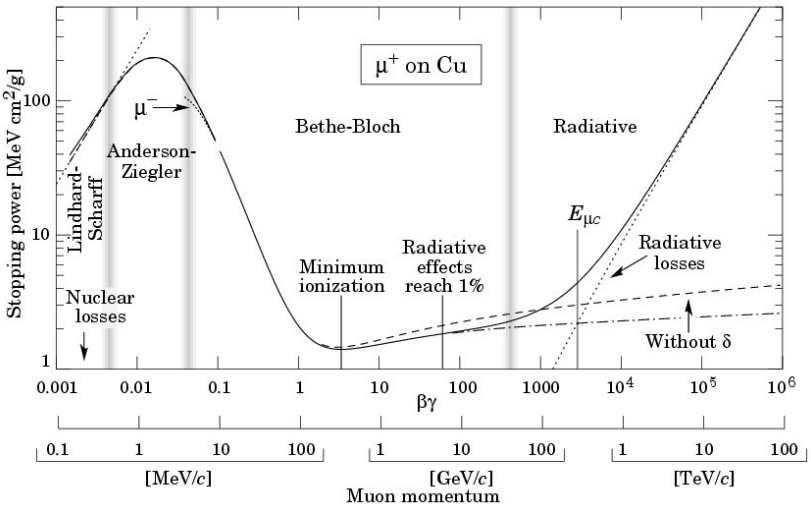


Figure 2.4. Corrections of stopping power for muons on Copper [15].

In order to have an idea about the order of magnitude of the electrical signal that will be produced on the cathode wires, let us consider a minimum ionizing muon (p $\cong 300\,\mathrm{MeV/c}$) passing through 1 cm of Ar-CO_2. Using the energy loss calculation in Equation 2.2, the expected energy loss will then be $3.2\times10^3\,\mathrm{eV}$. According to Reference 2.3, the energy to create an ion-electron pair is about 30 eV, so we expect approximately 107 pairs to be generated within the time it takes for the muon to penetrate 1 cm, i.e. $3.3\times10^{-11}\,\mathrm{sec}$. Hence, a current of about $5\times10^{-7}\,\mathrm{A}$ will be generated, $25\,\mu\mathrm{V}$ will be produced on a $50\,\Omega$ resistor, a too small to be detected. On the other hand, the avalanche effect in the chamber will provide a significant gas gain. While the exact magnitude of this gain requires a detailed simulation, we can get a rough estimate from Figure 2.5, which shows the gas gain of a similar gas detector using Ar-CO_2 mixture. As can be seen from the figure, the gas composition and the applied high voltage significantly change the outcomes, but it is safe to assume a gas gain of at least 10^4 for our wire chamber. With such a gain the generated pulse will have a magnitude of about 250 mV. If a high efficiency detector is desired, one should be able to work with signals of magnitude at least 10 times smaller, meaning we need an electronic amplifier that can work at $\sim 25\,\mathrm{mV}$.

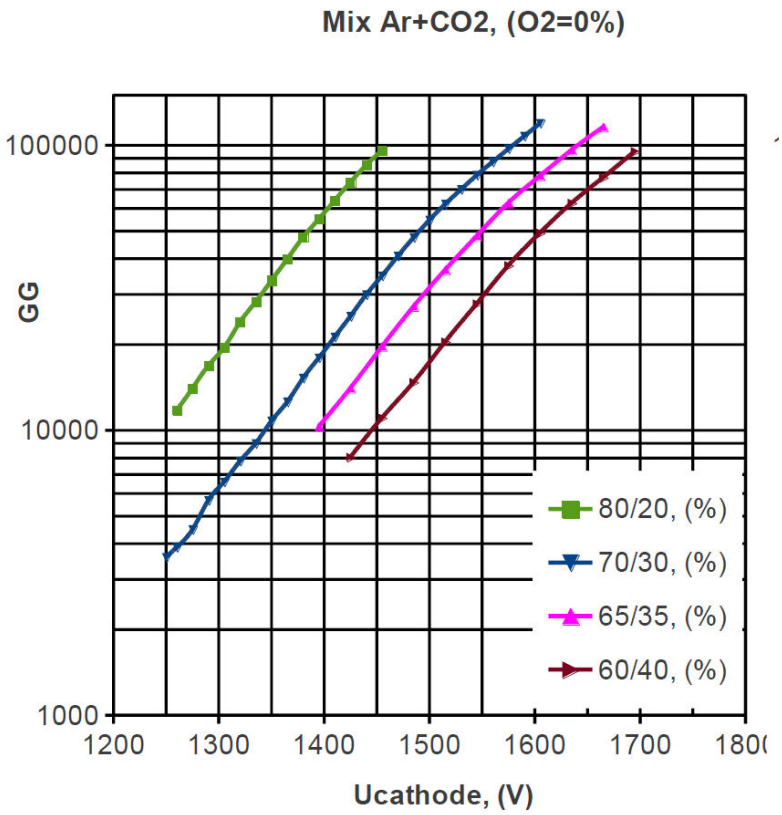


Figure 2.5. Gas gain for mixture Ar-CO_2 [16].

3. BASIC INTEGRATED COMPONENTS OF DWC ELECTRONICS

The readout electronics of a Delay Wire Chamber (DWC) has to perform two fundamental functions:

(i) the amplification of very short and small electrical pulses from the signal wires,
(ii) delay the pulses by an amount proportional to the position of what wires they are collected.

In this chapter, we will introduce the integrated components that are responsible for these two fundamental functions: propagation delays and operational amplifiers (op-amps).

3.1. Propagation Delay

In the DWC electronics, propagation delays are implemented in the form of integrated circuits (IC). Outputs of this IC is generated with time differences, namely adds a varying delay. From different output pins these signals can be obtained. In this IC, passive components are used as delay elements.

A passive delay line is basically formed by inductors and capacitors. Each unit of delay consists of one capacitor and one inductor. By connecting these units in series one can get different delay times. Since, this circuit does not include resistors ideally, no attenuation is observed, hence, the gain of each signal is one ideally. But, in reality capacitors and inductors have equivalent series resistance, so the gain must be lower than one.

In this scheme each delay components have the same delay value due to the usage of the same inductor and capacitor values.

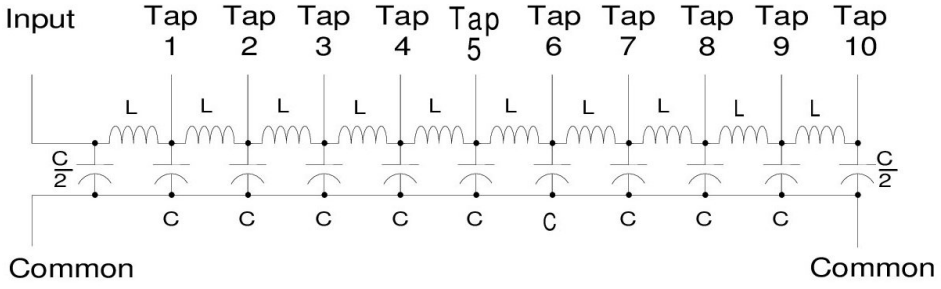


Figure 3.1. The Schematic diagram of the propagation delay which has been taken from the related company by special request.

$$\text{Delay per section:} \qquad \sqrt{L \times C} \tag{3.1}$$

$$\text{Line impedance:} \qquad \sqrt{L \div C} \tag{3.2}$$

But in reality it is not possible to get an ideal delay line so resistances added to each cycle in a serial way.

3.2. Operational Amplifiers

3.2.1. What Is An Operational Amplifier?

Op-amp is an ideal amplifier with infinite gain and bandwidth. As it can be seen in the Figure 3.2, a basic op-amp construction includes one positive input and one negative input, one output and two power connections; positive and negative DC supply voltages.

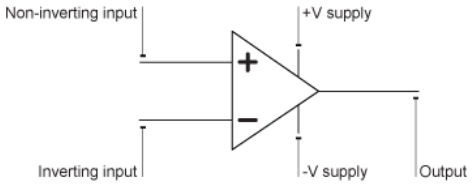


Figure 3.2. A Basic Op-amp Scheme[7]

3.2.2. What Are Operational Amplifiers Made of?

Op-amps are made of transistors. In general, transistors include Bipolar Junction Transistor (BJT) and Field Effect Transistor (FET) types. BJTs have very high input impedance and very low output impedance. FETs are almost ideal transistors and they are assumed to have infinite input impedance. They also have very low output impedance. This is very crucial since an ideal amplifier has to have infinite input impedance and zero output impedance. This is due to the fact that the input signal must not be attenuated and must be amplified ideally. Hence, there is no input leakage current entering into the op-amp. Zero output impedance is necessary in order to receive whole the amplified signal. Transistors are the cheapest and the most basic electronic components that can achieve this. This is the reason why op-amps are made of transistors.

3.2.3. Some Concepts In Operational Amplifiers

In this subsection, we review the basic glossary relating to the successful operation of an op-amp.

3.2.3.1. Gain Concept In Op-Amp. Ideal op-amps have infinite open loop differential gain. In reality, typical open loop differential DC gain ranges from 10^5 to 10^6. Due to transistor gains infinite gain is impossible.

Feedback is the directing back the outputs as inputs into the same system. Conceptually, negative feedback is used to eliminate undesired components, errors or fluctuations of output, which are resulted from the changes in the inputs or disturbances in different stages. In electronic systems, positive feedback is generally considered harmful for the circuit since it increases the noise. Therefore, in electronic circuits negative feedback is a widely used concept. When a negative feedback is applied to an op-amp the resulting gain is much lower and named as 'closed loop gain'.

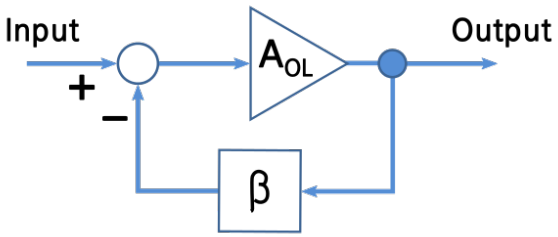


Figure 3.3. Feedback Scheme[8]

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL} \times Feedback} \tag{3.3}$$

3.2.3.2. Bandwidth. There is a range of frequencies in which a circuit can operate. The difference between the upper bound and the lower bound of operation is called the 'bandwidth' of the circuit. In general, op-amps have very low bandwidth due to their very high gain. The multiplication of gain and bandwidth is constant. There are two types of op-amps: uncompensated and compensated. By using capacitive feedback the bandwidth can be increased. If capacitive feedback is applied internally in an op-amp, this kind of op-amp is called 'compensated'. If not that kind of op-amp is called 'uncompensated'.

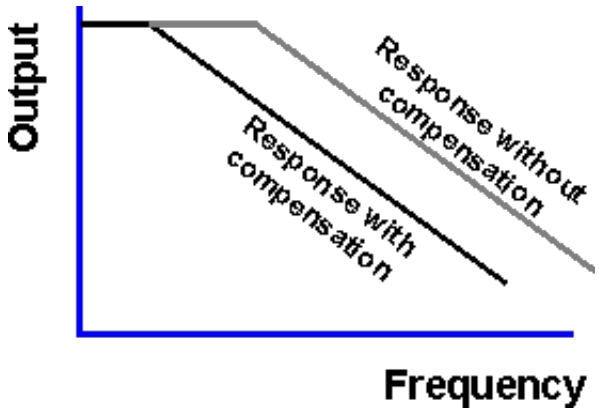


Figure 3.4. Op-amp frequency response with and without frequency compensation.[12]

In general, op-amps are used in low frequency applications but if there is a need for an high frequency application capacitive feedback or the use of uncompensated op-amps are must. If uncompensated op-amps are used in this case external capacitive feedback must be applied.

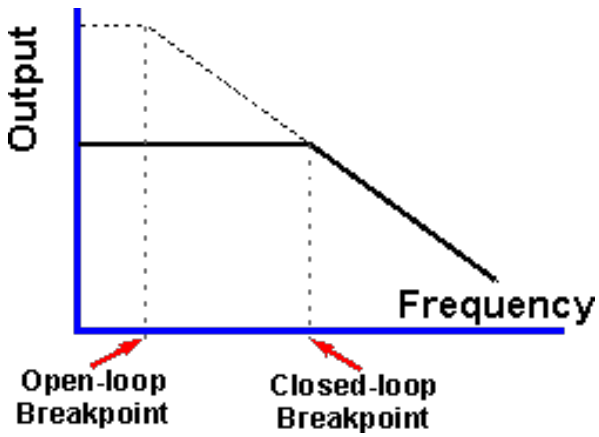


Figure 3.5. Closed loop op-amp frequency response. Applying feedback will reduce the gain but increase the bandwidth.[12]

3.2.3.3. Power Supply. For proper operation, op-amps must be externally DC powered. This way, transistors are biased into the correct region. In order to get rid of the AC noise present in the supply and ground rails by-pass capacitors must be used. They are also called 'decoupling capacitors'. This noise can cause unstability in the circuit. On the other hand, output saturates at a certain voltage level due to external DC powering. In general, the negative and the positive saturation values are equal. For example, in op-amp 741, which is the most common and versatile type of op-amp, output voltage swing is between -13 and $+13$ Volts for ± 15Volts.

3.2.3.4. Slew Rate. The slew rate of an op-amp is the indicator of quality at which the output follows the step change in the input. If the step change in the input causes a change in the output that is higher than the slew rate the output cannot follow the shape of the input and saturates at some point. Another case is that the change in the input may be faster than the slew rate. Hence, the output cannot follow. These cases are called 'slew rate limiting'. Slew rate is a function of voltage change per time and for op-amps typically is given by volt per microseconds.

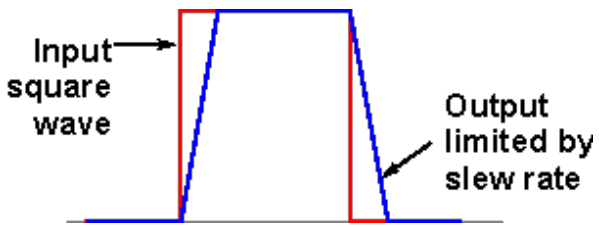


Figure 3.6. Op-amp slew rate illustration.[13]

3.2.3.5. Common Mode Rejection Ratio (CMRR). Op-amps are used as a differential amplifier and ideally common mode signals are totally rejected. An ideal amplifier would give zero output when common mode inputs are applied, which means zero common mode gain, but this is not the case in reality since op-amps have finite CMRR. CMRR can be calculated as differential gain over common mode gain.

3.2.3.6. Power Supply Rejection Ratio (PSRR). Ideally op-amps must reject the changes in the supply voltages. However, real op-amps have finite PSRR which results in a change at output when there is a variation at power supplies.

3.2.4. Inverting And Non-Inverting Amplifiers

By using op-amps and external resistances one can get two main types of amplifiers: inverting and non-inverting amplifiers.

3.2.4.1. Inverting Amplifiers. The Figure 3.7 represents a basic inverting op-amp circuit. It consists of two external resistances one is connected from negative input and the other is from negative input to output terminal. The connection node between these two resistances is called 'virtual earth summing point'. The positive input is generally connected to ground (or zero voltage).

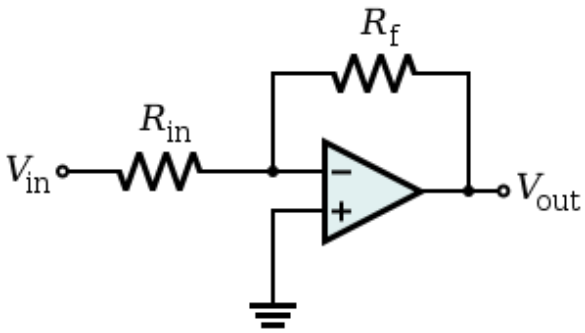


Figure 3.7. A basic inverting op-amp circuit [6]

How to calculate output voltage in an inverting op-amp?

According to Kirchoff's Voltage Law, it can be obtained:

$$V_{out} = -V_{in} \times \frac{R_f}{R_{in}} \tag{3.4}$$

and also this is the gain of an inverting amplifier:

$$Gain = \frac{R_f}{R_{in}} \tag{3.5}$$

It can be seen the gain is negative, output voltage is also negative. This means polarity. Because the input signal is given to inverting terminal so this causes in a sin-wave 180° phase shift.

3.2.4.2. Non-Inverting Amplifiers. In the Figure 3.8, in the same circuit, op-amp's negative input is grounded, and the signal is given to positive input. By the Kirchoff's Current Law gain and output voltage of the circuit can be calculated.

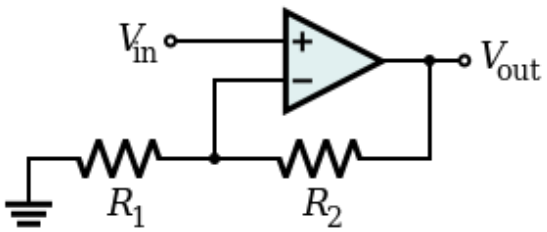


Figure 3.8. A basic non-inverting op-amp circuit [9]

$$V_{out} = -V_{in} \times (1 + \frac{R_2}{R_1}) \tag{3.6}$$

and also this is the gain of an non-inverting amplifier:

$$Gain = 1 + \frac{R_2}{R_1} \tag{3.7}$$

4. ELECTRONICS OF DELAY WIRE CHAMBER

4.1. Overview of the Circuit Schematics

The overall schematics of a DWC readout circuit, as utilized by CERN experiments, is shown in the Figure 4.1.

On the left side of the schematics, the first jag (J1) is seen. This is for the incoming signal. There are sixty pins; the first pin is for anode signal, seven of the pins are grounded, and the rest of them are for the cathode wires.

To the right of the J1, propagation delays, labeled EP9150, are seen. These are necessary in order to create the time gap between two outgoing signals. Each component provides 50 ns delay, in total, 250 ns delay can be obtained because there are five components in the circuit.

After the incoming signal from the cathode wires leaves out the propagation delays, they are directed to two parallel amplification stages as seen in the upper part and the bottom part of the circuit schematic. Both of them consist of two stage op-amp circuits. The first stage is a non-inverting op-amp circuit, the second one is an inverting circuit. Inverting parts of the circuits make 180 degree phase shift so shape of output signals will be inverted and amplified.

On the other hand, in the middle of the circuit, there is just a single stage op-amp circuit, which is connected to the anode wire. Since this line directly connected to incoming signal, the signal experiences no amplitude reducing effect (attenuation) from the propagation delays. Thus, one inverting op-amp is enough to provide an adequate amplification of the signal.

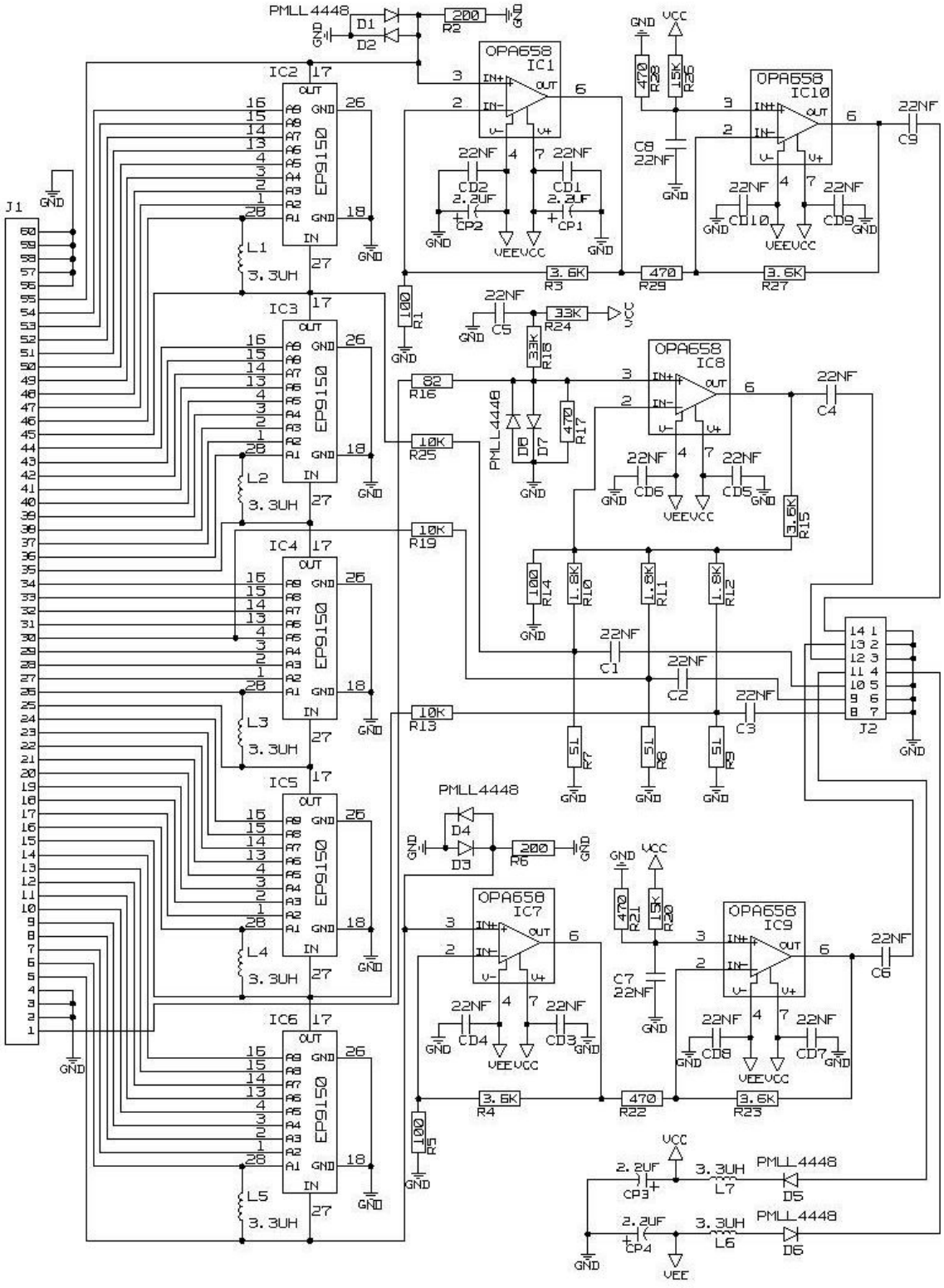


Figure 4.1. Electronic schematics of DWC [1].

To the right side of the electronics diagram, there is the second jag(J2). It has fourteen pins; six of them are grounded, 8^{th} , 9^{th},and 10^{th} number of pins are directly connected the input jag; J1. 12^{th} is output of the anode wire, 13^{th} output belongs to bottom part of the circuit and the 14^{th} output is for outgoing signal from the upper part of the circuit. 4^{th} and 11^{th} pins are directly linked to a separate part of the circuit. This subcircuit is responsible for voltage supply protection for the whole circuit. Negative and positive voltage supplies are given from this small part to the whole system through 4^{th} and 11^{th} pins.

When the incoming signal passes the delay lines separate two signals with some time difference. Then one will go to the down part of the circuit the other one will go to the upper part of the circuit. These are the two stages of the circuit. Incoming signal passes through non-inverting and inverting op-amp circuits, is amplified by these circuits and goes to output pins at J2; pin 13 and pin 14. By this way, electronic read-out signal can be obtained.

4.2. Specifics of the Components

In this section we review some specific functions and properties of the crucial components of the circuit.

A number of capacitors are used for decoupling (bypass) capacitor and noise elimination. Values of the resistors are set the provide needed feedback gain. While the use of inductors are generally undesirable due to unwanted electromagnetic effects, they are used to eliminate the effects of capacitive loading. Lastly, diodes are used as 'flyback diodes' in this circuit and they eliminate sudden voltage spikes and arcing.

In the CERN version of the circuit scheme, EP9150s were used as the delay components. This components has a $200\,\Omega$ characteristic impedance with 50 ns delay and is a ten tap SMD (Surface Mount Device). However, this brand of delay is no longer produced, so AIZ-502 (J-SMD) is used in our implementation. AIZ-502 has about $0.5\,\Omega$ resistance per tap when measured by an ohmmeter. Maximum DCR for

AIZ-502 is listed as 5.6 Ω on its datasheet, as we would expect from series connection over ten taps.

OPA658 was used in the circuit as an other important component, but this is not produced any more, OPA694 is used as an improved version of OPA658.

OPA694 is a kind of wide band, low-power, current feedback op-amp [18]. This op-amp is a standard eight pin op-amp with SO-8 package. This package is a standard surface mount package. It uses low power supplies which is ±5 V. Typical value for op-amp supplies is ±12 V. This is the reason why this op-amp is a low power op-amp.

As the datasheet of OPA694 is reviewed, it can be easily deduced that the op-amp is mainly a large band width op-amp. The op-amp is primarily used for radio frequency (3kHz to 300GHz) applications. These frequency values are useful especially for telecommunications systems like radios, TV, etc. and this op-amp can be used in the pre-filter or pre-amplifier stage of those systems due to its large frequency bandwidth. In addition, this op-amp supplies high gains despite of its large bandwidth. This means that its gain-bandwidth product is also very high. It can operate at a high frequency with high gain. Although this op-amp enjoys large frequency bandwidth and gain-bandwidth product, in this study, this op-amp is not used for these properties.

OPA694 has 1700 V/μs slew rate. This value is a very high slew rate value since a typical 741 op-amp slew rate is around 0.5 V/μs [17]. In this study, particles appear for a very short time period and the detector must detect the particles fast enough. Therefore, a high slew rate op-amp must be used in order not to miss the resulting signal at the input.

Although there are certain techniques for eliminating the offset voltage externally, this op-amp eliminates it by means of its internal circuitry.

On the other hand, this op-amp cannot eliminate noise by its internal circuitry. There are several noise sources in this configuration. The wires can work as an antenna and adds external noise into the system. Components such as resistors and op-amps lead to oscillations at the output due to negative feedback. Oscillations cannot be defined as noise scientifically, but it adds up to the general noise value, hence the resulting effect of oscillations on the circuit is like a noise. To prevent the destructive effect of noise and smooth out the output, a 22 nF capacitor is connected to the output of subcircuits before reading-out.

4.3. Fourier Analysis of the Test Signal

The Fourier transformation of a signal enables the study of its frequency components. The real and the imaginary parts of our calibration signal are shown in the Figure 4.2. Absolute value of the Fourier transformation represents the frequency magnitude of the signal at this point, and in the Figure 4.3 its argument gives the location information (phase) of the signal.

Based on these figures most of the calibration signal is confined to below ~ 500 MHz. Hence, in order to have proper response from our DWC circuit, we have to use circuit components whose bandwidth is 500 MHz or more. In particular, the choice of OPA694 was made based on this observation [18].

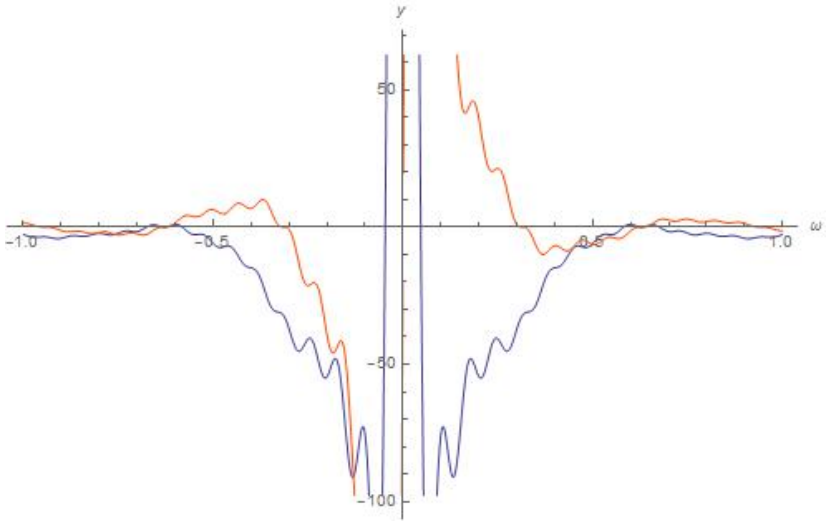
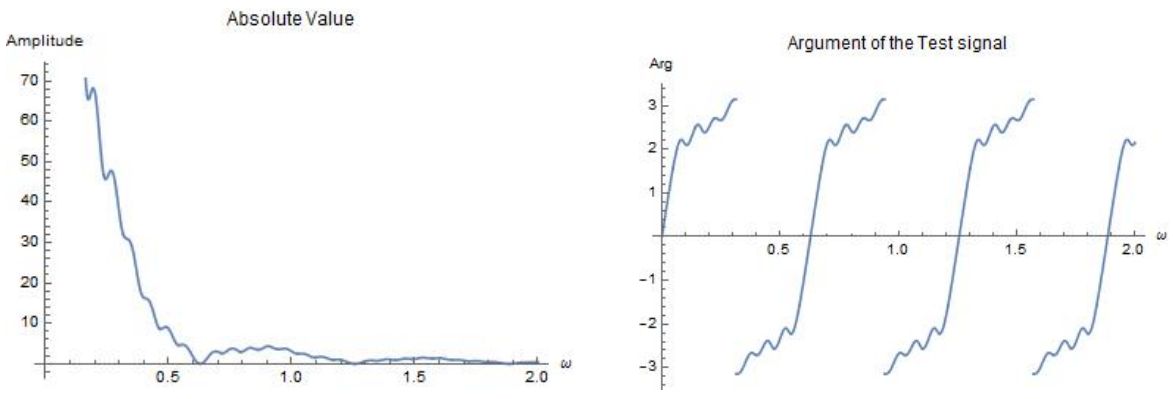


Figure 4.2. The result of the Fourier Transformation of the DWC's calibration signal which is solved by Mathematica.The blue line represents the real part of the signal. The orange line represents the imaginary part of the calibration signal.



(a) (b)

Figure 4.3. (a) The absolute value of the Fourier Transformation for the test signal. (b) The argument of the Fourier Transformation for the test signal.

5. EXPERIMENT

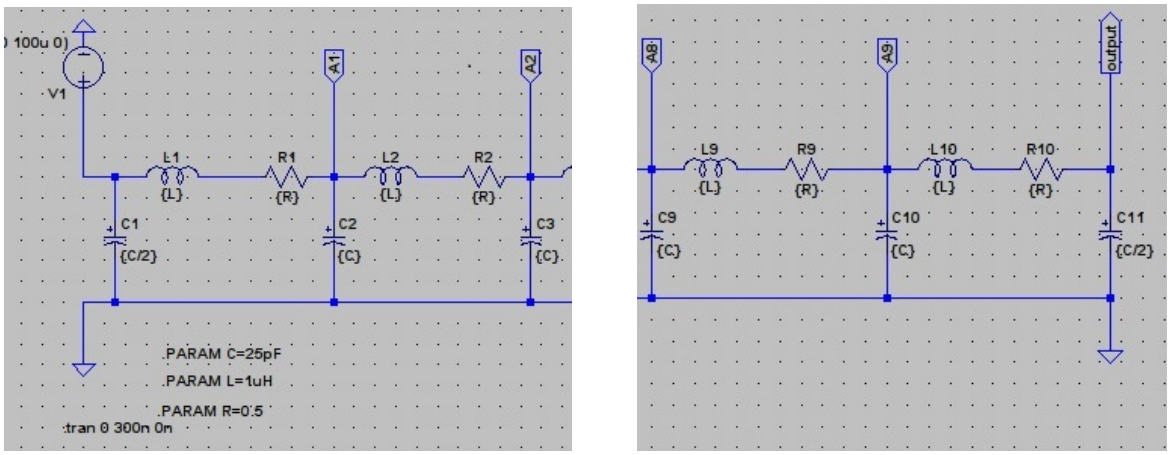
In this study, to figure out the working principle of an electronic circuit of a DWC, various software studies and hardware studies were pursued. LTspice IV (Linear Technology-Simulation Program with Integrated Circuit Emphasis) and Tina-Ti (Toolkit for Interactive Network Analysis-Texas Instruments) simulation programs were used for understanding the behavior of the circuit before starting to the implementation in actual hardware, first on a breadboard and later on PCB (Printed Circuit Board). As we still describe below, each major functionality of the circuit was studied separately first, and later combined together. Hence the propagation delays, amplification stages, etc. were all simulated and implemented as subcircuits and tested before all of them were put together as the final product.

5.1. Simulation

LTspice IV and Tina-Ti are both free, high performance, SPICE (Simulation Program with Integrated Circuit Emphasis) based, analog electronic circuit simulator programs. They have different graphical user interferences and we started our simulations with LTspice IV because of its somewhat easier use, particularly for implementing models of non-LT, non-Ti components like AIZ-502. We later decided to use Tina-Ti as the op-amps we use, OPA694, are produced by Texas Instruments. Furthermore, using both programs allowed us the cross check the reliability of our simulated results.

5.1.1. Simulation of the Delay Component

We first start with the simulation of the propagation delay in order to understand its working principles. These simulations were initially performed before the AIZ-502 components reached us, as we needed to assess the behavior of the component and we wanted to observe the delay as well as attenuation characteristics as a function of the direct current resistance (DCR) between taps



(a) (b)

Figure 5.1. (a) The beginning part of the LTspice delay line simulation. (b) The last part of the LTspice delay line simulation.

According to the Figure 3.1, the simulation of propagation delay was done with LTspice IV. The necessary information, delay per section (5.0 ± 1.0 ns) and line impedance (200 Ω), was given in the datasheet of AIZ-502. Hence, its inductance and capacitance values were calculated with the formulations in the equations (3.1) and (3.2). In addition, as mentioned in the section 4.2, in a propagation delay, its components have equivalent series resistance. As the datasheet, the resistance per tap should be approximately 0.5 Ω[19]. Thus, 0.5 Ω resistance was added for each tap in the simulation of propagation delay lines. The schematics drawn in LTspice IV is shown in the Figure 5.1.

In our all experiments, a short pulse of 40 mV input voltage has been used as a test signal which is mentioned in J.Spaanggard's DWC guide[1]. It is a positive signal with a rise time of 10 ns, a flat top of 20 ns and a fall time of 60 ns. This pulse is repeated with a 10kHz frequency.

In Figure 5.2, the green line represents the input signal with 40 mV peak amplitude up to 90 ns, and, the blue line is output signal with 92 mV amplitude and 50 ns delay time. This is the behavior of an AIZ-502 passive ten tap delay line. However, there are some disturbances on the output signal as well as reflections in the input, be-

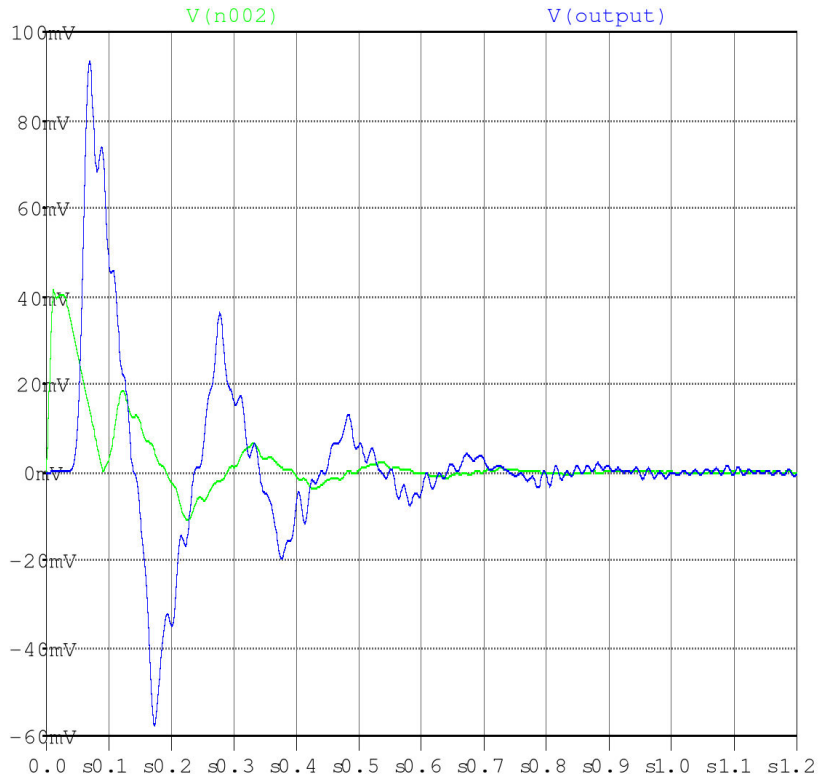


Figure 5.2. LTspice simulation result of propagation delay with 0.5 Ω series resistance. Green line represents the input signal, blue line represents the output signal.

cause of the Nyquist Criteria; which is the reason of unstable behavior. In addition, the input impedance of the delay component is much bigger than the output impedance, so the output signal is two times bigger than the input.

A possible way to attenuate these reflections is to increase the resistance per tap. As an example, instead of using 0.5 Ω series resistance, we show the results when we use 120 Ω per section in the Figure 5.3. The output signal starts again with a 50 ns delay, but the peak is reached another 50 ns later and the peak amplitude is reduced to 14 mV. This reduction is not desirable, on the other hand, in order to make stable of the system and not to amplify the noise on the output signal, it can be an advantage.

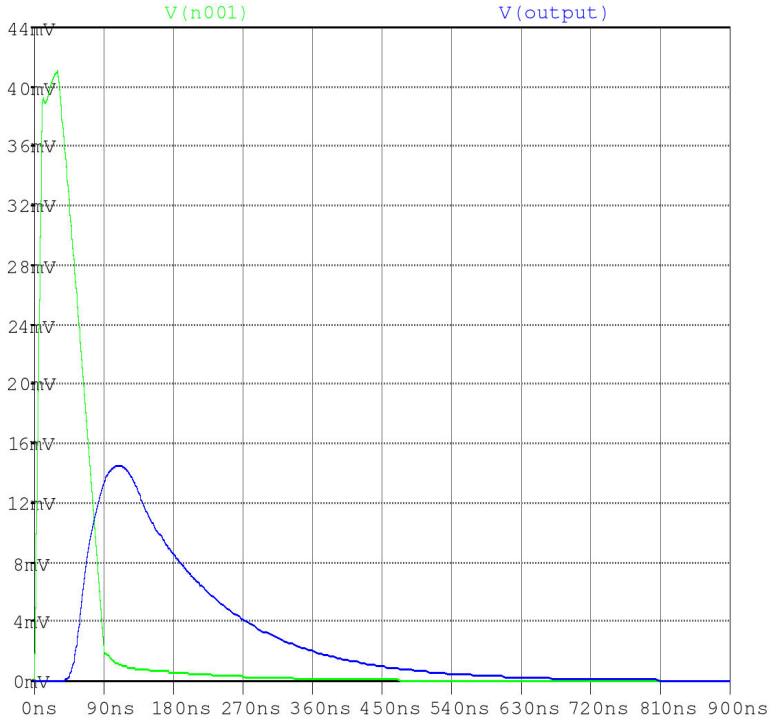


Figure 5.3. LTspice simulation result of propagation delay with 120 Ω series resistance. Green line represents the input signal, blue line represents the output signal.

5.1.2. Simulation of Cathode Signal Amplification Subcircuit

Besides from delaying the signal, amplifying is the other feature of the DWC's readout circuit. In the Figure 5.4, there are two copies of true amplifying subcircuits. In order to figure out their expected behavior, one subcircuit's simulation is performed using Tina-Ti.

The yellow line in the Figure 5.5 is 40 mV input test signal, the green line represents output signal with measured peak amplitude of −2.48 V. It can be deduced that the first non-inverting part of the subcircuit amplifies the incoming signal 35 times, and the inverting part makes an effect on ongoing signal which is that converts the signal which creates a polarity in the output signal and amplifies 2 times so output signal is obtained around −2.48 V.

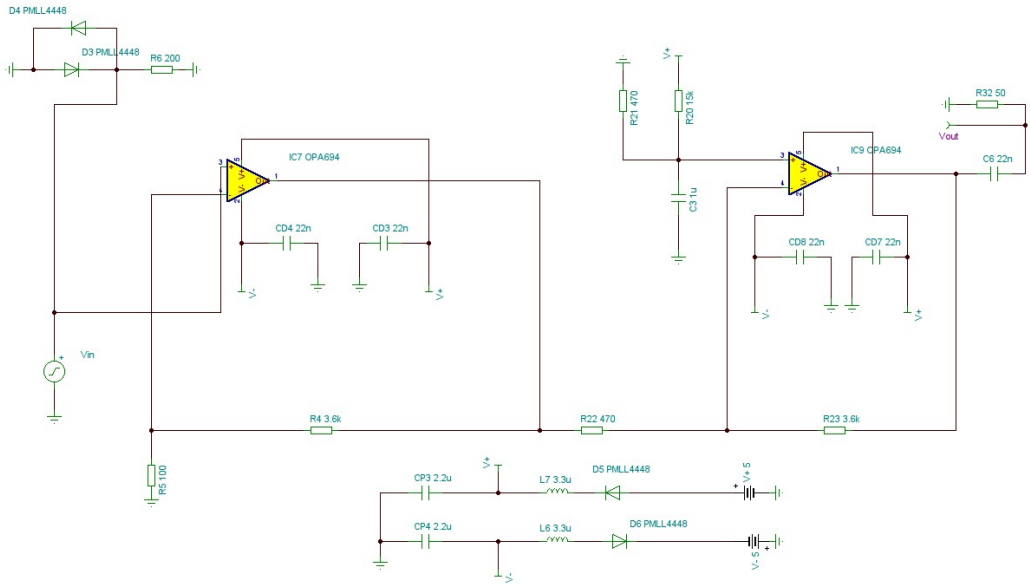


Figure 5.4. Tina-Ti simulation of the subcircuit responsible for amplifying the cathode wire signals

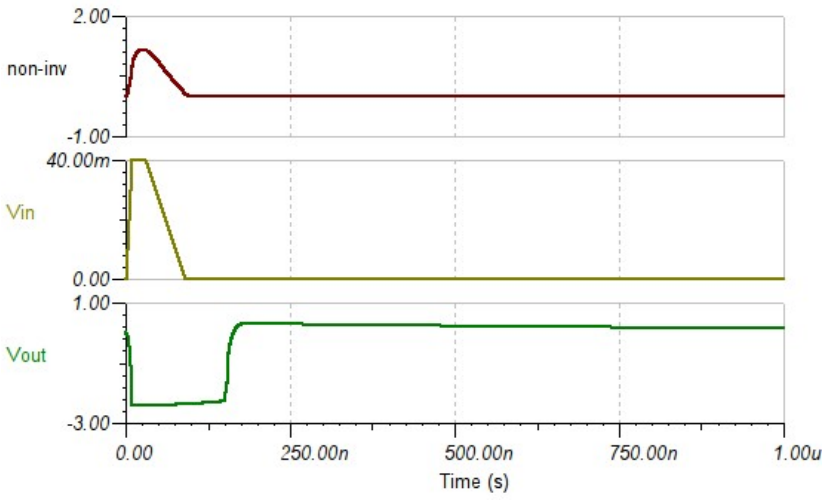


Figure 5.5. Tina-Ti simulation result of the amplification subcircuit. Yellow line is the input, green is the output signal of the amplification stage. Red line represents the first op-amp's output of the amplification stage.

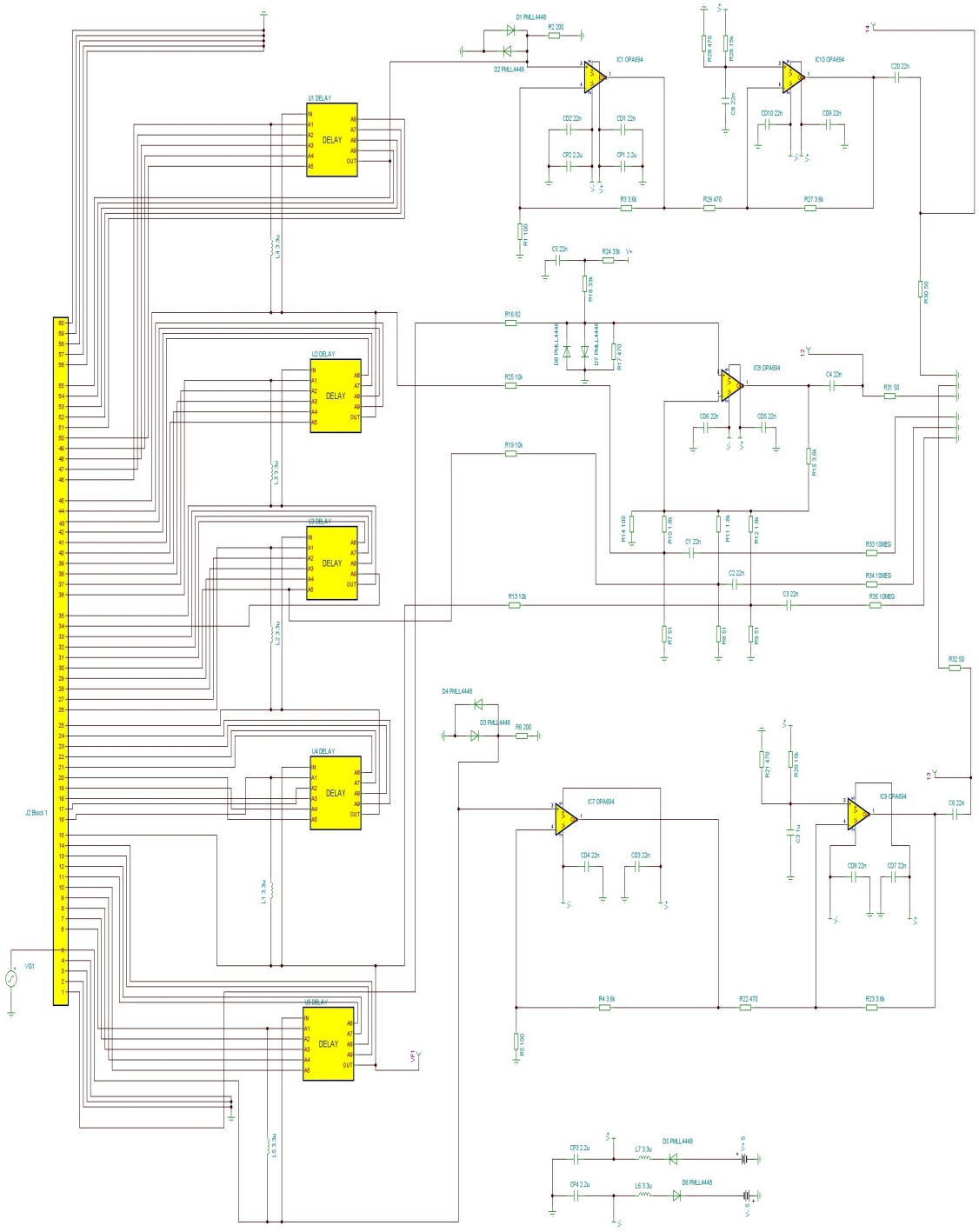
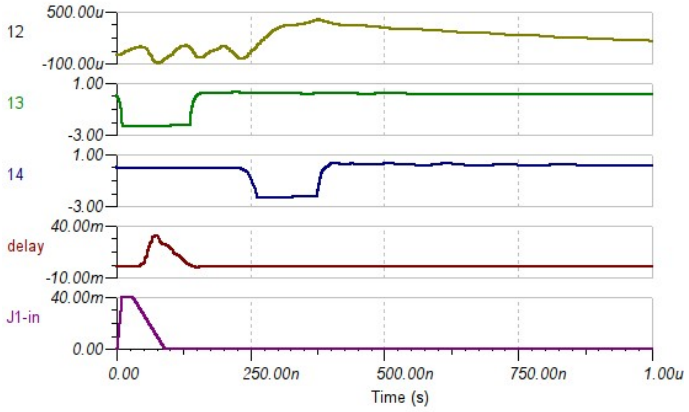
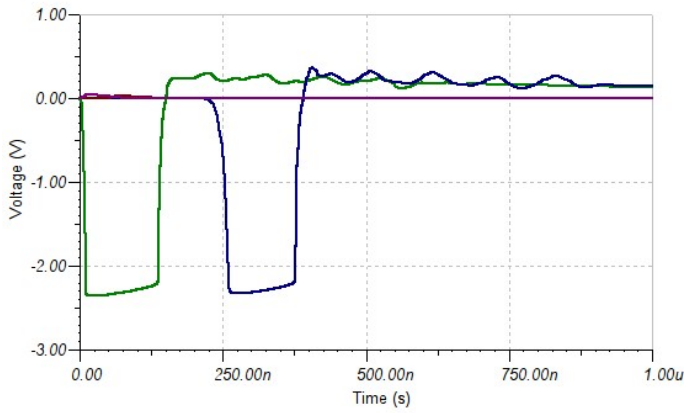


Figure 5.6. Tina-Ti simulation of the whole circuit

Since it has been also understood working principle of the inverting and non-inverting amplifying parts in the DWC's entire circuit, the whole circuit scheme has been built in Tina-Ti and has been run.



(a)



(b)

Figure 5.7. (a) Tina-Ti simulation result of the circuit as a whole. (b) Same as the (a), but the outputs are plotted on the same canvas for early comparison of the amplitudes and times.

The test signal has been given through the 5^{th} pin of J1 to the circuit. This is the lowest part of the circuit. By this way the incoming signal can directly reach the bottom amplifying part of the circuit by bypassing the propagation delays. On the other hand, a signal coming through the 5^{th} pin has to travel all the propagation delays before reaching the upper amplification subcircuit, i.e. 250 ns later than it reaches the bottom amplification subcircuit. Reading out of the outgoing signal is made through the 13^{th} and 14^{th} pins of J2. When the results of two output signals are compared, as seen in the Figure 5.7 (b) there are approximately 245 ns delay between them, and they have the same amplitude.

With satisfactory results from the simulations, we proceed to the implementation of the circuit on hardware.

5.2. Implementation on Hardware

For the delay wire chamber to be deployed at an actual beam line, it is essential that its readout circuit is implemented on a reliable way within the confines of a small volume. This necessitates printing the circuit on a small board by an industrial facility. However, for prototyping, we have to start on a breadboard, then proceed to a hand-drawn PCB (Printed Circuit Board), before we go to the final production.

5.2.1. Implementation on Breadboard

First of all, one of the propagation delays has been run on the breadboard in order to see if it works as in the simulation. According to the Figure 5.8, as yellow line is input and blue line is output signals, it can be clearly seen the behavior of the component and the simulation results are consistent with each other.

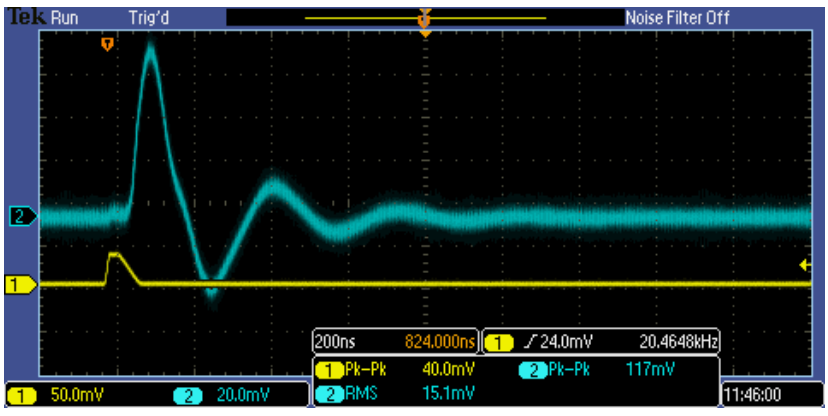


Figure 5.8. The oscilloscope screenshot from the testing of an AIZ-502 unit. Yellow line (1) represents the input signal. Blue line (2) represents the output signal.

Then, the subcircuit has been built on breadboard without propagation delays, and attempted to have the same result in the Figure 5.5.

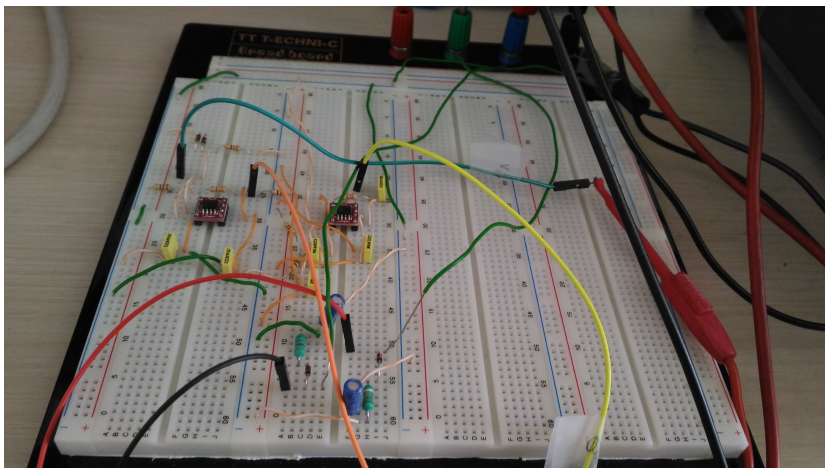


Figure 5.9. Setting up the 2-stage amplification subcircuit on a breadboard with the voltage protection part.

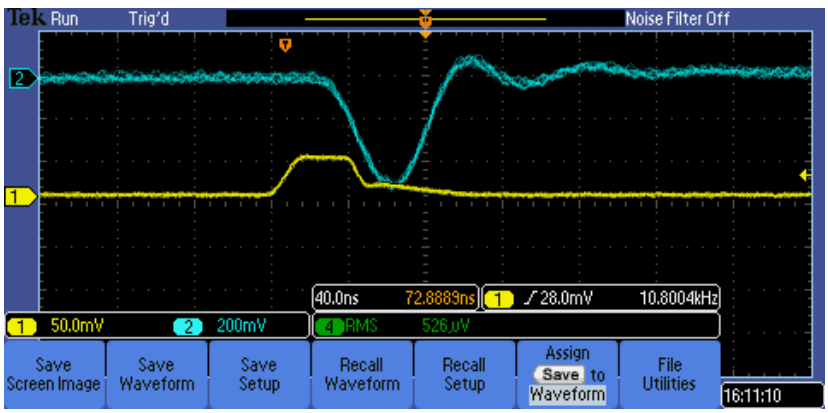


Figure 5.10. The oscilloscope screenshot from the test of the amplification subcircuit on the breadboard. The yellow line (1) represents input signal. The blue line (2) represents output signal.

However, the expected result cannot be obtained. Its gain is not correspond with the simulation result which was mentioned in the section 5.1.1. On the other hand, when the circuit is removed and constructed again, noise, feedback and some other disturbances are observed that cannot allow us to have the correct behavior of the circuit. There is instability. These problems mainly come in sight because of the extensional cables from the probes, and the wires which are necessary to have connection between nodes on the breadboard. Thus, it is needed a more steady system. The length of the cables and the wires should be minimized. Moreover, there should not be any cable which is wound on the built circuit, because these cables act as an antenna. Thus, the inconvenient output result has appeared on the oscilloscope.

5.2.2. Implementation on the Hand-Drawn Printed Circuit Board

The subcircuit has been constructed on PCB. There are both two stages of the whole circuit and also the voltage supply part. It has been aimed to give the supply voltages in a more proper way. By this way, if there is some problem because of that, it can also be eliminated.

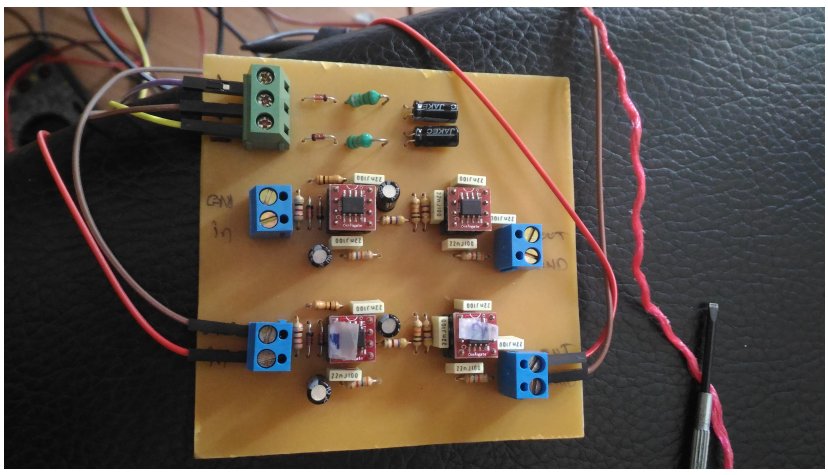


Figure 5.11. The amplificatin subcircuits of the DWC constructed on a hand-drawn PCB.

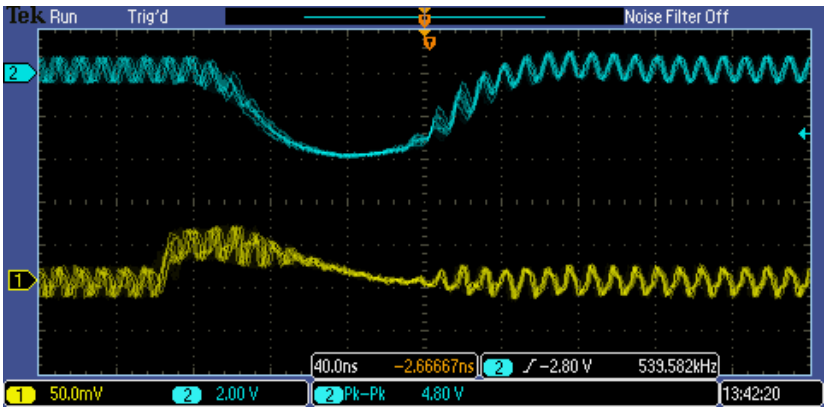
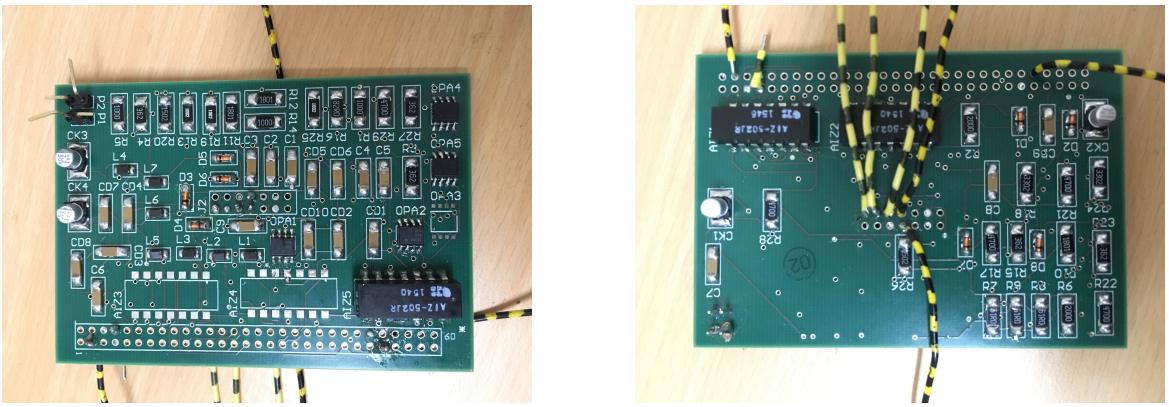


Figure 5.12. The oscilloscope screenshot from the test of amplification subcircuits on the hand-drawn PCB. The yellow line (1) represents the input signal. The blue line (2) represents the output signal.

Although, the gain of the subcircuit is fairly suitable to simulation result when it has been constructed on PCB, there is still slightly noise again, which we cannot eliminate, and it adds on the output signal. Moreover, when the voltage supplies are activated an unwanted oscillation also adds on the input signal. On the other side, it is pretty coherent with the simulation result.

5.2.3. Implementation on the PCB

Since the simulation results and the hardware measurements are consistent with each other, PCB has been ordered from Hi-Tech Corporation at Macedonia which is able to produce PCBs up to thirty-six layers. However, two round PCB has been produced because of some layout mistakes. In the very first round, mistakes has been attempted to be fixed and the circuit is run. However, our study and the following measurements are based on the second round PCB. Soldering of the components has been completed in our laboratory as can be seen in the Figure 5.13.



(a) (b)

Figure 5.13. (a) The front side of the soldered PCB. (b) The back side of the soldered PCB.

Soldering has been made part by part. By this way, it can be detected if there was some inconsistency with the PCB. Firstly, the cathode stages has been soldered and measured. While the measuring, the high amount of oscillation is observed in each part, and it cannot be possible to discriminate the output signal with the oscillation feedback. The results of our tests can be seen in the Figures 5.14 and 5.15.

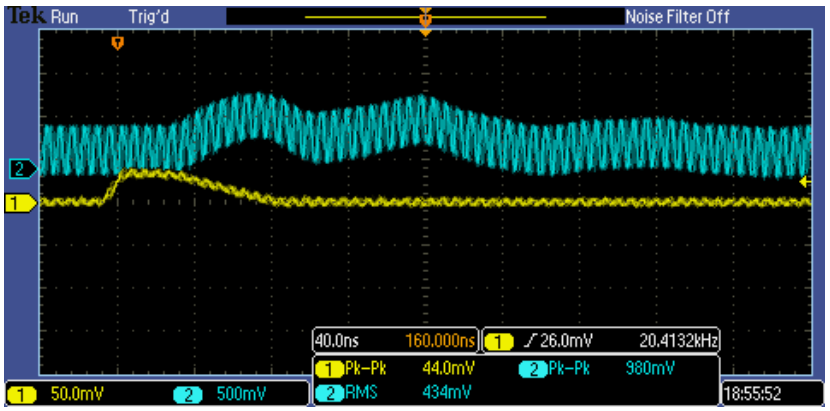


Figure 5.14. The oscilloscope screenshot from the test of the first op-amp stage of the upper amplification part. Yellow line (1) represents the input signal. Blue line (2) represents the output signal.

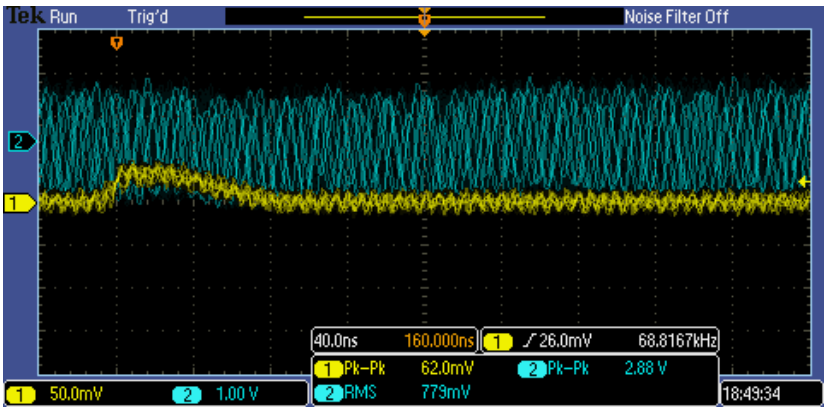
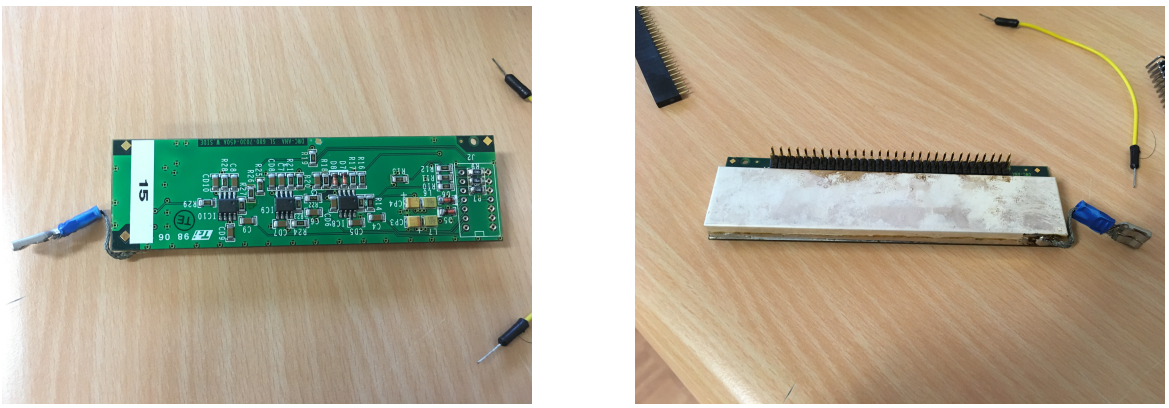


Figure 5.15. The oscilloscope screenshot from the test of the upper amplification part. Yellow line (1) represents the input signal. Blue line (2) represents the output signal.

However, we had a chance to do the same measurements with CERN's PCB which has was used in DWC, and to compare its result with us, so we might detect our problem.



(a) (b)

Figure 5.16. Example PCB used at CERN in DWC. (a) Front side and (b) back side of the PCB. It can be seen in the Figure (b)the initial op-amps are shielded.

Due to the studies which has been done by using CERN's electronic card, we can determine the our needs, and we turned to study on second round PCB card again.

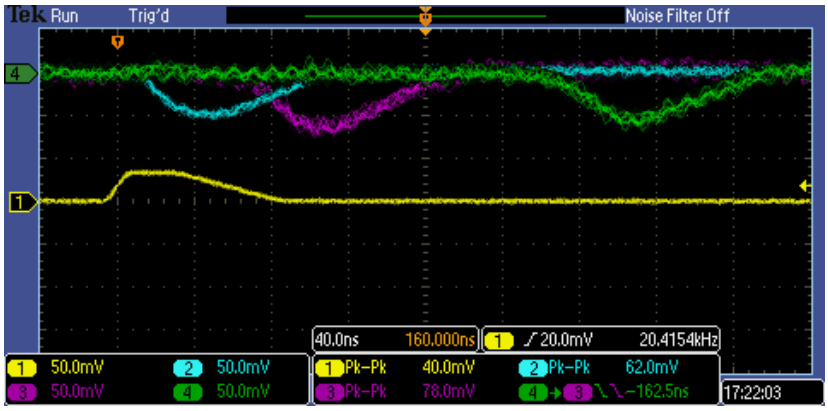


Figure 5.17. The oscilloscope screenshot of the CERN's PCB. The calibration signal was given by the upper side of the circuit. As expected, the signal reached first upper output (blue line) and then bottom part of the circuit (green line). Purple line is the anode signal.

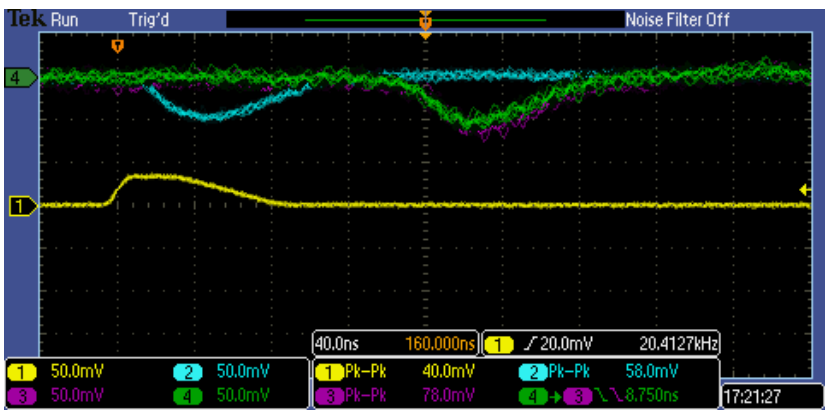


Figure 5.18. The oscilloscope screenshot of the CERN's PCB card. The calibration signal (yellow line) was given by the middle part of the circuit. Blue line represents output of the anode signal. As expected, purple (out-14) and green (out-13) lines are on top of the each other.

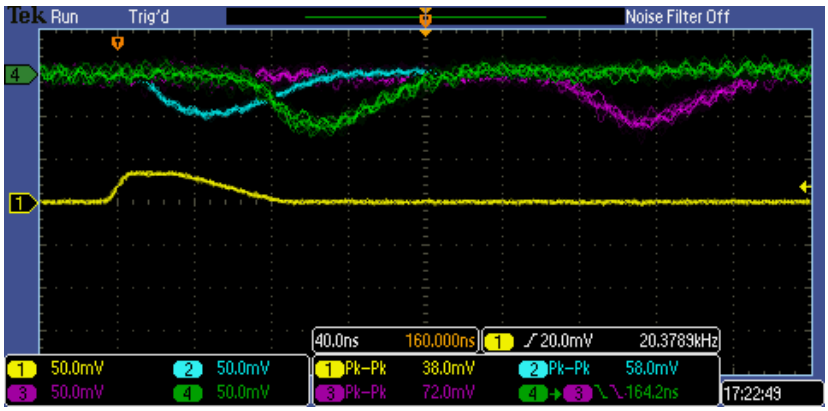


Figure 5.19. The oscilloscope screenshot of the CERN's PCB. The calibration signal was given by the bottom part of the circuit. Green line represents the out-12 (anode signal), blue line represents out-13, purple line is out-14.

Firstly, there is a part in the circuit, as can be seen in the Figure 5.20, which is called 'voltage divider' in electronics. Two resistors and one capacitor are used as voltage divider on the second part of the each op-amp stages. The aim of using voltage divider in an op-amp circuit is that if there is offset between inverting and non-inverting legs of an op-amp it will effect unity gain of the circuit. This is one of the main usages of voltage dividers. By using voltage divider our aim is to even up this incoherency and to modify offset between two input legs.

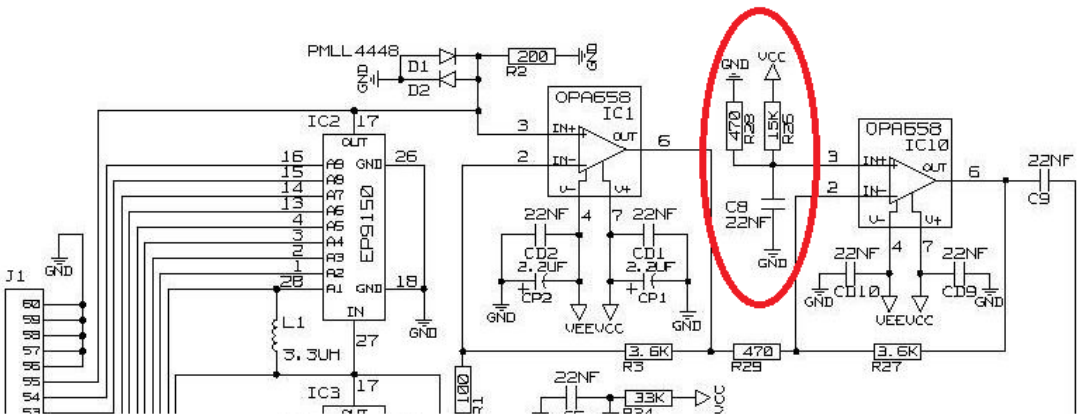


Figure 5.20. Voltage divider part is at the right side of the cathode stage, connected to the third leg of the op-amp.

Due to this aim, divider resistors which are used for the two op-amp stages are replaced with potentiometers in order to get proper resistor values as in the Figure 5.21. But we cannot make to work effectively it with ±5.0V supply voltage as in the Figure 5.22. It is worked with maximum between ±3.0V and ±3.5V voltage supply. The oscilloscope screenshots in the Figures 5.23, 5.24, and 5.25 exhibit the situation. As it is completely defined in the data sheet of OPA694, our supply voltage value range was consistent with its production range [18].

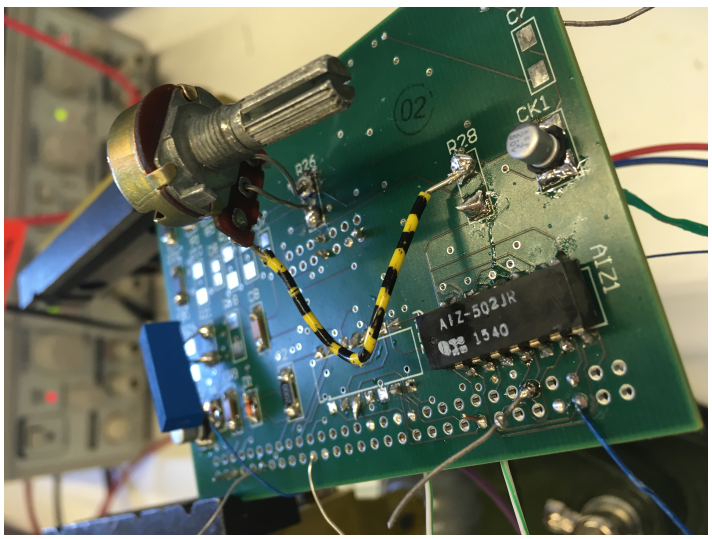


Figure 5.21. There are two potentiometer which able us to determine the right resistance divider values.

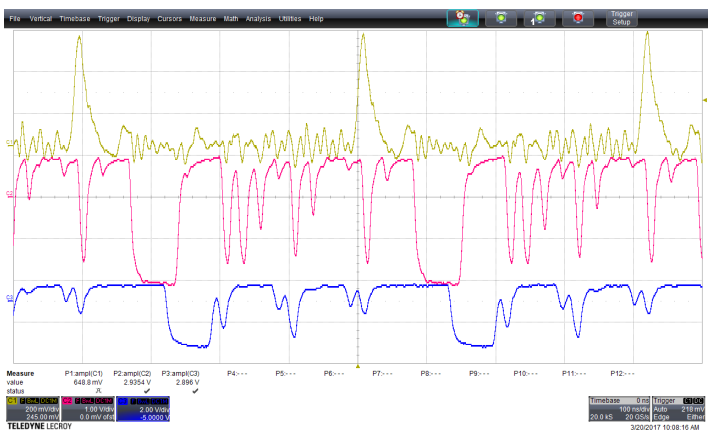


Figure 5.22. The oscilloscope screenshot represents the best result with ±5.0 V voltage supply while determining potentiometer values.

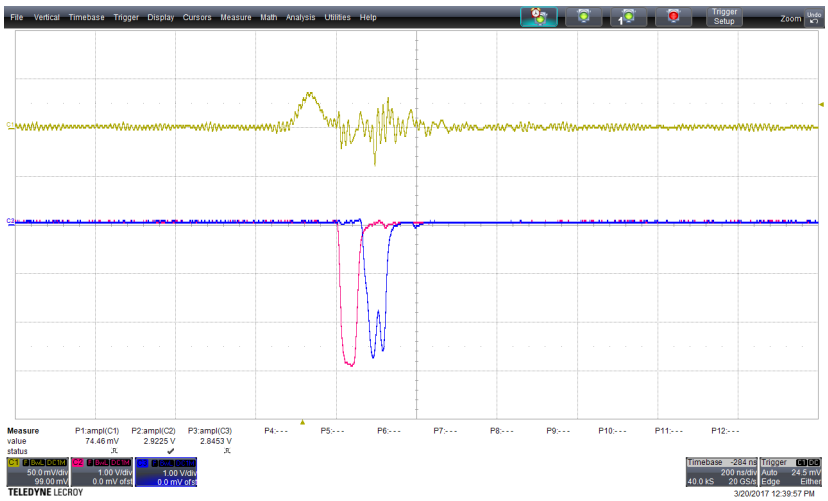


Figure 5.23. The oscilloscope screenshot represents the results with ±2.8 V voltage supply with the potentiometer.

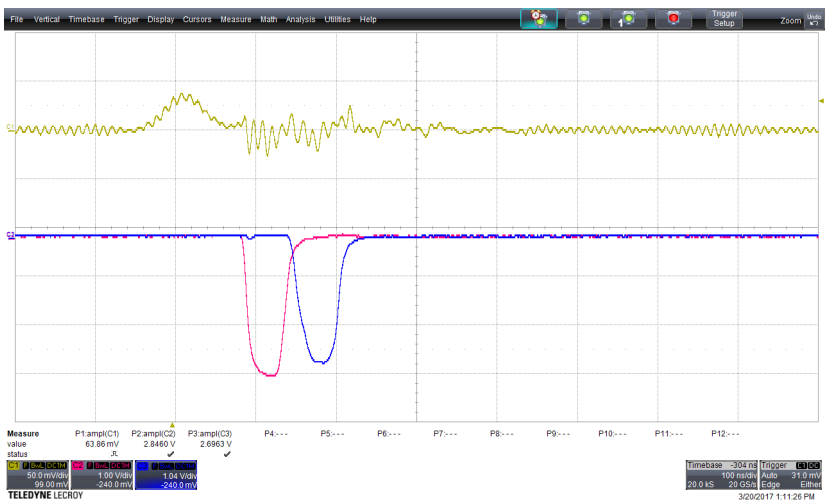


Figure 5.24. The result with ±3.0 V voltage supply with the potentiometer.

The calibration signal has been given the middle of the circuit, so it is aimed to take the best resistance values from the potentiometers. According to the Figure 5.24 measurement, potentiometers results are determined for R_{20}= 17k Ω, R_{21}= 54.5k Ω, R_{26}= 7.25k Ω, and R_{28}= 3k Ω.

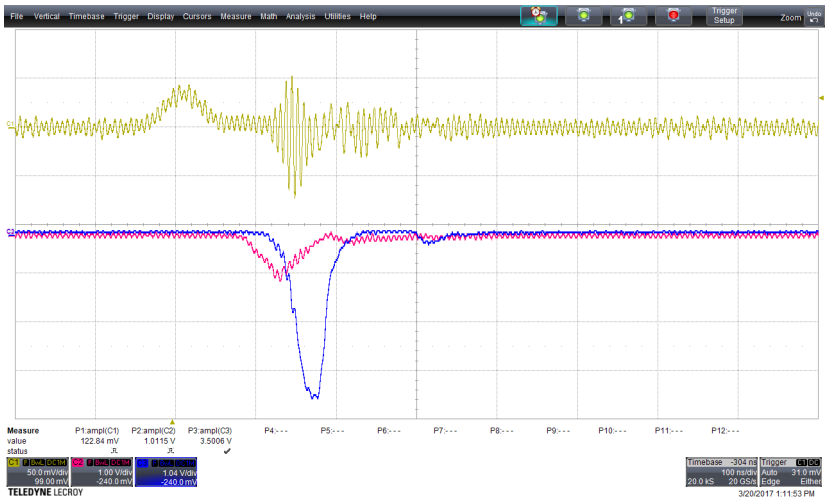
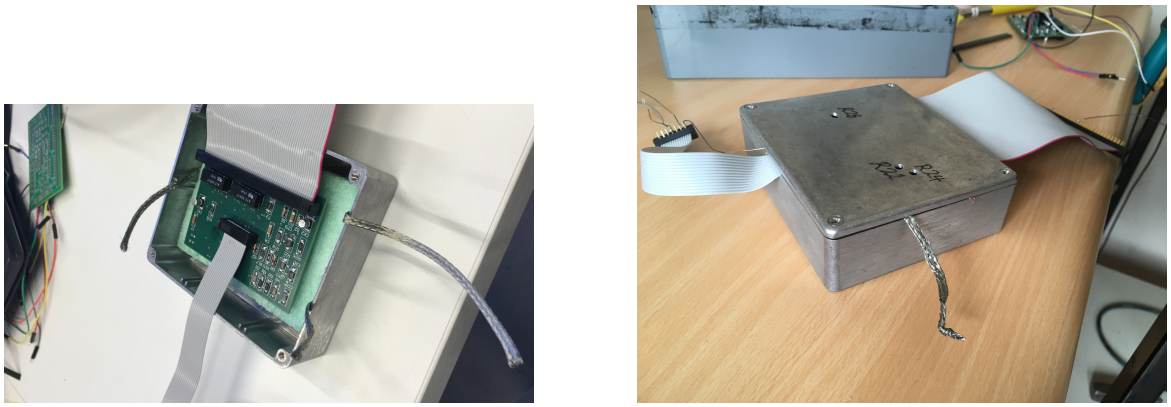


Figure 5.25. The oscilloscope screenshot represents the result with ±3.5 V voltage supply with the mentioned in the subsection 5.2.3 resistance values.

Second of all, propagation delays and op-amps are very sensitive to pick up every signal at the around and added them to the output signal, especially the first op-amps in each amplifier stages, should be shielded. In addition, we figured out that the probe cables which allow us to connect between the circuit and the oscilloscope, and even the cables which are used for connection between the nodes and components acted as antenna, so the length of the cables should be minimized and to refrain from oscillation the grounding is a must.

According to what we have experienced from the tests, we have carried forward out study in a next level. As can be seen in the Figure 5.26, for shielding we have used a small sized aluminum box and have made internal grounding. As we experienced from prior trials, grounding is very important for our circuit's effective working. We put out the cables from the circuit to avoid the interactions which can also cause unwanted



(a) (b)

Figure 5.26. (a) Inside of the shielded box. (b) Shielded box with small holes which let us to reach SMD potentiometers and to adjust right resistance values.

oscillation. By milling machine, we have made small leaks to the box and took out the flat cables to make measurements.

The oscilloscope screenshots in the Figures 5.27 and 5.28 exhibit the results after the necessary corrections.

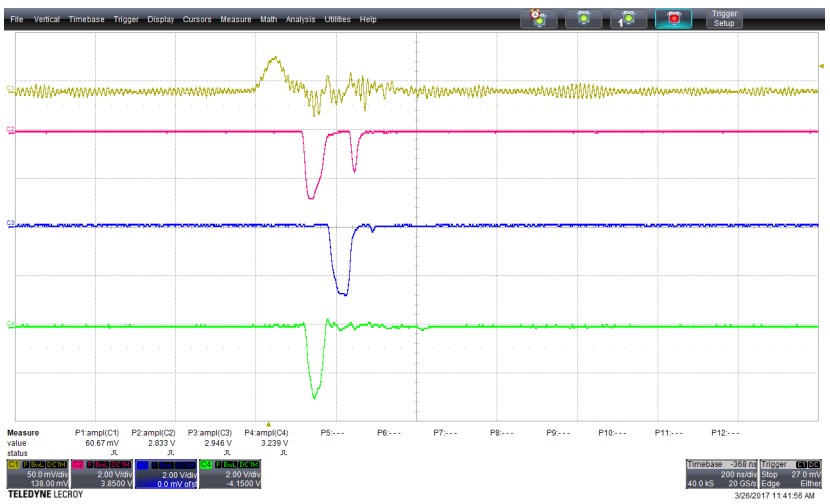


Figure 5.27. The oscilloscope screenshot represents the result of the shielded circuit with $\pm 3.0\,\mathrm{V}$ voltage supply.

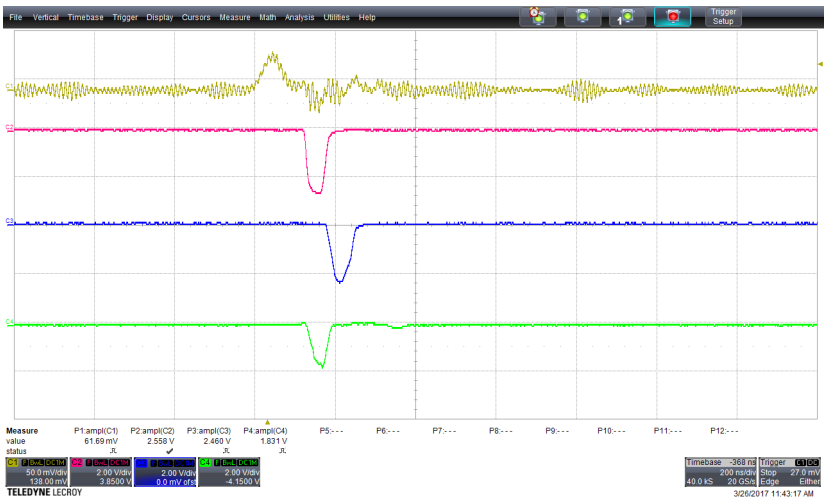


Figure 5.28. The oscilloscope screenshot represents the result of the shielded circuit with ±2.8 V voltage supply.

5.2.4. A New Approach to Electronic Schematic of DWC

After the necessary modifications on the DWC's circuit, one different improvement is done. Oscillations which is added input and output signals might be occur because of the reflections which is caused by the two op-amps effect each other. Hence, a NPN (Negative-Positive-Negative) type transistor has been used as a buffer. Its aim to isolate two op-amp stages each other, so unwanted reflection might be eliminated.

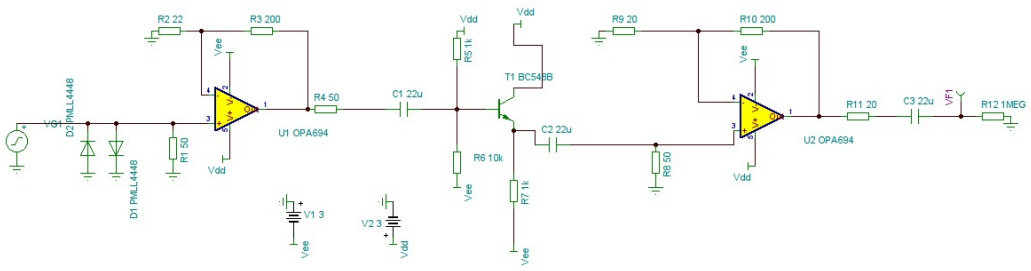


Figure 5.29. The Tina-Ti circuit simulation with transistor buffer

As can be seen in the Figure 5.29, a basic two stage non-inverting amplifier circuit has been designed. NPN-transistor is used for isolation between two stages. It has been designed to obtain an output signal which is 100 times bigger than the input signal. Due to the simulation result of the circuit in the Figure 5.30, as expected, when the input, 40 mV calibration signal, is applied, ±4.0V output signal is acquired.

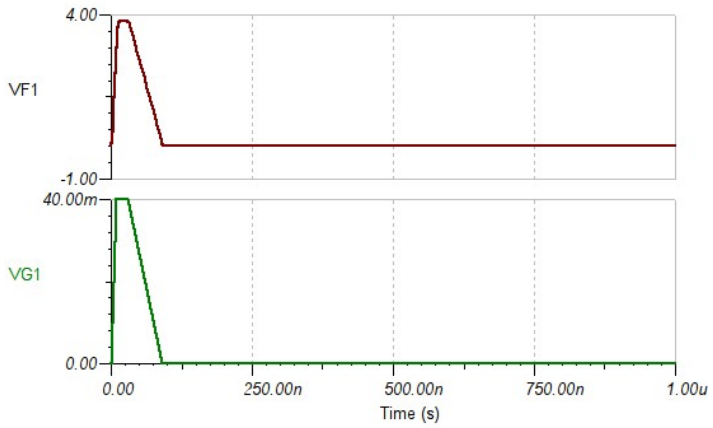


Figure 5.30. The Tina-Ti simulation result of the circuit with transistor buffer

In the next step, the same circuit is built on breadboard, but instead of BC548B type transistor JC548 type has been used, the only difference between them is that their legs order is different.

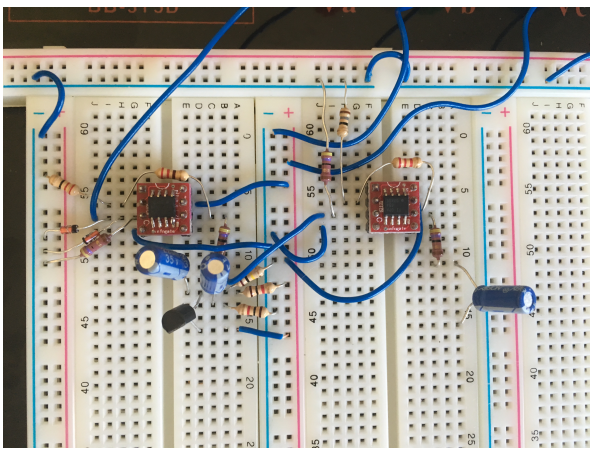
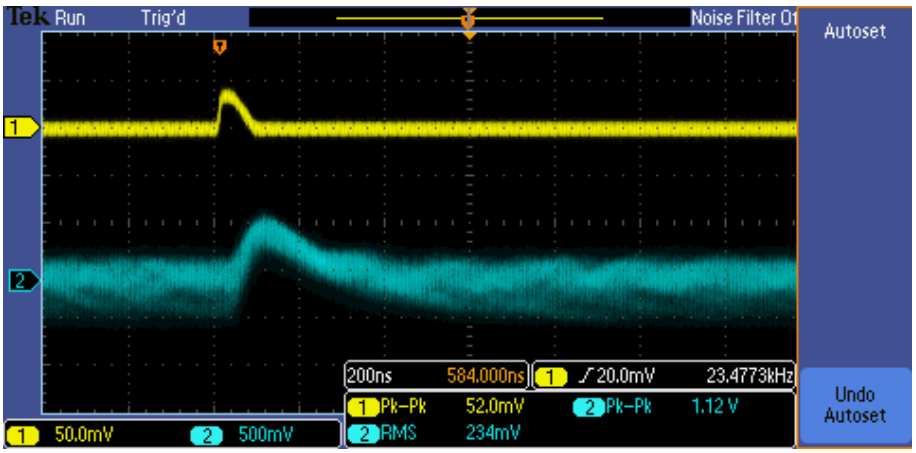
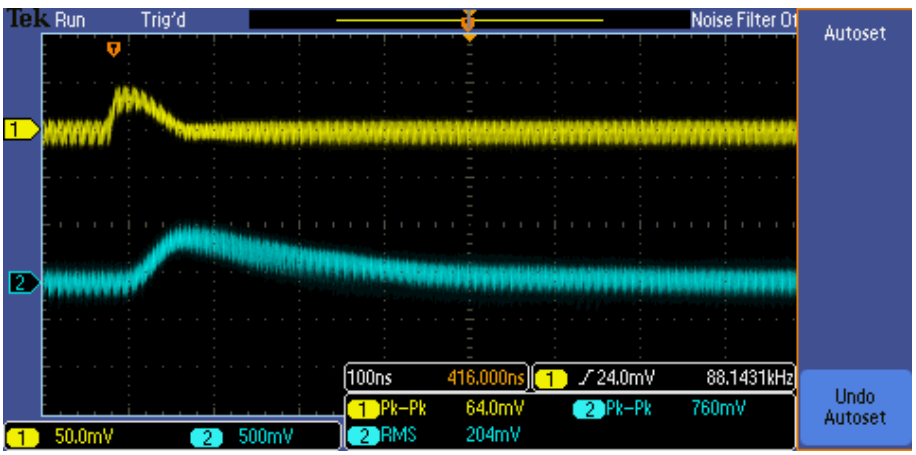


Figure 5.31. Implementation on breadboard of the circuit with transistor buffer



(a)



(b)

Figure 5.32. (a) and (b) are the oscilloscope screenshots of the circuit with transistor buffer with ±5.0V voltage supply

In the Figure 5.32 (a) and (b) belong to the measurement which has been done with ±5.0V supply voltages. It is obvious that there is instability both in input and output signals. In addition, the gain in the output signal is too few. When we consider all kinds of particles, their energy values are broad spectrum and it would be useful that if we can get at least 100 times bigger an output signal.

On the other hand, in the Figure 5.33 when ±3.5V supply voltage is applied, there is not any reflection on input signal and any oscillations on output signal,but the circuit's gain is approximately 20 times as input signal.

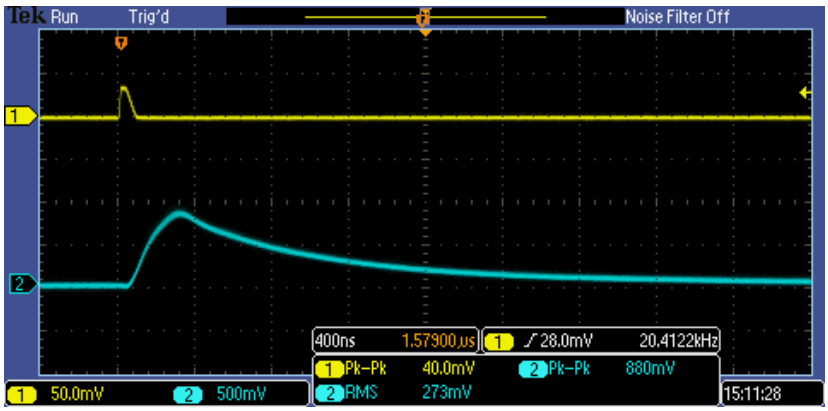


Figure 5.33. The oscilloscope screenshot of the circuit with transistor buffer with ±3.5V voltage supply

6. CONCLUSION

A Delay Wire Chamber (DWC) is a kind of gaseous ionization detector that works in the proportional regime at the detection region. When a particle passes through the chamber full of gas, ionization occurs and negatively charged particles drift to the positive anode wires; an avalanche process occurs. By this time, in the cathode wires an image current is similarly induced. This current reaches propagation delays and splits into two signals, each traveling through separate amplification stages to the output. This way, two signals with time differences are obtained at the output, allowing the extraction of the information about the position of the tracked particles.

In this theses, we have described our implementation of the electronics needed for a DWC. Despite the gas amplification the cathode wire currents are very small and short, necessitating delicate work. The large amplification and the high bandwidth needed makes the readout highly sensitive to noise from the environment, and it is very difficult to achieve stable operation due to feedback and reflections. Furthermore we have found out that the selected opamps do not perform according to the specifications at the rated supply voltage of ±5.0V. To overcome these issues, we have developed ad-hoc solutions, which included decreasing the supply voltage to ±3.0V - ±3.5V, grounding the circuit at multiple locations, using a shielding case, and implementing variable resistors at the reference legs of the op-amps that allow manual tuning of their behavior.

While these efforts allowed us to successfully build to working circuits to be used in the first Boğaziçi DWC, the need for manual tuning is still an issue. Under different environmental conditions, the amount of compensation provided by the variable resistors changes. Finding a working point that provides reasonably high amplification as well as stability of the output signals in many different environmental conditions has proven difficult. As a final solution, we tried to separate two op-amp stages from each other by the use of a simple JC548 transistor buffer in order to eliminate feedback, thus overcoming the stability problem. This attempt was partially successful and it

was concluded that with a high-bandwidth buffer, such as OPA693, stable operation will be possible.

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APPENDIX A: .NET AND .CIR SCRIPTS FOR LTSPICE-IV AND TINA-TI

The following .NET and .CIR scripts can be found in the supplementary CD.

(i) .NET Scripts for LTspice-IV
   (a) .NET Script of the Propagation Delay with 0.5 Ω Internal Resistance for LTspice-IV
   (b) .NET Script of the Propagation Delay with 120 Ω Internal Resistance for LTspice-IV

(ii) .CIR Scripts for Tina-TI
   (a) .CIR Script of the Subcircuit for Tina-TI
   (b) .CIR Script of the Whole Circuit for Tina-TI

APPENDIX B: THE OSCILLOSCOPE SCREENSHOTS OF THE PCB

The screenshots belong to legs between J1-40 AND J1-4 moving two at a time.

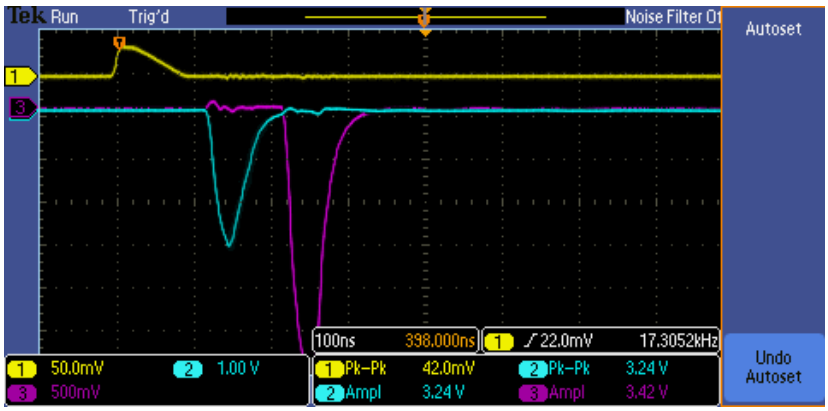

Figure B.1. Oscilloscope screenshot of the PCB on the J1-40. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

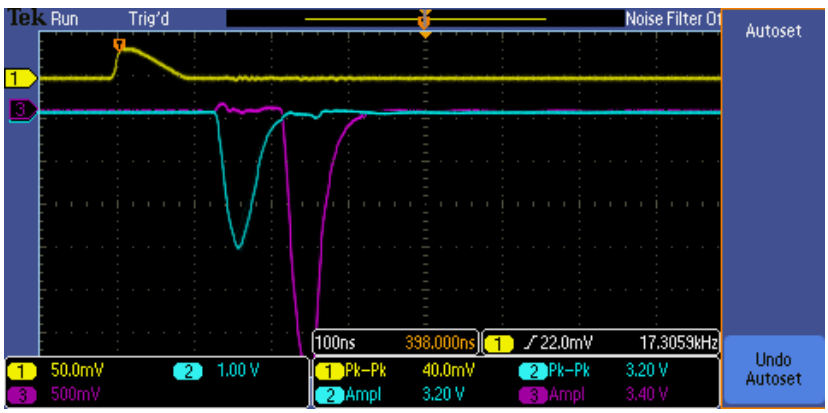

Figure B.2. Oscilloscope screenshot of the PCB on the J1-36. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

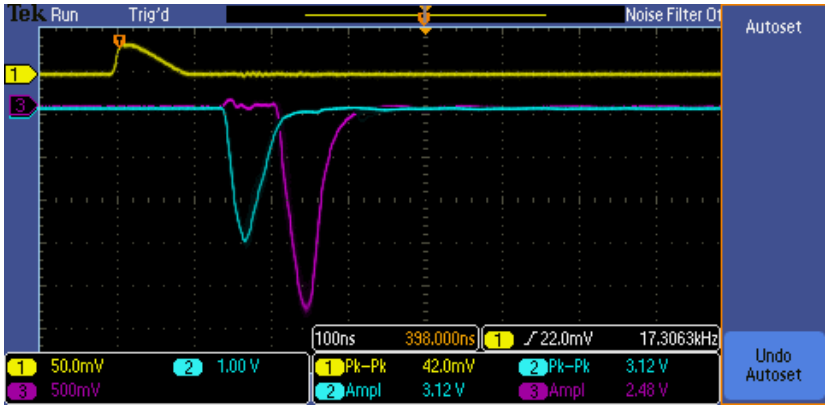

Figure B.3. Oscilloscope screenshot of the PCB on the J1-34. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

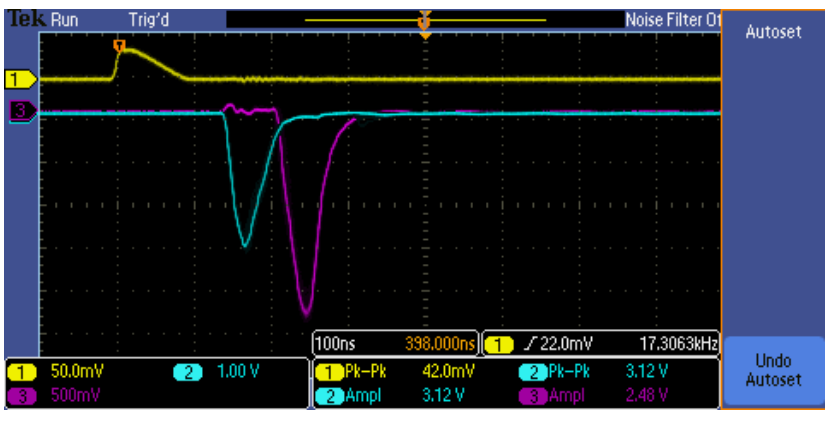

Figure B.4. Oscilloscope screenshot of the PCB on the J1-32. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

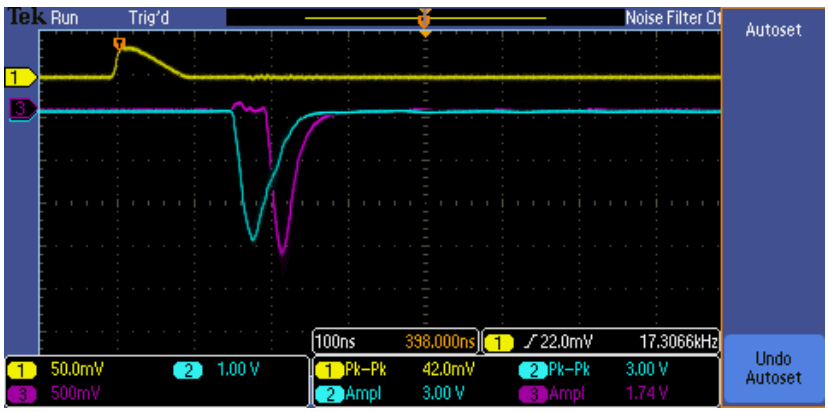

Figure B.5. Oscilloscope screenshot of the PCB on the J1-30. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

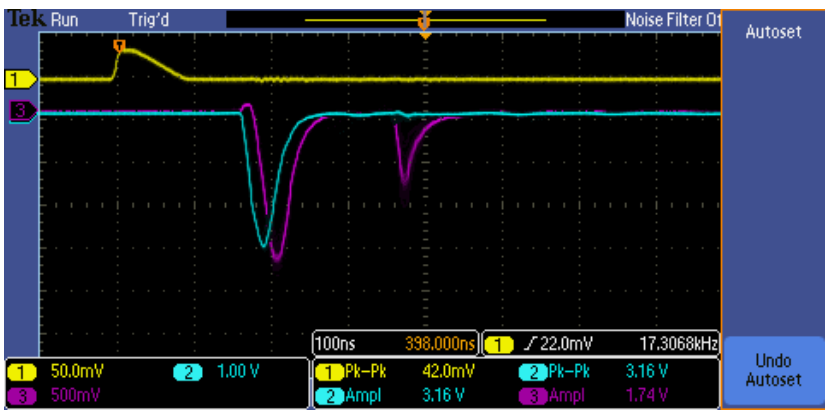

Figure B.6. Oscilloscope screenshot of the PCB on the J1-28. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

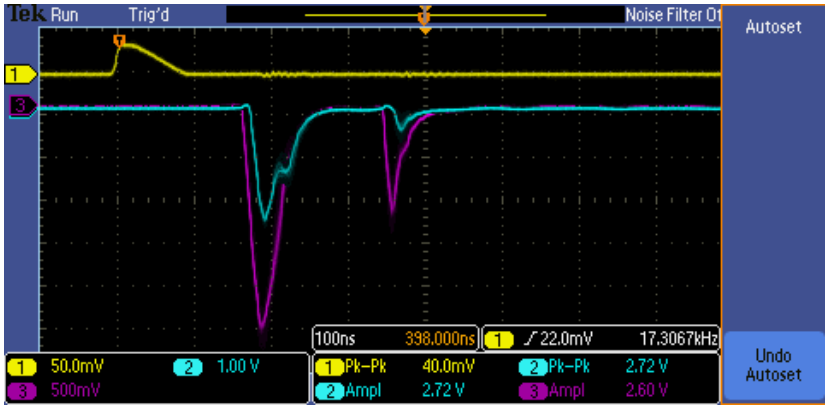

Figure B.7. Oscilloscope screenshot of the PCB on the J1-26. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

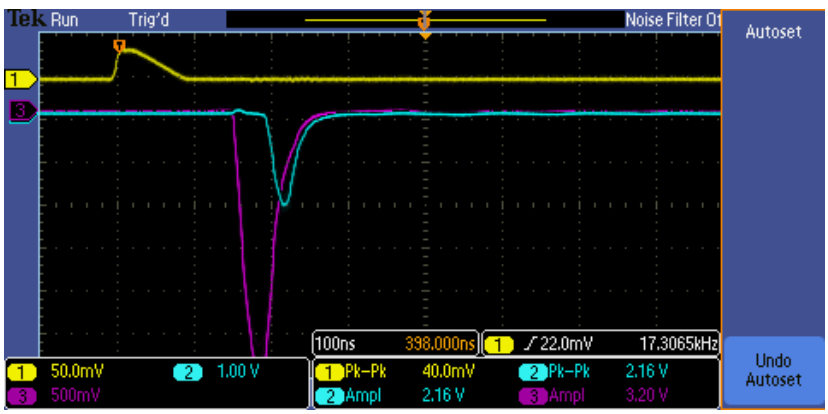

Figure B.8. Oscilloscope screenshot of the PCB on the J1-24. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

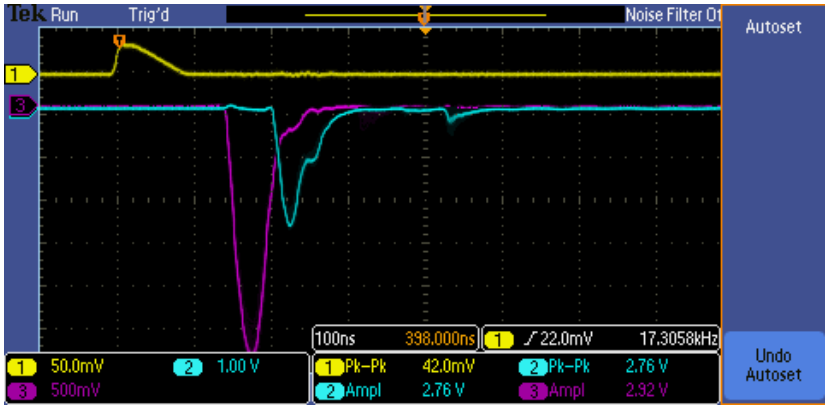

Figure B.9. Oscilloscope screenshot of the PCB on the J1-22. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

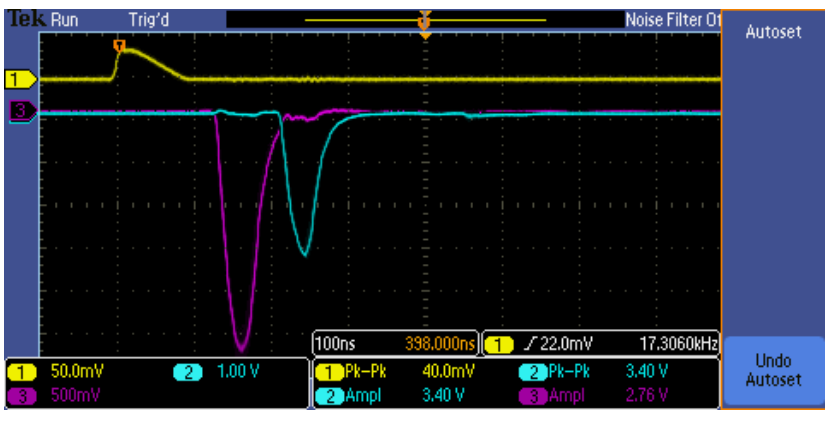

Figure B.10. Oscilloscope screenshot of the PCB on the J1-20. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

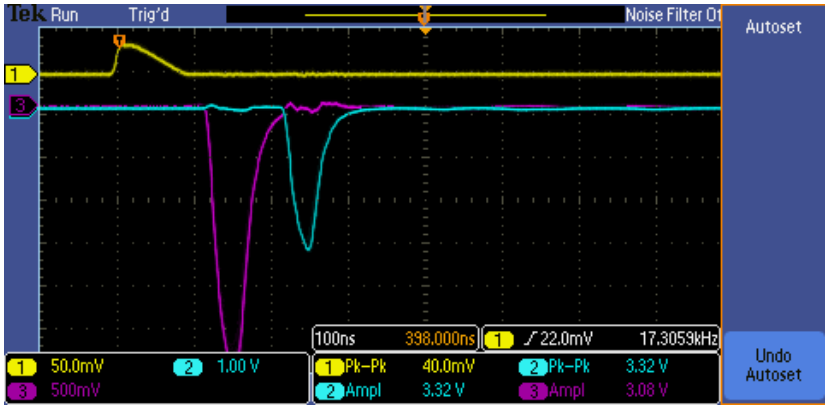

Figure B.11. Oscilloscope screenshot of the PCB on the J1-18. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

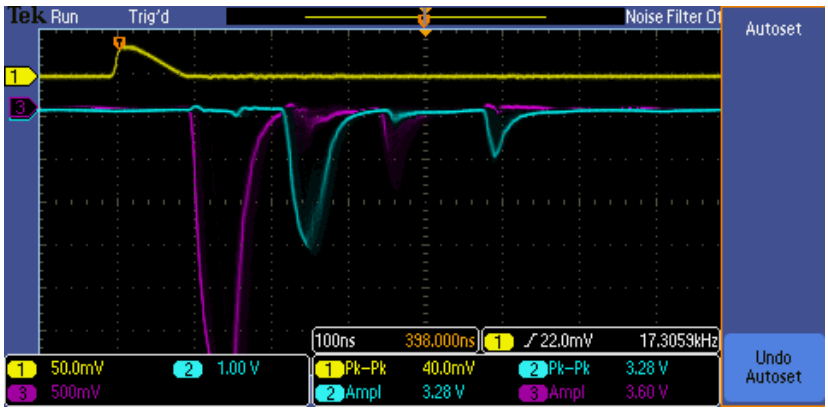

Figure B.12. Oscilloscope screenshot of the PCB on the J1-16. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

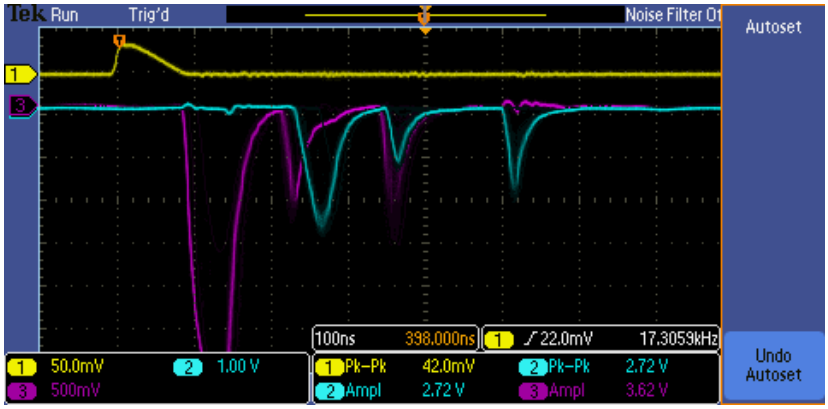

Figure B.13. Oscilloscope screenshot of the PCB on the J1-14. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

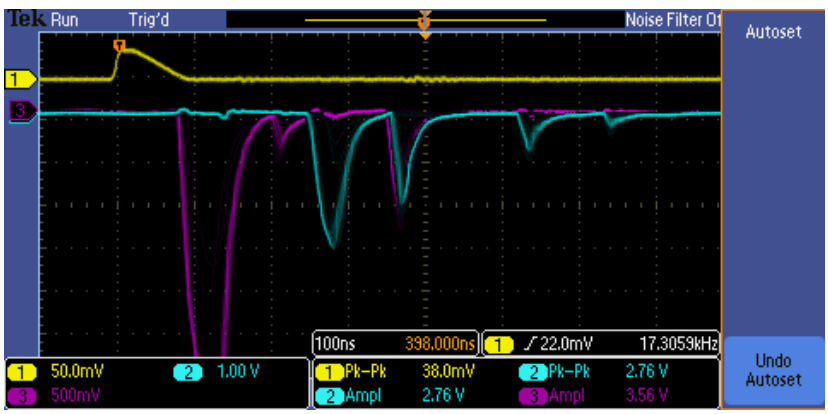

Figure B.14. Oscilloscope screenshot of the PCB on the J1-12. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

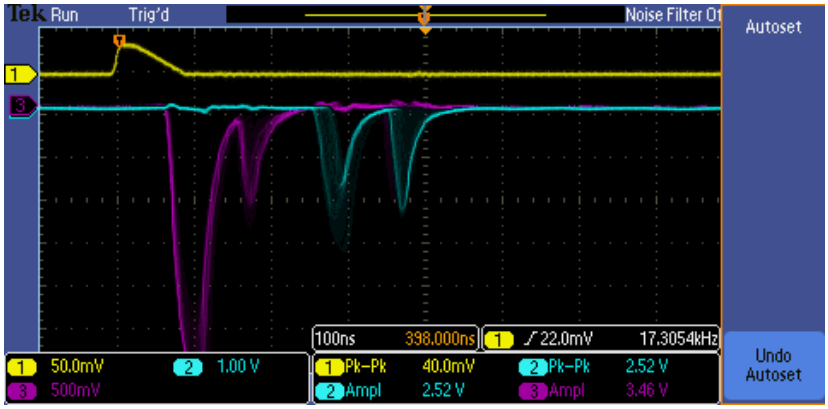

Figure B.15. Oscilloscope screenshot of the PCB on the J1-10. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

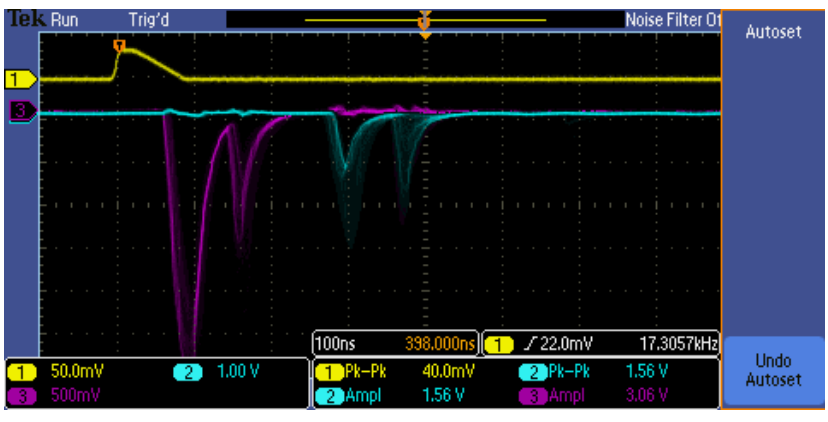

Figure B.16. Oscilloscope screenshot of the PCB on the J1-8. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

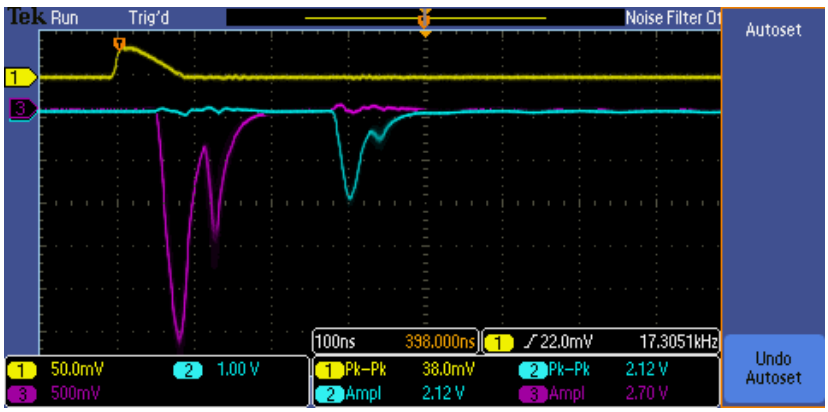

Figure B.17. Oscilloscope screenshot of the PCB on the J1-6. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.

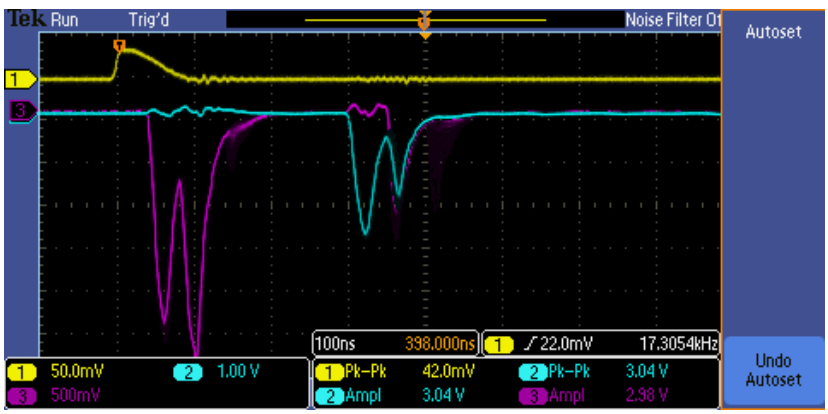

Figure B.18. Oscilloscope screenshot of the PCB on the J1-6. Yellow line represents input signal. Blue line represents output 14, and purple line represents output 14.