CONVERSION OF CURRENT MODE CONTINUOUS TIME SIGMA DELTA CONVERTERS FROM 1 BIT TO 3 BITS

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ABSTRACT

CONVERSION OF CURRENT MODE CONTINUOUS TIME SIGMA DELTA CONVERTERS FROM 1 BIT TO 3 BITS

Sigma delta analog digital converters which are widely used in electronics are gradually achieving faster speeds and lower power consumption. The most important factor that affects speed and power consumption is the type of the sigma delta analog digital converter. To achieve higher speed, using continuous time design instead of discrete time design is more reasonable. The other factor that affects the performance of the sigma delta analog to digital converter is the mode of the design which is current mode or voltage mode. Current mode design has a lot of advantages against voltage mode design but there are a few disadvantages of the current mode design when the resolution of the sigma delta analog digital converter increases.

First of all, in this thesis, there is a summary of a one bit 4^{th} order continuous time current mode sigma delta analog digital converter with 128 MHz sampling frequency and 32 MHz operating frequency which was designed before. Also, the test of the same structure is included. Moreover, upgrading the structure from one bit to three bit and the test of the new structure are explained. Hence, a three bit 4^{th} order continuous time current mode sigma delta analog digital converter with 128 MHz sampling frequency and 32 MHz operating frequency is presented.

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1 BİTLİK AKIM KİPLİ SÜREKLİ ZAMANLI SİGMA DELTA ÇEVİRİCİLERİN 3 BİTE ÇEVİRİLMESİ

Günümüzde elektronik uygulamalarda sıkça kullanılan sigma delta analog sayısal dönüştürücülerde giderek yüksek hızlara ve düşük güç harcamalarına ulaşılmaktadır. Hızı ve güç harcamasını etkileyen en önemli etken sigma delta analog sayısal dönüştürücünün çeşididir. Daha yüksek hızlara ulaşmak için ayrık zamanlı tasarım kullanmak yerine sürekli zamanlı tasarım kullanmak daha mantıklıdır. Sigma delta analog sayısal dönüştürücünün performansını etkileyen diğer bir etken de tasarımın akım modlu veya gerilim modlu olmasıdır. Tasarımın akım modlu olmasının gerilim modlu olmasına göre artıları çok fazladır ancak çözünürlük arttıkça akım modlu tasarımda gerilim modlu tasarıma göre birkaç eksi durum oluşmaktadır.

Bu tezde ise başta daha önceden sürekli zamanlı akım modlu tasarlanmış bir 32 MHz çalışma frekansı 128 MHz örnekleme frekansı olan dördüncü derece bir bant geçiren bir bitlik sigma delta analog sayısal dönüştürücü hakkında kısa bir özet ve bu yapının testi bulunmaktadır. Ardından bu yapının bir bitten üç bite çıkartılması anlatılmıştır ve yeni yapının testi yapılmıştır. Sonuç olarak 128 MHz örnekleme frekansı, 32 MHz çalışma frekansı olan üç bitlik bir dördüncü derece bant geçiren akım modlu, sürekli zamanlı sigma delta analog sayısal dönüştürücü tasarımı sunulmuştur.

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LIST OF SYMBOLS/ABBREVATIONS

g_m	Transistor conductance
w	Transistor width
ADC	Analog to Digital Converter
BNC	Bayonet Neill-Concelman
CRFF	Cascade of Resonators Feedforward Form
DAC	Digital Analog Converter
PCB	Printed Circuit Board
SNR	Signal to Noise Ratio

1. INTRODUCTION

Sigma delta analog digital converters consist of three blocks which are filter, quantizer and digital analog converter blocks as depicted in Figure 1.1.

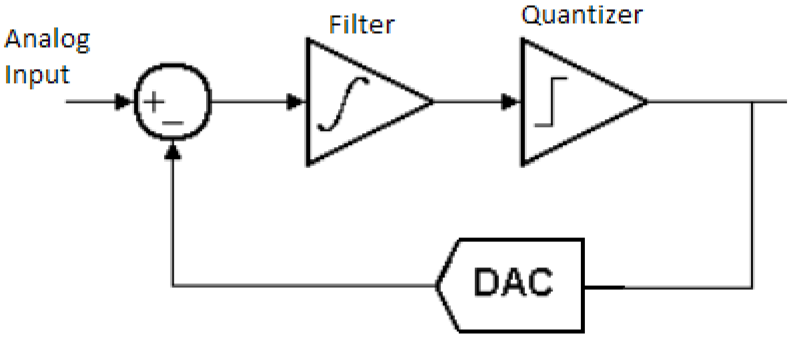


Figure 1.1. Sigma delta analog digital converter modulator block

The first block is the filter block which can be different types because of order and the type of the filter. The order of the filter increases the filtering performance and type of the filter determines which frequencies need to be filtered. The main duty of this block is to reduce noise caused by the signals at unwanted frequencies and the feedback signal. The shape of the output of this block is the filtered shape of the input of the block. Additionally, noise reduction varies from filter to filter. Usually low pass and bandpass filters are used in sigma delta converters. The order of the filter increases signal to noise reduction ratio. Switched capacitor filters are mostly used in most designs but they require a clock to turn the switches on and off. This type of design is called discrete time design which the input signals are sampled with switched capacitor logic. However, filtering can be done continuously by using continuous time filters. Continuous time filters consist of g_m-C filters instead of switched capacitor filters. By using continuous design higher speeds can be achieved because there is no limiting of clock that controls charging and discharging of the capacitors; thus there is no settling time the capacitors to be charged and discharged. Another concern is the mode of the filter. Voltage mode sigma delta converters are used widely but current modes are gaining popularity day by day. If the design is voltage mode, the input and the output of this block is a small voltage on a DC voltage.

Thus, this block should be designed carefully, so that the voltage of the nodes in this block won’t be higher than supply voltage. Moreover, the voltage difference at the nodes shouldn’t be high because high voltage causes delays because of the capacitances of the nodes. However in current mode designs there is no delay because of the node capacitances. Therefore, current mode designs are faster than voltage modes. Nevertheless, in current mode designs instead of voltage limitation, there is maximum current limitation which can be solved by increasing the w of the transistors. Hence, the output current of the filter block should not be higher than the input limitation of the comparator block. Another advantage of current mode designs is the addition of the signals in current mode designs is easier than the addition of the signals in voltage mode designs because addition of currents is a lot easier than voltages.. Also, the filter block is designed differentially because the comparison of two signals is truer then comparing a signal to a constant value in the quantization block.

The second block is the quantization block which first compares the previous signals to each other. If there are two differential inputs of the quantizer, a single comparator block would be enough to find whether the signal is positive or negative; therefore, the output will be a single bit. Additionally, the quantization block can have more resolution than 1 bit. In that case, signals are not only compared to each other but also compared to each other plus some additional constant signals. Hence, the difference between those signals is compared with some constant values, so the resolution increases. Moreover the resolution increases, the output of the DAC looks similar with the input of the whole design. In addition, the outputs of the quantization block are voltages and also, they represent the output bits. As the resolution increases, the output bits increases, too. Furthermore, the input of the quantization block can be voltage or current like in filter block.

The third block is the digital analog converter block which is the feedback of the conversion. The output bits of the comparator are turned into an analog signal with this block. If the output signal of the digital analog converter is voltage it is hard to make subtraction with the main input of the sigma delta converter, but if the design is current mode instead of voltage mode, the output of the digital analog converter will be current and the subtraction will be very easy.

2. SUMMARY OF THE FIRST ANALOG DIGITAL CONVERTER

First design is a 4th order bandpass one bit current mode sigma delta analog digital converter. Three main structures of the first design are summarized in this section. Further details of this section can be found from the publications of the original designer when it is prepared.

2.1 Filter Block

[1] designed a current mode 4th order bandpass filter for sigma delta analog digital conversion which can be seen in Figure 2.1. This filter is a 4th order Cascade of Resonators Feedforward Form (CRFF) filter. Furthermore, the rectangles represent integrators and the big trapezoids represent the coefficients of the filter. The small trapezoids are for limiting the input of the integrators.

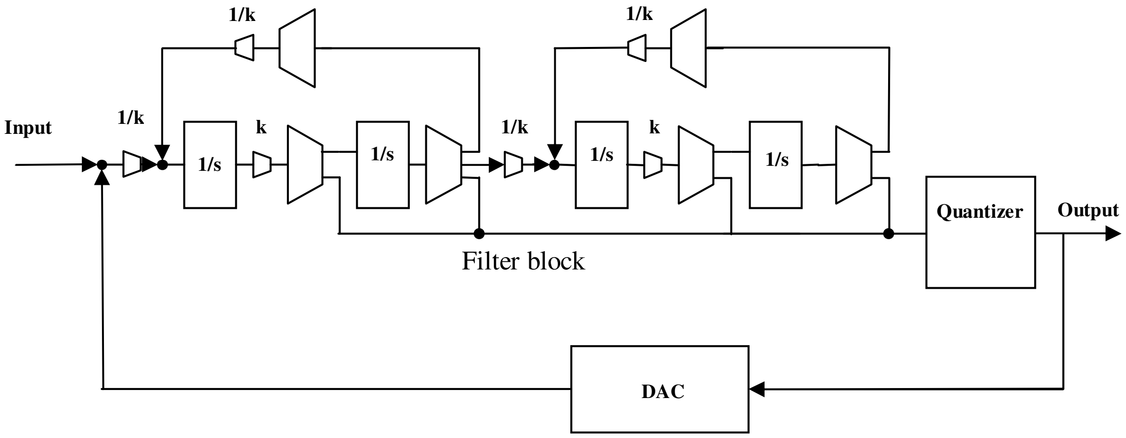


Figure 2.1. 4th order bandpass current mode CRFF filter block used in sigma delta ADC

For precision, each designed current mode integrator is supplied with a different source which is nearly the same voltage as the others.

2.2 Quantizer Block

Quantizer block in Figure 2.2 consists of a single comparator because the analog digital converter is one bit. The comparator compares two input currents rather than comparing one of the inputs with a constant value. Hence, all the signals in the analog digital converter are symmetrical signals because the comparator has to compare two currents to each other. Furthermore, comparator has a digital output value which changes with the clock and two output signals for DAC which changes with the clock. One of those two output signals for DAC is a pulse when the digital output value is logic ‘1’ and the other is a pulse when the digital output value is logic ‘0’.

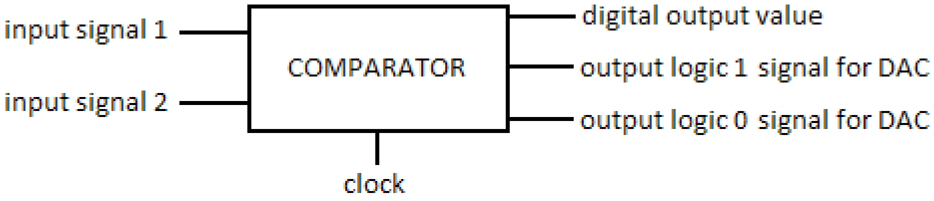


Figure 2.2. Quantizer block

2.3 Digital Analog Converter Block

Digital analog converter block in Figure 2.3 consists of a single circuit. This circuit generates 20 µA at the output signal 1 and -20 µA at the output signal 2 when the input is logic ‘1’ and generates -20 µA at the output signal 1 and 20 µA at the output signal 2 when the input is logic ‘0’. This circuit is also a return zero digital analog converter which generates 0 µA at the output signals at the end of the clock. Thus, output signals return to the value ‘0’ at the end of the clocks. To synchronize the clocks and returns there are some delay structures in DAC block.

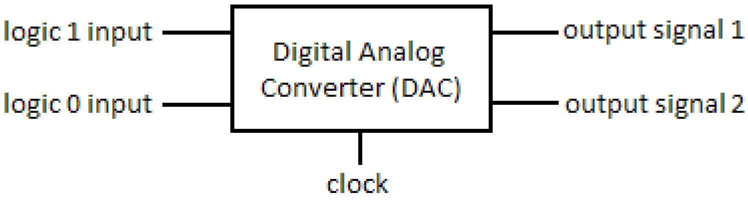


Figure 2.3. Digital Analog Converter Block

2.4 Simulation Results

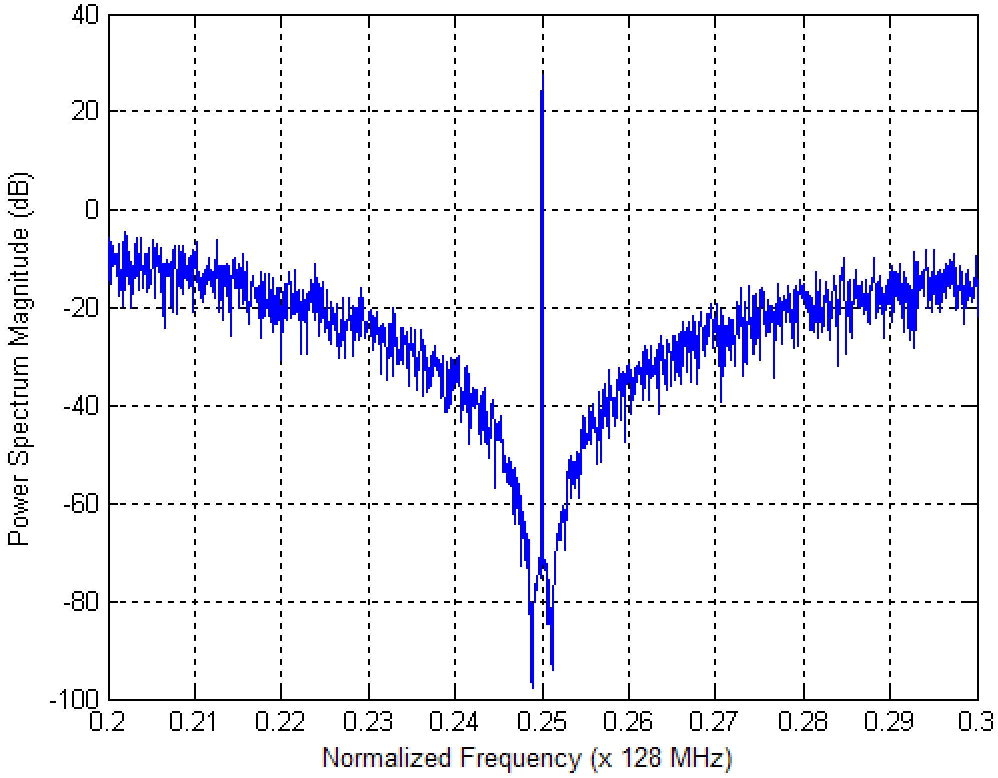


Figure 2.4. The ideal SNR output of a 4th order bandpass sigma delta converter

The ideal SNR output of a 4th order bandpass sigma delta converter using the coefficients can be seen in Figure 2.4 [2]. SNR is calculated with the ideal outputs in MATLAB. The HSPICE outputs of the designed converter are simulated in MATLAB and the simulation results of the designed converter can be seen in Figure 2.5. SNR is calculated as 68 dB in this design. A prototype chip of the first design was produced in an earlier work and the next section is about the preparation of the test PCB of the first design and the test of the first design.

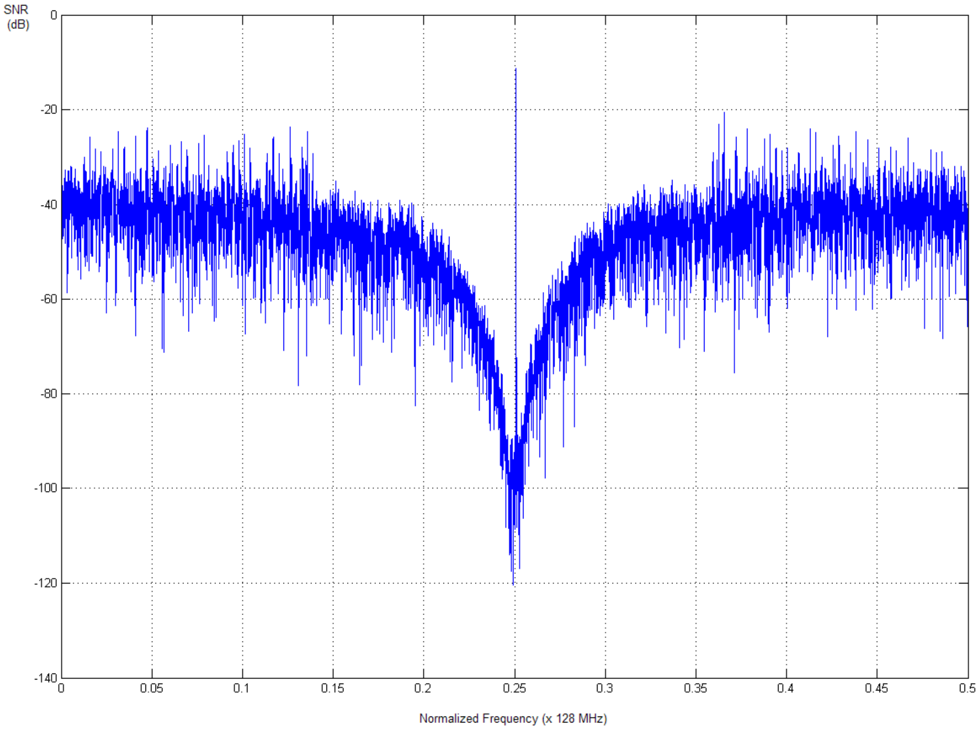


Figure 2.5. The MATLAB simulation result of the designed a 4th order bandpass sigma delta converter

3. TEST OF THE FIRST ANALOG DIGITAL CONVERTER

3.1 Preparation of the PCB

First of all, the pins and the pin specifications of the chip can be seen in Figure 3.1. and Table 3.1. Moreover, a socket is used for plugging chip into the PCB which can be seen in Figure 3.2. The inputs for the PCB can be seen in Table 3.2

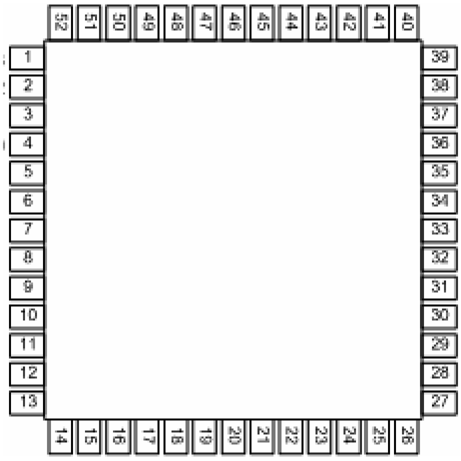


Figure 3.1. Pins of the Chip

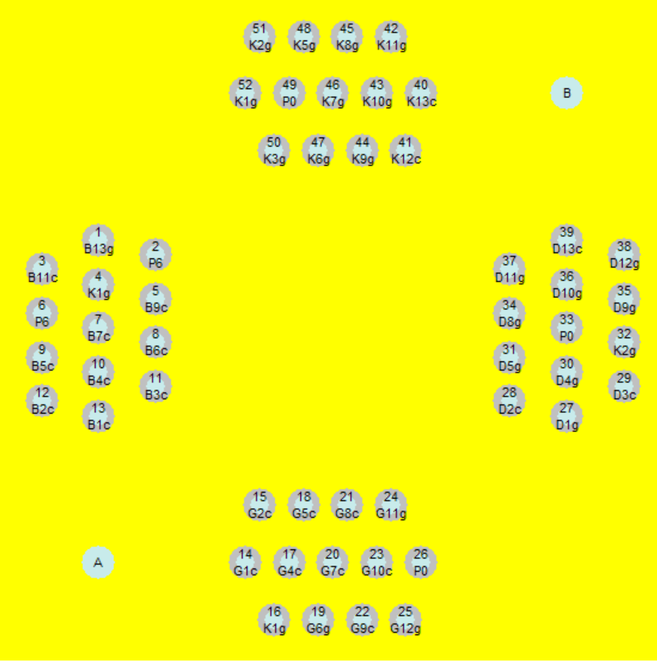


Figure 3.2. Socket for plugging chip into PCB

Table 3.1. Pins and pin specifications of the first chip

Pin	**Pin Specifications**
1	128 MHz clock input
2	Digital ground voltage
3	128 MHz clock output
4	Digital supply voltage
5	128 MHz digital data output
6	Digital ground voltage
7	Byte ready signal output
8	16 MHz Q0 digital output
9	16 MHz Q1 digital output
10	16 MHz Q2 digital output
11	16 MHz Q3 digital output
12	16 MHz Q4 digital output
13	16 MHz Q5 digital output
14	16 MHz Q6 digital output
15	16 MHz Q7 digital output
16	Digital supply voltage
17	32 MHz clock output
18	32 MHz digital data output
19	Clock input for other test circuits
20	Integrator test circuit data output
21	Quantizer test circuit digital output
22	DAC test circuit positive current output
23	DAC test circuit negative current output
24	Positive input current for test circuits
25	Negative input current for test circuits
26	Analog ground voltage
27	Test circuits NMOS bias control voltage
28	Filter positive current output
29	Filter negative current output
30	Filter positive voltage input
31	Filter negative voltage input
32	Analog supply voltage
33	Analog ground voltage
34	Positive input for slow ADC
35	Negative input for slow ADC
36	Filter NMOS cascode bias control voltage
37	Slow ADC NMOS cascode bias control voltage
38	DAC bias voltage input
39	DAC bias voltage output
40	NMOS cascode bias voltage output
41	PMOS cascode bias voltage output
42	NMOS cascode bias voltage input
43	PMOS cascode bias voltage input
44	4th integrator supply voltage
45	3rd integrator supply voltage
46	2nd integrator supply voltage
47	1st integrator supply voltage
48	Positive input for fast ADC
49	Analog ground
50	Negative input for fast ADC
51	Analog supply voltage
52	Digital supply voltage

Table 3.2. PCB inputs of the first design

Pin	**Pin Specifications**
P0	Analog Ground
P1	Voltage source input
P2	Fast mode voltage signal input (32 MHz)
P3	Filter test voltage signal input (8 MHz)
P4	Slow mode voltage signal input (8 MHz)
P5	Test circuits voltage signal input
P6	Digital Ground
P7	Fast mode 128 MHz data output
P8	Fast mode 128 MHz clock output
P9	Byte-ready output
P10	Q0, 16 MHz data output
P11	Q1, 16 MHz data output
P12	Q2, 16 MHz data output
P13	Q3, 16 MHz data output
P14	Q4, 16 MHz data output
P15	Q5, 16 MHz data output
P16	Q6, 16 MHz data output
P17	Q7, 16 MHz data output
P18	Slow mode 32 MHz data output
P19	Slow mode 32 MHz clock output
P20	Test circuits clock input
P21	Integrator data output
P22	Quantizer data output

3.1.1 Biasing and Supplying of the Chip

There are plenty of supply and bias voltages which need that much voltage sources. Instead of using many voltage sources, a single voltage source is used with voltage regulators and potentiometers to produce different bias and supply voltages of the chip. Furthermore, those bias and supply voltages will be precise when precise potentiometers are used.

LM317 voltage regulator is used in when generating voltage. The voltage difference between ADJ pin and V_{OUT} pin in LM317 is always 1.25 V. A resistor between 100 Ω and 200 Ω is recommended to be placed between ADJ pin and V_{OUT} pin. To generate voltages larger than 1.25 V, a single resistor is used between those two pins. Therefore, the current flowing from V_{OUT} to ADJ is constant and the same as the current flowing from ADJ to ground. If a precise potentiometer is placed between ADJ pin and the ground the voltage of the V_{OUT} can be precisely chosen. There weren't any precise potentiometers with resistance value 1-500 Ω during the design of the PCB, so a 1 KΩ resistor is placed parallel to the potentiometer to lower the total resistance to 1-500 Ω.

While generating voltages less than 1.25 V a precise potentiometer can be placed between V_{OUT} pin and ADJ pin while ADJ pin is connected to the ground. The voltage between V_{OUT} and ADJ is constant but the third pin of the potentiometer is between 1.25 V and 0 V. This out pin of the potentiometer is affected by the current flowing through, but those pins are always connected to the gates of the MOS transistors, thus no current will be flowing through them.

Both analog and digital supply voltages of the chip are 2.5 V. But those voltages are separated from each other; hence, analog circuits and digital circuits are not affected by each other. The supply voltages of the integrators which are also 2.5 V are separated from other voltages too because filter coefficients can be tuned precisely with changing the supply voltages of the integrators. However, all integrators can be supplied with same voltage with switches when needed. NMOS bias voltage is nearly 1.78 V and PMOS bias voltage is nearly 0.51 V. The bias voltage used in DAC current sources is 1.18 V. Switches can be used to choose bias voltages between voltages generated in PCB and voltages generated in the chip. Voltage generation circuits in PCB can be seen through Figure 3.3 to Figure 3.12.

Some capacitors with value 15.2 μF are placed parallel to the outputs to lower the ripple effect of the generated voltages caused by voltage regulators. There are also some more surface mount capacitors with value 100 nF connected between same places but at closer distance to the pins of the chip to lower these effects more. There is also a bigger capacitor between the input voltage P1 and the analog ground.

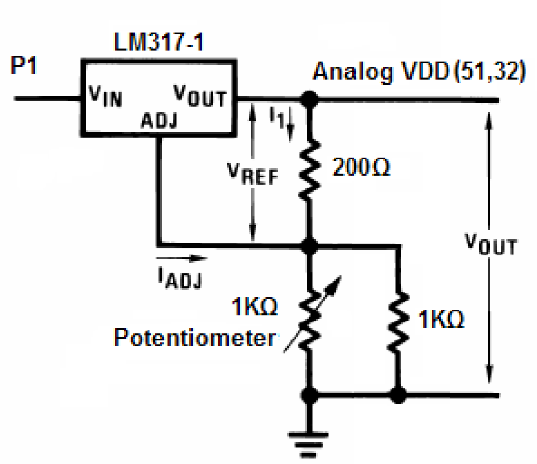


Figure 3.3. Generation of the analog supply voltage

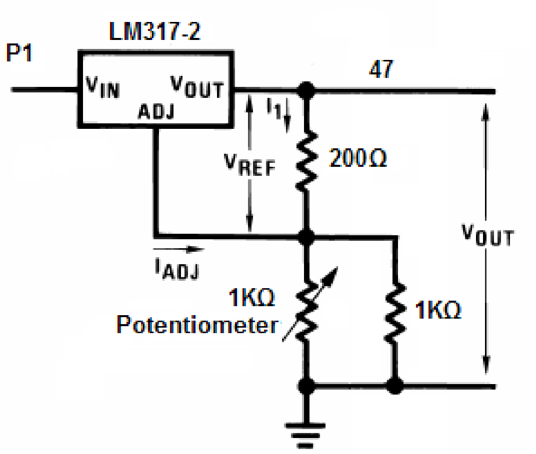


Figure 3.4. Generation of the supply voltage of the 1st integrator

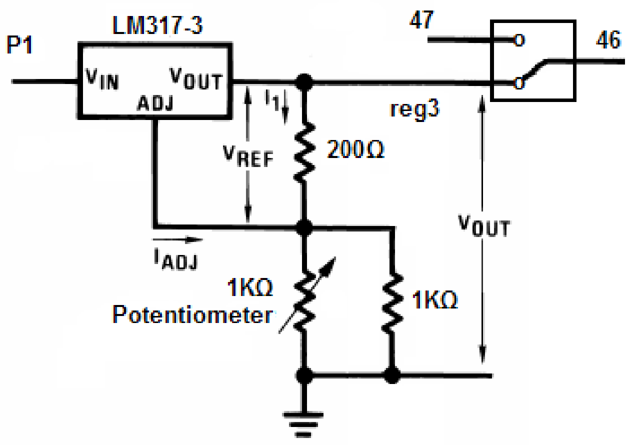


Figure 3.5. Generation of the supply voltage of the 2nd integrator

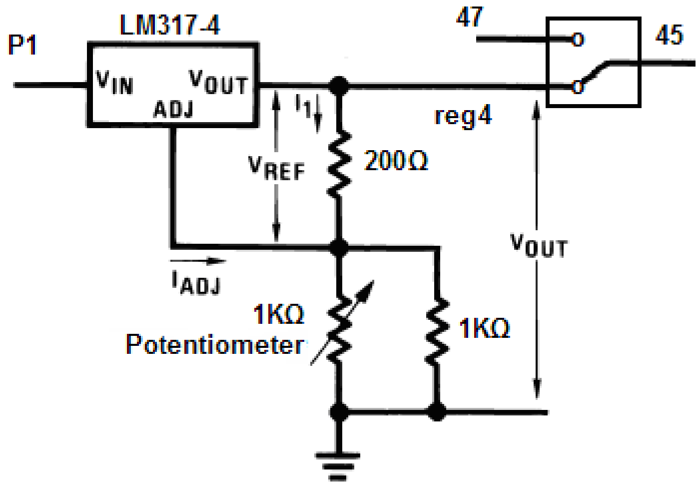


Figure 3.6. Generation of the supply voltage of the 3rd integrator

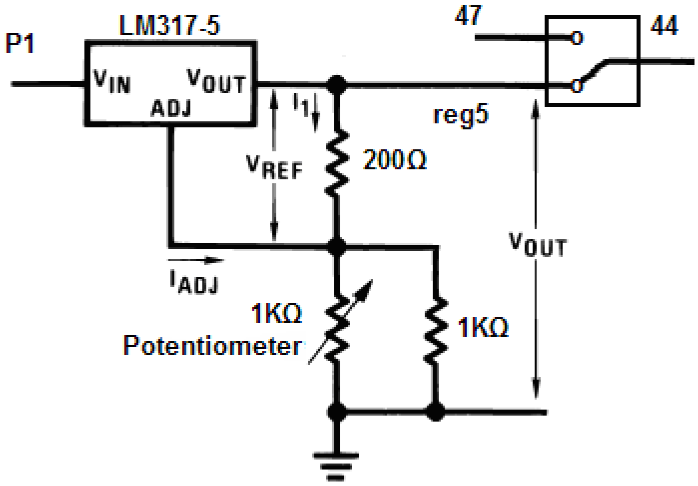


Figure 3.7. Generation of the supply voltage of the 4th integrator

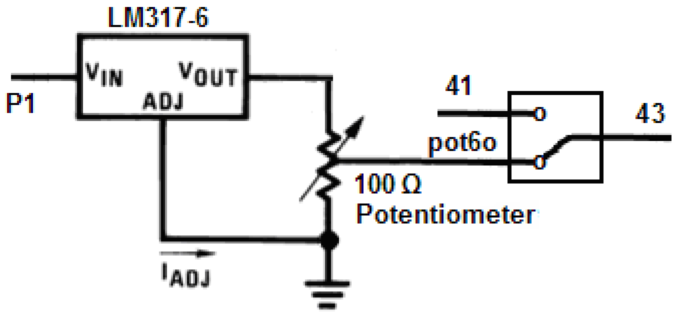


Figure 3.8. Generation of the bias voltage of the PMOS transistors

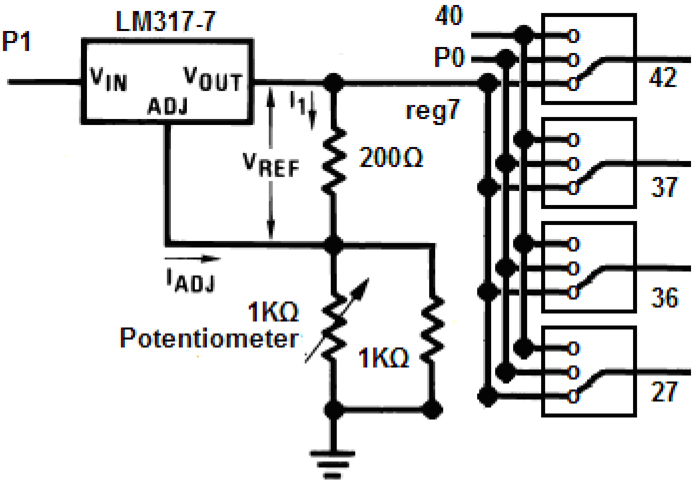


Figure 3.9. Generation of the bias voltage of the NMOS transistors for slow and fast modes and generation of the NMOS cascode bias control voltage for filter and test circuits. Those voltages are chosen with switches.

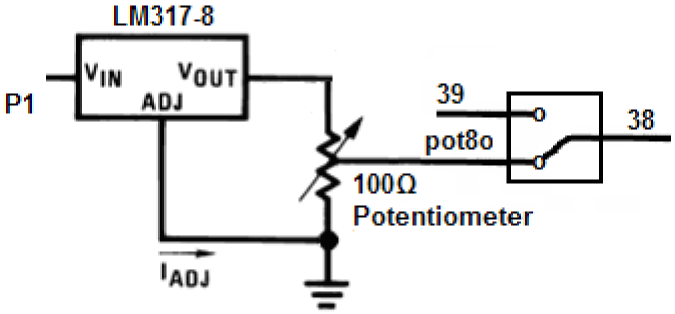


Figure 3.10. Generation of the bias voltage for DAC

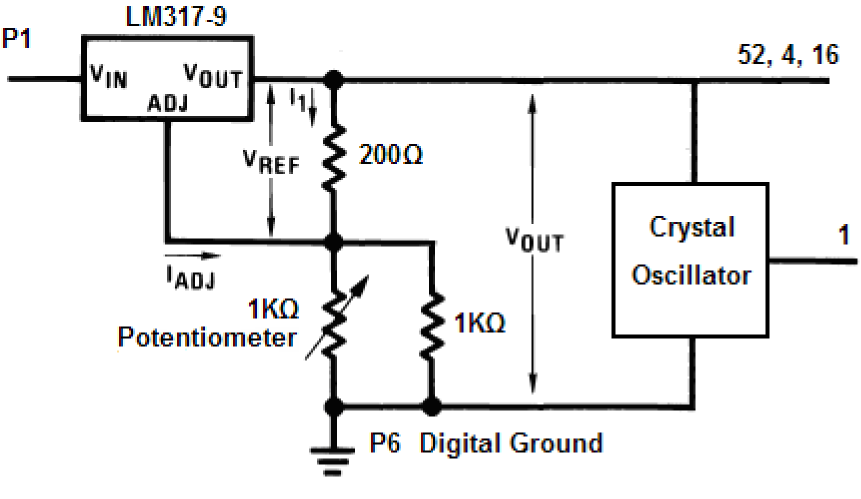


Figure 3.11. Generation of the digital supply voltage and the clock signal

While testing filter alone, the output voltage and current should be adjusted with potentiometers to have optimum results which can be seen in Figure 3.12.

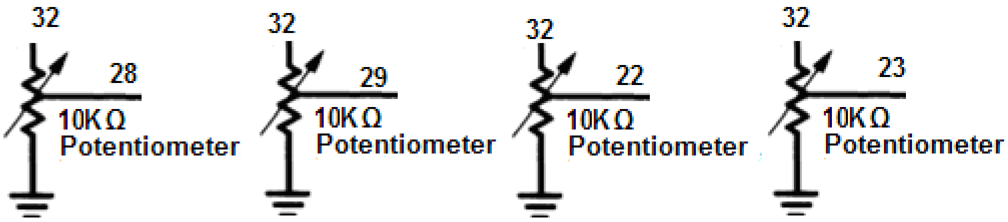


Figure 3.12. Filter test output voltage and current adjustment

3.1.2 Input Blocks

Signal inputs of the chip are symmetrical, but the signal processor that will be used in the tests has a single output. Using two signal processors instead of one may cause delays between two signals and a phase noise occurs. Thus, a transformer is used to convert a single signal into two symmetrical signals with the same amplitude. Moreover, small capacitances are connected between the output of the transformers and the inputs of the chip because the DC levels between those nodes are different. There are 8 inputs of the chip, which are two symmetrical for slow mode, two symmetrical for fast mode, two symmetrical for filter and two symmetrical for other test circuits. Figure 3.13 shows detailed information about these blocks.

3.1.3 Output Blocks and the Final Scheme of the PCB

The outputs of the slow mode and fast mode converters are connected to a BNC connector output to measure the results precisely. Other pins are connected to logic connectors, so that the results can be measured when needed. Final scheme of the PCB can be seen in Figure 3.14 and the photos of the PCB can be seen in Figure 3.15 and 3.16

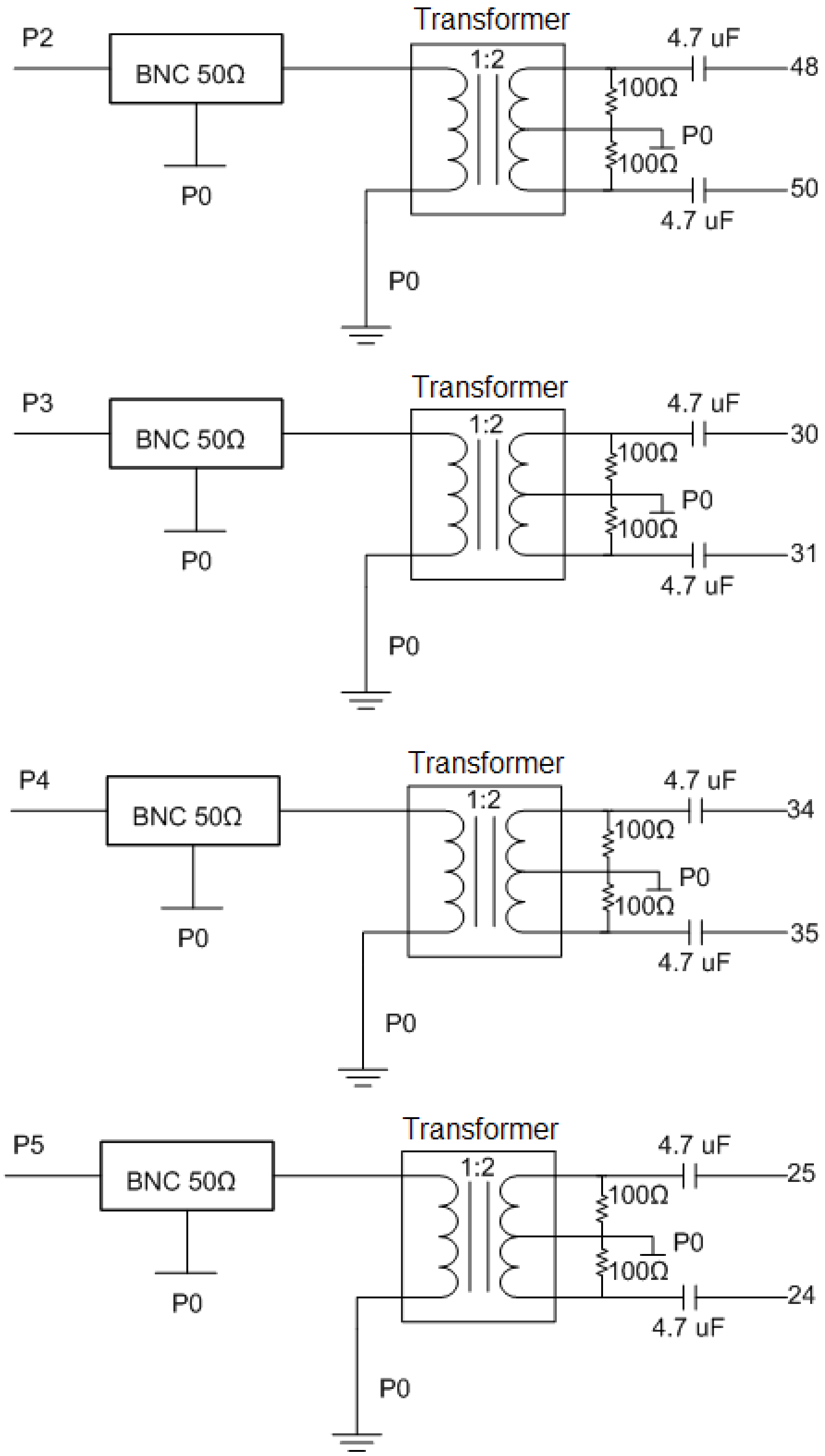


Figure 3.13. Conversion of the single inputs into symmetrical inputs.

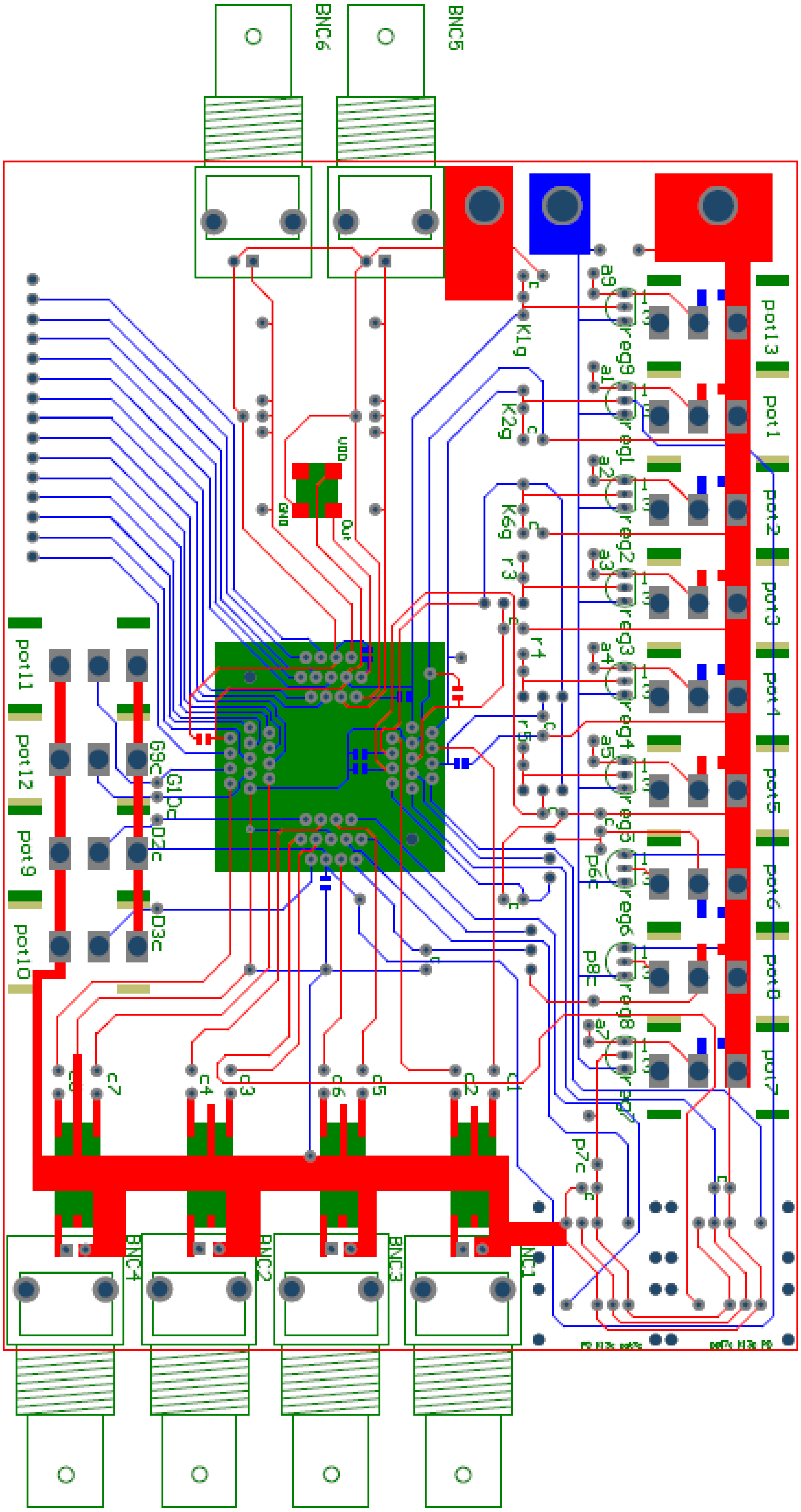


Figure 3.14. Scheme of the PCB.

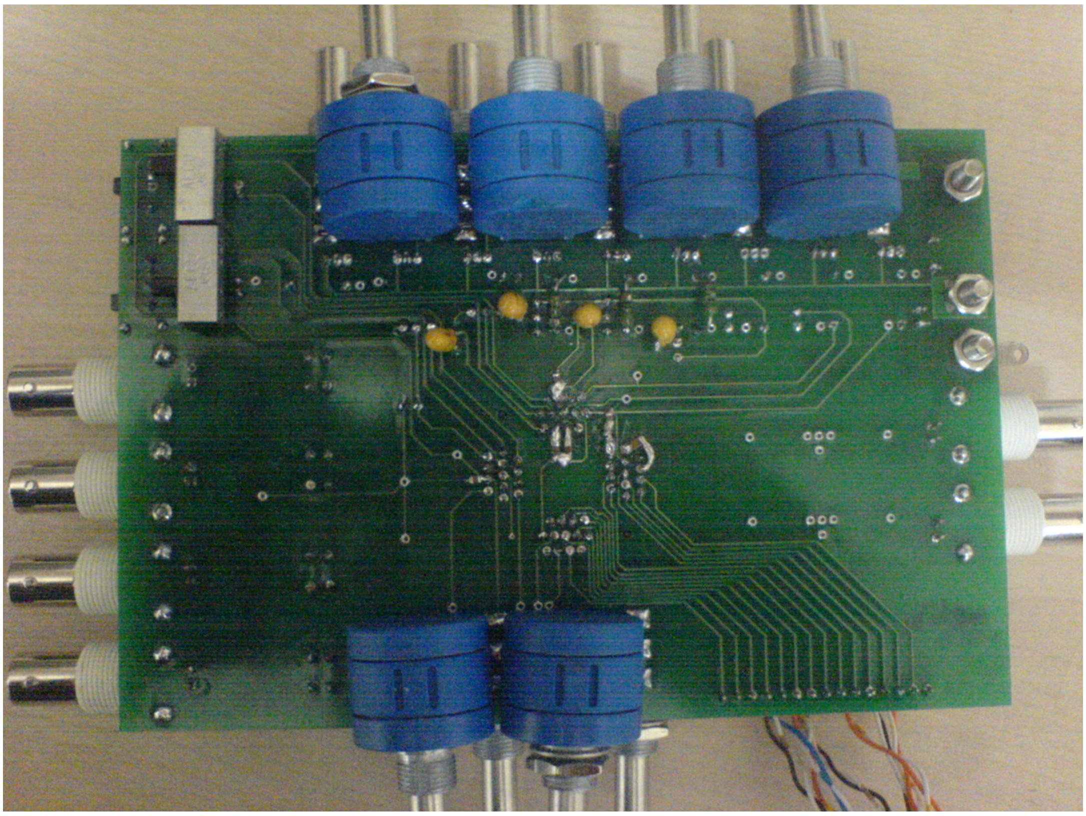


Figure 3.15. Photo of the PCB from above.

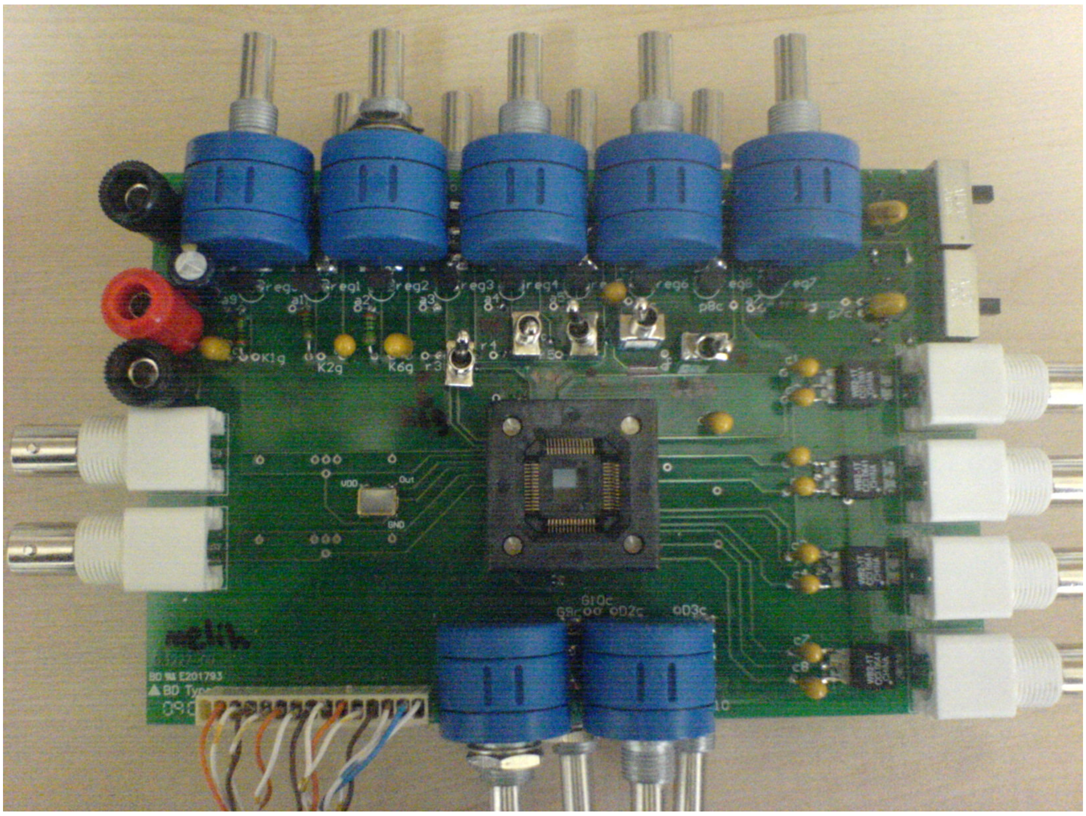
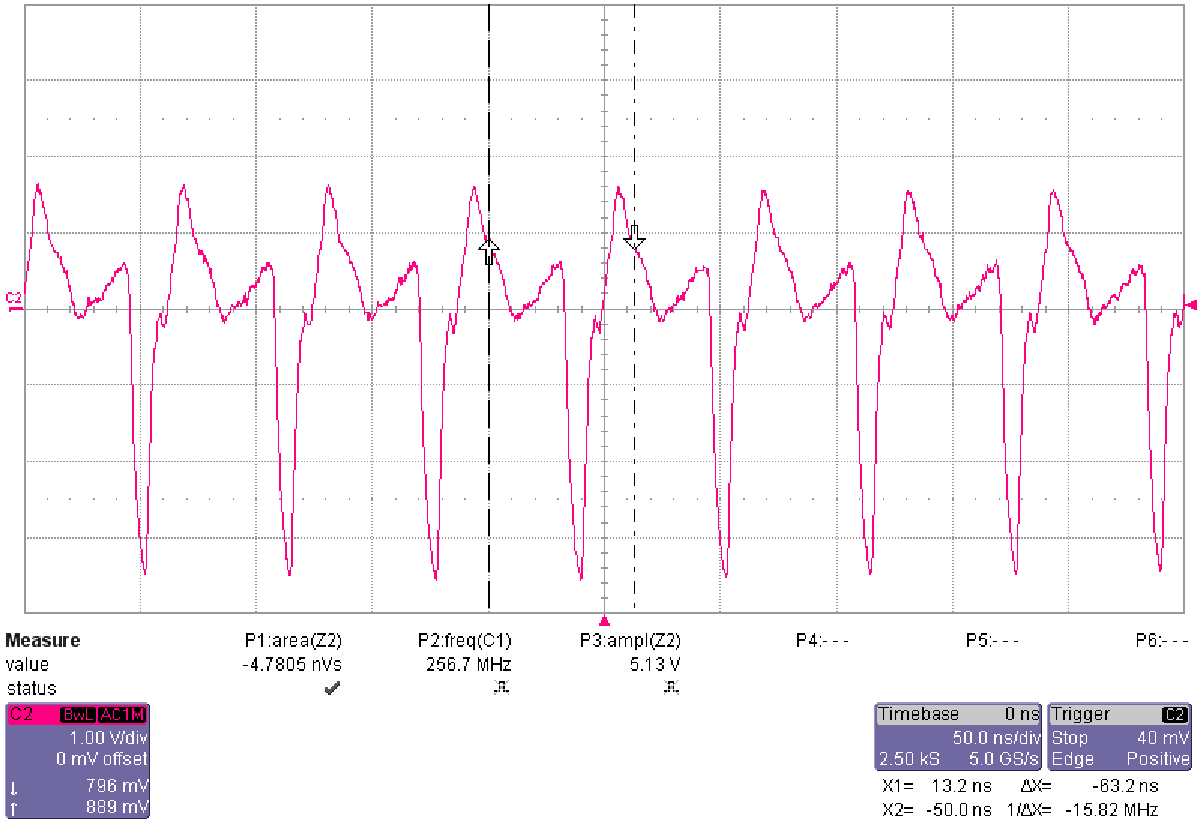


Figure 3.16. Photo of the PCB from below

3.2 Test of the PCB

3.2.1 Test of the Fast Mode

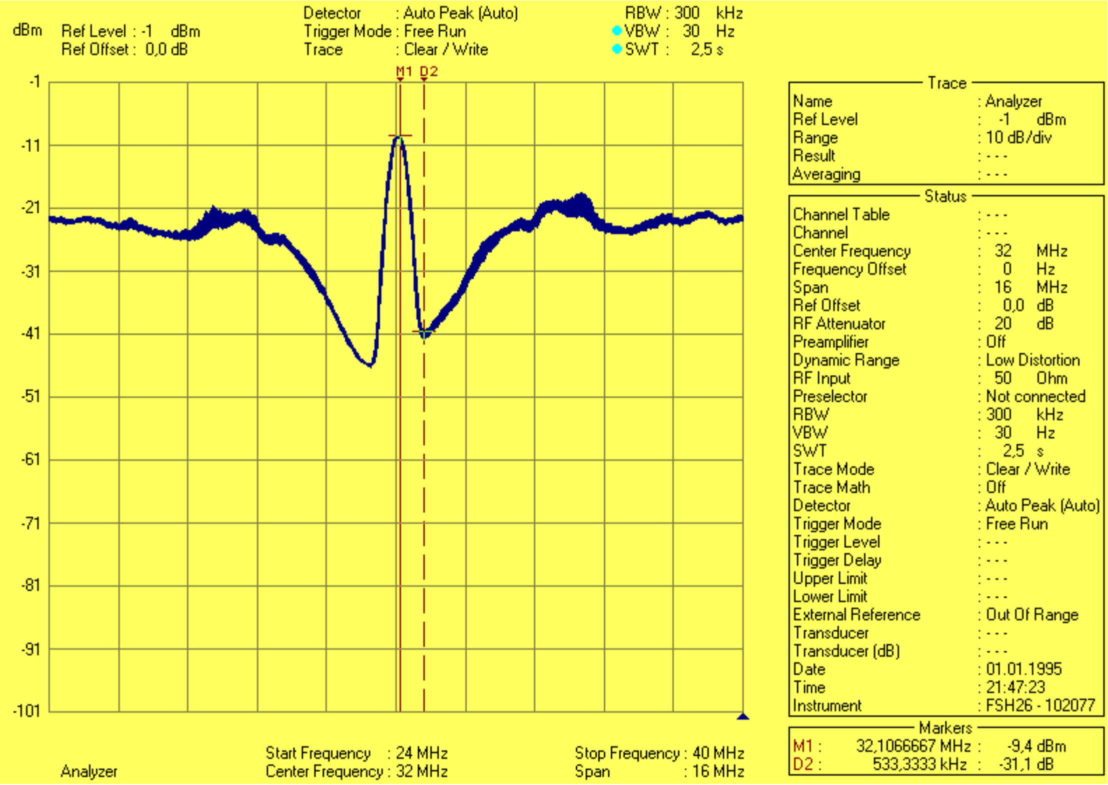
In this section, fast mode of the chip which has 32 MHz operating, 128 MHz sampling frequency is tested. Bias voltages and supply voltages are adjusted to the optimum values. When the input is a 100 mV peak to peak sine signal, the output of the chip measured in an oscilloscope can be seen in Figure 3.17.



```
Measure   P1:area(Z2)   P2:freq(C1)   P3:ampl(Z2)   P4:- - -   P5:- - -   P6:- - -
value     -4.7805 nVs   256.7 MHz     5.13 V
status    ✓

C2 BwL AC1M
   1.00 V/div
   0 mV offset
↓  796 mV
↑  889 mV

Timebase      0 ns   Trigger      C2
     50.0 ns/div     Stop      40 mV
2.50 kS   5.0 GS/s   Edge   Positive
X1=   13.2 ns    ΔX=      -63.2 ns
X2=  -50.0 ns  1/ΔX=   -15.82 MHz
```

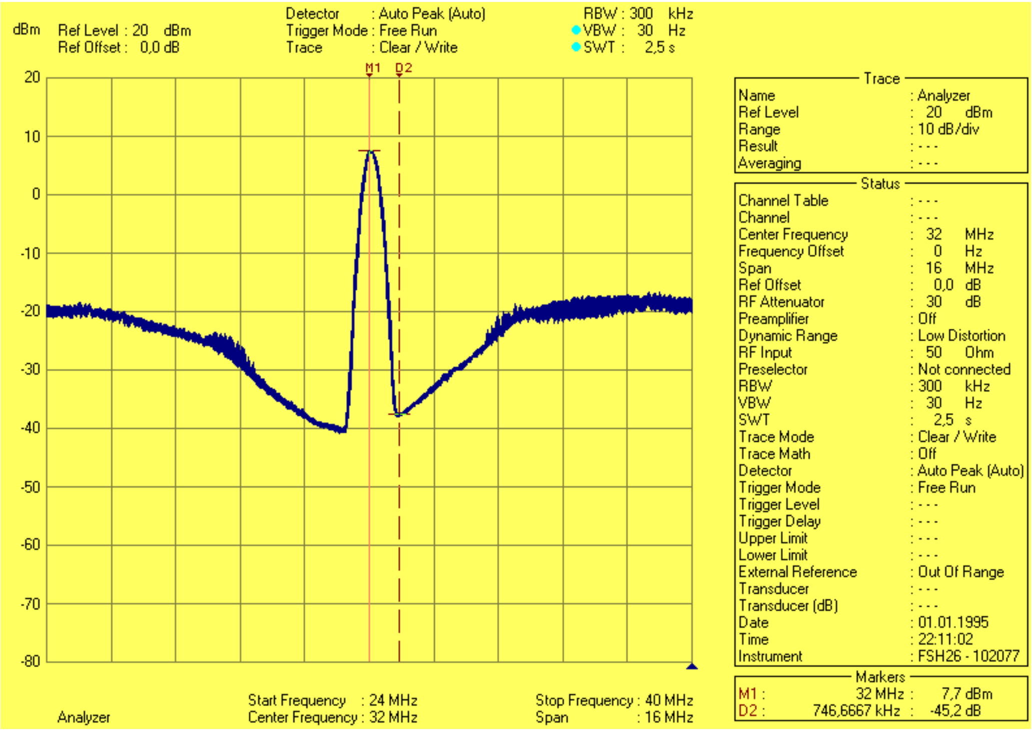
Figure 3.17. The output of the chip measured in an oscilloscope when the input is a 32 MHz 100mV peak to peak sine signal

To see the signal to noise ratio, the output of the chip is connected to a spectrum analyzer. Signal to noise ratio is 31.1 dB when the input is a 50 mV peak to peak sine signal, and the Fourier transform of output measured in a spectrum analyzer can be seen in Figure 3.18. When the sine signal input is increased to 330 mV peak to peak, Signal to noise ratio is also increased to 45.2 dB, which can be seen in Figure 3.19. If the sine signal input is increased to 450 mV peak to peak, noise cancelation is lowered and sigma delta shape is deteriorated as seen in Figure 3.20. The graph of signal to noise ratio versus input voltage can be seen in Figure 3.21. As seen in the figure, signal to noise ratio increases nearly linearly as the input voltage increases; then, reaches its maximum value when the input voltage is 330 mV and begins to deteriorate after 340 mV input voltage.



```
Ref Level : -1    dBm
Ref Offset :  0,0 dB

Detector      : Auto Peak (Auto)
Trigger Mode : Free Run
Trace         : Clear / Write

RBW : 300   kHz
VBW :   30   Hz
SWT :     2,5 s

Trace
Name                 : Analyzer
Ref Level            :   -1     dBm
Range                : 10 dB/div
Result               : - - -
Averaging            : - - -

Status
Channel Table        : - - -
Channel              : - - -
Center Frequency     :   32     MHz
Frequency Offset     :    0     Hz
Span                 :   16     MHz
Ref Offset           :    0,0   dB
RF Attenuator        :   20     dB
Preamplifier         : Off
Dynamic Range        : Low Distortion
RF Input             :   50     Ohm
Preselector          : Not connected
RBW                  : 300      kHz
VBW                  :   30     Hz
SWT                  :    2,5   s
Trace Mode           : Clear / Write
Trace Math           : Off
Detector             : Auto Peak (Auto)
Trigger Mode         : Free Run
Trigger Level        : - - -
Trigger Delay        : - - -
Upper Limit          : - - -
Lower Limit          : - - -
External Reference   : Out Of Range
Transducer           : - - -
Transducer (dB)      : - - -
Date                 : 01.01.1995
Time                 : 21:47:23
Instrument           : FSH26 - 102077

Markers
M1 :     32,1066667 MHz :    -9,4 dBm
D2 :       533,3333 kHz :   -31,1 dB

Start Frequency   : 24 MHz        Stop Frequency : 40 MHz
Center Frequency : 32 MHz         Span              : 16 MHz
```

Figure 3.18. The Fourier transform of the output measured in spectrum analyzer when the input is a 50 mV peak to peak sine signal.



Ref Level : 20 dBm
Ref Offset : 0,0 dB
Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trace : Clear / Write
RBW : 300 kHz
VBW : 30 Hz
SWT : 2,5 s

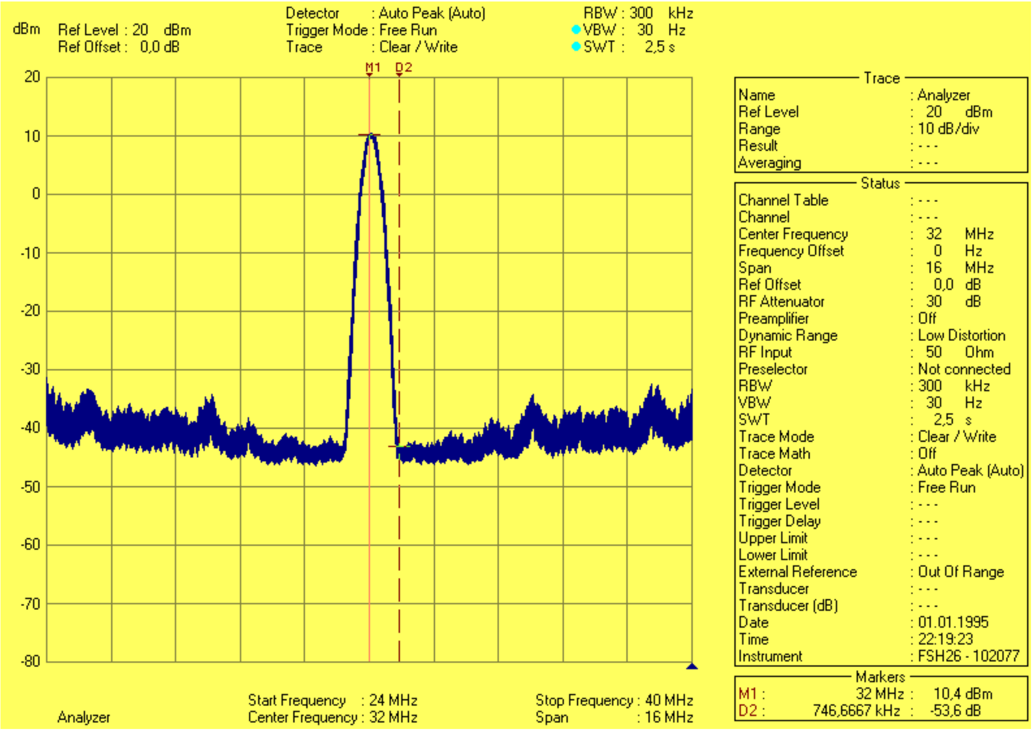
Trace
Name : Analyzer
Ref Level : 20 dBm
Range : 10 dB/div
Result : - - -
Averaging : - - -

Status
Channel Table : - - -
Channel : - - -
Center Frequency : 32 MHz
Frequency Offset : 0 Hz
Span : 16 MHz
Ref Offset : 0,0 dB
RF Attenuator : 30 dB
Preamplifier : Off
Dynamic Range : Low Distortion
RF Input : 50 Ohm
Preselector : Not connected
RBW : 300 kHz
VBW : 30 Hz
SWT : 2,5 s
Trace Mode : Clear / Write
Trace Math : Off
Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trigger Level : - - -
Trigger Delay : - - -
Upper Limit : - - -
Lower Limit : - - -
External Reference : Out Of Range
Transducer : - - -
Transducer (dB) : - - -
Date : 01.01.1995
Time : 22:11:02
Instrument : FSH26 - 102077

Markers
M1 : 32 MHz : 7,7 dBm
D2 : 746,6667 kHz : -45,2 dB

Start Frequency : 24 MHz
Center Frequency : 32 MHz
Stop Frequency : 40 MHz
Span : 16 MHz

Figure 3.19. The Fourier transform of the output measured in spectrum analyzer when the input is a 330 mV peak to peak sine signal.



Ref Level : 20 dBm
Ref Offset : 0,0 dB
Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trace : Clear / Write
RBW : 300 kHz
VBW : 30 Hz
SWT : 2,5 s

Trace
Name : Analyzer
Ref Level : 20 dBm
Range : 10 dB/div
Result : - - -
Averaging : - - -

Status
Channel Table : - - -
Channel : - - -
Center Frequency : 32 MHz
Frequency Offset : 0 Hz
Span : 16 MHz
Ref Offset : 0,0 dB
RF Attenuator : 30 dB
Preamplifier : Off
Dynamic Range : Low Distortion
RF Input : 50 Ohm
Preselector : Not connected
RBW : 300 kHz
VBW : 30 Hz
SWT : 2,5 s
Trace Mode : Clear / Write
Trace Math : Off
Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trigger Level : - - -
Trigger Delay : - - -
Upper Limit : - - -
Lower Limit : - - -
External Reference : Out Of Range
Transducer : - - -
Transducer (dB) : - - -
Date : 01.01.1995
Time : 22:19:23
Instrument : FSH26 - 102077

Markers
M1 : 32 MHz : 10,4 dBm
D2 : 746,6667 kHz : -53,6 dB

Start Frequency : 24 MHz
Center Frequency : 32 MHz
Stop Frequency : 40 MHz
Span : 16 MHz

Figure 3.20. The Fourier transform of the output measured in spectrum analyzer when the input is a 450 mV peak to peak sine signal.

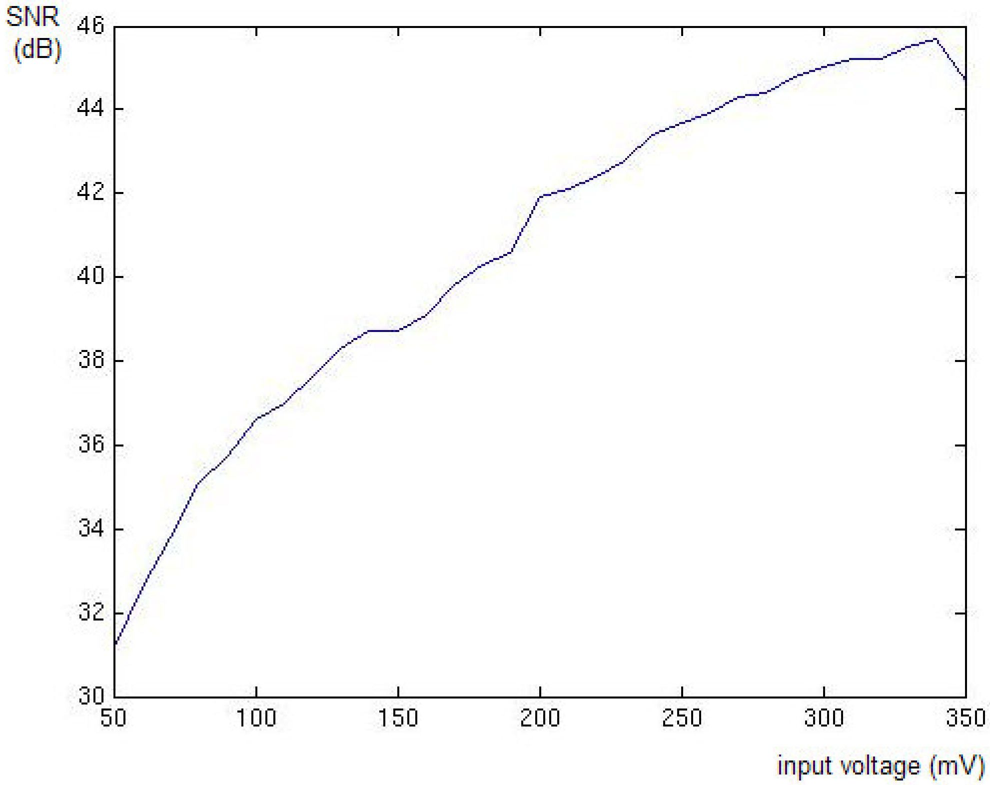


Figure 3.21. Signal to noise ratio versus input voltage graph.

3.2.2 Test of the Slow Mode

In this section, slow mode of the chip which has 8 MHz operating, 32 MHz sampling frequency is tested. Like the fast mode, slow mode bias voltages and supply voltages are adjusted to the optimum values. When the input is a 100 mV peak to peak sine signal, the output of the chip measured in an oscilloscope can be seen in Figure 3.22.

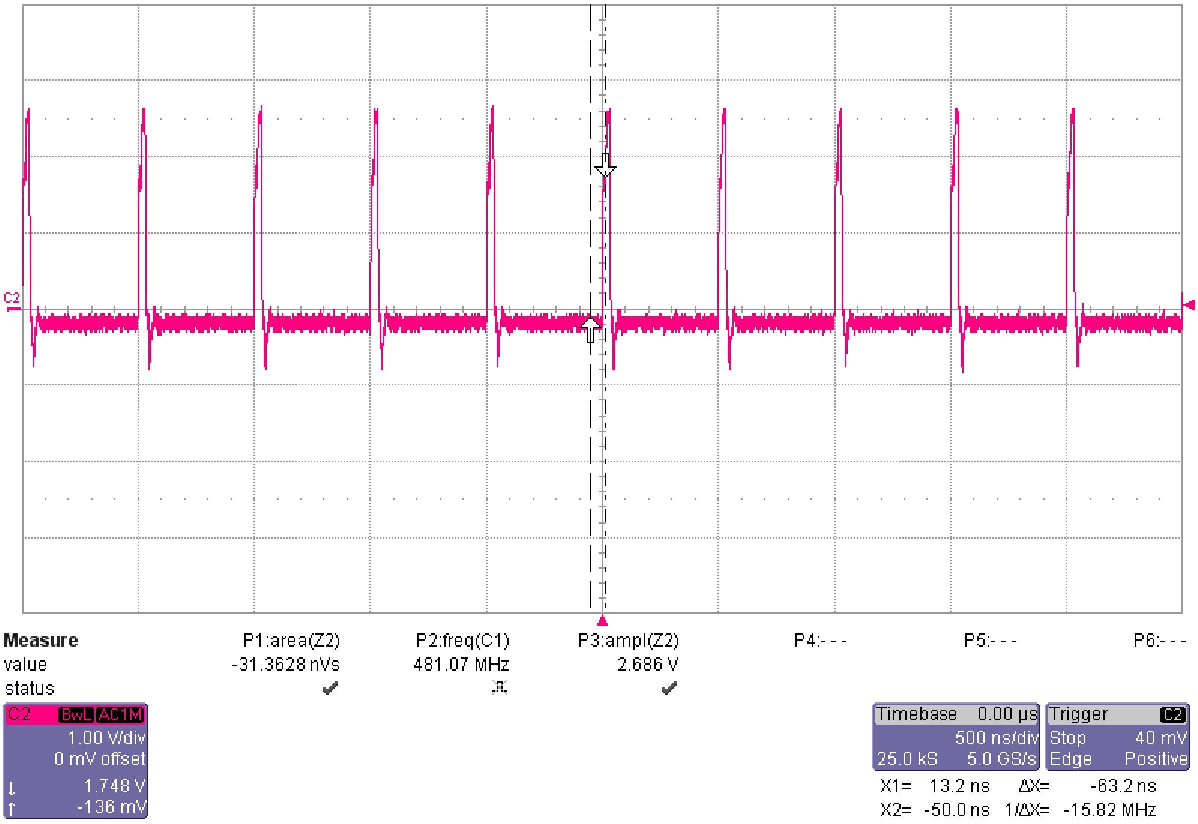
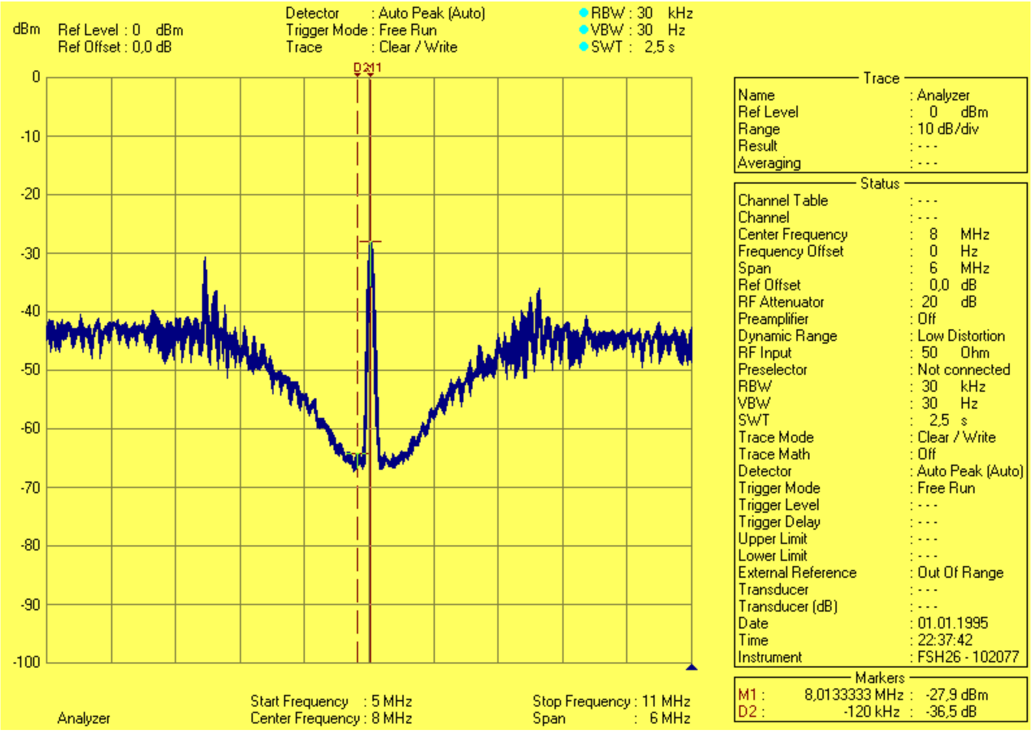


Figure 3.22. The output of the chip measured in an oscilloscope when the input is a 8 MHz 100 mV peak to peak sine signal

The output of the chip is connected to a spectrum analyzer again to see the new results. Signal to noise ratio is 36.5 dB when the input is a 50 mV peak to peak sine signal, and the Fourier form transform of output measured in a spectrum analyzer can be seen in Figure 3.23. When the sine signal input is increased to 260 mV peak to peak, Signal to noise ratio is also increased to 50.6 dB, which can be seen in Figure 3.24. If the sine signal input is increased to 450 mV peak to peak, noise cancelation is lowered and sigma delta shape is deteriorated as seen in Figure 3.25. The results could be better but the output of the chip is not connected to a BNC connector in PCB. Hence the results of the spectrum analyzer are not as good as they are expected due to the additional wiring added for the connections.



Ref Level : 0 dBm
Ref Offset : 0,0 dB

Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trace : Clear / Write

RBW : 30 kHz
VBW : 30 Hz
SWT : 2,5 s

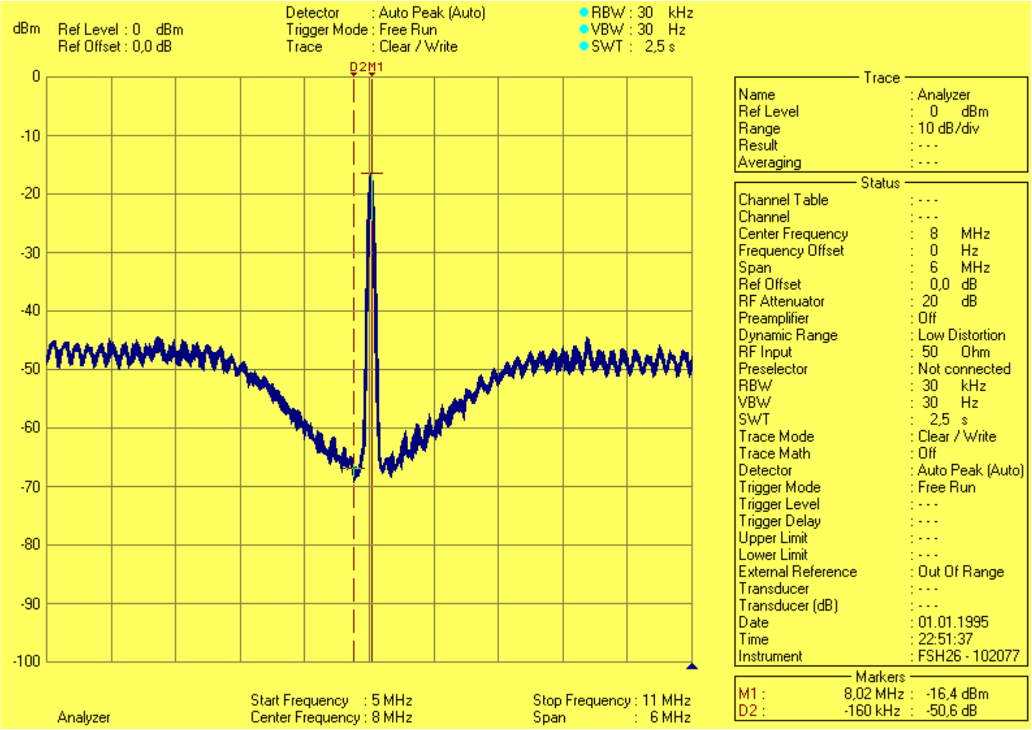
Trace
Name : Analyzer
Ref Level : 0 dBm
Range : 10 dB/div
Result : - - -
Averaging : - - -

Status
Channel Table : - - -
Channel : - - -
Center Frequency : 8 MHz
Frequency Offset : 0 Hz
Span : 6 MHz
Ref Offset : 0,0 dB
RF Attenuator : 20 dB
Preamplifier : Off
Dynamic Range : Low Distortion
RF Input : 50 Ohm
Preselector : Not connected
RBW : 30 kHz
VBW : 30 Hz
SWT : 2,5 s
Trace Mode : Clear / Write
Trace Math : Off
Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trigger Level : - - -
Trigger Delay : - - -
Upper Limit : - - -
Lower Limit : - - -
External Reference : Out Of Range
Transducer : - - -
Transducer (dB) : - - -
Date : 01.01.1995
Time : 22:37:42
Instrument : FSH26 - 102077

Markers
M1 : 8,0133333 MHz : -27,9 dBm
D2 : -120 kHz : -36,5 dB

Start Frequency : 5 MHz
Center Frequency : 8 MHz
Stop Frequency : 11 MHz
Span : 6 MHz

Figure 3.23. The Fourier form transform of the output measured in spectrum analyzer when the input is a 50 mV peak to peak sine signal.



Ref Level : 0 dBm
Ref Offset : 0,0 dB
Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trace : Clear / Write
RBW : 30 kHz
VBW : 30 Hz
SWT : 2,5 s

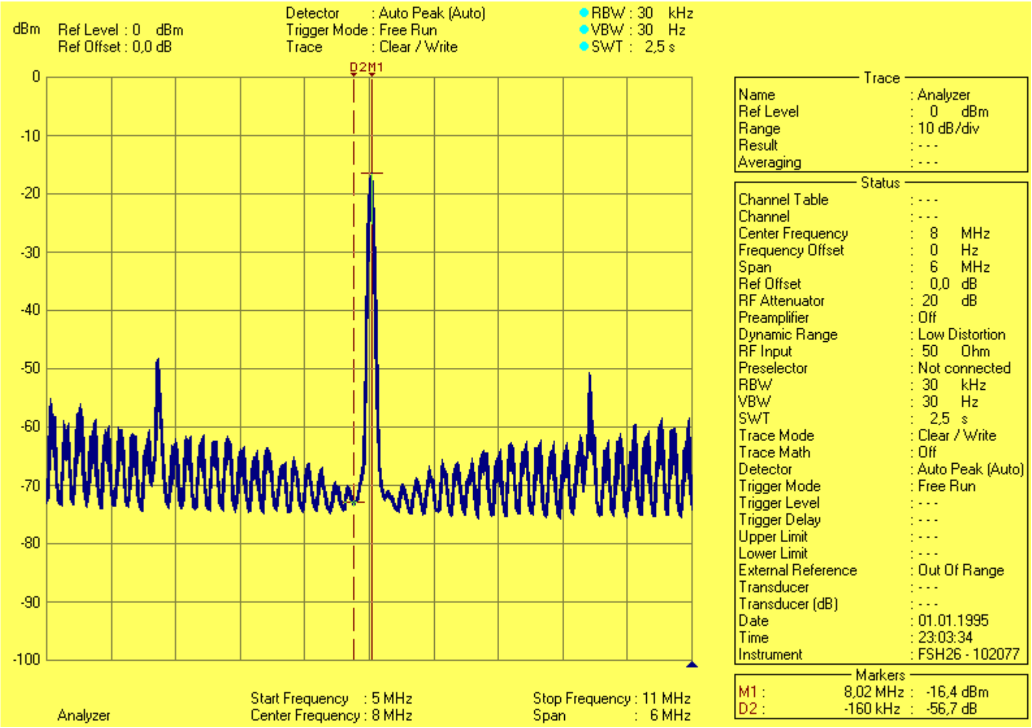
Start Frequency : 5 MHz
Center Frequency : 8 MHz
Stop Frequency : 11 MHz
Span : 6 MHz

Trace
Name : Analyzer
Ref Level : 0 dBm
Range : 10 dB/div
Result : - - -
Averaging : - - -

Status
Channel Table : - - -
Channel : - - -
Center Frequency : 8 MHz
Frequency Offset : 0 Hz
Span : 6 MHz
Ref Offset : 0,0 dB
RF Attenuator : 20 dB
Preamplifier : Off
Dynamic Range : Low Distortion
RF Input : 50 Ohm
Preselector : Not connected
RBW : 30 kHz
VBW : 30 Hz
SWT : 2,5 s
Trace Mode : Clear / Write
Trace Math : Off
Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trigger Level : - - -
Trigger Delay : - - -
Upper Limit : - - -
Lower Limit : - - -
External Reference : Out Of Range
Transducer : - - -
Transducer (dB) : - - -
Date : 01.01.1995
Time : 22:51:37
Instrument : FSH26 - 102077

Markers
M1 : 8,02 MHz : -16,4 dBm
D2 : -160 kHz : -50,6 dB

Figure 3.24. The Fourier form transform of the output measured in spectrum analyzer when the input is a 260 mV peak to peak sine signal.



Ref Level : 0 dBm
Ref Offset : 0,0 dB
Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trace : Clear / Write
RBW : 30 kHz
VBW : 30 Hz
SWT : 2,5 s

Start Frequency : 5 MHz
Center Frequency : 8 MHz
Stop Frequency : 11 MHz
Span : 6 MHz

Trace
Name : Analyzer
Ref Level : 0 dBm
Range : 10 dB/div
Result : - - -
Averaging : - - -

Status
Channel Table : - - -
Channel : - - -
Center Frequency : 8 MHz
Frequency Offset : 0 Hz
Span : 6 MHz
Ref Offset : 0,0 dB
RF Attenuator : 20 dB
Preamplifier : Off
Dynamic Range : Low Distortion
RF Input : 50 Ohm
Preselector : Not connected
RBW : 30 kHz
VBW : 30 Hz
SWT : 2,5 s
Trace Mode : Clear / Write
Trace Math : Off
Detector : Auto Peak (Auto)
Trigger Mode : Free Run
Trigger Level : - - -
Trigger Delay : - - -
Upper Limit : - - -
Lower Limit : - - -
External Reference : Out Of Range
Transducer : - - -
Transducer (dB) : - - -
Date : 01.01.1995
Time : 23:03:34
Instrument : FSH26 - 102077

Markers
M1 : 8,02 MHz : -16,4 dBm
D2 : -160 kHz : -56,7 dB

Figure 3.25. The Fourier form transform of the output measured in spectrum analyzer when the input is a 450 mV peak to peak sine signal.

4. CONVERSION OF THE ADC FROM 1 BIT TO 3 BIT

4.1 Introduction to the 3 Bit Design

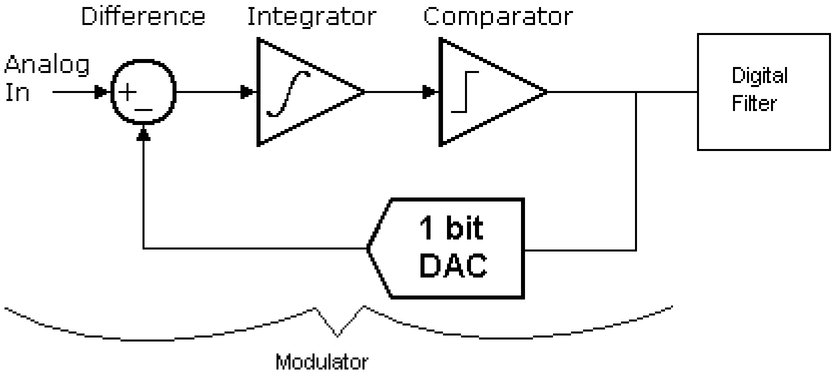


Figure 4.1. 1 bit sigma delta modulator

The conversion of the 1 bit old design which can be seen in Figure 4.1 to 3 bit new design in figure 4.2 will be explained in this section. First of all, the output of the 1 bit comparator is designed as it compares the differential outputs of the filter with each other and the quantizer output is '1' if the positive input is more than negative input and '0' if vice versa. The output of the new comparator block is now 3 bit so there are $2^3 = 8$ different levels of outputs. To compare filter differential outputs more precisely it has to be known how large the difference of the differential outputs is. So, these outputs should also be compared with each other plus some extra current to find the difference between them. There are 8 different levels of outputs so there must be $2^3 - 1 = 7$ comparators. Therefore, there must be 7 differential inputs for 7 comparators. So, the outputs of the filter must be copied to those converter blocks.

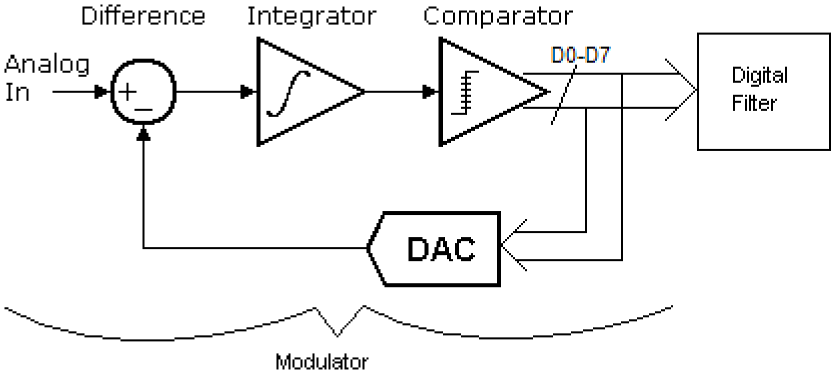


Figure 4.2. 3 bit sigma delta modulator

4.2 New Quantization Block

The new quantization block now consists of 7 comparators and current mirror block. Usually continuous time sigma delta modulators like [2] have a sample and hold circuitry so that quantization can be done frequently at a clock frequency, but comparators used in this design are already comparing the input signals frequently at a clock frequency. Thus, there is no need to use a sample and hold circuitry in this design.

The outputs of the filter are between +350 µA and -350 µA. Hence, each current mirror will have a 500 µA DC current. Moreover, the output thresholds will be +300 µA, +200 µA, +100 µA, 0 µA, -100 µA, -200 µA, -300 µA. As long as the input is larger than those threshold values, the output will be ‘1’, otherwise the output will be ‘0’. The output levels of the comparators and the 3 bit values can be seen in Table 4.3. The new quantization circuitry can be seen in Figure 4.3. Estimated power used in current mirrors is 500 µA x 2.5 V x 8 x 2 =16 mW.

Table 4.1. Comparator current levels and outputs

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Y2**	**Y1**	**Y0**
Less than -300 µA	0	0	0	0	0	0	0	0	0	0
-300 µA to -200 µA	0	0	0	0	0	0	1	0	0	1
-200 uA to -100 µA	0	0	0	0	0	1	1	0	1	0
-100 µA to 0 µA	0	0	0	0	1	1	1	0	1	1
0 µA to 100 µA	0	0	0	1	1	1	1	1	0	0
100 µA to 200 µA	0	0	1	1	1	1	1	1	0	1
200 µA to 300 µA	0	1	1	1	1	1	1	1	1	0
More than 300 µA	1	1	1	1	1	1	1	1	1	1

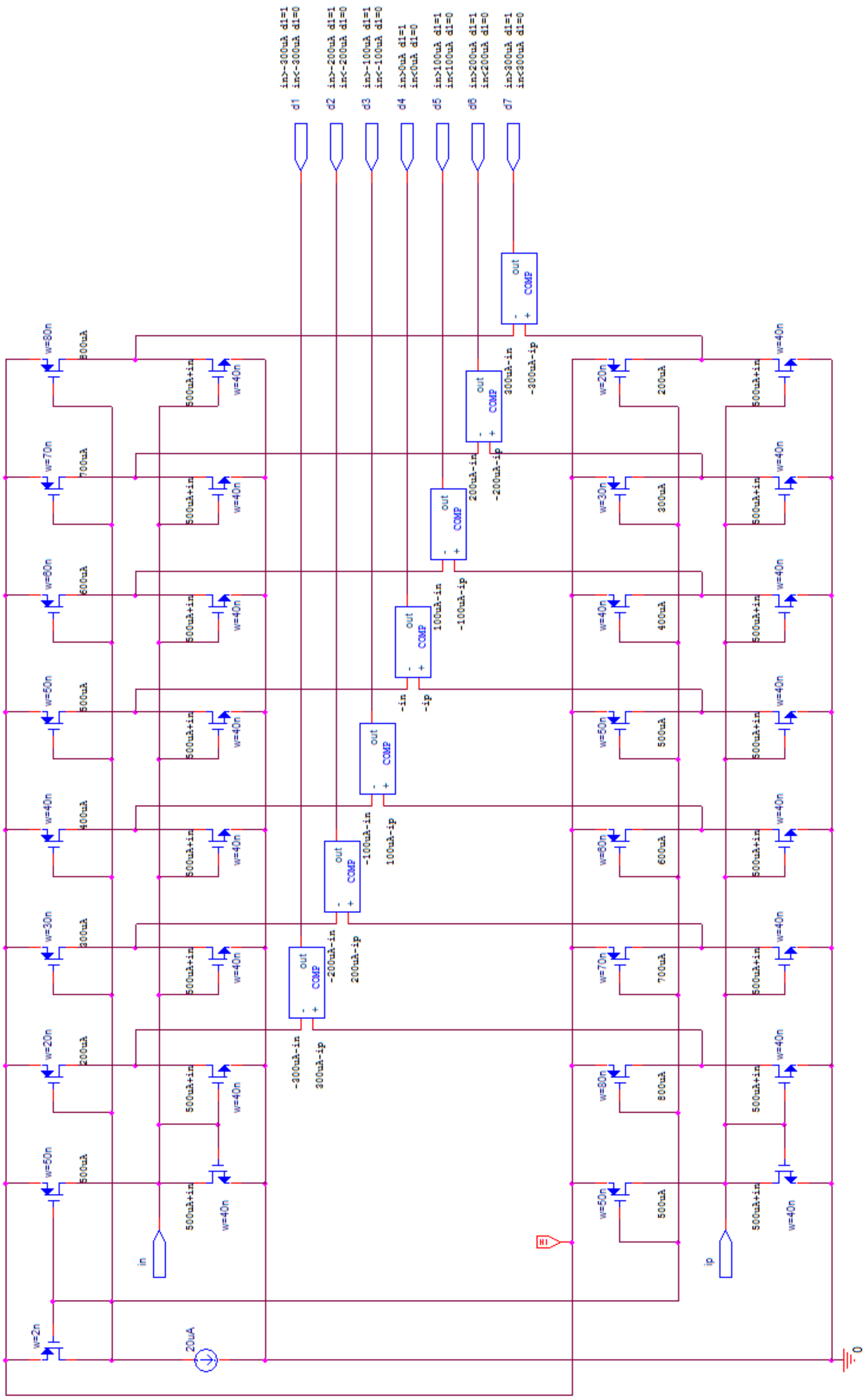


Figure 4.3. New quantization circuitry with current mirrors

4.3 Reconfiguration of the DAC

According to the comparators output first DAC block either generates -20 µA or +20 µA. In the new system, there are 7 comparators. Therefore 7 DAC circuits will be used in the new DAC block. The outputs of the DAC circuits are connected to each other so the new output generates -140 µA to 140 µA depending of the output of the comparator. 140 µA is very high for the input due to 20 µA. So a current divider block which can be seen in Figure 4.4 is used to lower the current to its quarter, so the output of the new DAC block changes between -35 µA to +35 µA(-35 µA, -25 µA, -15 µA, -5 µA , 5 µA , 15 µA , 25 µA , 35 µA).

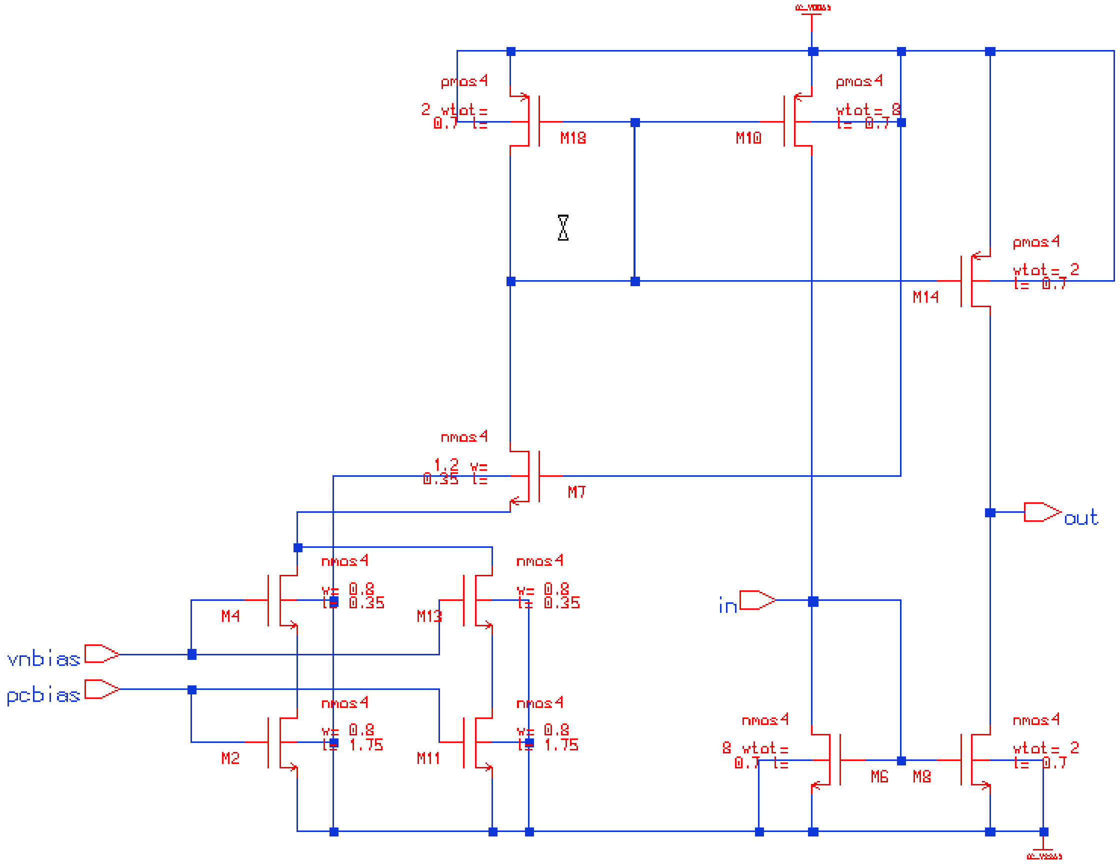


Figure 4.4. Current divider

4.4 Configuration of the Output Block

Quantization block has 7 outputs which are also the outputs of the comparators in same block. The output of the general circuit must be 3 bits. Therefore, an output block is needed to convert 7 quantizer outputs to 3 bit outputs.

Table 4.2. Quantizer outputs, encoder inputs and 3 bit binary code

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**q7**	**q6**	**q5**	**q4**	**q3**	**q2**	**q1**	**q0**	**Y2**	**Y1**	**Y0**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	0
0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	1	0	1
0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	1	1	0
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1

In Table 4.2, 7 quantizer outputs which are also a thermometer code, encoder inputs and binary code equivalents can be seen. Before the conversion of quantizer outputs to binary code, conversion of thermometer code to encoder inputs is required. If it is assumed that D0=1 D8=0,

$$q(x)=D(x)\oplus(D(x+1)) \qquad (1)$$

For example, $q(5)=D(5)\oplus D(6)=1\oplus 1=0$ when the output is $(101)_2$. Hence, this conversion block can be done with XOR gates. The encoder inputs are used for another flash DAC unit which has an analog output between 2.5 V and 0 V and this output value changes depending of the encoder inputs. But this flash DAC unit requires the inverted values of the encoder inputs. Therefore, XNOR gates are used to have the same outputs without using inverters so there will be less latency between inverted outputs. Furthermore, the output of the flash DAC unit is not precise but it is an abrupt output which can be measured easily. It is not precise because of V_{GS} voltages of the transistors, delay of the transistors when they are turned off or on, inequality of the resistors and the capacitance of the gate voltages of the transistors. The output block converting the 7 comparator outputs to encoder inputs can be seen in Figure 4.5.

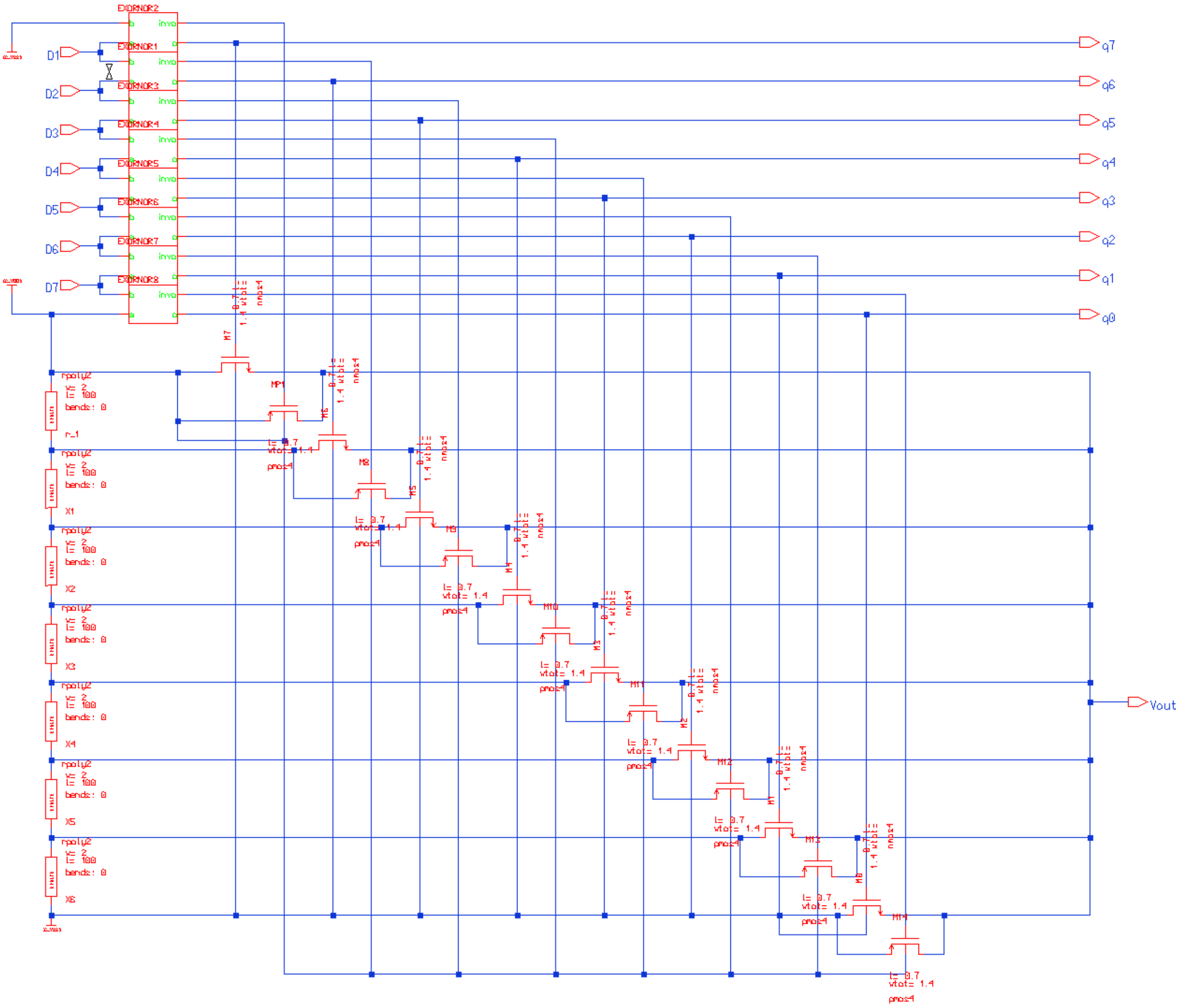


Figure 4.5. Output block used to convert 7 comparator outputs to encoder inputs and a single abrupt output

Conversion of encoder inputs to binary code can be done easily via an encoder. The encoder consists of NAND and NOR gates. In Figure 4.6, 8 to 3 encoder can be seen. NAND and NOR gates can be seen in Figure 4.7. The new design scheme made in Mentor tool can be seen in Figure 4.8 and the layout can be seen in Figure 4.9. The signal to noise ratio of the HSPICE simulation of the scheme can be seen in Figure 4.10.

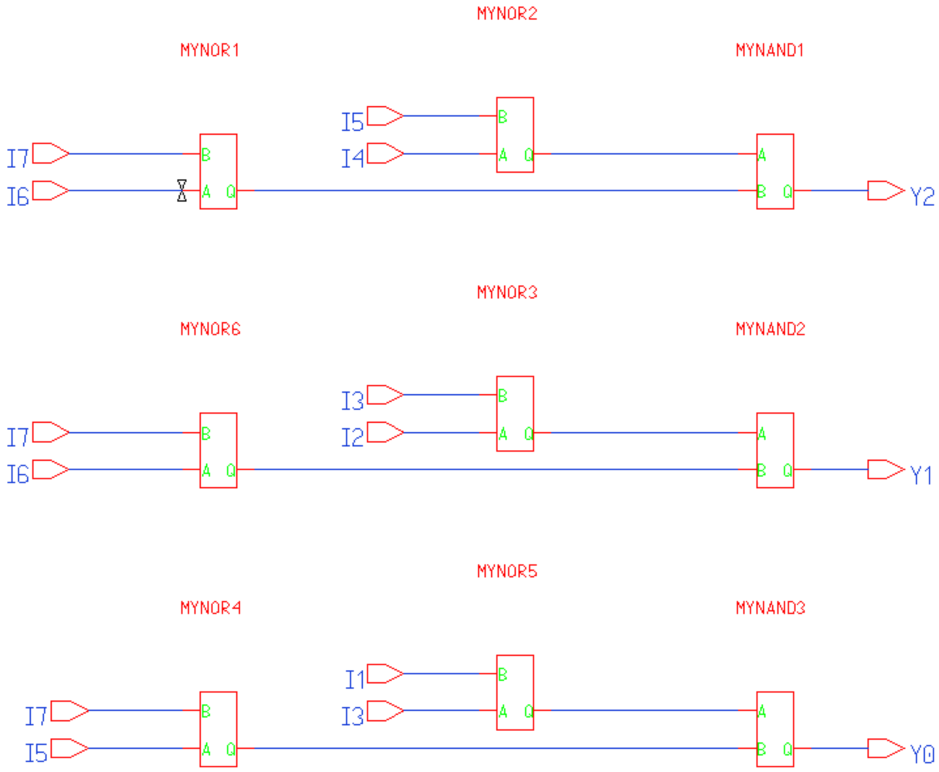


Figure 4.6. 8 to 3 encoder

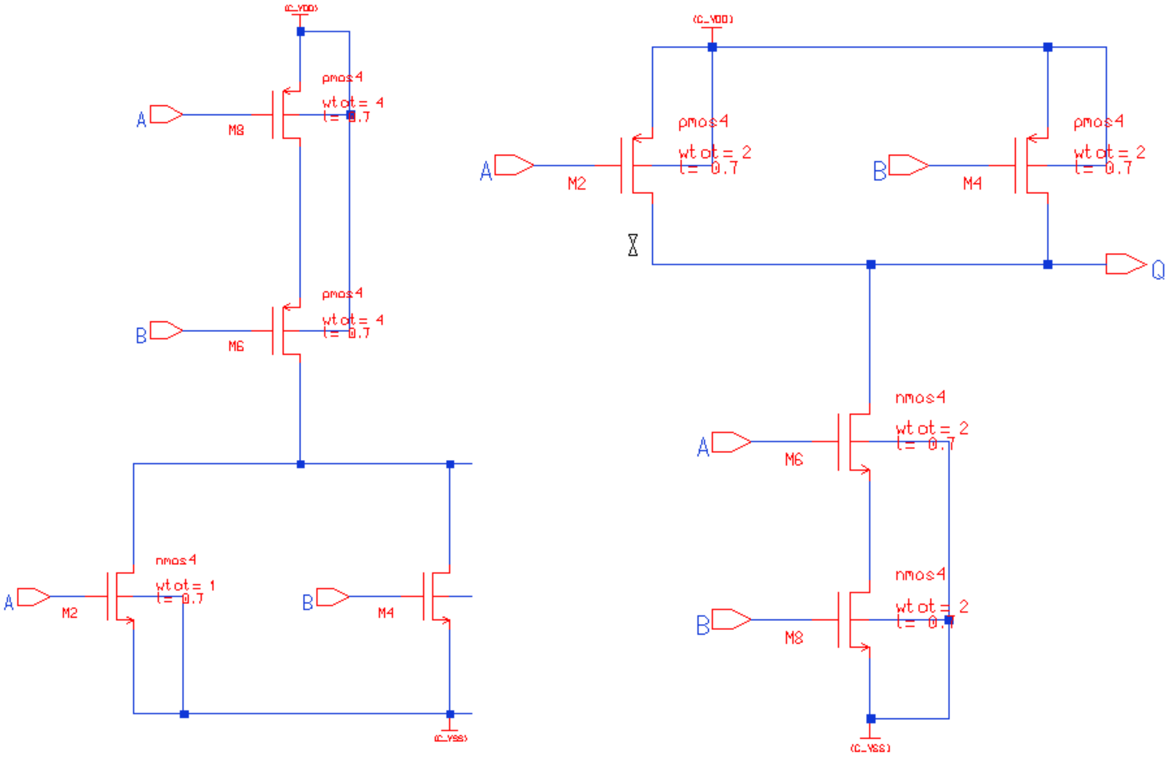


Figure 4.7. NOR gate and NAND gate

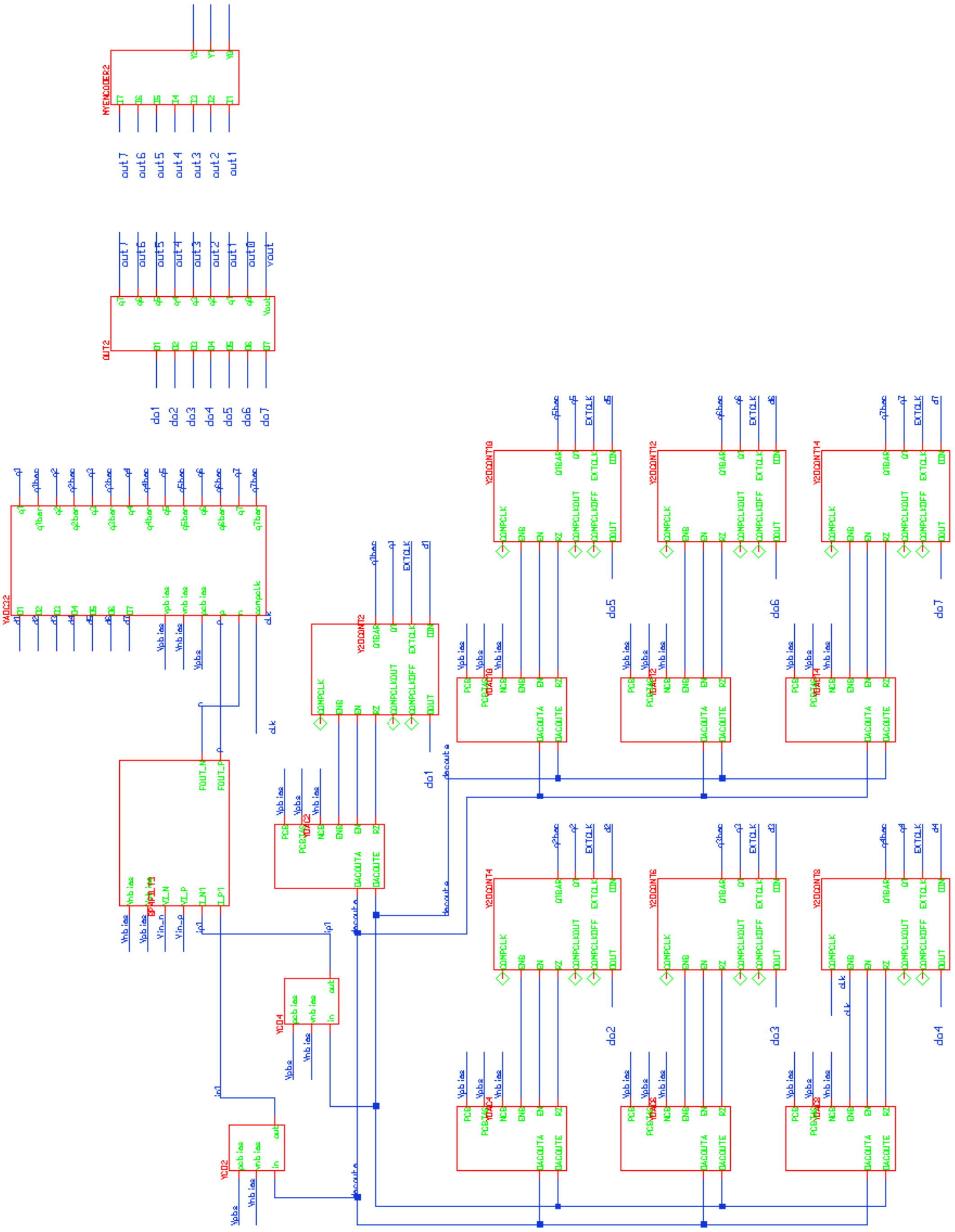


Figure 4.8. New design scheme made in Mentor tool

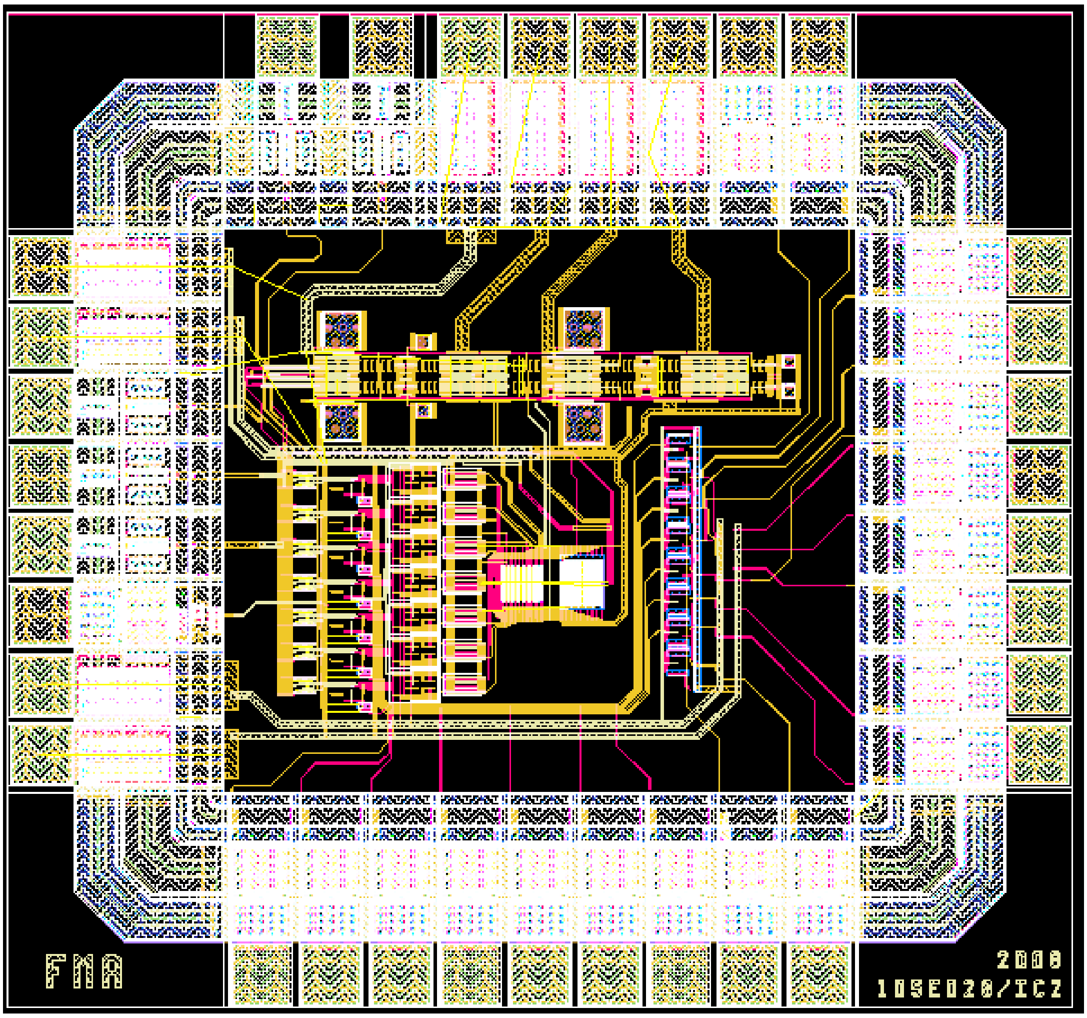


Figure 4.9. The layout of the new design

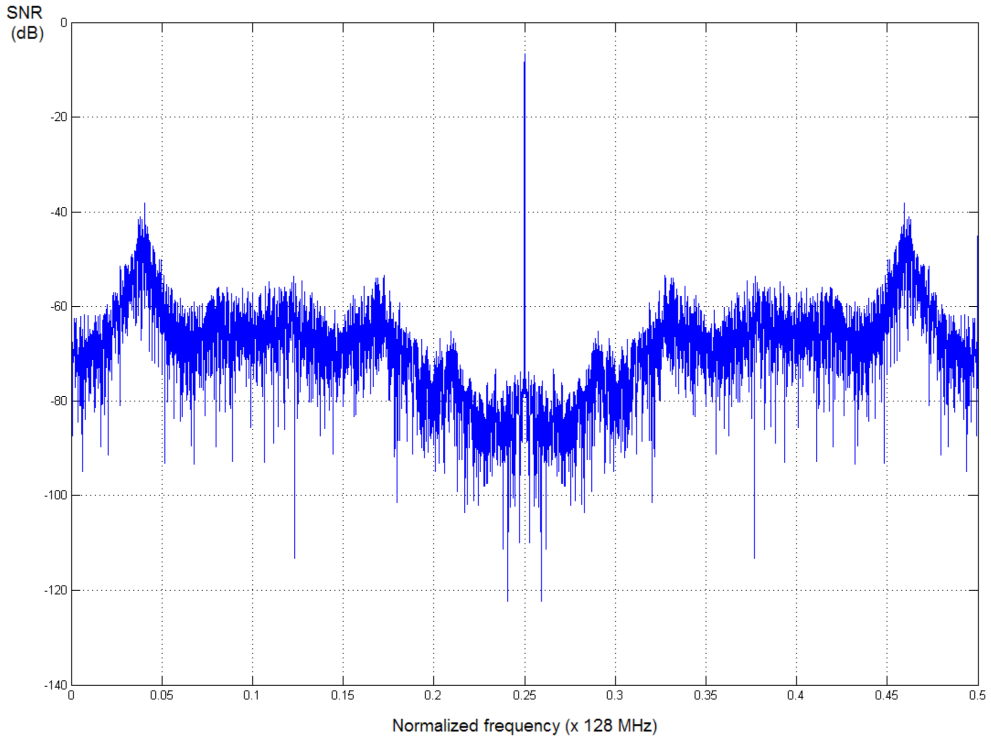


Figure 4.10. The signal to noise ratio of the HSPICE simulation of the scheme

5. 3 BIT DESIGN TEST RESULTS

5.1 PCB Redesign

A new PCB is designed to test the new 3 bit sigma delta modulator because the previous PCB had some problems and the new sigma delta modulator outputs are different from the previous one. The pins of the new chip and socket connections for plugging chip into the new PCB are the same as the previous design and can be seen in Figure 5.1 and 5.2. Nevertheless, the pins specifications of the chip and the PCB are different from previous one and can be seen in Table 5.1 and 5.2.

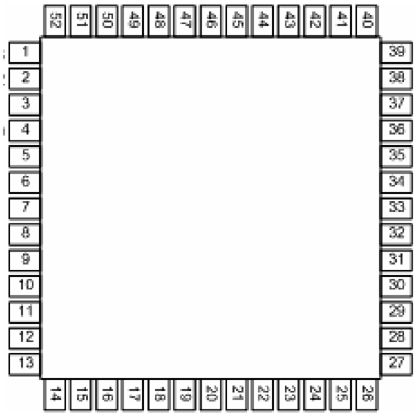


Figure 5.1. The pins of the new chip

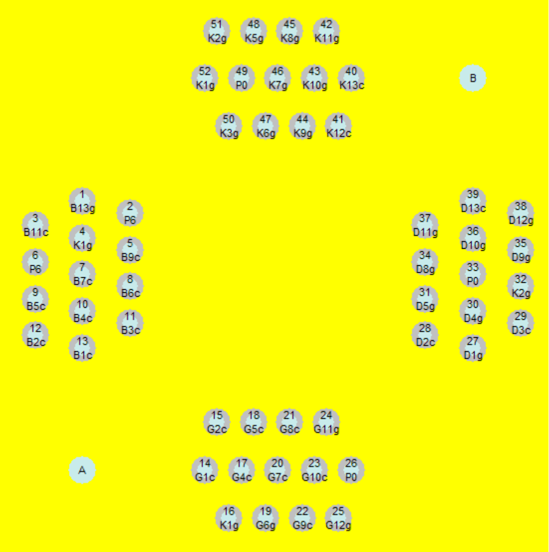


Figure 5.2. Socket connections for plugging chip into the new PCB

Table 5.1. Pins and pin specifications of the new chip

Pin	**Pin Specifications**
1	Null
2	Null
3	Null
4	Analog supply voltage
5	Analog ground voltage
6	DAC bias voltage input
7	NMOS cascode bias voltage input
8	PMOS cascode bias voltage input
9	128 MHz clock input
10	Digital ground voltage
11	Digital supply voltage
12	Null
13	Null
14	Null
15	Null
16	Quantizer output d1
17	Quantizer output d2
18	Quantizer output d3
19	Quantizer output d4
20	Quantizer output d5
21	Quantizer output d6
22	Quantizer output d7
23	Serial output
24	Encoder input Q7
25	Null
26	Null
27	Null
28	Null
29	Encoder input Q6
30	Encoder input Q5
31	3 bit binary output Y0
32	3 bit binary output Y1
33	3 bit binary output Y2
34	Encoder input Q4
35	Encoder input Q3
36	Encoder input Q2
37	Null
38	Null
39	Null
40	Null
41	Null
42	Encoder input Q1
43	Encoder input Q0
44	4th integrator supply voltage
45	3rd integrator supply voltage
46	2nd integrator supply voltage
47	1st integrator supply voltage
48	Positive input for ADC
49	Negative input for ADC
50	Null
51	Null
52	Null

Table 5.2. PCB inputs of the new design

Pin	**Pin Specifications**
P0	Analog Ground
P1	Voltage source input
P2	Input signal
P6	Digital Ground
SEROUT	Serial output
PQ0	Encoder input Q0
PQ1	Encoder input Q1
PQ2	Encoder input Q2
PQ3	Encoder input Q3
PQ4	Encoder input Q4
PQ5	Encoder input Q5
PQ6	Encoder input Q6
PQ7	Encoder input Q7
Pd1	Quantizer output d1
Pd2	Quantizer output d2
Pd3	Quantizer output d3
Pd4	Quantizer output d4
Pd5	Quantizer output d5
Pd6	Quantizer output d6
Pd7	Quantizer output d7
PY0	3 bit binary output Y0
PY1	3 bit binary output Y1
PY2	3 bit binary output Y2

5.1.1 Biasing and Supplying of the Chip

Same bias and supply voltages are used on the chip. Hence, same voltage generation circuitry is used on the PCB. However, 500 Ω potentiometers are used instead of parallel 1 KΩ potentiometers and 1 KΩ resistors. Those voltage generation circuits are nearly the same of the previous PCB.

5.1.2 Input and Output Blocks

Like in the previous design, a transformer is used to convert a single signal into two symmetrical signals with the same amplitude. Moreover, small capacitances are connected between the output of the transformer and the input of the chip again to ignore the DC level differences between the inputs of the chip and the outputs of the transformer. In the new design there is only one transformer. Hence, there are only two inputs of the chip which are symmetrical. Figure 5.3 shows detailed information about the input block.

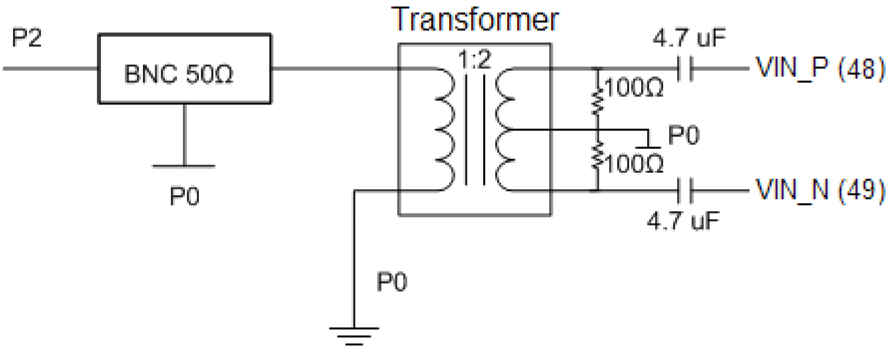


Figure 5.3. Input block converting singular input to differential input

There are 4 kinds of outputs of the chip, which are analog output, 3 bit binary outputs, encoder inputs and the outputs of the comparators. BNC connectors are used to have better results in analog and 3 bit binary outputs which can be seen in Figure 5.4 and 5.5. Encoder inputs and the outputs of the comparators are connected to logic converters instead.

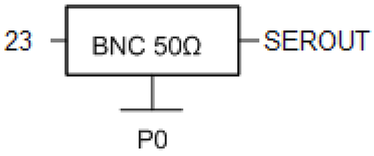


Figure 5.4. 3 bit analog output.

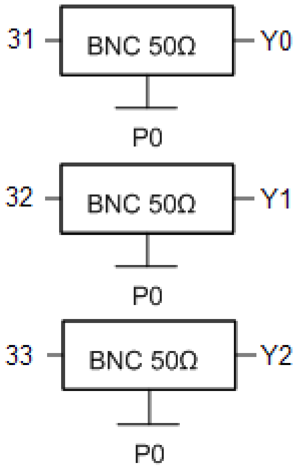


Figure 5.5. 3 bit binary outputs

5.1.3 Final Scheme of the PCB

Final scheme of the PCB can be seen in Figure 6 and the photos of the PCB can be seen in Figure 5.7 and 5.8.

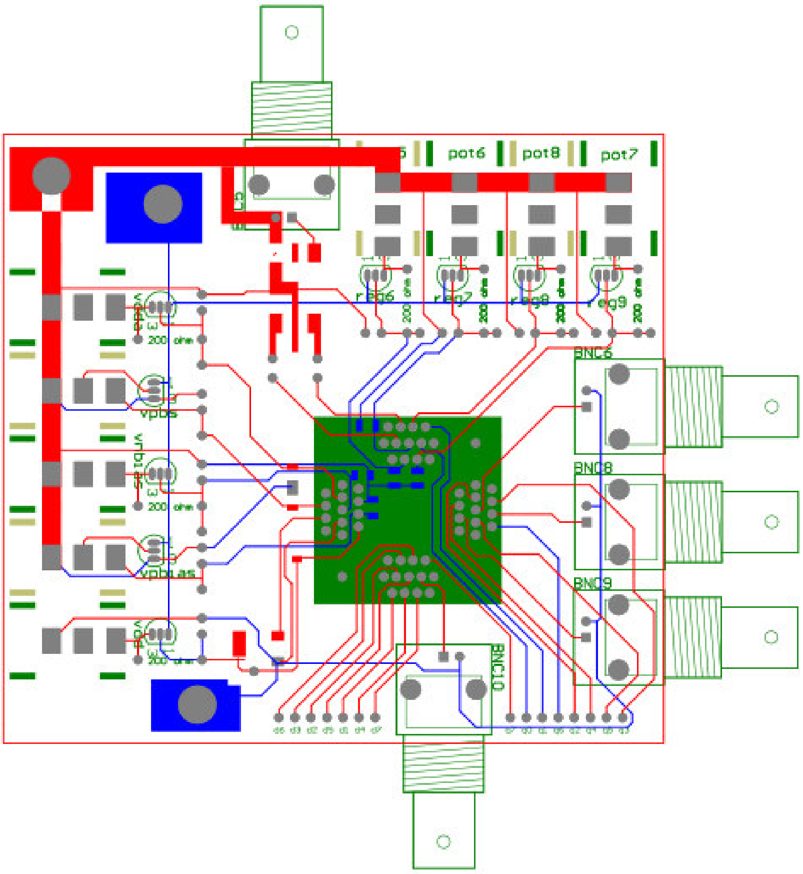


Figure 5.6. Scheme of the PCB

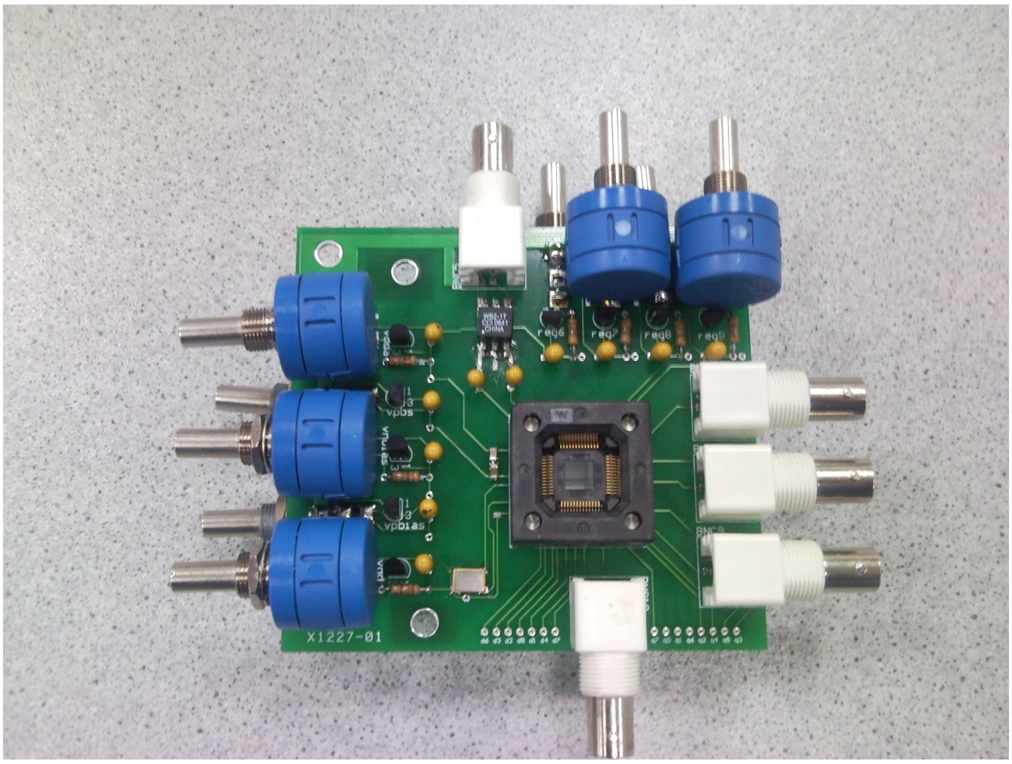


Figure 5.7. Photo of the PCB from above

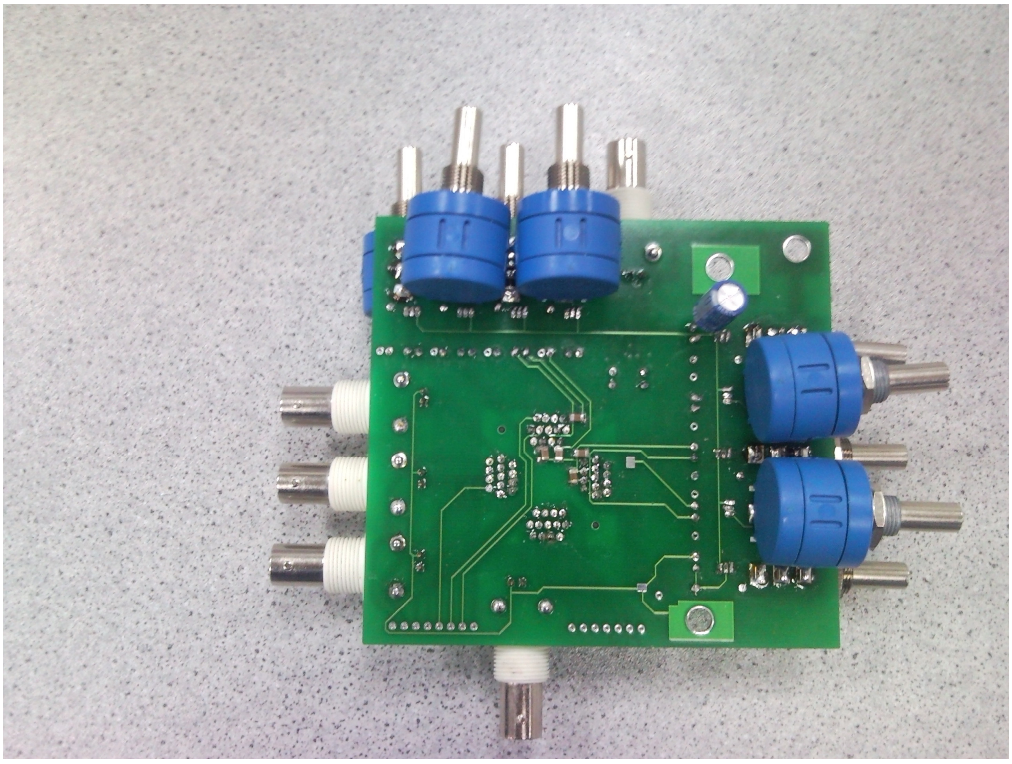


Figure 5.8. Photo of the PCB from below.

5.2 Test of the New PCB

Supply and bias voltages are set by tuning the potentiometers and these voltages can be seen in Table 5.3.

Table 5.3. Supply and bias voltages used in PCB

Node	**Voltage**
Analog supply voltage	2.5 V
Digital supply voltage	2.5 V
Supply voltage of the 1st integrator	2.5 V
Supply voltage of the 2nd integrator	2.5 V
Supply voltage of the 3rd integrator	2.5 V
Supply voltage of the 4th integrator	2.5 V
DAC bias voltage input	1.18 V
NMOS cascode bias voltage input	1.78 V
PMOS cascode bias voltage input	0.52 V

First of all, the output signal is checked with an oscilloscope which can be seen in Figure 5.9 after supply voltages and bias voltages are set. Like seen in the figure output voltage is an analog voltage changing every 7.8125 ns (128 MHz) and changes from 0 V to 2 V. The output voltage value has some noise and it doesn't change fast enough. This is can be because of the latency of the transistors while switching on or off and because of the length of the wires from the output node to the output pin. Also the output voltage must be up to 2.5 V but it is 2 V maximum. This is probably caused by the V_{GS} voltage of the gate transistors. The result from this output will be abrupt but that was known before the design and more precise results can be achieved from digital outputs which will be given detailed information later.

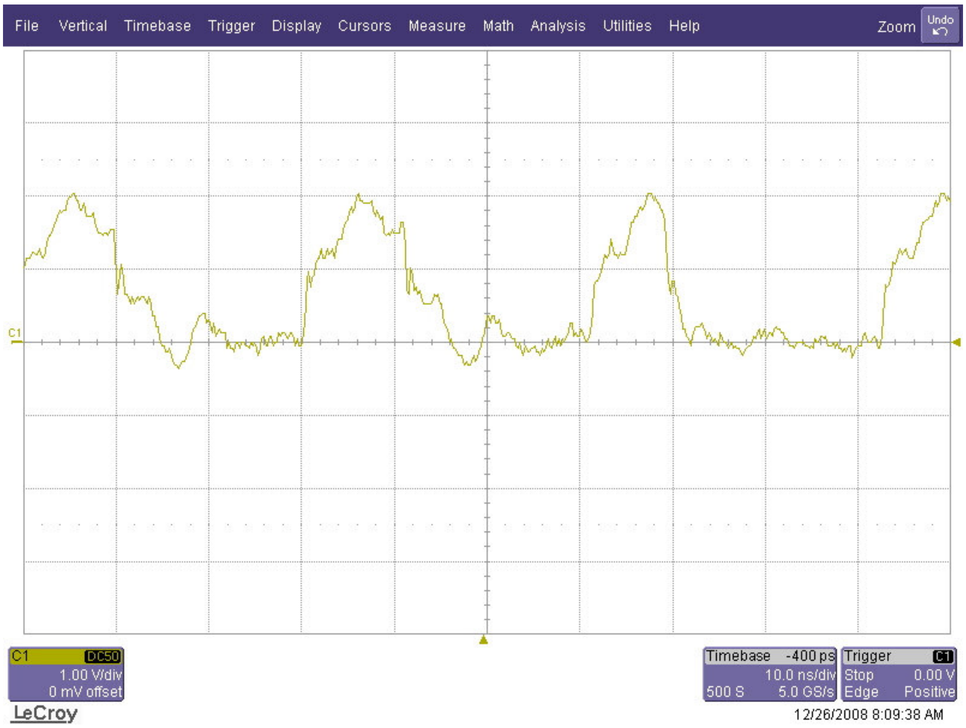


Figure 5.9. 3 bit analog output in time domain measured at oscilloscope

If the analog output is connected to a spectrum analyzer, the signal to noise ratio (SNR) can be measured. Two types of spectrum analyzers are used to measure SNR and the results can be seen in Figure 5.10 and 5.11. From those results, 58 dB SNR is calculated from the first spectrum analyzer and 60 dB SNR is calculated from the second. During the calculations and design, it is expected and calculated that the SNR would be 72 dB but the results were lower than expected. These results were abrupt so 3 bit binary outputs are measured and swept enough time and each 3 bit logic value is computed frequently equal to the clock period. Those logic values are used to calculate the SNR using a fast Fourier transform (FFT) code in MATLAB and the MATLAB result can be seen in Figure 5.12. The SNR from the MATLAB code is around 55-60 dB which is still lower than expected. Before investigating the cause of the low SNR, 1 bit outputs are checked. 1 bit output is equal to the highest order of the 3 bit digital signal. Therefore the highest order of the 3 bit digital signal is connected to spectrum analyzers to check 1 bit SNR results which can be seen in Figure 5.13 and 5.14. 1 bit SNR is 55 dB in spectrum analyzer 1 and nearly 57 dB in spectrum analyzer 2. Each extra bit should increase SNR by 6 dB so SNR should be 67 - 69 dB from the design instead of 58 - 60 dB. Hence, conversion to 3 bit blocks is checked.

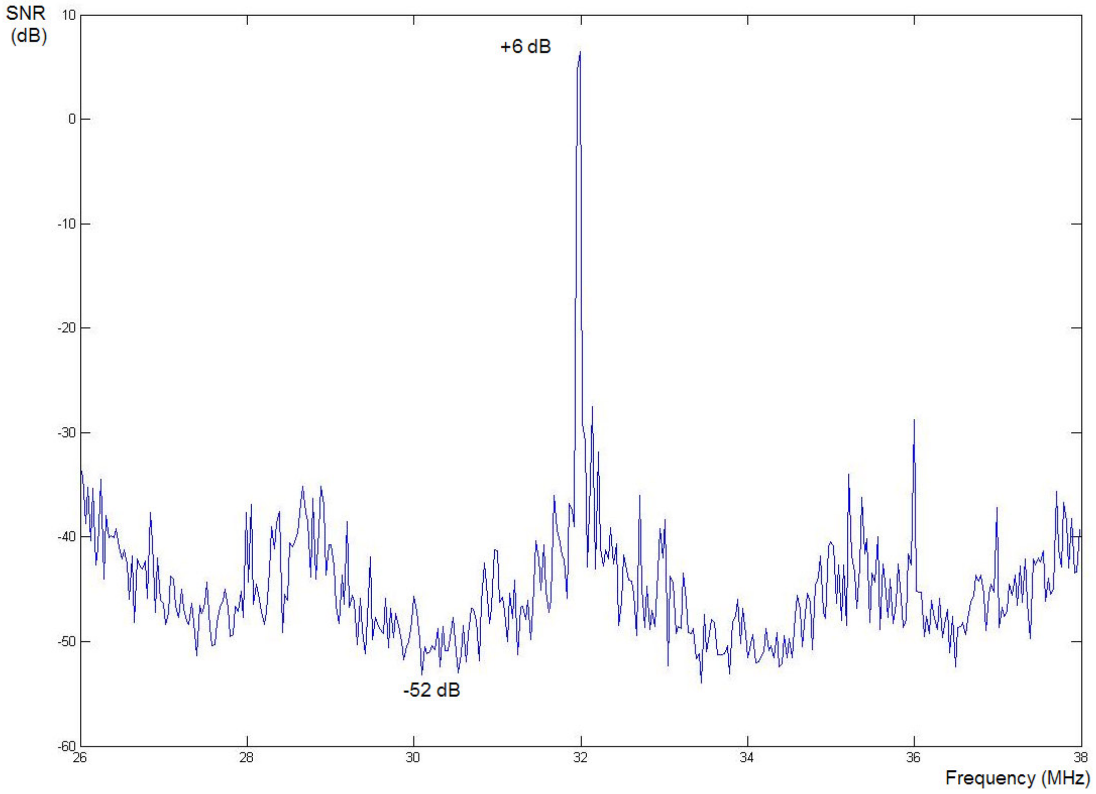
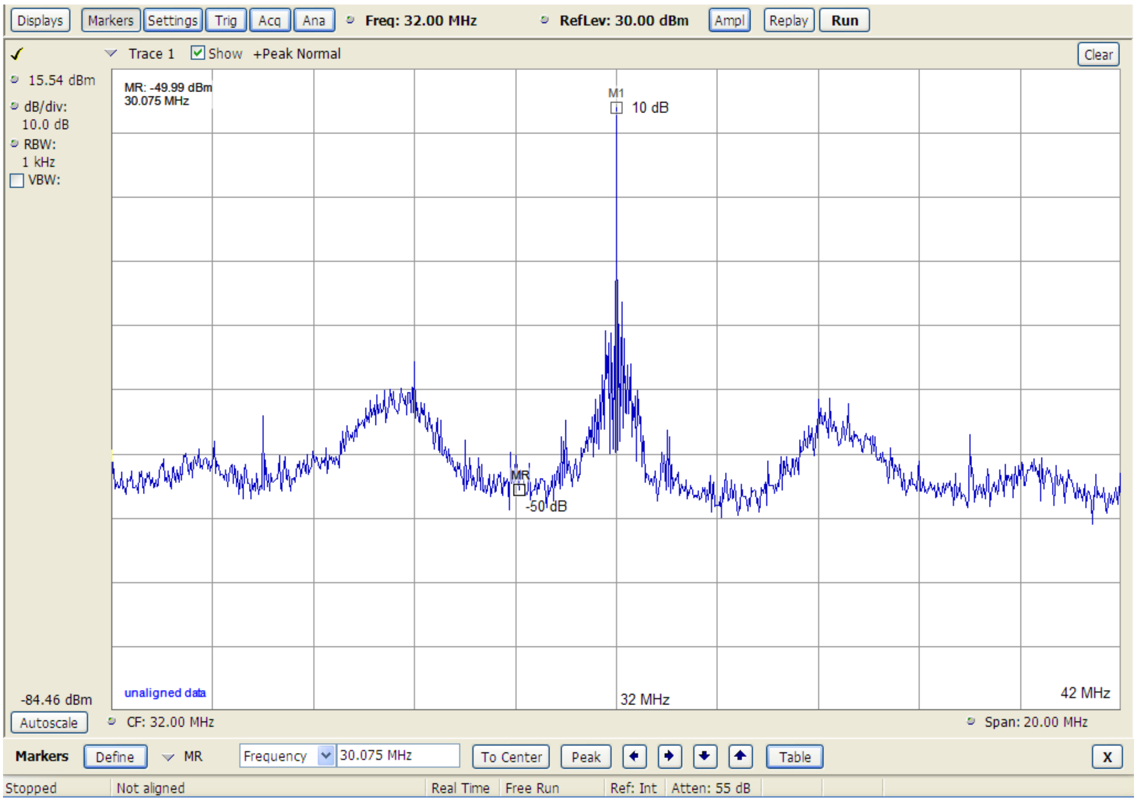


Figure 5.10. 3 bit analog output result measured at spectrum analyzer 1



Freq: 32.00 MHz

RefLev: 30.00 dBm

Trace 1 ☑ Show +Peak Normal

15.54 dBm

dB/div: 10.0 dB

RBW: 1 kHz

☐ VBW:

MR: -49.99 dBm
30.075 MHz

-84.46 dBm

CF: 32.00 MHz

Span: 20.00 MHz

Markers MR Frequency 30.075 MHz

Stopped | Not aligned | Real Time | Free Run | Ref: Int | Atten: 55 dB

Figure 5.11. 3 bit analog output result measured at spectrum analyzer 2

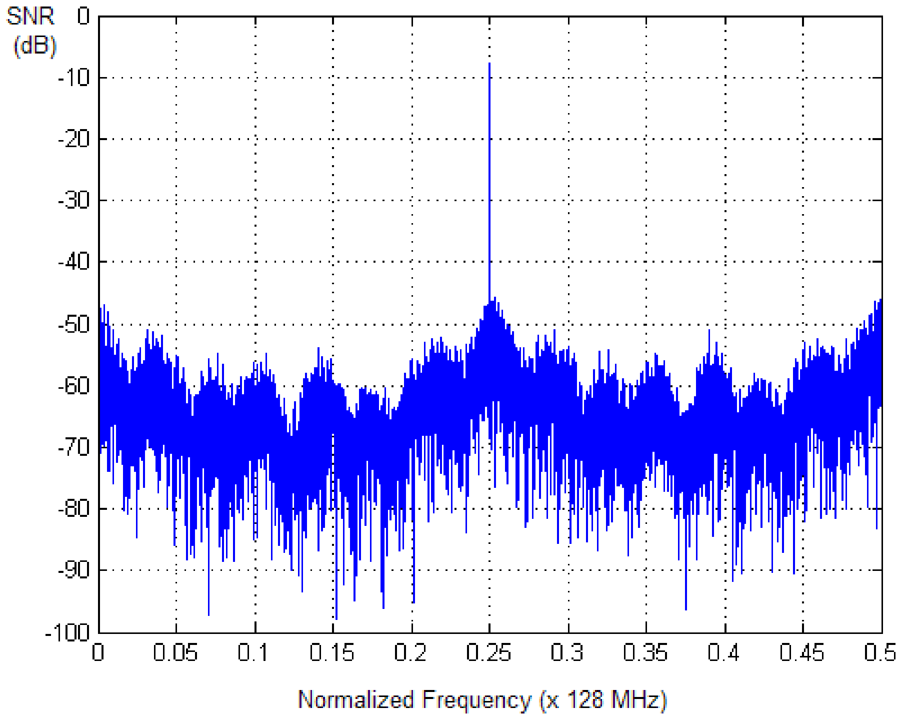


Figure 5.12. Result of the 3 bit binary digital outputs in MATLAB

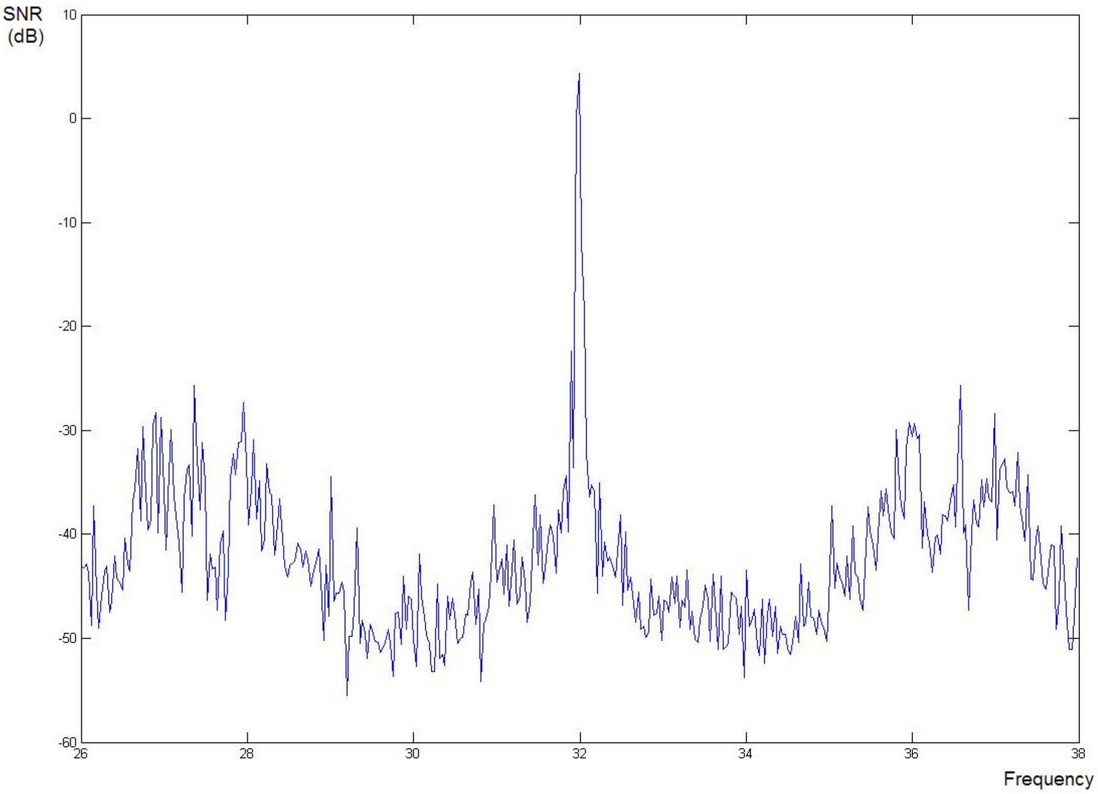
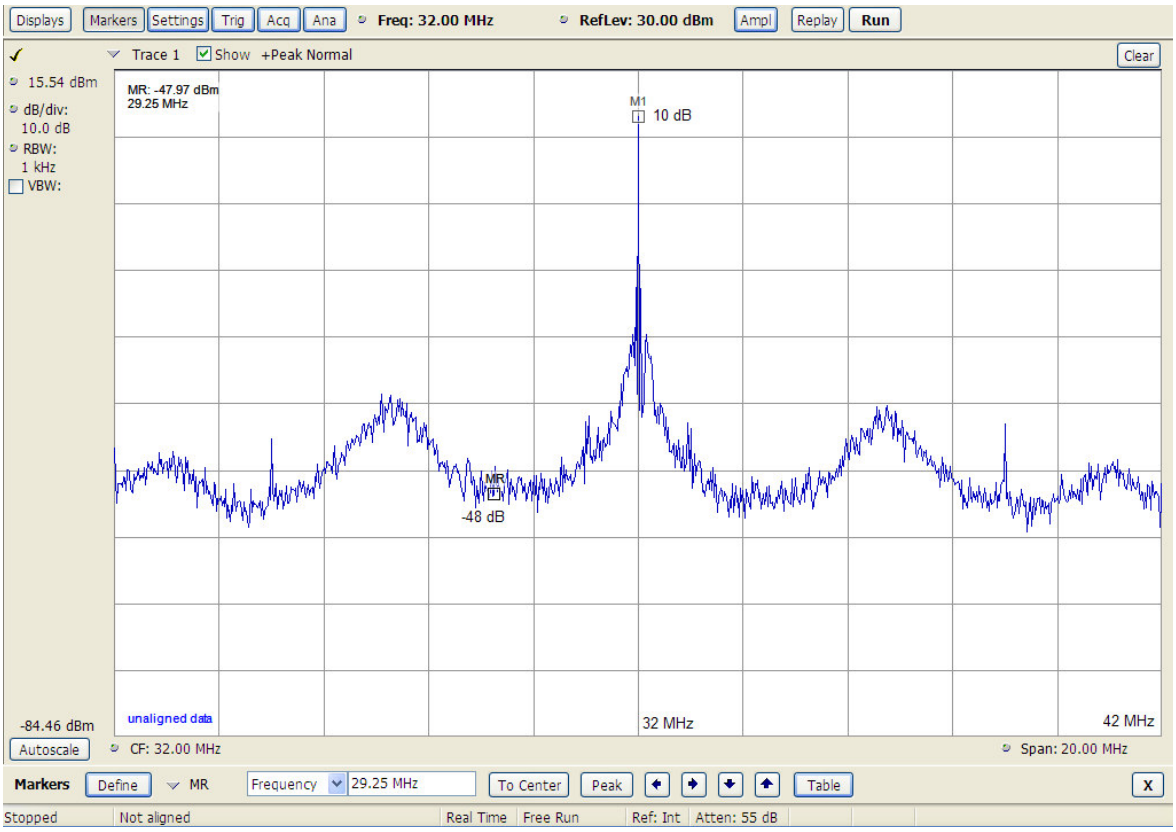


Figure 5.13. 1 bit analog output result measured in spectrum analyzer 1



Freq: 32.00 MHz

RefLev: 30.00 dBm

Trace 1 ☑ Show +Peak Normal

15.54 dBm

dB/div: 10.0 dB

RBW: 1 kHz

☐ VBW:

MR: -47.97 dBm
29.25 MHz

-84.46 dBm

CF: 32.00 MHz

Span: 20.00 MHz

MR Frequency 29.25 MHz

Stopped | Not aligned | Real Time | Free Run | Ref: Int | Atten: 55 dB

Figure 5.14. 1 bit analog output result measured in spectrum analzyer 2

5.3 Finding the Mistakes

5.3.1 Current Divider

First of all, current divider circuit is controlled. In Figure 5.15 bottom left side of the circuit is a current source circuit which generates 20 µA. This current flows through transistor M18. Therefore the current flowing through transistor M10 is 4 times of current flowing from transistor M18 because of the w ratios of the transistors (8/2). Hence the maximum current that could flow through the input of the circuit is ±80 µA but in the design current can be ±140 µA. Thus, circuit is tested with a pulse current source that flows ±140 µA each 7.8125 ns (128 MHZ) through input and the output is observed. The output is ±35 µA and has very very low latency that could be ignored, so the circuit is working although it has problems which can be seen in Figure 5.16. Also, current source block generates 30 µA instead of 20 µA. So instead of 80 µA, 120 µA current which is close to 140 µA is flowing through transistor M10. This circuit is operating correctly because of the low difference between the current flowing and the current that should flow. Hence, w of the transistor is lowered from 2 to 1 so the maximum current that could flow through transistor M10 will be 240 µA which will be enough to operate. New results can be seen in Figure 5.17 and it can be seen that there is no difference at the figures although the design is corrected.

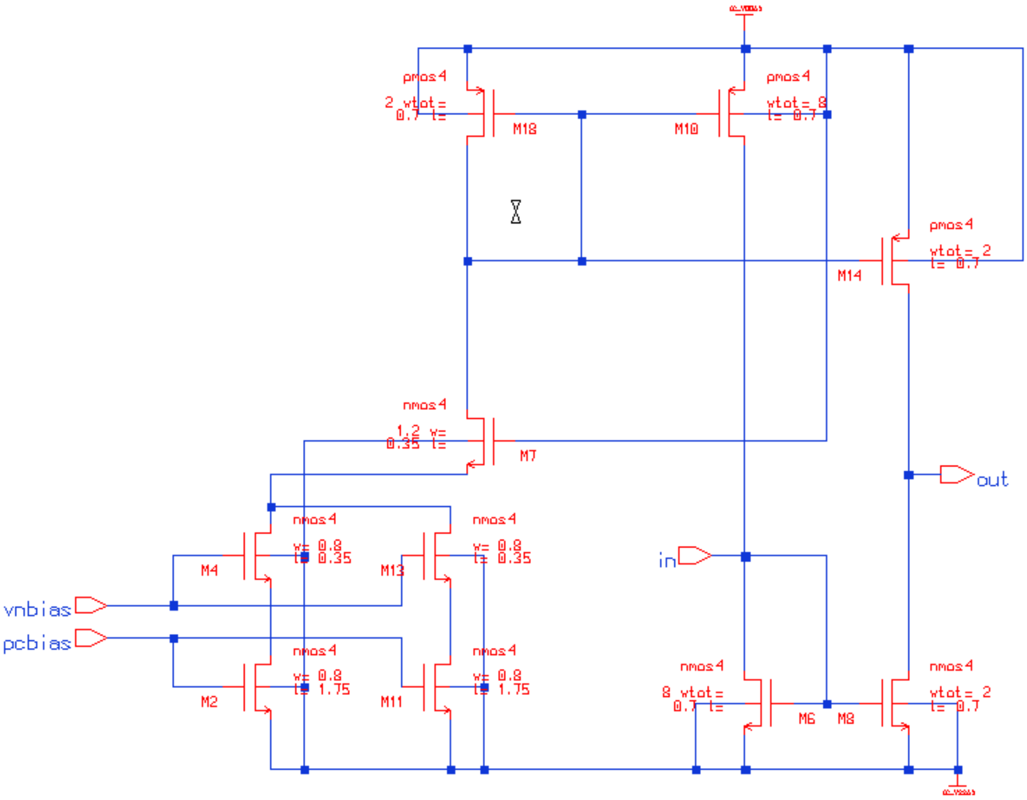


Figure 5.15. Current divider block

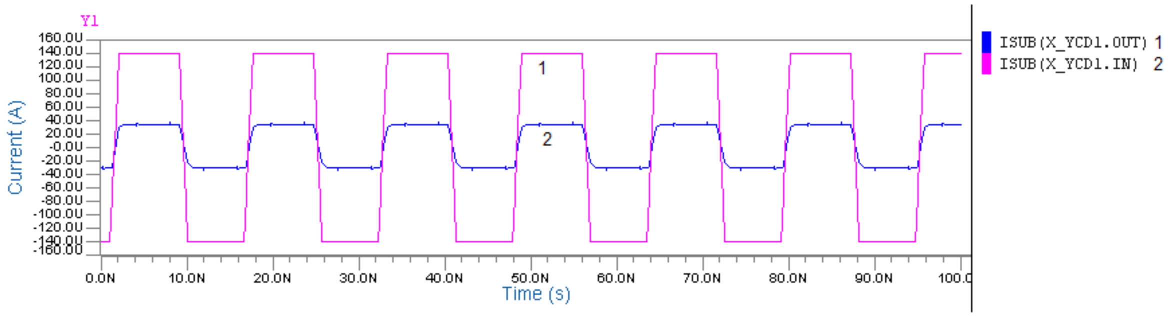


Figure 5.16. Result of the current divider with mistake

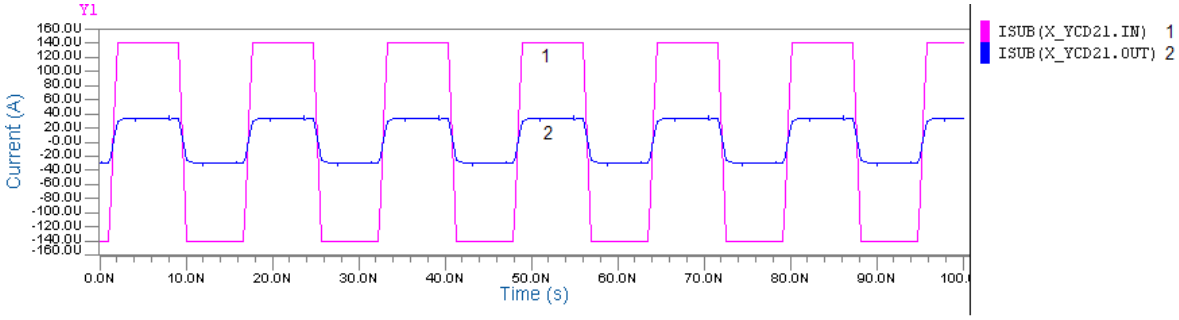


Figure 5.17. Result of the corrected current divider

5.3.2 New Quantizer Block

The quantizer block is investigated and the same problem is found on the circuitry. The input current value changes between ±350 µA and it is compared with ±300 µA. Therefore ±650 µA can flow through MOS transistors but it is designed that ±400 µA can flow through those transistors. Furthermore, maximum input current of the comparator circuit can be 350 µA, but 650 µA is forced into those inputs. The same current source used in current divider is also used in this block. The test of this comparison is shown in Figure 5.18. 350 µA differential sine signals at 128 MHz are applied to the inputs of the quantizer and the quantization outputs are observed and can be seen in Figure 5.19. VDATA values in the figure are the outputs of the quantizers and I value is the input. The quantization is not as good as expected. Hence, w of the transistors should change. The new circuitry can be seen in Figure 5.20. In the new circuitry, input currents are compared with ±240 µA instead of ±300 µA because it is thought that 300 µA is a bit high for comparison. Therefore, new table for outputs will be like in Table 5.4 and the test results of the new quantizer block are shown in Figure 5.21. The quantization results in the figure are better than old ones and also fit the results in the table. Also, lowering the currents reduced power dissipation to 11 mW.

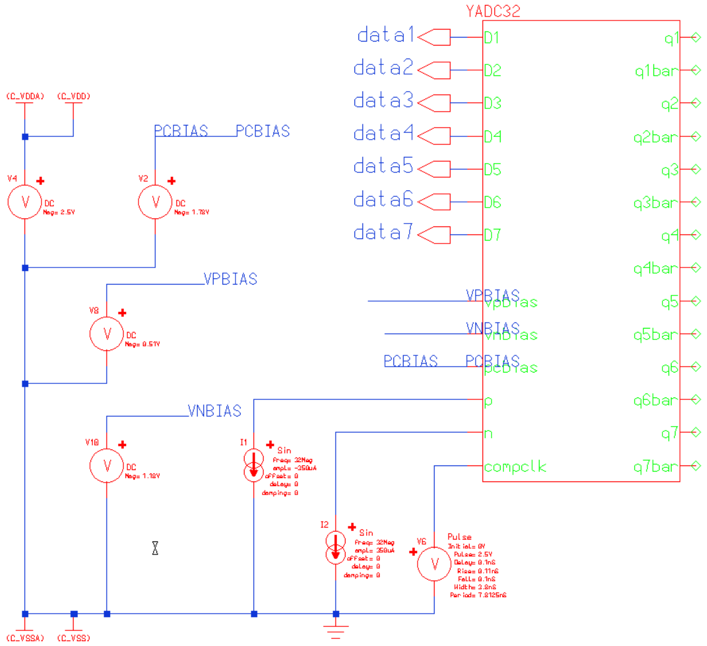


Figure 5.18. Test of the quantizer block

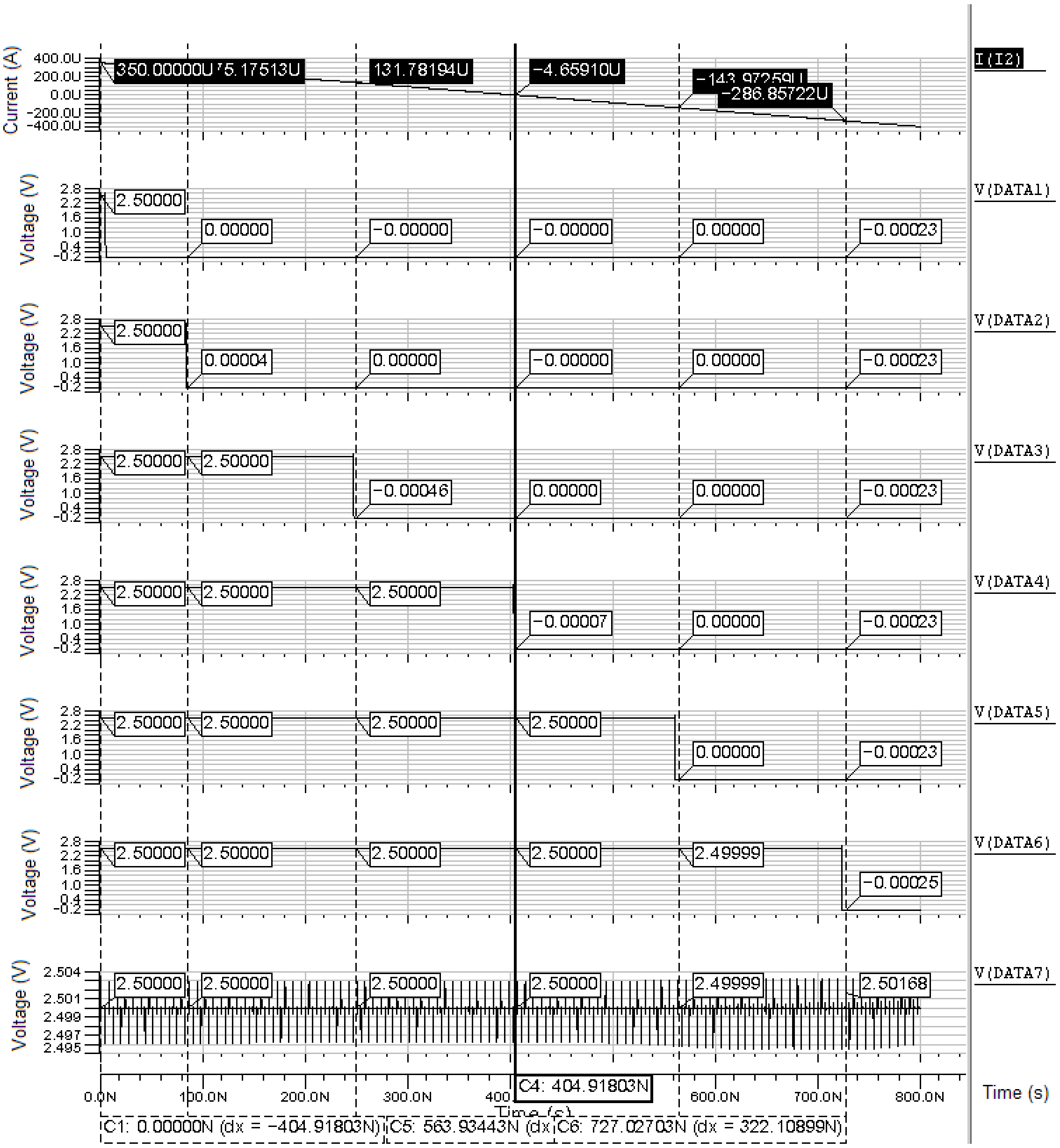


Figure 5.19. Results of the quantizer block

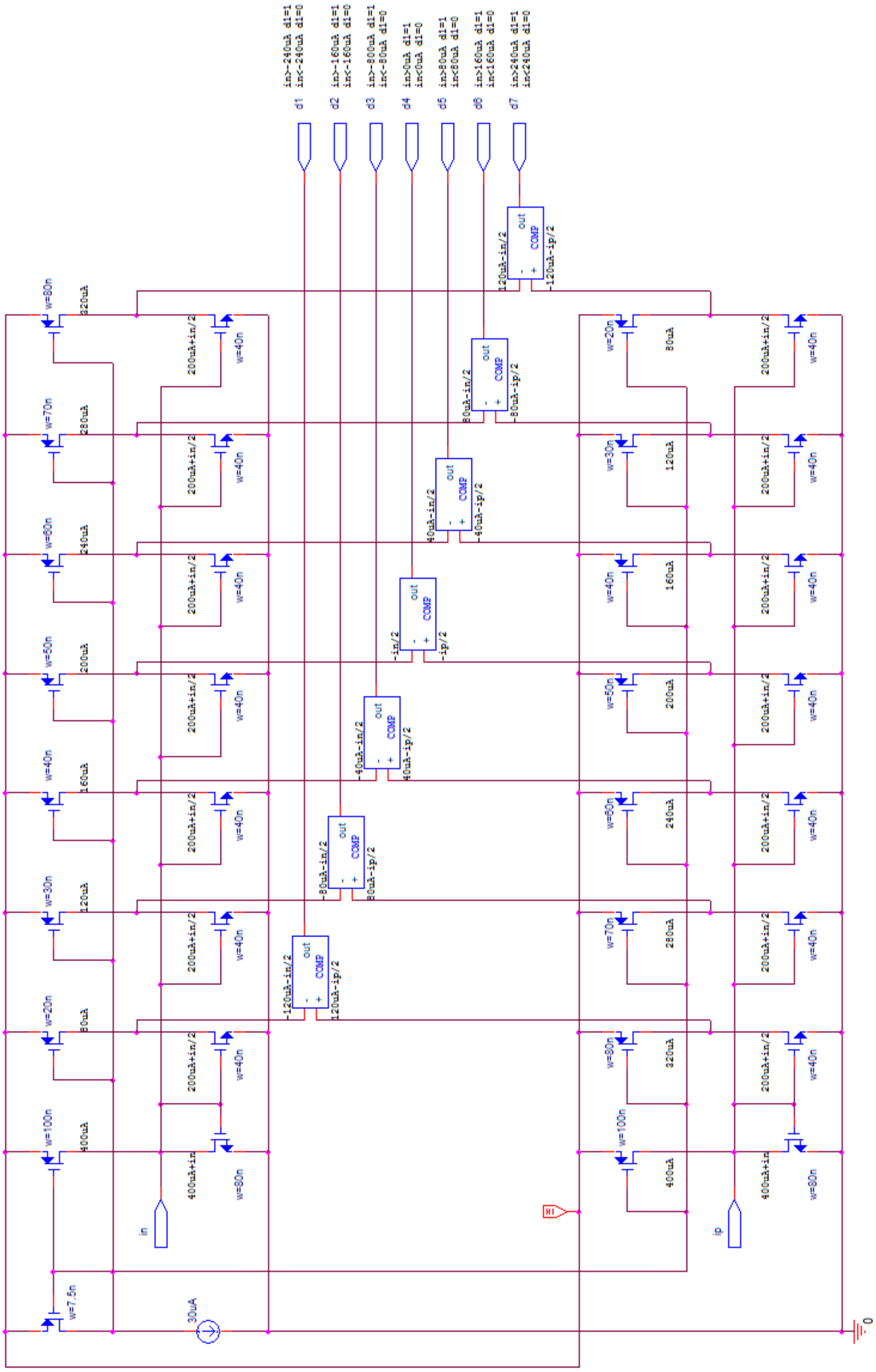


Figure 5.20. Changes in the quantizer block

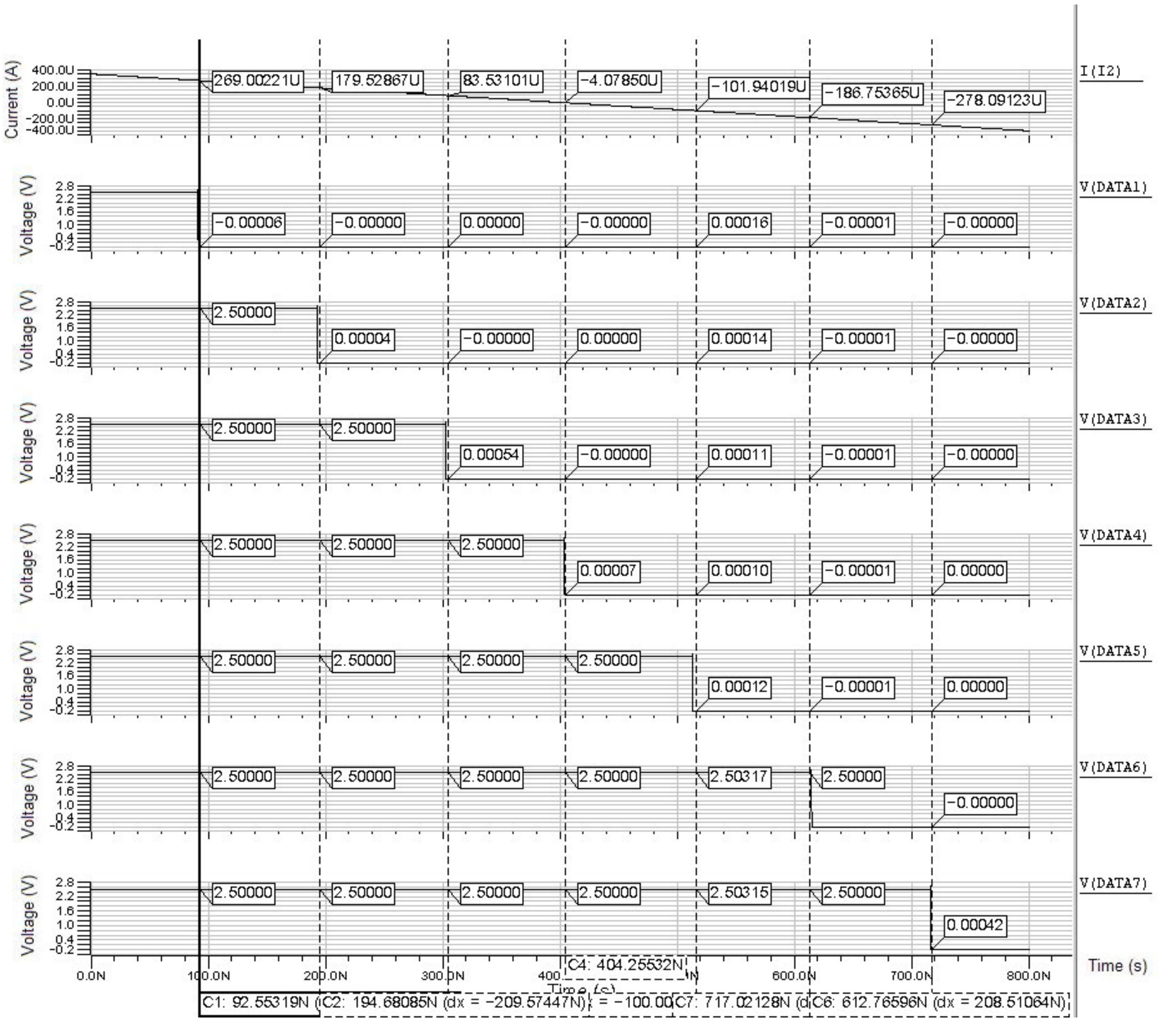


Figure 5.21. Test results of the new quantizer block

Table 5.4. New currents compared in the design

	D7	D6	D5	D4	D3	D2	D1	Y2	Y1	Y0
Less than -240 µA	0	0	0	0	0	0	0	0	0	0
-240 µA to -160 µA	0	0	0	0	0	0	1	0	0	1
-160 uA to -80 µA	0	0	0	0	0	1	1	0	1	0
-80 µA to 0 µA	0	0	0	0	1	1	1	0	1	1
0 µA to 80 µA	0	0	0	1	1	1	1	1	0	0
80 µA to 160 µA	0	0	1	1	1	1	1	1	0	1
160 µA to 240 µA	0	1	1	1	1	1	1	1	1	0
More than 240 µA	1	1	1	1	1	1	1	1	1	1

5.3.3 Control of the Output Blocks

Output block is added to the quantizer block to check the results. Figure 5.22 shows the analog output with the change of quantizer outputs. Figure 5.23 shows the analog output and 3 bit digital outputs. Analog and digital outputs are working correctly.

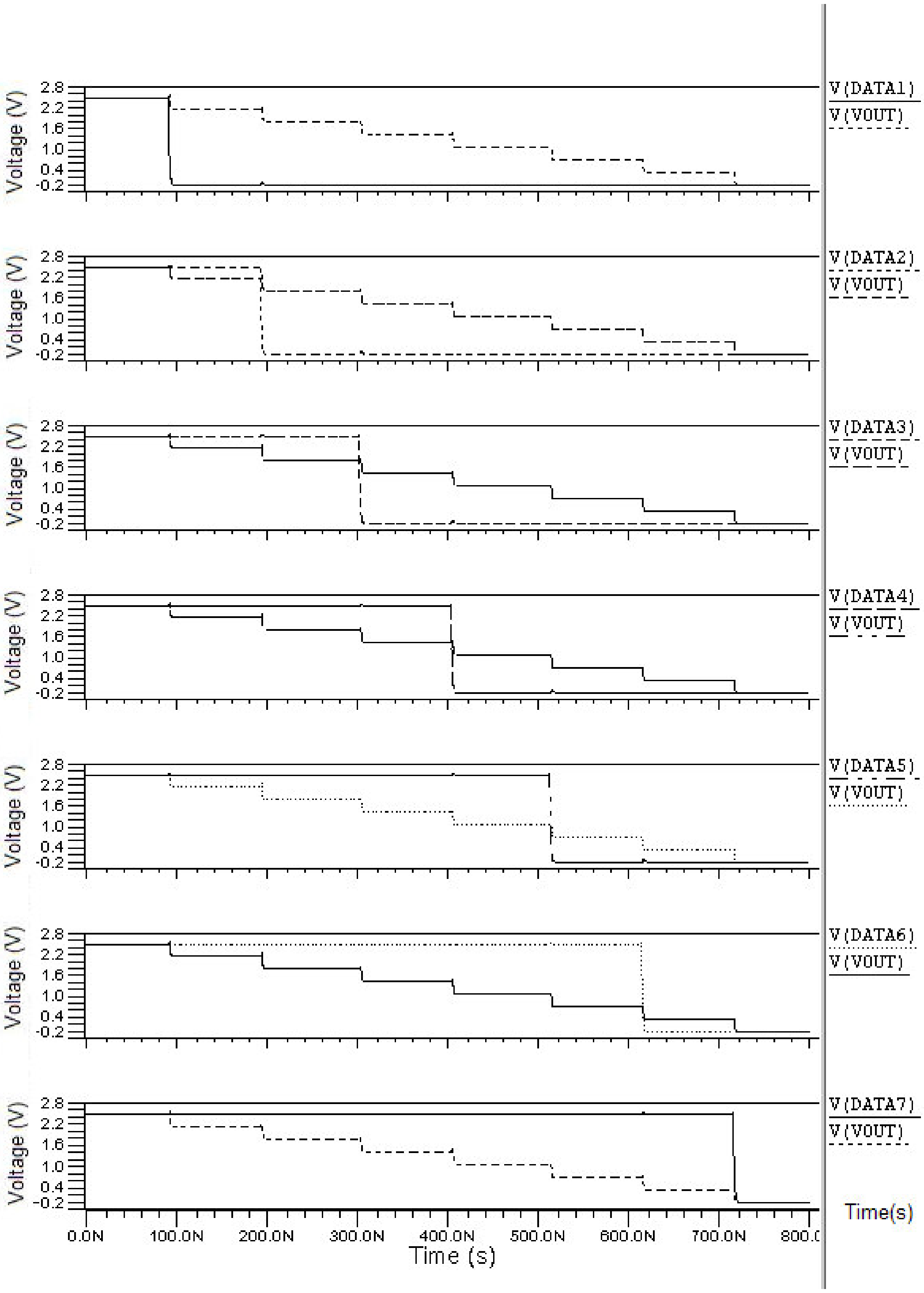


Figure 5.22. The analog output voltage with the change of the quantizer outputs.

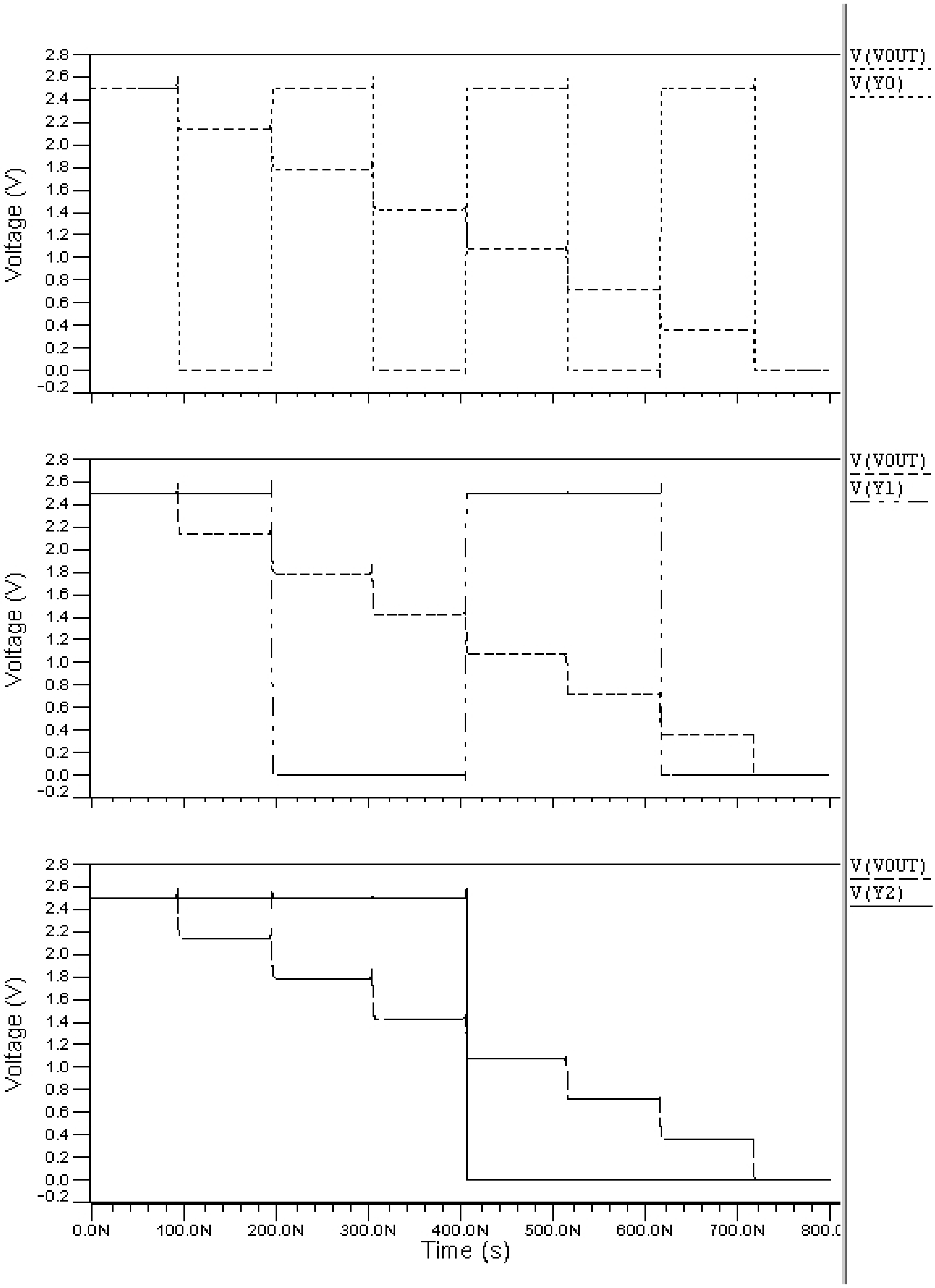


Figure 5.23. The analog output and the 3 bit digital outputs

5.3.4 New Sigma Delta Modulator after the Changes

After the changes made on the design, the new design is simulated in HSPICE and the new SNR is 72 dB as seen in Figure 5.24.

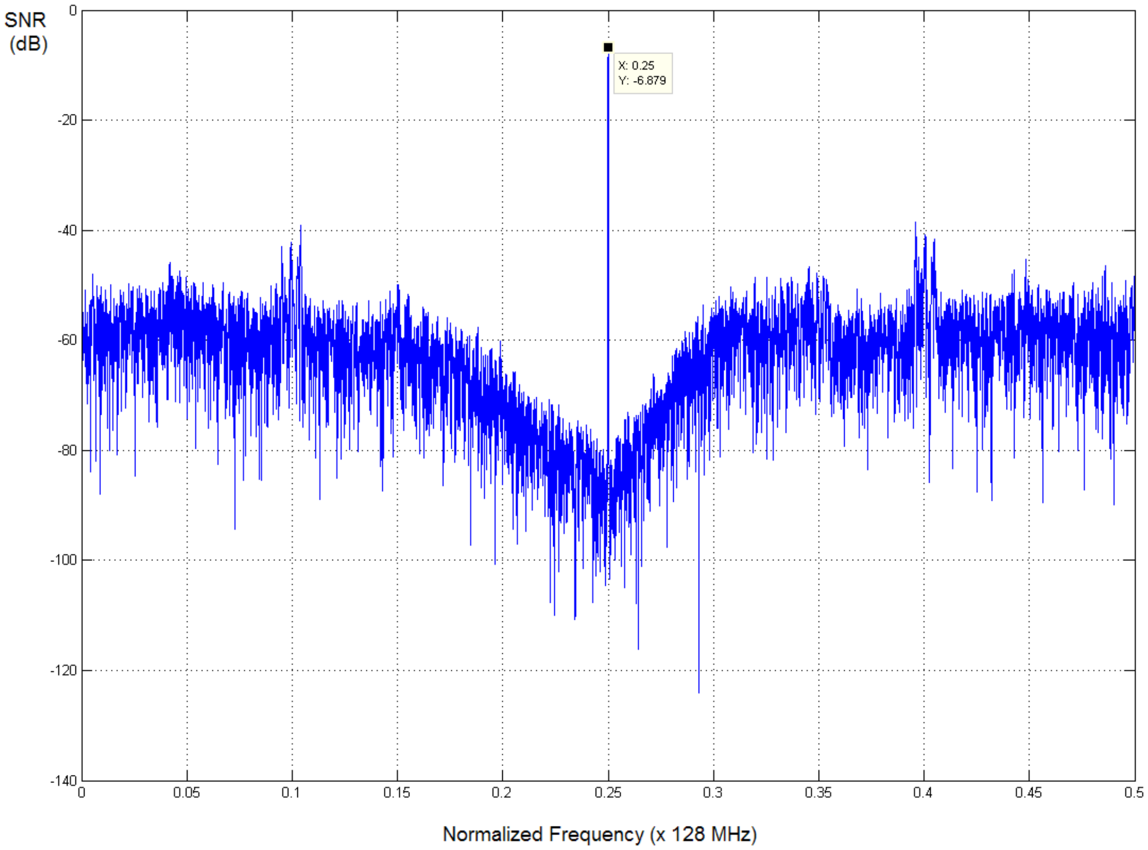


Figure 5.24. SNR of the final design

6. CONCLUSION AND FUTURE WORK

1 bit sigma delta modulator and conversion of 1 bit to 3 bit sigma delta converter is explained in this thesis. The designed 1 bit sigma delta converter could have 60 dB maximum when calculated and the test results achieved 46 dB SNR. Conversion to 3 bit should increase SNR by 6 dB for each additional bit, so the 3 bit design could have 72 dB SNR, but the produced design had 60 dB SNR maximum. This is probably caused by the mistakes done during design and the short circuit problem of all supply voltages. All the supply voltages are short circuited so filter can't be tuned. The PCB of the first design had some problems and SNR was lower than expected, and although the second design had problems, the SNR of the second design is increased by 14 dB due to the changes done in PCB and conversion to 3 bit. After the problems are solved SNR of the last design is 72 dB and SNR is increased by 12 dB additionally. If the design is compared with similars like in Table 6.1 it is very good compared to other designs. Comparisons are made by two ways.

figure of merit1 = 4kt x technology x operation frequency x SNR / power dissipation

figure of merit2 = 4kt x operation frequency x allowable bits / power dissipation

Table 6.1. Performance of the design compared to other sigma delta converters

Reference	Degree and Bit	Type	Tech.	V_{DD}	Sampling frequency	Operating frequency	dB (SNR)	Bits allowable	Power Dissipation	Figure of Merit 1	Figure of Merit 2
3 bit design	4/3	CT ΣΔ	0.35	2.5 V	128 MHz	32 MHz	60 dB	10	21 mW	53,33	1524
[3] Breems L. J. 2004	4/4	CT ΣΔ	0.18	1.8 V	32 MHz	10 MHz	67 dB	11	122 mW	3,30	90
[4] Kulchycki S. D. 2008	4/4	CT ΣΔ	0.18	1.2 V	240 Mhz	7.5 MHz	77 dB	12	89 mW	10,74	101
[5] Vink, J 1998	2/5	DT ΣΔ	0.35	3.3 V	54 MHz	5 MHz	43 dB	7	60 mW	0,41	58
[6] Breems, L.J 2004	2/4	CT ΣΔ	0.18	1.8 V	160 MHz	10 MHz	67 dB	11	123 mW	3,28	89
[7] Raf Schoofs 2007	3/1	CT ΣΔ	0.18	1.8 V	160 MHz	10 MHz	72 dB	12	7.5 mW	95,55	1600
[8] Di Giandomenico 2003	4/4	CT ΣΔ	0.13	1.5 V	300 MHz	15 MHz	67 dB	11	70 mW	6,24	235
[9] Mitteregger, G. 2006	3/4	CT ΣΔ	0.13	1.2 V	640 MHz	20 MHz	80 dB	13	20 mW	130,00	1300
Design after corrections	4/3	CT ΣΔ	0.35	2.5 V	128 MHz	32 MHz	72 dB	12	23.3 mW	191.4	1647.5

When 1 bit and 3 bit designs are compared, SNR is increased only 4 dB instead of 12 dB according to HSPICE simulations. When Figure 6.1 and 6.2 are compared, noise shaping of the 3 bit design is not as sharp as the noise shaping of 1 bit design. The lowest node in Figure 6.1 is -120 dB but the lowest node in Figure 6.2 is -110 dB. As future work, improvements can be done by changing the feedback coefficients and using cascoded current mirrors during copy operation at the inputs of the comparators.

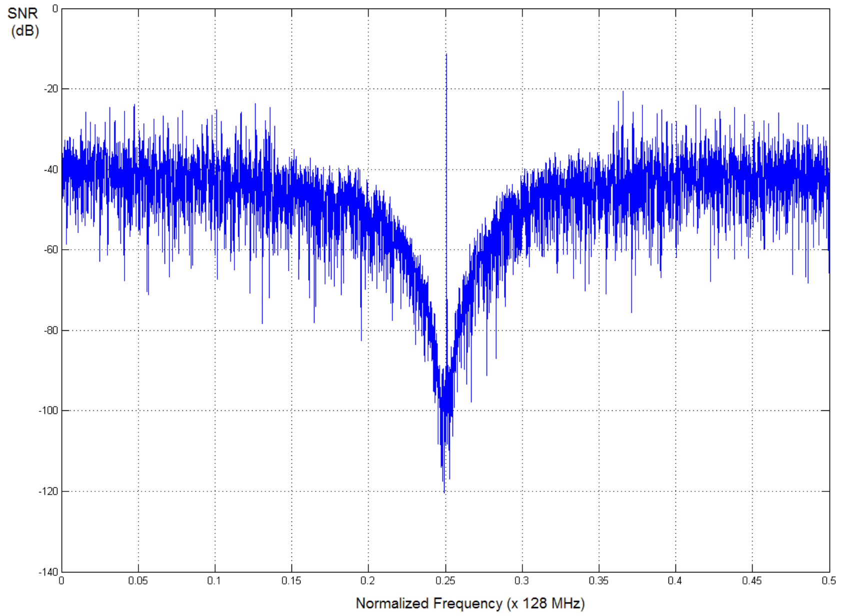


Figure 6.1. SNR of the 1 bit design

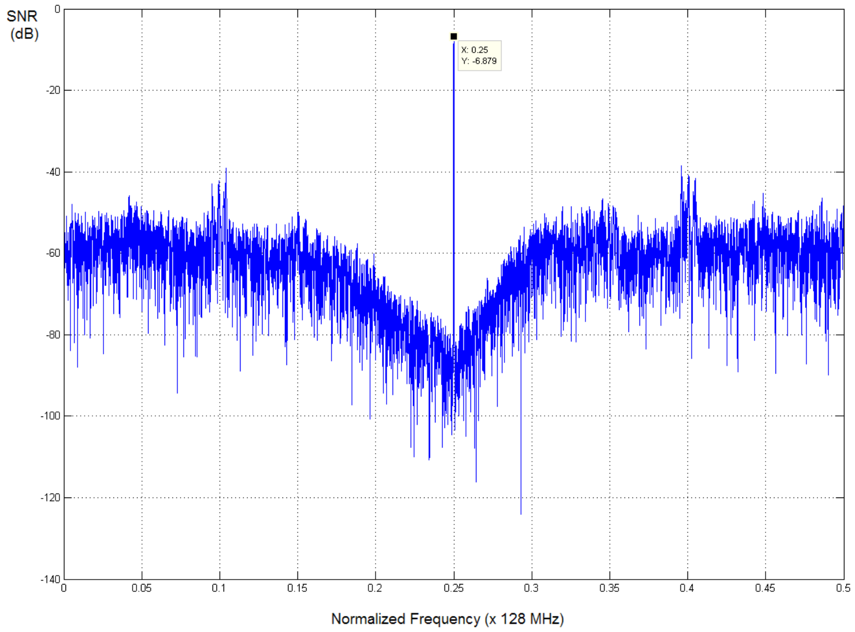


Figure 6.2. SNR of the 3 bit design

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