DESIGN OF NEGATIVE GROUP DELAY CIRCUITS WITH MOS-ONLY APPLICATIONS

by

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ABSTRACT

DESIGN OF NEGATIVE GROUP DELAY CIRCUITS WITH MOS-ONLY APPLICATIONS

Physical size, design flexibility, noise, signal attenuation, and distortion are a few of the issues that arise in the design of analog electrical circuits. Additionally, a major difficulty with electronic systems is their time delay, particularly when high order filters are present. The literature, especially in the last 10 years, provides a variety of applications for negative group delay (NGD) implemented with electronic circuits as well as mathematical models to address that issue. The signal amplification and the group delay linearity are the major design parameters for the NGD that is employed to achieve low distortion at the output. A flexible NGD design and the operation range of the NGD circuit is additionally required to expand the application area.

In this thesis, active NGD circuits based on MOSFETs to decrease the physical size of the design using Current Feedback Operational Amplifier (CFOA), Operational Transconductance Amplifier (OTA-C) based voltage mode and transimpedance-mode NGD circuits have been designed. Moreover, a mathematical approach to design such analog electronic circuits have been demonstrated. The relation of the NGD frequency operation range and NGD value is presented and example designs are demonstrated using well-defined parameters. Along with the calculations and simulation results, an experimental verification is presented in a lab setting. The findings demonstrate that a time advance is possible in a specific frequency range without a direct dependence on the system gain value.

ÖZET

MOSFET UYGULAMALARI İLE NEGATİF GRUP GECİKMESİ DEVRE TASARIMLARI

Fiziksel boyut, tasarım esnekliği, gürültü, zayıflama ve bozulma, analog elektrik devrelerinin tasarımında ortaya çıkan sorunlardan birkaçıdır. Ek olarak, elektronik sistemlerle ilgili büyük bir zorluk, özellikle yüksek dereceli filtreler mevcut olduğunda, ortaya çıkan zaman gecikmeleridir. Literatür, özellikle son 10 yılda, elektronik devrelere dayalı negatif grup gecikmesi (NGD) için çeşitli elektronik uygulamalar ve bu konuyu ele almak için matematiksel modeller sunmaktadır. Kuvvetlendirme ve grup gecikme doğrusallığı açısından, kullanılan negatif grup gecikmesinin önceki sistemi bozmaması önemlidir. Uygulama alanını genişletmek için ayrıca esnek bir NGD tasarımı ve NGD devresinin uygun çalışma aralığı gereklidir.

Bu tezde, Akım Geri Beslemeli İşlemsel Yükseltici (CFOA), İşlemsel İletkenlik Yükseltici (OTA-C) tabanlı transempedans modlu NGD devresini kullanarak, tasarımın fiziksel boyutunu küçültmek için MOSFET'lere dayalı aktif NGD devreler tasarlandı. Buna ek olarak böyle bir analog elektronik devre tasarlamak için matematiksel bir yaklaşım sunuldu. NGD frekans çalışma aralığı ve NGD değeri arasındaki ilişki sunularak ve iyi tanımlanmış parametreler ile tasarımlar elde edildi. Hesaplamalar ve simülasyon sonuçlarıyla birlikte, laboratuvar ortamında deneysel bir doğrulama yapıldı. Bulgular, sistem kazanç değerine doğrudan bağımlı olmaksızın belirli bir frekans aralığında bir zaman ilerlemesinin sunulan devreler ile mümkün olduğunu göstermektedir.

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C_{ox}	The gate oxide capacitance of a MOSFET per unit area
C_{gd}	Gate-to-drain capacitance
C_{gs}	Gate-to-source capacitance
f	Frequency
H	Transfer Function
T_{ox}	The thickness of gate-oxide
V_{THON}	Threshold voltage of NMOS transistor for zero substrate bias
V_{THOP}	Threshold voltage of PMOS transistor for zero substrate bias
V_{ov}	Over-drive voltage of the MOSFET
α	Scaling Factor
β	Resistance Scaling Factor
ϕ	Phase (degree)
Θ	Angle
μ_n	Electron mobility
μ_p	Hole mobility
τ_g	Group Delay
τ_{ngd}	Negative Group Delay
ω	Angular Frequency
$\omega_{zero-crossing}$	Negative Group Delay Zero-Crossing Angular Frequency

LIST OF ACRONYMS/ABBREVIATIONS

BPF	Band Pass Filter
CFOA	Current Feedback Operational Amplifier
GD	Group Delay
IC	Integrated Circuit
F.O.M.	Figure of Merit
LPF	Low Pass Filter
LTI	Linear Time Invariant
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NGD	Negative Group Delay
NGDC	Negative Group Delay Circuit
NMOS	N-Channel Metal Oxide Semiconductor
OA	Operational Amplifier
OTA	Operational Transconductance Amplifier
PMOS	P-Channel Metal Oxide Semiconductor
RMSE	Root Mean Square Error

1. INTRODUCTION

1.1. Motivation

I have worked with physically long sensor arrays in the industry. There are two important points of working with such sensor arrays: the first one is to capture the real-time aspect of the data monitoring and the second part is to synchronize the sensor array outputs. The time delay of the system may result an output which is misleading if the time delay is high, correlated with the length of the array. There are studies statistically to predict those output values to eliminate such time delays for real-time applications. However, in order to calculate the parameters of such a predictor, an adaptive approach is typically required. The majority of the parameters relate to a particular application for a particular input type. In this work, a time advancement method is applied by merely relying on the frequency range of the input signal resulting analog negative group delays. Additionally, an adaptation can be made by adding a time delay to the leading input in order to solve the problem of time delay between two or more inputs to a system. However, that results in an increase in the system's overall delay. The delayed inputs can be adjusted to the leading input using a negative group delay application.

1.2. Negative Group Delay

In signal processing, the phase delay is delay of the phase for a specific single tone sinusoidal with basic one frequency component. It denotes the phase shift of the output signal compared to the input signal caused due to the transfer function of the system. In addition to that, the group delay is the time delay of the amplitude envelope. When investigating a signal having numerous frequency components rather than a single tone, it is crucial to pay attention to the group delay of the system. The negative derivative of the phase delay for each frequency component serves as the group delay's mathematical definition.

Negative group delay (NGD) is an interesting physical phenomenon and can be used for signal anticipation. In NGD circuits the output visually appears time advanced compared to input thus signal prediction is possible but this effect is not in contradiction with causality principle. In fact the key point is that the input signal should be band limited which means instantaneous jumps in the input signal is not allowed and derivatives of the input signal remain bounded. In other words in these circuits NGD occurs in general in a specific frequency band. Although NGD can be observed also in passive circuits active elements are needed if the output signal is to be used to drive other circuits or systems. As a summary the phase delay of a system is the phase shift of a single sinusoidal input to the output of that system. The group delay denotes the time delay of the envelope of the signal.

The physical explanation comes from the wave propagation in a medium [1]. In a dispersive medium the response of the system depends on the frequency of the incoming signal's frequency [2]. The physical aspects are described in [1, 3–5]. It is shown that the medium of the wave propagating can change the frequency components of the incoming wave so that the envelope of the wave is advanced in time [1, 5].

In this thesis, the electronic system aspect of the NGD is investigated. Therefore, first the studies such that [1,4,6–11] which focused on NGD for an electronic system, are discussed further in this chapter. The electronic system design considerations include bandwidth, amplification or attenuation, noise, cut-off frequency as well as time domain characteristics of the system where the time delay is a part of it. For the real time systems, reducing the time delay of the system becomes an important problem to be solved to improve the performance of the system. Especially when the system takes multiple sensor inputs to process. In addition to that some systems use the group delay of the system as the input to process. For instance, in the study [12] the sensor uses the phase difference of two signal. The NGD in such system can handle such delay problems while paying regard to the problems that mentioned above, [6]. The negative group delay means a negative time delay for the amplitude envelope of the signal. The negative group delay is discussed in [6] as a time advancement phenomenon in a system where the input is a band-limited pulse.

In an LTI system, with the input $x(t)$ and the output $y(t)$, the transfer function of the system is given as

$$H(j\omega) = Y(j\omega)/X(j\omega) \tag{1.1}$$

where $Y(jw)$ and $X(jw)$ are the output and the input signal's Laplace transforms, with $(s \rightarrow j\omega)$, respectively. For the given system transfer function the phase shift is defined as

$$\phi = \arg(H(j\omega)) = \arg(Y) - \arg(X) \tag{1.2}$$

where ϕ is the phase shift of the system. The group delay is defined as

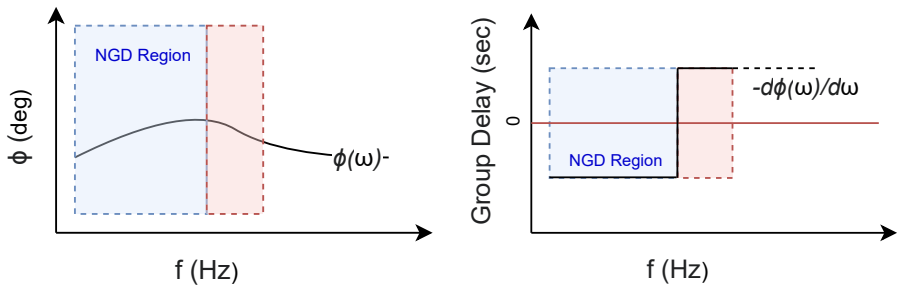
$$\tau_g(\omega) = -\frac{d\phi(\omega)}{d\omega} \tag{1.3}$$

where $\tau_g(\omega)$ denotes the group delay response of the system with respect to angular frequency.

The equation (1.3) shows that a monotone increasing phase delay with respect to the frequency results a negative group delay. However, that also means an unstable system. Therefore, a system phase response as in Figure 1.1, where the phase delay increases to a certain level and then decreases, can be an example phase response of a stable NGD system. In such a system group delay is negative until the phase delay decreases with frequency.

1.2.1. General Mathematical Model

For a circuit the phase and group delay properties can directly be derived from its transfer function. In this section, the first and second order transfer functions are investigated in terms of group delay and it is shown how it is effected by the coefficients of the transfer function.



(a) (b)

Figure 1.1. A phase response example of a basic stable NGD.

The general first order transfer function $H_1(s)$ is given as

$$\begin{aligned} H_1(s) &= \frac{b_0 + b_1 s}{a_0 + a_1 s} \\ &= \frac{b_0}{a_0} \frac{1 + \dfrac{b_1 s}{b_0}}{1 + \dfrac{a_1 s}{a_0}} \\ &= \frac{b_0}{a_0} \frac{1 + \tau_z s}{1 + \tau_p s} \\ &= K \frac{1 + \tau_z s}{1 + \tau_p s} \end{aligned} \tag{1.4}$$

where $\tau_z = b_1/b_0$, $\tau_p = a_1/a_0$ are respectively zero and pole time constants and $K = b_0/a_0$. Here K is the gain of the circuit and a_i, b_i are positive real numbers. Obviously, there are two parameters affecting the phase and one additional parameter defining the gain.

For the first order transfer functions, using (1.3) gives group delay as

$$\tau_{g1} = -\frac{d \arctan(\dfrac{b_1 \omega}{b_0})}{d\omega} + \frac{d \arctan(\dfrac{a_1 \omega}{a_0})}{d\omega}. \tag{1.5}$$

Rearranging this expression gives group delay as

$$\tau_{g1} = -\frac{b_1 b_0}{b_1^2 \omega^2 + b_0^2} + \frac{a_1 a_0}{a_1^2 \omega^2 + a_0^2}. \tag{1.6}$$

In this expression, there are 4 possibilities for four parameters a_0, a_1, b_0 and b_1, when the parameters a_0 and b_0 are selected equal:

- $a_1 > b_1$ and a_1 and b_1 are much larger (1000 times) than $a_0 = b_0$
- $a_1 < b_1$ and a_1 and b_1 are much smaller (1/1000 times) than $a_0 = b_0$
- $a_1 > b_1$ and a_1 and b_1 are much smaller (1/1000 times) than $a_0 = b_0$
- $a_1 < b_1$ and a_1 and b_1 are much larger (1000 times) than $a_0 = b_0$

Thus, the four possible parameter choice provides 6 group delay models. The 3 of them corresponds to a valid NGD operation as shown in Figure 1.2.

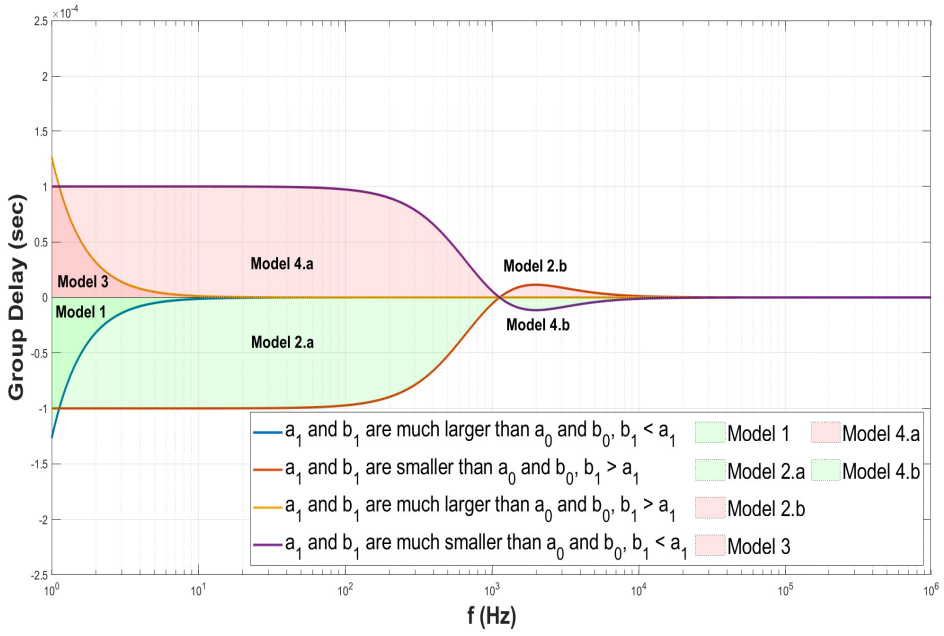


Figure 1.2. Regions illustrating the group delays for different selection of parameters, $a_0 = b_0$.

In Figure 1.2, the frequency and corresponding group delay values are shown depending on a_n and b_n coefficients. An actual circuit can be designed by a proper selection of passive component values which will result the desired a_n and b_n values. They are selected for the visualization of the Models for the NGD in this section.

1.2.1.1. Model 1 NGD Operation. The Model 1 NGD structure is obtained by selecting $a_1 > b_1$ when a_1 and b_1 are substantially greater than $a_0 = b_0$. The downside of that

concept is that the group delay varies significantly with frequency. As a result, there may be undesirable distortion at the output. The same operation is achieved when the a_1 and b_1 coefficients are selected equal and $b_0 > a_0$ and both b_0 and a_0 are much smaller than $a_1 = b_1$. Because of that the symmetrical parameter selection is not included in the Figure 1.2.

1.2.1.2. Model 2 NGD Operation. The Model 2 NGD structure is obtained by selecting $a_1 < b_1$ when a_1 and b_1 are substantially smaller than $a_0 = b_0$. In contrast to Model 1, Model 2 achieves a flat NGD until a frequency value is reached. Model 2.b in Figure 1.2, shows how the group delay goes from negative to positive at particular frequency setting. Furthermore, with Model 4.b, a NGD can be achieved in a frequency operation range. However, similar to Model 1, the value of the group delay varies with frequency. The same operation is achieved when the a_1 and b_1 are selected equal and $a_0 > b_0$ and both b_0 and a_0 are much larger than $a_1 = b_1$. Because of that the symmetrical parameter selection is not included in the Figure 1.2.

In general the Model 4.b is used for high frequency NGD applications such as in the studies [8,13–15] and the Model 1, in the study [6]. NGD value, NGD adaptability, NGD frequency range applicability to the input signal, and system amplification are all essential NGD features. In that manner, in this study Model 2 is used for the NGD operation with constant gain in the NGD operation range. The Model 2 is used in the studies [1, 10, 16–20].

Similarly the second order transfer function is investigated. The general second order transfer function $H_2(s)$ is given as

$$H_2(s) = \frac{b_0 + b_1 s + b_2 s^2}{a_0 + a_1 s + a_2 s^2}. \tag{1.7}$$

For the second order transfer functions, using (1.3) gives the group delay as

$$\tau_{g2} = -\frac{d \arctan(\frac{b_1 \omega}{b_0 - b_2 \omega^2})}{d\omega} + \frac{d \arctan(\frac{a_1 \omega}{a_0 - a_2 \omega^2})}{d\omega}. \tag{1.8}$$

Rearranging this expression, the group delay can be written as

$$\tau_{g2} = -\frac{b_1(b_0 + b_2\omega^2)}{b_1^2\omega^2 + (b_0 - b_2\omega^2)^2} + \frac{a_1(a_0 + a_2\omega^2)}{a_1^2\omega^2 + (a_0 - a_2\omega^2)^2}. \tag{1.9}$$

First selecting $a_2 = b_2 = a_0 = b_0$, there are four possibilities for selecting a_1 and b_1, which results same group delay models with the first order transfer function group delay models, shown in Figure 1.3.

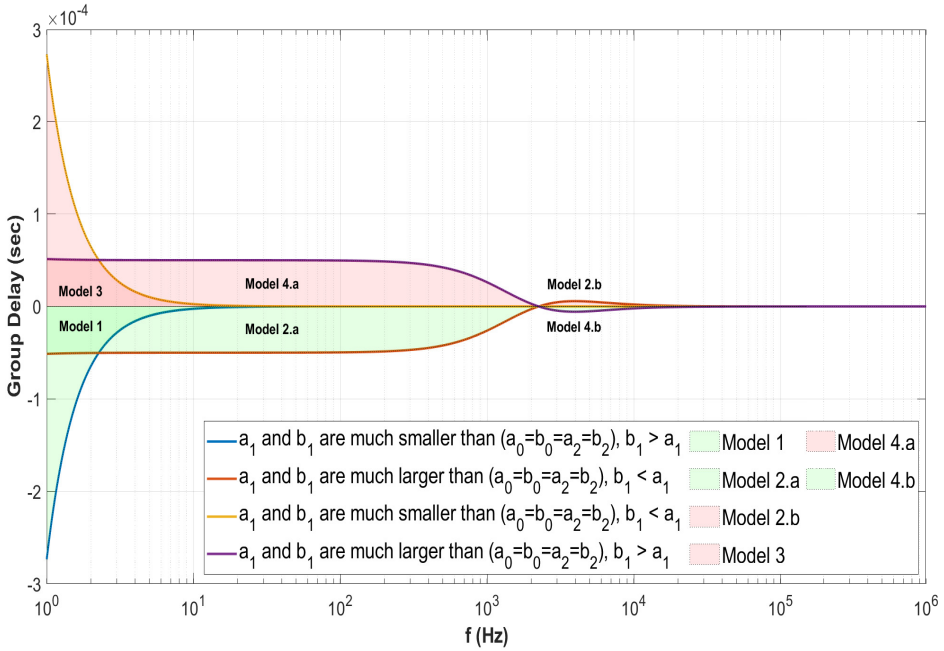


Figure 1.3. Regions illustrating the group delays for the second order transfer function, $a_0 = b_0 = a_2 = b_2$.

In Figure 1.3, it is shown that with following parameter selections similar NGD regions with the first order transfer function is possible:

- $b_1 > a_1$ and a_1 and b_1 are much smaller (1/1000 times) than $a_0 = b_0 = a_2 = b_2$
- $a_1 > b_1$ and a_1 and b_1 are much larger (1000 times) than $a_0 = b_0 = a_2 = b_2$
- $a_1 > b_1$ and a_1 and b_1 are much smaller (1/1000 times) than $a_0 = b_0 = a_2 = b_2$
- $b_1 > a_1$ and a_1 and b_1 are much larger (1000 times) than $a_0 = b_0 = a_2 = b_2$

Moreover, for the NGD models achieved from these possibilities, to see the effect of the parameters a_0 and b_0 on NGD model 1 and 2, a_2 and b_2 kept equal and 2 NGD models are categorized as follows:

- $a_0 > b_0$ and a_1 & b_1 are much smaller (1/1000 times) than $a_2 = b_2$, $b_1 > a_1$
- $a_0 > b_0$ and a_1 & b_1 are much larger (1000 times) than $a_2 = b_2$, $b_1 < a_1$
- $b_0 > a_0$ and a_1 & b_1 are much smaller (1/1000 times) than $a_2 = b_2$, $b_1 > a_1$
- $b_0 > a_0$ and a_1 & b_1 are much larger (1000 times) than $a_2 = b_2$, $b_1 < a_1$

Figure 1.4 illustrates that different selection of the parameters a_0 and b_0 changes the original NGD Model 1 and Model 2.a at low frequencies. As mentioned previously in the first order NGD models, in Model 1 the group delay is negative. However, it varies significantly with frequency. In the second order transfer function Model 2.a.1 and Model 2.a.2, although NGD varies with frequency, that effect is small compared to the first model. The next section lists the transfer functions and circuit types that have been found in the literature.

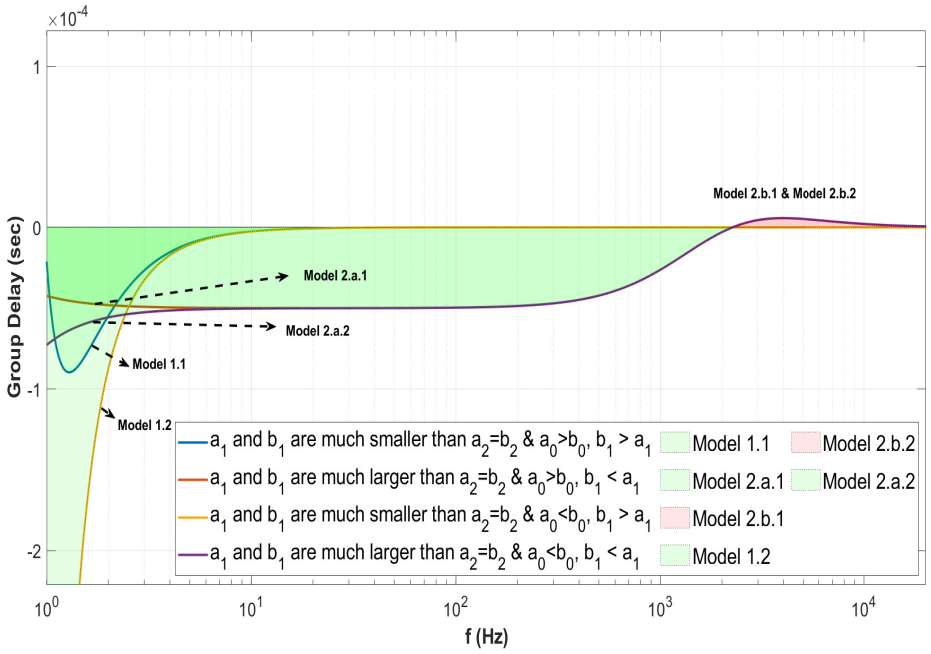


Figure 1.4. Regions illustrating the NGD for the second order transfer function for different a_0 and b_0, $a_2 = b_2$.

1.3. Literature Review

In this section, some important NGD circuits appeared in the literature are investigated with the proposed circuits from several studies. An interesting electronic circuit based NGD system is introduced in [1]. There are several NGD studies with passive RC, RLC Network [6, 8]; with OA based differentiator and active RC, RLC filters [1, 2, 4, 7, 21] or with Taylor type prediction using the mathematical model of NGD based circuit [17, 18]. A brief collection of proposed topologies in the literature is seen in the Table 1.1. In the studies [1, 7, 21] the NGD value is obtained more easily compared to other studies because of the number of components that are used for NGD parameters. In addition to that the NGD value is not independent from the system's gain value. In that sense, the study [18] is more flexible to select different NGD values and different gain values where the system used has the same topology with [1, 7, 21]. The studies [2, 4, 8] can be put into the category same with the study [18]. However, an additional inductance is used as a passive component.

Table 1.1. The NGD Circuit Topologies in the Literature.

Reference	**Circuit Topology**	**Transfer Function**
[1, 7, 21]	OA Based Differentiator	$b_1 s + b_0$
[2, 4]	OA Based Active RLC Filter	$\frac{b_2 s^2 + b_1 s + b_0}{a_2 s^2 + a_1 s + a_0}, a_1 = b_1, a_0 = b_0$
[6, 19]	Passive RC Filter	$\frac{b_1 s + b_0}{a_1 s + a_0}, a_1 = b_1, a_0 > b_0$
[8]	Passive RLC Network	$\frac{(a_1 b_0 + 1) b_1 s + a_1}{b_1 a_1 s}$
[10]	Cascaded CFOA Based Active Filter	$\frac{b_2 s^2 + b_1 s + b_0}{a_1 s + a_0}$
[11]	Function Based	$\frac{b_2 s^2 + b_1 s + b_0}{a_2 s^2 + a_1 s + a_0}$
[17]	BJT Based Delay Summation	$a_0 + a_1 . e^{(-s t_d)} + a_2 . e^{(-2 s t_d)}$
[18]	OA Based Active RC Filter	$\frac{b_1 s + b_0}{a_1 s + a_0}$

The study [17] uses delay elements to estimate the input with an additional transmission line. In the study [10], a cascaded CFOA based NGD is introduced. The design procedure is simplified for the low frequency range. The given circuit in the [10] is tested with a mathematical pulse function. The test methodology used in this study is introduced in the next section.

There is one CFOA based active NGD circuit which introduces a cascadable NGD structure [10]. The NGD values of the given studies varies from ns to μs range. In Chapter 2, new CFOA based active NGDCs are introduced.

1.4. Test Methodology

In this section the test methodology used in the thesis is presented. To test the circuits, a LPF with Sallen-Key topology is used to reshape a pulse signal. After that the outputs of the LPF and NGD circuit is given to data monitoring instrument to investigate the group delay, as shown in Figure 1.5.

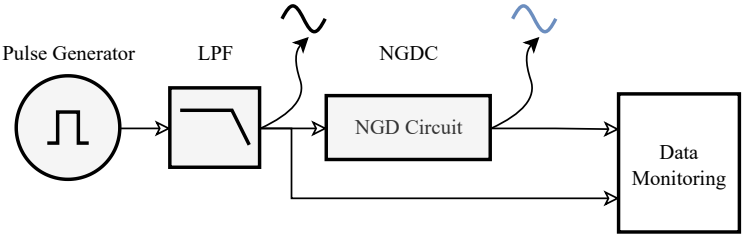


Figure 1.5. Test System Block Diagram.

The time advanced signal obtained from the output terminal of NGD circuit is not an exact replica of the input. Therefore, to investigate the signal error a similar method is used as in the study [18] and [20]. The input signal is reconstructed as adding a positive delay to the output of NGDC that is equal to the magnitude of the NGD value.

The signals illustrated in Figure 1.5 are shown qualitatively in time domain in Figure 1.6. The red one in the Figure 1.6, corresponds to that signal which is used to calculate the error in the NGDC output. For simulation LT Spice Simulation program is used.

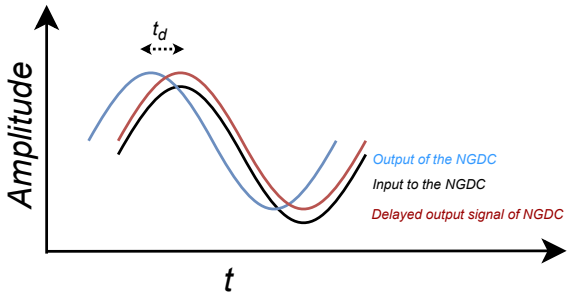


Figure 1.6. The outputs of NGDC and LPF with Reconstructed Input Signal.

Root Mean Square Error (RMSE) is calculated as

$$RMSE = \sqrt{\frac{1}{b-a}\sum_{i=a}^{b}(x_{in}[i] - x_{out}[i + \tau_{ngd}/T_{sample}])^2} \tag{1.10}$$

where $x_{in}[i]$ and $x_{out}[i + \tau_{ngd}/T_{sample}]$ are the normalized input to NGDC and the normalized delayed output of the NGDC, respectively. a and b are the indexes of the sampled signals. Where a and b are the start index and end index, respectively. The

input signal and the output signal of the NGDC are sampled with $T_{sample} < |\tau_{ngd}|$ to make the calculations in MATLAB, where i is the index of the sampled input and output. Also where τ_{ngd}/T_{sample} term is selected as an integer.

Furthermore, the cross-correlation of the NGD structure's input and output can be regarded as the deterministic correlation between two deterministic signals in this case. The cross-correlation of the NGD's input and output is explored in order to corroborate the NGD value and to demonstrate the correlation [22]. The output and input data are captured in LTSpice and processed in MATLAB to achieve this. Because of the possibility of DC offset and changing amplification/attenuation at the output, the data must first be normalized before cross-correlation can be calculated, given as

$$R_{xy}(m) = E\{x_{n+m}y_n^*\} = E\{x_n y_{n-m}^*\}. \tag{1.11}$$

The normalized input and output of the NGD are x and y, respectively. Thus, if the cross-correlation's highest value occurs in the negative indices, the output is lagging; otherwise, the NGD exists, and a time advanced output is obtained.

2. CFOA BASED ACTIVE NGD CIRCUITS AND APPLICATIONS

2.1. Introduction

There are 14 new NGD circuits that are introduced in this chapter with 9 of them having a second order transfer function employing 5 passive components, the remaining ones have a first order transfer function with varying passive component number from 3 to 6, shown in Figures 2.2-2.9. For the sake of completeness, the NGD circuit presented in [10] is also given in addition to the 14 circuits.

The symbol of CFOA is shown in Figure 2.1.

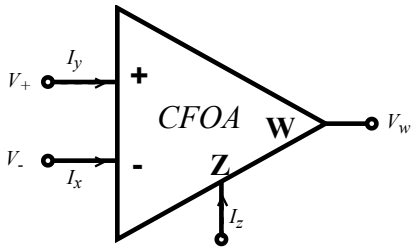


Figure 2.1. CFOA Symbol.

According to its simplified mathematical model [23] the inverting input's current is reflected to the compensation node Z and the output voltage at W terminal is a copy of the voltage at the compensation node. Therefore, the CFOA mathematical model is given as

$$\begin{bmatrix} V_- \\ i_z \\ V_w \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_+ \\ i_x \\ V_z \end{bmatrix} \tag{2.1}$$

where V_-, V_+, V_z and V_w are the voltages at the inverting input, non-inverting input, compensation and output nodes, respectively.

The general form of first and second order transfer functions are repeated for convenience given as

$$H_1(s) = \frac{b_0 + b_1 s}{a_0 + a_1 s} \tag{2.2}$$

and

$$H_2(s) = \frac{b_0 + b_1 s + b_2 s^2}{a_0 + a_1 s + a_2 s^2} \tag{2.3}$$

respectively.

For the presented first order type topologies a single capacitor is used to achieve both the pole and zero of the system. In addition to that the coefficient of s at the denominator is always smaller than the coefficient of s in the numerator as mentioned in the Chapter 1, $b_1 > a_1$. The first and the second order transfer functions are obtainable from presented circuits, shown in Figure 2.2 to Figure 2.4 and Figure 2.5 to 2.9, respectively given in the equations (2.2) and (2.3). In the second order transfer functions, the NGD will be achieved where the a_1 is smaller than b_1 and where they are positive numbers. The operation ranges and parameters are defined in the design section.

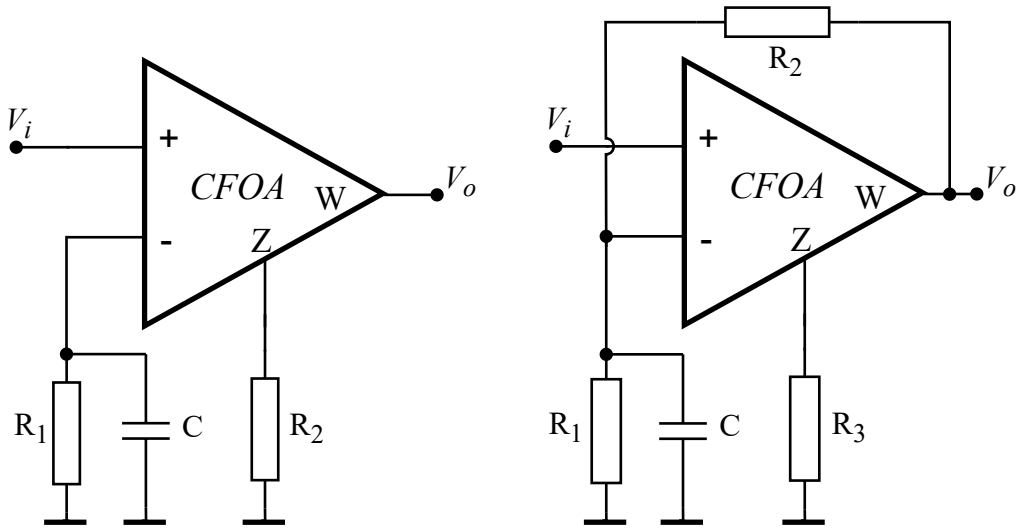
2.2. Proposed Circuits and Transfer Functions

In this section, the proposed circuits and their transfer functions are introduced.

2.2.1. First Order NGD Circuits

First, NGD circuits that have a first order transfer functions are given in Figures 2.2-2.4, followed by Table 2.1 which gives their transfer functions.

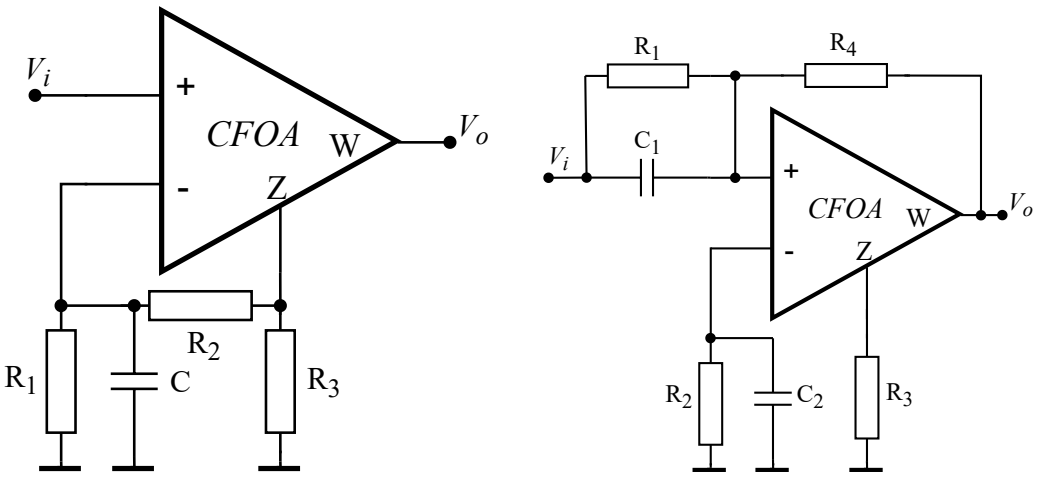
The CFOA Based NGD Circuit 1-2 are given in Figure 2.2 with 3 and 4 passive components, respectively.



(a) (b)

Figure 2.2. Proposed Circuit 1 (a) Circuit 2 (b).

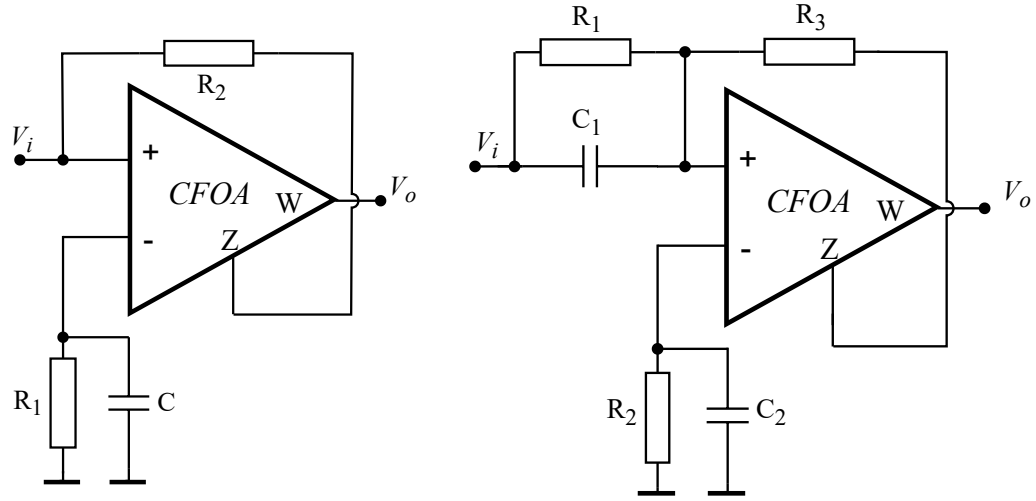
The CFOA Based NGD Circuit 3-4 are given in Figure 2.3 with 4 and 6 passive components, respectively.



(a) (b)

Figure 2.3. Proposed Circuit 3 (a) Circuit 4 (b).

The CFOA Based NGD Circuit 5-6 are given in Figure 2.4 with 3 and 5 passive components, respectively. The first order transfer functions of the proposed circuits are given in Table 2.1.



(a) (b)

Figure 2.4. Proposed Circuit 5 (a) Circuit 6 (b).

Table 2.1. The Transfer Functions of the Introduced Circuits 1-6, $1/G_n = R_n$.

Circuit	**Transfer Function**	**Condition**	**Passive Component Number**
1*	$\frac{G_1 + sC}{G_2}$	–	3
2	$\frac{G_1 + G_2 + sC}{G_2}$	$G_3 \cong 0$	4
3	$\frac{G_1 + G_2 + sC}{G_2}$	$G_3 \cong 0$	4
4	$\frac{G_2 + sC_2}{G_3}$	$G_1 > G_2$, $C_1 \cong C_2, G_4 \cong 0$	6
5	$\frac{G_1 + G_2 + sC}{G_2}$	–	3
6	$\frac{G_2 + sC_2}{G_3}$	$G_1 > G_2$, $C_1 \cong C_2$	5

*The circuit topology 1 is the same with the Cascaded CFOA's first stage of the study [10]

2.2.2. Second Order NGD Circuits

NGD circuits that have a second order transfer functions are given in Figure 2.5, 2.6, 2.7, 2.8 and 2.9 followed by the transfer functions that are belong to the introduced circuits, in Table 2.2.

The CFOA Based NGD Circuit 7-8 are given in Figure 2.5 with 5 passive components.

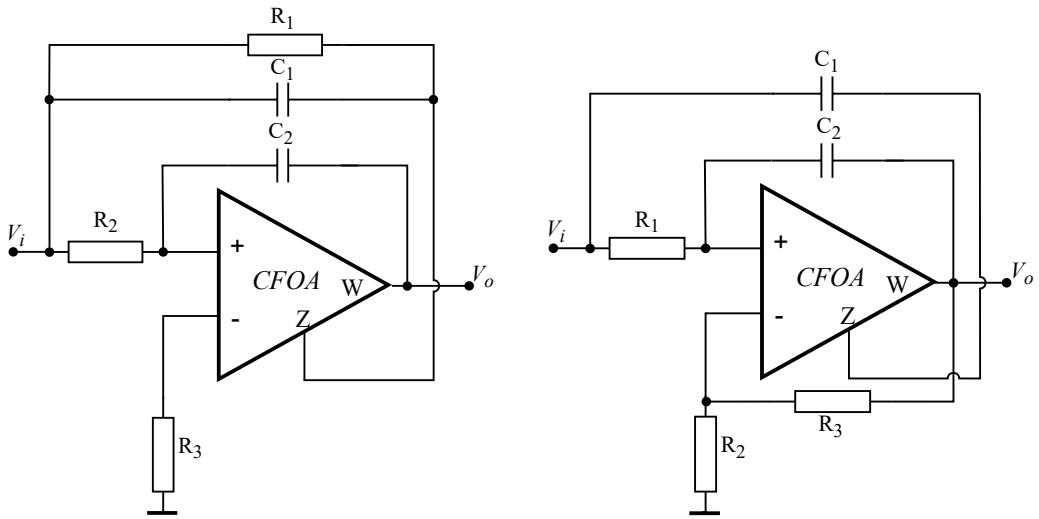
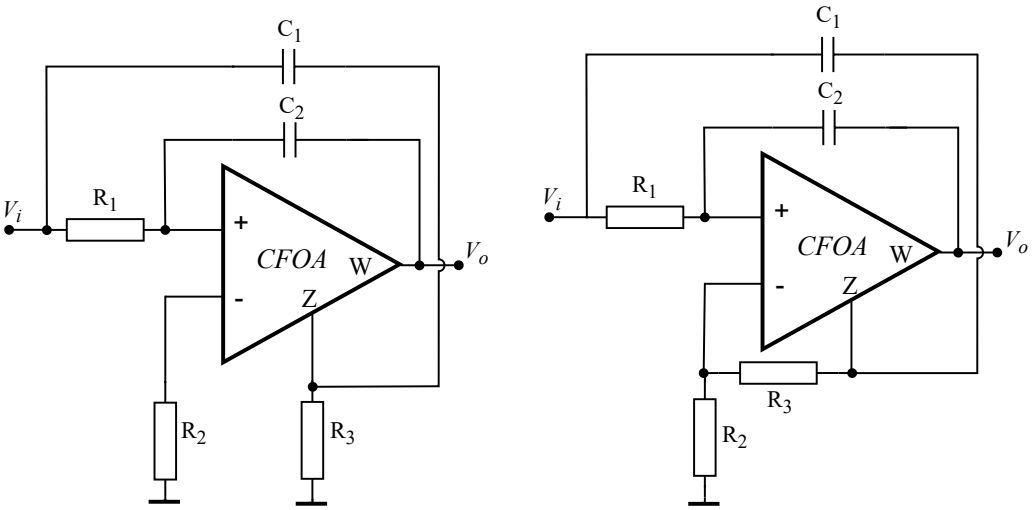


Figure 2.5. Proposed Circuit 7 (a) Circuit 8 (b).

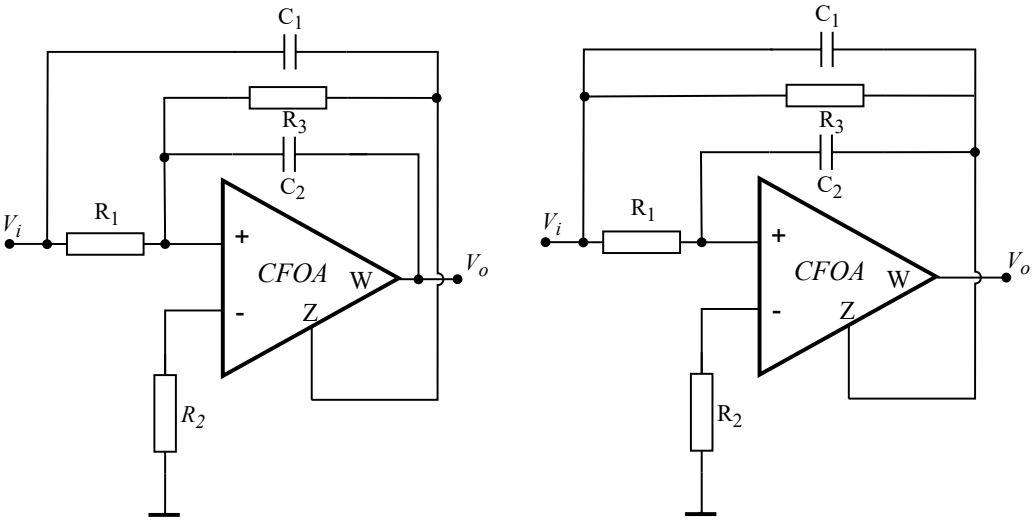
The CFOA Based NGD Circuit 9-10 are given in Figure 2.6 with 5 passive components.



(a) (b)

Figure 2.6. Proposed Circuit 9 (a) Circuit 10 (b).

The CFOA Based NGD Circuit 11-12 are given in Figure 2.7 with 5 passive components.



(a) (b)

Figure 2.7. Proposed Circuit 11 (a) Circuit 12 (b).

The CFOA Based NGD Circuit 13-14 are given in Figure 2.8 with 5 passive components. The CFOA Based NGD Circuit 15 is given in Figure 2.9 with 5 passive components.

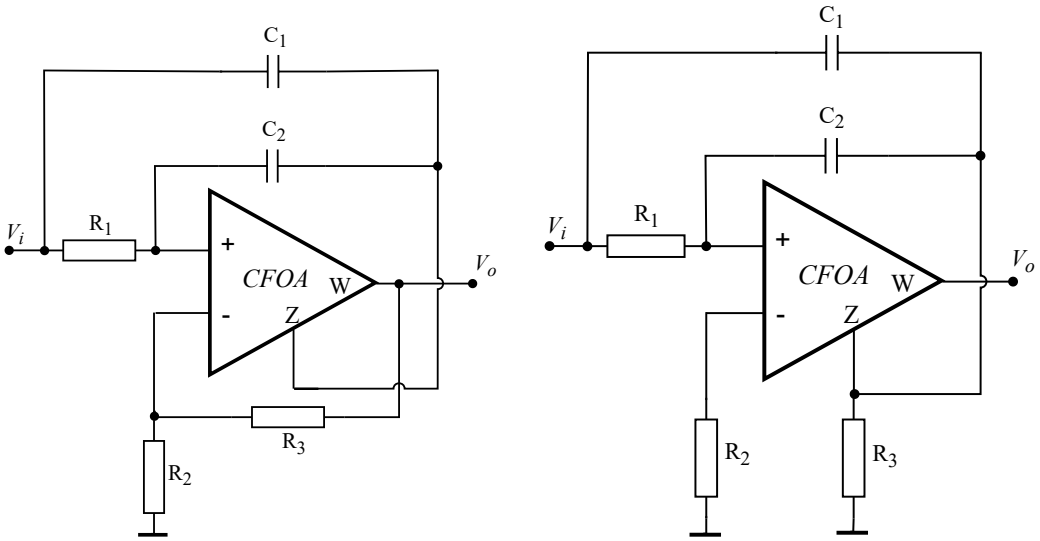


Figure 2.8. Proposed Circuit 13 (a) Circuit 14 (b).

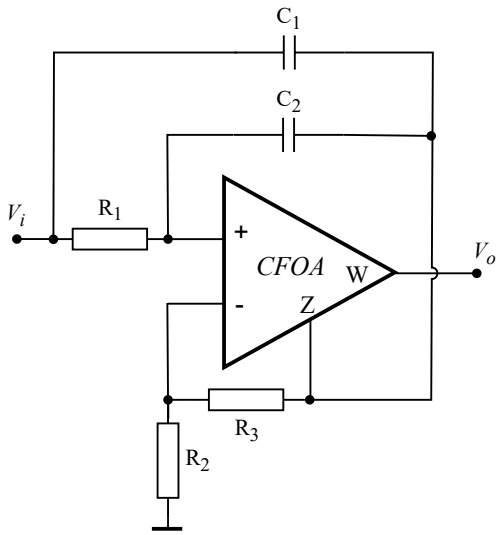


Figure 2.9. Proposed Circuit 15.

The second order transfer functions of the proposed circuits are given in Table 2.2.

Table 2.2. The Transfer Functions of the Introduced Circuits 7-15, $1/G_n = R_n$.

Circuit	**Transfer Function**	**Condition**	**Passive Component Number**
7	$\frac{G_2G_1 + G_2G_3 + (C_1G_2 + C_2G_1)s + C_1C_2s^2}{G_2G_1 + G_2C_1 + (C_1G_2 - C_2G_3)s + C_1C_2s^2}$	$C_1G_2 > C_2G_3$	5
8	$\frac{G_1G_2 + G_1G_3 + (C_1G_1)s + C_1C_2s^2}{G_1G_3 + (C_1G_1 - C_2G_2)s + C_1C_2s^2}$	$C_1G_1 > C_2G_2$	5
9	$\frac{G_1G_2 + (C_1G_1)s + C_1C_2s^2}{G_1G_3 + (C_1G_1 + C_2G_3 - C_2G_2)s + C_1C_2s^2}$	$(C_1G_1 + C_2G_3) > C_2G_2$	5
10	$\frac{G_1G_2 + 2G_1G_3 + (C_1G_1)s + C_1C_2s^2}{2G_1G_3 + (C_1G_1 - C_2G_2)s + C_1C_2s^2}$	$C_1G_1 > C_2G_2$	5
11	$\frac{G_1G_3 + G_1G_2 + (C_1G_1 + C_1G_3)s + C_1C_2s^2}{G_1G_3 - G_3G_2 + (C_1G_1 + C_1G_3 - C_2G_2)s + C_1C_2s^2}$	$C_1G_1 + C_1G_3 > C_2G_2$; $G_1 > G_2$	5
12	$\frac{G_1G_3 + G_1G_2 + (C_1G_1 + C_2G_1 + C_2G_3)s + C_1C_2s^2}{G_1G_3 + (C_1G_1 + C_2G_1 + C_2G_3 - C_2G_2)s + C_1C_2s^2}$	$C_1G_1 + C_2G_1 + C_2G_3 > C_2G_2$	5
13	$\frac{G_1G_2 + G_1G_3 + (C_1G_1 + C_2G_1)s + C_1C_2s^2}{G_1G_3 + (C_1G_1 + C_2G_1 - C_2G_2)s + C_1C_2s^2}$	$C_1G_1 + C_2G_1 > C_2G_2$	5
14	$\frac{G_1G_2 + (C_1G_1 + C_2G_1)s + C_1C_2s^2}{G_1G_3 + (C_1G_1 + C_2G_1 - C_2G_2)s + C_1C_2s^2}$	$C_1G_1 + C_2G_1 > C_2G_2$	5
15	$\frac{G_1G_2 + 2G_1G_3 + (C_1G_1 + C_2G_1)s + C_1C_2s^2}{2G_1G_3 + (C_1G_1 + C_2G_1 - C_2G_2)s + C_1C_2s^2}$	$C_1G_1 + C_2G_1 > C_2G_2$	5

2.3. Design Procedure and Parameters

The circuit 8 from Figure 2.5, is selected to be an example for design, other circuit designs can be made similarly. The selected circuit is repeated in Figure 2.10 for convenience.

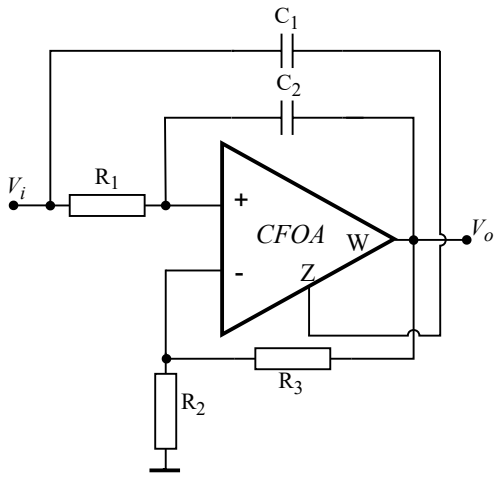


Figure 2.10. Circuit 8 Schematic.

The transfer function of this circuit is given as

$$H_2(s) = \frac{G_1G_2 + G_1G_3 + C_1G_1s + C_1C_2s^2}{G_1G_3 + (C_1G_1 - C_2G_2)s + C_1C_2s^2} \tag{2.4}$$

repeated from Table 2.2. First, the stability constraints of the circuit is calculated. The condition of stability for the given transfer function in (2.4) is given as

$$C_1R_2 > C_2R_1. \tag{2.5}$$

The phase response of the given system is written as

$$\phi(\omega) = \arctan(\frac{C_1G_1\omega}{G_1G_2 + G_1G_3 - C_1C_2\omega^2}) - \arctan(\frac{(C_1G_1 - C_2G_2)\omega}{G_1G_3 - C_1C_2\omega^2}). \tag{2.6}$$

Using (1.3) and (2.6) gives the group delay as

$$\tau_g(\omega) = \frac{(C_1G_1 - C_2G_2)(G_1G_3 + C_1C_2\omega^2)}{G_1^2G_3^2 + ((C_1G_1 - C_2G_2)^2 - 2C_1C_2G_1G_3)\omega^2 + C_1^2C_2^2\omega^4} - \frac{C_1G_1(G_1(G_2G_3) + C_1C_2\omega^2)}{G_1^2(G_2 + G_3)^2 + C_1G_1(C_1G_1 - 2C_2(G_2 + G_3))\omega^2 + C_1^2C_2^2\omega^4}. \quad (2.7)$$

The above expressions are exact expressions. However, the following simplifications are possible under the following conditions. The capacitor values are in the order of 10^{-9} Farads, the conductance values are in the order of 10^{-4} Siemens. Therefore, the expected value comparisons are given as

$$\frac{C_1G_1\omega}{G_1G_2 + G_1G_3 - C_1C_2\omega^2} < 1 \quad (2.8)$$

and

$$\frac{(C_1G_1 - C_2G_2)\omega}{G_1G_3 - C_1C_2\omega^2} < 1. \quad (2.9)$$

The component values are selected such that in the low frequencies the conditions (2.8) and (2.9) hold. Under the given conditions, the phase response in (2.6) is approximated as

$$\phi(\omega) \cong \frac{C_1G_1\omega}{G_1G_2 + G_1G_3 - C_1C_2\omega^2} - \frac{(C_1G_1 - C_2G_2)\omega}{G_1G_3 - C_1C_2\omega^2}. \quad (2.10)$$

Using (1.3) and (2.10) gives the group delay as

$$\tau_g(\omega) = \frac{C_1G_1 - C_2G_2}{G_1G_3 - C_1C_2\omega^2} - \frac{C_1G_1}{G_1G_3 + G_1G_2 - C_1C_2\omega^2} - \frac{2C_1^2C_2G_1\omega^2}{(G_1G_2 + G_1G_3 - C_1C_2\omega^2)^2} + \frac{(2C_1^2C_2G_1 - 2C_2^2C_1G_2)\omega^2}{(G_1G_3 - C_1C_2\omega^2)^2}. \quad (2.11)$$

Rearranging (2.11) gives the simplified group delay equation as

$$\tau_g(\omega) \cong \frac{C_1G_1^2G_3 - C_1^2C_2G_1\omega^2 - C_2G_1G_2G_3 + C_1C_2^2G_2\omega^2 + 2C_1^2C_2G_1\omega^2 - 2C_1C_2^2G_2\omega^2}{(G_1G_3 - C_1C_2\omega^2)^2} - \frac{C_1G_1^2G_2 + C_1G_1^2G_3 - C_1^2C_2G_1\omega^2}{(G_1G_2 + G_1G_3 - C_1C_2\omega^2)^2}. \tag{2.12}$$

The first term of (2.11) and (2.12) is positive at sufficiently low frequencies considering the stability condition (2.5). However, the second part of (2.11) and (2.12) is negative. Therefore, the second part must be dominant part to obtain NGD. The first term is selected as small as possible in magnitude considering the stability condition. Therefore, it determines the frequency where group delay value changes from positive to negative. The frequency for which the group delay value changes from negative to the positive can be estimated approximately. That frequency value is given as

$$\omega_{zero-cross} \cong \sqrt{\frac{R_2 + R_3}{R_1R_2R_3C_1C_2}}. \tag{2.13}$$

Now (2.11) is further simplified at low frequency to reduce the design complexity. It is used in the group delay calculations in the stable region, given as

$$\tau_g(\omega) \cong -\frac{C_1G_1}{G_1G_3 + G_1G_2 - C_1C_2\omega^2} + \frac{C_1G_1 - C_2G_2}{G_1G_3 - C_1C_2\omega^2}. \tag{2.14}$$

Moreover, for sufficiently low frequencies group delay becomes as

$$\tau_g(\omega) \cong -\frac{C_1G_1}{G_1G_3 + G_1G_2} + \frac{C_1G_1 - C_2G_2}{G_1G_3}. \tag{2.15}$$

To simplify the NGD calculation, equal resistances are selected as

$$R_1 = R_2 = R_3, R_n = 1/G_n \tag{2.16}$$

and with

$$C_2 = \alpha C_1 \tag{2.17}$$

where

$$0 < \alpha \leq 1. \tag{2.18}$$

Rearranging equations (2.13), (2.15) assuming resistor values are equal gives group delay function and zero-cross frequency as

$$\tau_g(\omega) \cong RC(\frac{1}{2} - \alpha) \tag{2.19}$$

and

$$\omega_{zero-cross} \cong \sqrt{\frac{2}{\alpha}}\frac{1}{RC} \tag{2.20}$$

respectively. The NGD value in magnitude decreases when the operation of the frequency increases. Therefore, the two values are needed to be maximized together in magnitude.

To zero crossing of the NGD function was given in (2.13), where NGD value changes from negative the positive after that frequency. Here we use F.O.M. as defined in [19]. The product of the zero crossing point and the group delay value is calculated. Thus, a more negative number indicates better F.O.M. The F.O.M. is expressed as

$$\text{F.O.M.} = \omega_{zero-cross} \times \tau_g(\omega) \cong \frac{\sqrt{2}}{\alpha}(\frac{1}{2} - \alpha), \quad 0 < \alpha \leq 1. \tag{2.21}$$

(2.21) is minimized to achieve NGD when the $\alpha = 1$. That is the stability margin point, where the two capacitors are selected equal valued. (2.21) shows that the stability boundary is the where NGD value and operation frequency range is minimized. To obtain a stable system R_2 is selected larger than R_1. The parameters are introduced in the next section.

It is important to note that in some cases, the gain can be vanished when the group delay is negative. Therefore, one has to ensure nonzero gain at the frequency band where the group delay is negative.

In our case, the gain of the system at low frequencies is written as

$$|H(\omega \cong 0)| = 1 + \frac{R_3}{R_2}. \tag{2.22}$$

Equation (2.22) shows that a gain exists in the frequencies of the operation where NGD is achieved. In Figure 2.11, if $R_2 > R_1$ the group delay increases with R_3 value. To show the NGD better how it depends on R_3 and other resistors, 3 variables are shown on the axes in Figure 2.11. After that, to prevent gain dependency on the NGD, R_3 is fixed. In other words R_3 is used to change only the gain of the circuit. In the equation 2.22, a lower R_3 will result in lower gain.

In Figure 2.11, It is shown that the negative group delay is almost constant in the stability region with constant R_3, left blank values represent positive group delay and right blank values represent an unstable system. In addition to that when R_1 and R_2 are selected equal, R_3 affects the group delay value. However, in Figure 2.11 it is shown that R_3 value does not affect whether the group delay is positive or negative when R_1 and R_2 are equal. Now let us select R_3 equal to R_1 and R_2 for design example purpose.

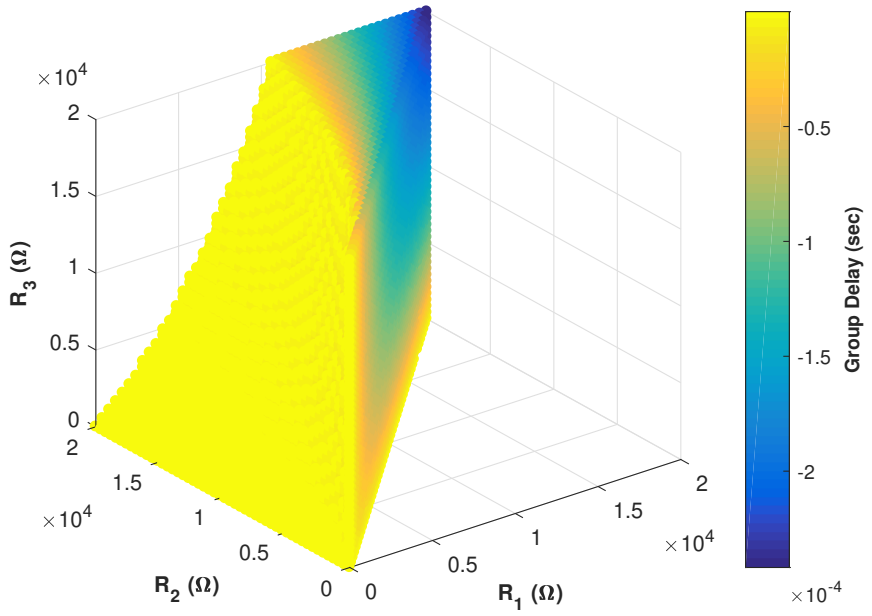


Figure 2.11. Group Delay vs Resistors @100Hz, R_1, R_2 and R_3 swept from 1 Ω to 20kΩ, $C_1 = C_2 = 22$ nF.

Therefore, with single parameter $C_1 = C_2$ a NGD flexibility is achieved without gain dependence. The NGD and NGD range is seen in the Figure 2.12. The capacitor values are given 2.2 nF, 22 nF and 220 nF. The higher capacitor value gives higher NGD. However, it decreases the operation frequency given in the equation 2.13.

The resistors are selected as

$$R_1 = R_2\beta = R_3 = 10\ \text{k}\Omega. \tag{2.23}$$

If $\beta = 0.98$, using equation (2.22) gives

$$|H(\omega \cong 0)| \cong 2. \tag{2.24}$$

Note that to achieve a NGD operation range up to 650Hz, using the equation (2.13), the capacitors are selected as

$$C_1 = C_2 = 22\ \text{nF}. \tag{2.25}$$

Note that to avoid unstable region R_2 value is selected to be 2 percent higher than other resistors, thus $\beta = 0.98$. Figure 2.12 shows that the gain at low frequencies is independent of the NGD value.

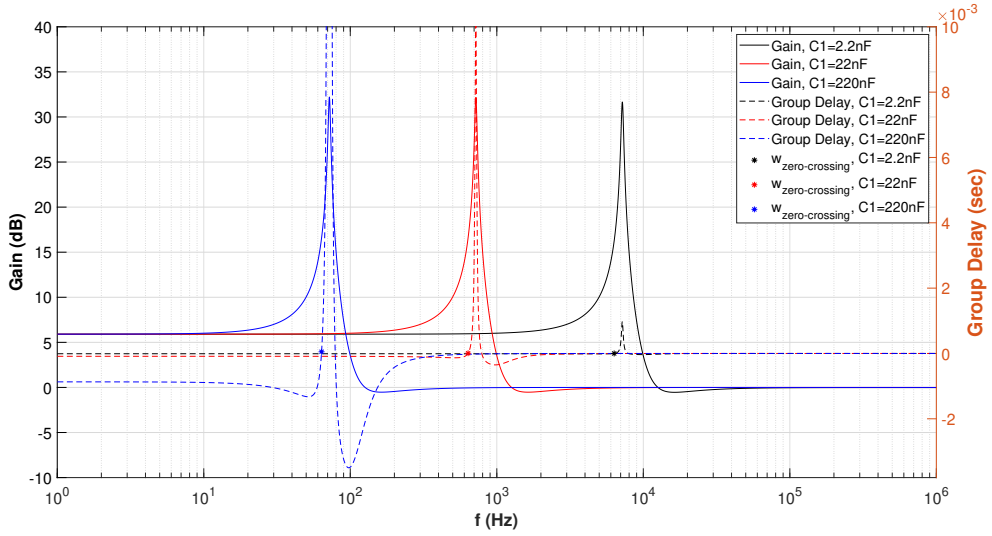
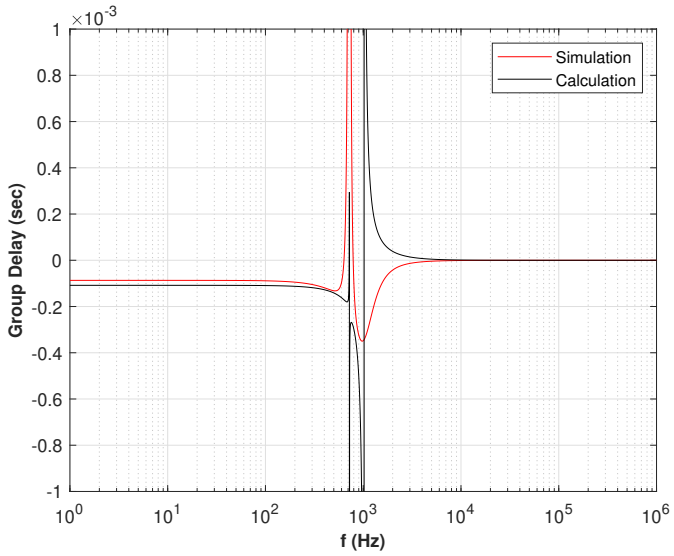


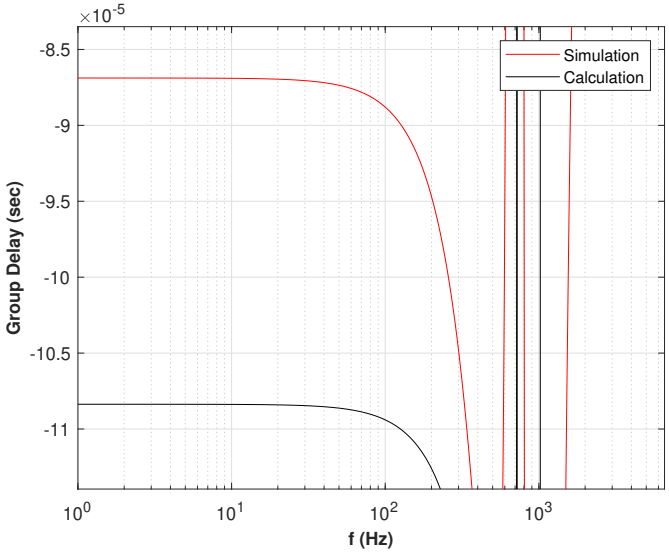
Figure 2.12. AC analysis of the Circuit 8, $R_1 = R_2\beta = R_3 = 10\ \text{k}\Omega$, $C_1 = C_2$ is 2.2 nF, 22 nF and 220 nF, $\beta = 0.98$ factor of R_2 for the stability.

The simulation with given parameters and calculation of the group delay are well-correlated at low frequencies, up to 650Hz, as shown in Figure 2.13.

The component values in the equation (2.23) and (2.25) give the results in the Figure 2.12.



(a)



(b)

Figure 2.13. (a) Group delay vs frequency, Calculation and Simulation Result (b) Zoom.

2.4. Test Results

The circuit schematic of the test setup is introduced in the Figure 2.14. The pulse input passes through a LPF and fed to the input of NGDC.

The LPF characteristic is summarized in the Table 2.4.

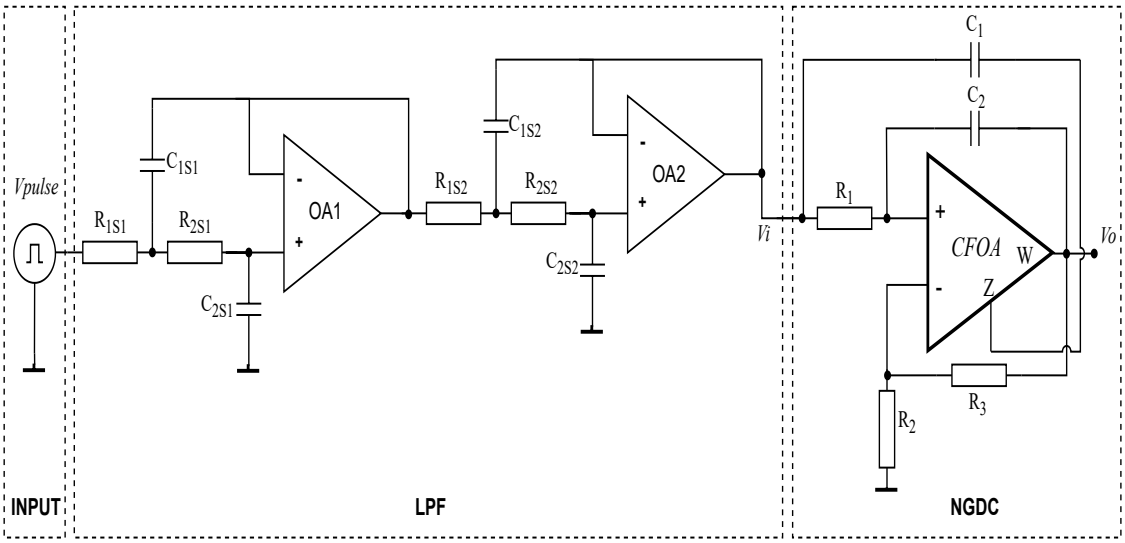


Figure 2.14. Circuit Schematic for the Test.

Table 2.3. LPF Passive Component Values.

R_{1s1}	9.76 kΩ
R_{2s1}	11.8 kΩ
C_{1s1}	110 nF
C_{2s1}	100 nF
R_{1s2}	5.76 kΩ
R_{2s2}	6.65 kΩ
C_{1s2}	261 nF
C_{2s2}	100 nF

The selected passive component values are given in Table 2.3. The test is done with a pulse input using the circuit in the Figure 2.14. The time domain analysis of the circuit in Figure 2.14 is given in the Figure 2.15, 2.17.

Table 2.4. LPF Characteristics.

Filter Response	Bessel
Filter Order	4
Pass-band Frequency (Hz)	100
Stop-band Frequency (Hz)	1k
Gain (V/V)	1
Stop-band Attenuation (dB)	-65.9
Group Delay (μs)	3400

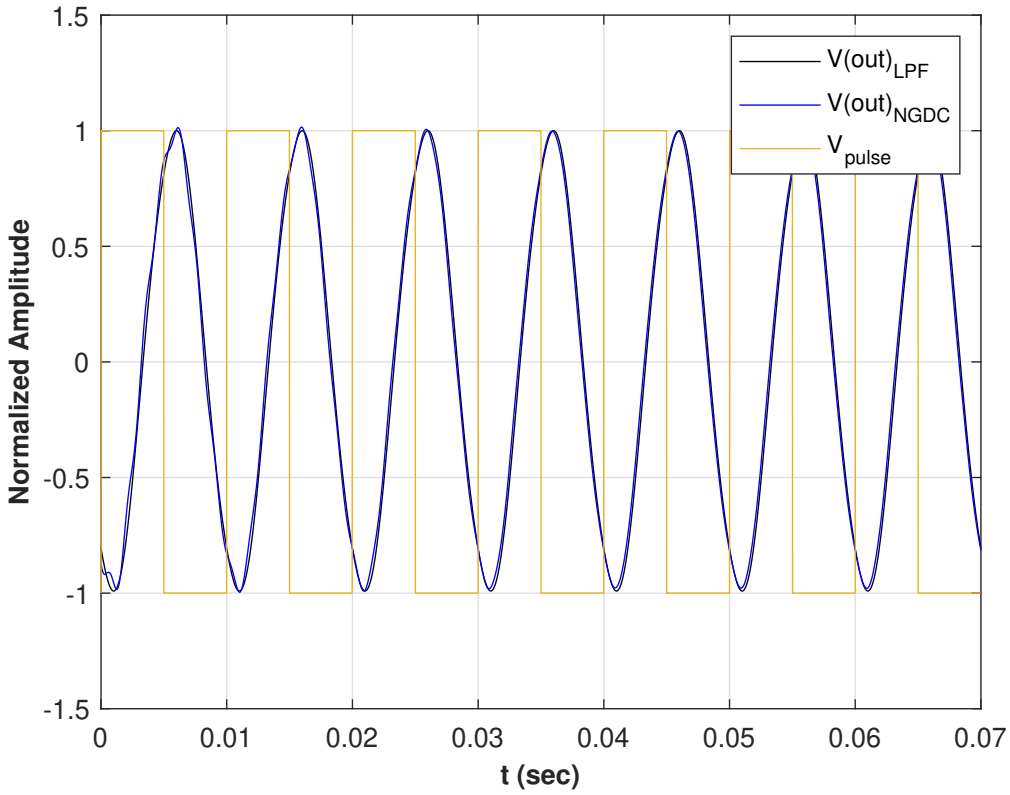


Figure 2.15. Time domain analysis of the NGDC output with LPF output, $V(out)_{LPF}$ is shown as V_i and $V(out)_{NGDC}$ is shown as V_o in Figure 2.14.

In Figure 2.15, due to time axis scale the time advancement is not clearly seen. To show the small time advancement at the output of the NGDC, a zoomed version of Figure 2.15 is given in Figure 2.16.

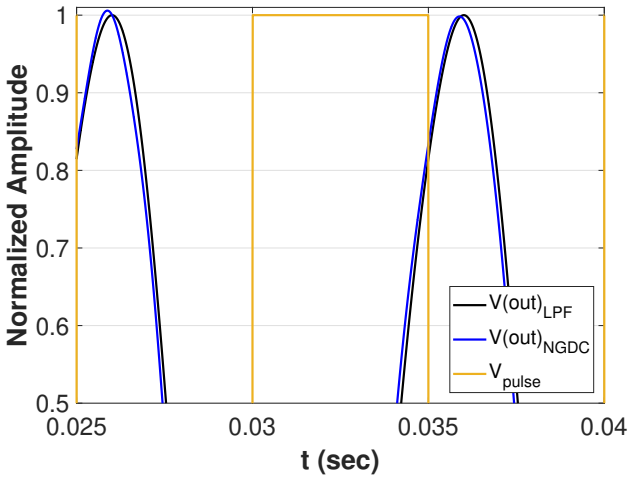


Figure 2.16. Time domain analysis of the NGDC output with LPF output, zoomed in $0.025 < t < 0.04$ sec, blue is the output of the NGDC.

Moreover, the cross-correlation of the output of the LPF and NGD is investigated to confirm the NGD value and the show the correlation [22]. The result is shown in Figure 2.17.

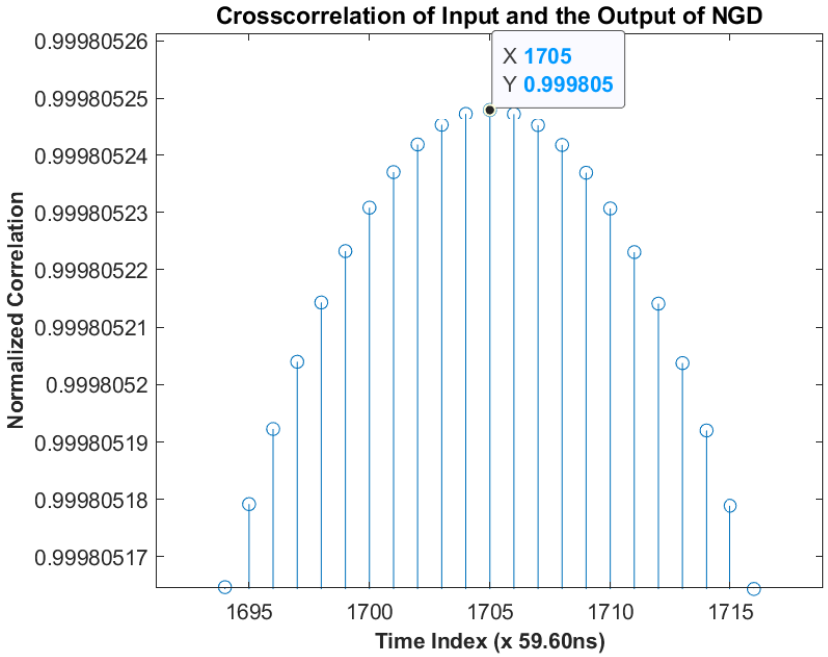


Figure 2.17. The Single Tone output of the LPF Cross-correlation Calculation, 1705x59.60ns, 101.6μs NDG on the Output.

To test the circuit in a more realistic environment, LPF in the circuit Figure 2.14 is removed and an audio signal is given directly into the NGDC. The input audio signal frequency is filtered to be in the operation range of the NGD, upto 500Hz. The transient response and the cross-correlation NGD value verification is seen in Figure 2.18 and in the Figure 2.19. In Figure 2.18, the time advancement is seen between the output and the input. The cross-correlation between the input and the output is given in Figure 2.19.

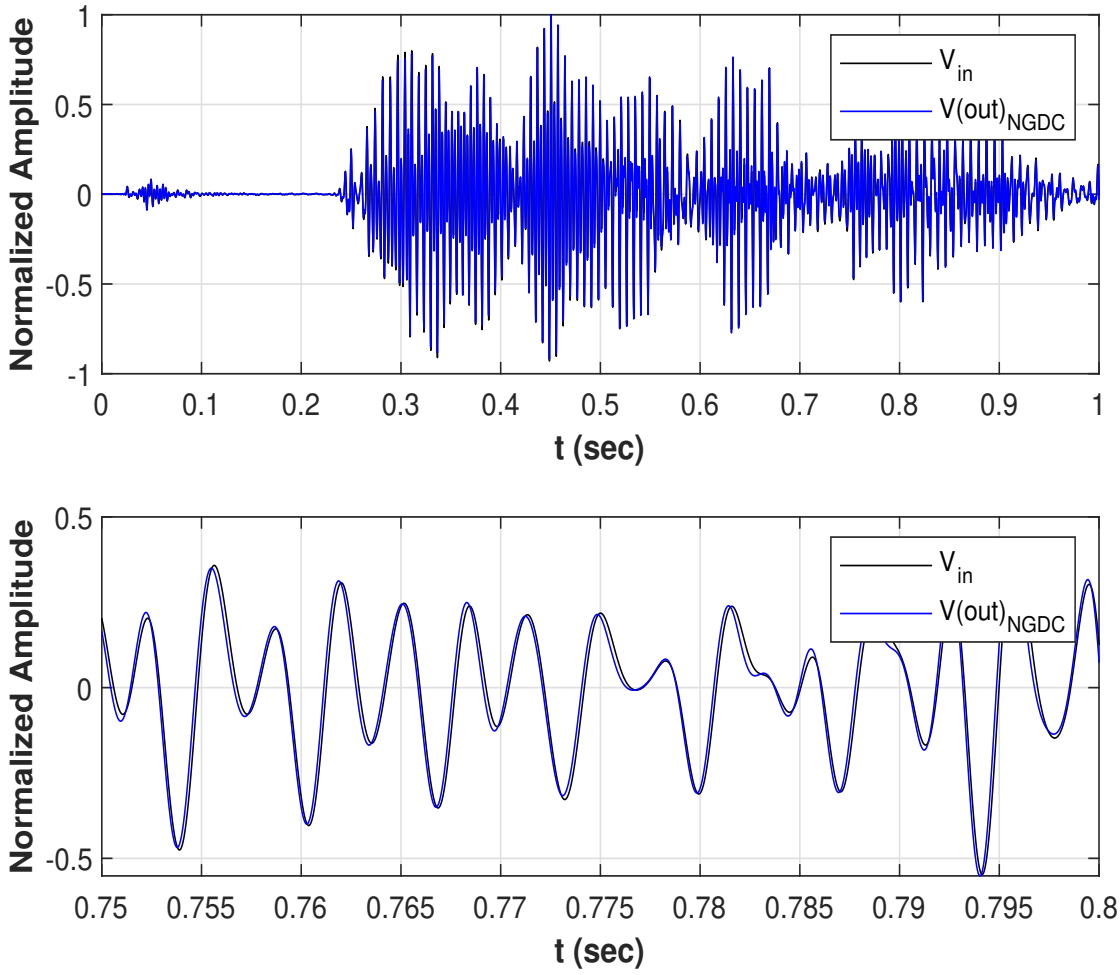


Figure 2.18. Experimental Setup: Time Domain Analysis of the Audio Input and the NGDC output, Blue is the output of the NGDC, with $C_1 = C_2 = 22$ nF, Zoomed

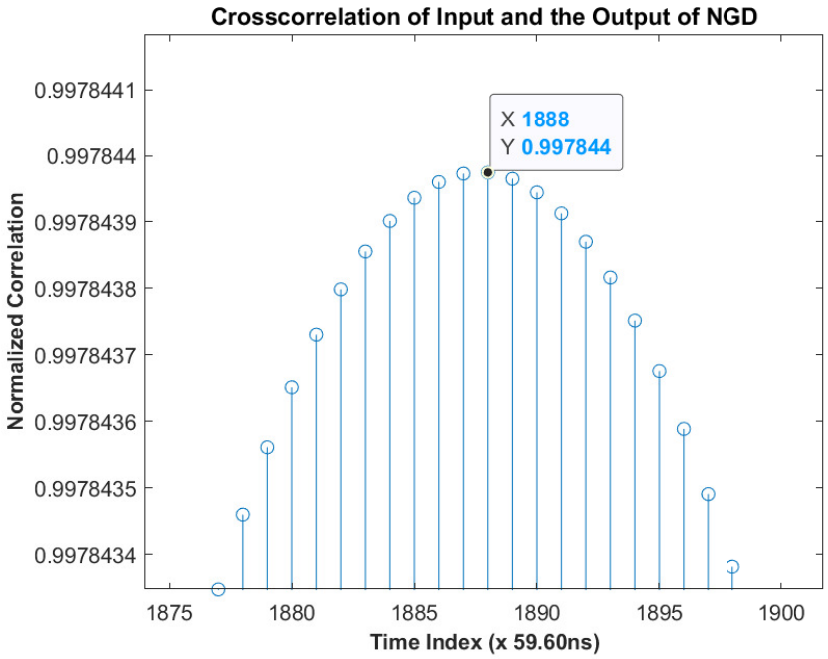


Figure 2.19. The Audio input (1s record) and output of the NGDC Cross-correlation Calculation, 1888x59.60ns, 112.5μs NDG on the Output.

3. MOSFET REALIZATION OF THE NGD CIRCUIT

3.1. Introduction

In Chapter 2, the CFOA based NGD topologies are introduced. The work presented before serves a guide for this part. Examples of NGDCs are given before both using a 1st order transfer function with one capacitor and using a 2nd order transfer function with two capacitors.

In this chapter, a differentiator like circuit is constructed similar to the circuit in the study [1,7,21] without using a resistor component. A similar topology exists in the study [10], where an active CFOA based cascadable NGD is introduced. The circuit is given in the previous chapter, in Figure 2.4.a. As shown in Figure 2.4.a, the current at the inverting input of the CFOA is reflected to compensation node. Also, the voltage at the output is the copy of the compensation's node voltage.

The goal in this Chapter is to realize that circuit, using a differential pair and a current mirror without a resistor but using MOSFETs and an additional capacitor. A circuit diagram in the Figure 3.1 illustrates this idea. The input voltage signal is converted to current using Z_i and that current is made to flow through Z_f. A differential pair is selected as the first stage of the circuit followed by the current feedback to the input.

In the next section, it is shown that selecting a resistor for Z_f and a capacitor for Z_i results a differentiator transfer function, using the CFOA mathematical model given in (2.1).

Furthermore, to avoid passive elements grounded resistors are realized with MOSFETs. In the study [24] grounded and two port resistors are realized in the CFOA based oscillator circuitry. Using same approach to the system, one transistor for the Z_i and two transistors for the Z_f gives the schematic in Figure 3.2. The differential pair is used with single ended input.

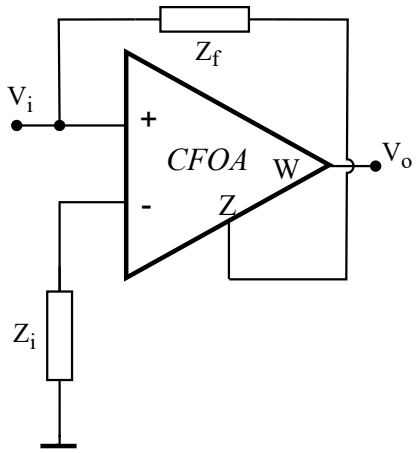


Figure 3.1. The Circuit Diagram of the Mos-Realization NGD Application.

3.2. Design Procedure and Parameters

Considering the CFOA mathematical model, the non-grounded node of Z_i is equal to the input voltage V_i. The current flowing through Z_i is $i_x = V_i/Z_i$. This current is mirrored at node Z. When Kirchoff's Current Law is applied at that node, the relation between input and output voltage is written as

$$\frac{V_i}{Z_i} = \frac{V_o - V_i}{Z_f}. \tag{3.1}$$

Rearranging (3.1) gives the transfer function of the circuit in Figure 3.1 as

$$\frac{V_o}{V_i} = 1 + \frac{Z_f}{Z_i}. \tag{3.2}$$

(3.2) shows that a resistive feedback and a capacitive load at the inverting input of CFOA results a transfer function similar to the study of [1] and the circuit in [10].

The transfer function with appropriate passive elements $Z_f = R_f$ and $Z_i = C_i$ is given as

$$\frac{V_o}{V_i} = 1 + sR_fC_i. \tag{3.3}$$

Using equations (1.2) and (1.3) gives the phase and group delay of the circuit, expressed as

$$\phi = \omega R_fC_i \tag{3.4}$$

and

$$\tau_g = -R_fC_i \tag{3.5}$$

respectively.

(3.3) shows that the gain and the group delay are not independent. With a variable resistor, NGD value can be made adjustable. In [24], a grounded and two-port linear resistor realization is proposed for a Mos-C All-pass Filter. Adding a resistor element similar to that study using two MOSFETs, in the feedback results flexible NGD circuit in terms of controlling its group delay value.

3.3. Voltage Controllable NGD Circuit

The proposed circuit is given in Figure 3.2. The transistors M_{10} and M_{11} form the resistive feedback to the input. The current value is dependent on the resistor between V_o and V_{in}.

The overdrive voltages (V_{ov}) of the transistors are selected to be in the range of 0.2-0.3V. The transistor parameters are used to calculate the g_m values of the transistors, [25]. The transconductace value is written as

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D}. \tag{3.6}$$

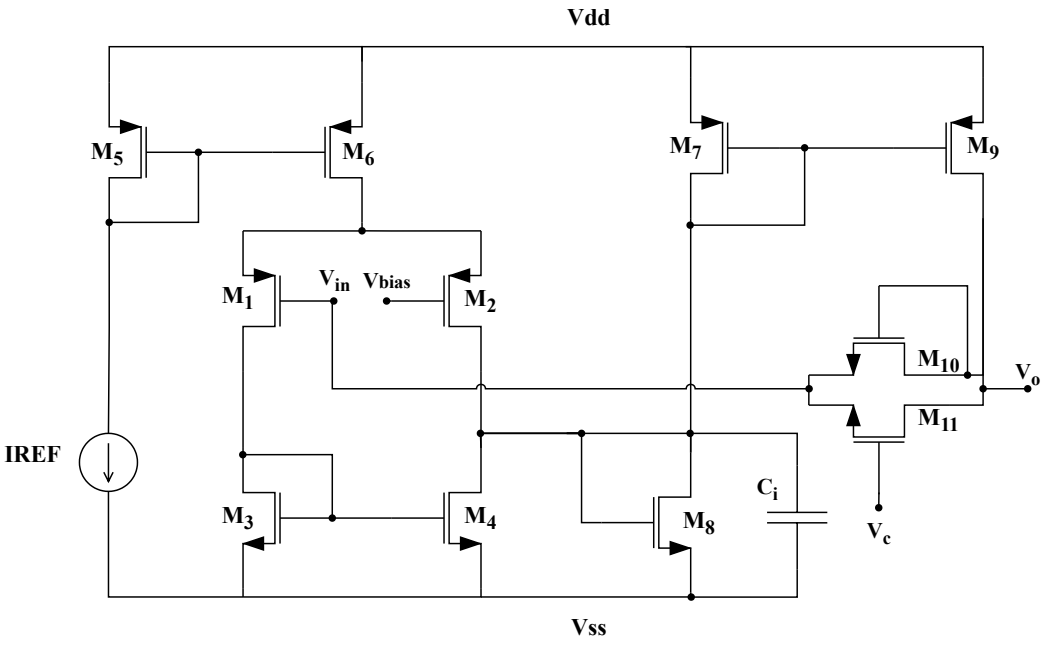


Figure 3.2. The Schematic of the Voltage Controlled NGD Circuit.

IREF in Figure 3.2 is selected as 100μA. To keep the first block transistors V_{ov} values about 0.2V range the transistor sizes are selected as in considering the current equation of the MOSFET in the saturation region, expressed as

$$i_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{ov})^2. \tag{3.7}$$

Using the resistor model in the study [24], the R_f is defined as

$$R_f = \frac{1}{\mu_n C_{ox} W/L(V_c - 2V_{th0n})}. \tag{3.8}$$

The parameters of the transistor is summarized in Table 3.1.

Table 3.1. Parameters of the transistors.

Reference	**Value**
V_{DD}	1.8V
V_{SS}	0 V
I_{REF}	100 µA
V_{bias}	0.7 V
V_{THON}	0.371 V
V_{THOP}	–0.395 V
μ_{n}	276.47 cm^2/Vs
μ_{p}	118.02 cm^2/Vs
T_{ox}	$4.1{\cdot}10^{-9}$ m
L	0.36 µm

The bias voltage of the circuit is selected as 0.7V. Therefore, the voltage control at the NMOS V_c is swept between 1.6V to 1.8V. Combining equations (3.5) and (3.8) with parameters in Table 3.1 gives the group delay value in the form of

$$\tau_g = \frac{C_i}{\mu_n C_{ox} W/L(V_c - 2V_{th0n})}. \tag{3.9}$$

The transistors M_{7-9} are sized as $0.72\mu m$. That limits the current flowing to the transistors M_{10} and M_{11}.

Operation of the circuit can be summarized as follows:

- Adjusting C_i for both NGD operation range and NGD value
- Adjusting V_c to adjust NGD value

3.3.1. Test and Simulation Results

The MOSFET dimensions are given in Table 3.2. The AC analysis is done with selecting C_i=100nF and the controlled voltage is swept from 1.6V to 1.8V with 0.1V intervals.

Table 3.2. The Transistor Dimensions.

Transistors	W	L	W/L
$M_{1,2}$	$14.4\mu m$	$0.36\mu m$	40
$M_{3,4}$	$3.6\mu m$	$0.36\mu m$	10
$M_{5,6}$	$28.8\mu m$	$0.36\mu m$	80
$M_{7,8,9}$	$0.72\mu m$	$0.36\mu m$	2
$M_{10,11}$	$14.4\mu m$	$0.36\mu m$	40

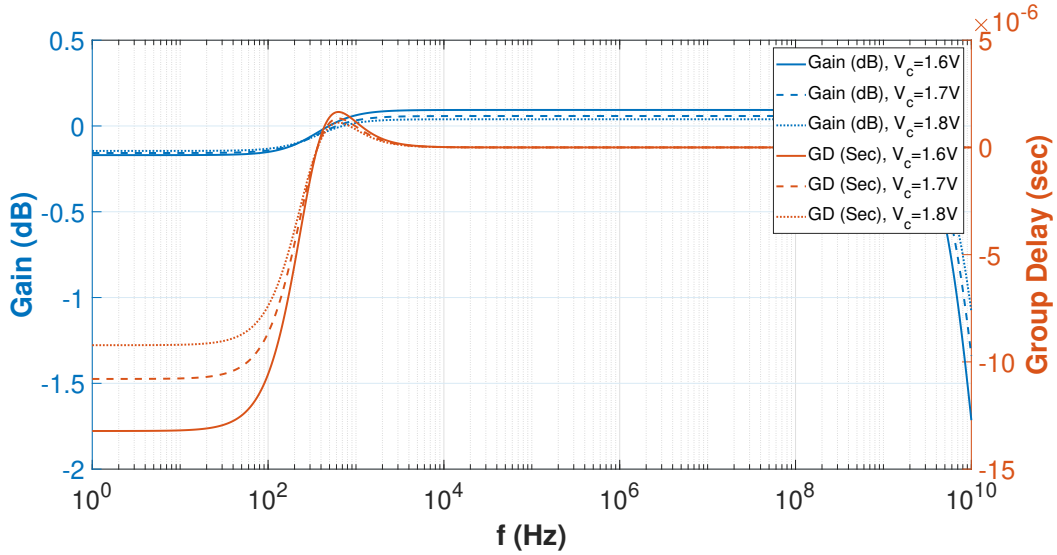


Figure 3.3. The AC Response, V_c=1.6V,1.7V,1.8V.

The phase response of the circuit is given in Figure 3.4.

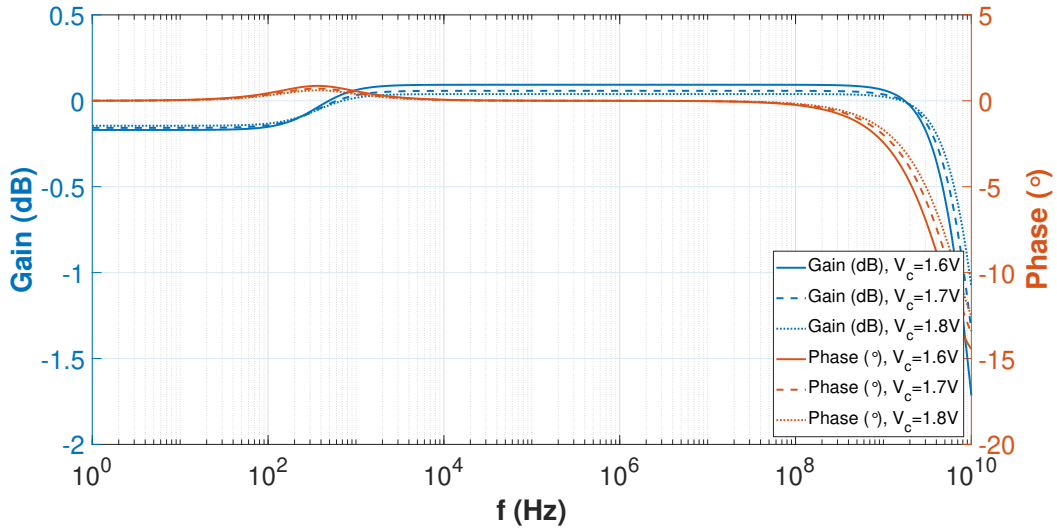


Figure 3.4. The Phase Response, V_c=1.6V,1.7V,1.8V.

The group delay value is summarized in Table 3.3, using 100nF capacitor. In the 4th Chapter, a transimpedance-mode NGD circuit is proposed.

Table 3.3. The Simulation Results.

V_c	1.6V	1.7V	1.8V
Calculation	-12.57μs	-11.25μs	-10.18μs
Simulation	-13.21μs	-10.79μs	-9.21μs

4. OTA-C BASED TRANSIMPEDANCE-MODE NGD CIRCUIT

4.1. Introduction

In this chapter an OTA-C based Negative Group Delay circuit is proposed for current output systems. The application areas extend from audio systems to mechanical systems or any sensor signal anticipation. A NGD value of about 100ns to 200μs is observed to be achievable with three different capacitor values without any resistive passive components, operation range limit varies from 700 Hz to 700 kHz. The NGD and the operation range is showed to be flexible without gain dependency. An example design is built for a specific NGD value of 15 µs and time domain analysis is done with both a single tone sinusoidal and a band-limited audio record, in the range of 1 Hz–7 kHz.

Sensors for industrial applications have not only static but also dynamic characteristics. This means in general, the physical quantities like temperature, displacement, pressure and others cannot be converted to voltage or current instantaneously but time is required for this conversion. Therefore certain amount of delay cannot be avoided. However in many applications like robotics this delay is a problem. In such cases use of a transfer function with negative group delay is a promising solution for such delays as mentioned previously.

Many industrial sensors have current outputs [26, 27]. In this chapter, an OTA based NGD circuit is introduced which accepts current signal as its input and with its NGD property in a certain frequency band it can be used for signal delay compensation. In this way the time delayed signal from the sensor can be made time advanced, in other words the delay between the actual physical phenomenon and sensor output can be reduced.

4.2. Design Procedure and Analysis

In this section, a current input OTA-C based NGD circuit is introduced without a resistive passive component, unlike CFOA based circuits in Chapter 2 and which may be useful for current mode sensors.

The OTA symbol is given in 4.1.

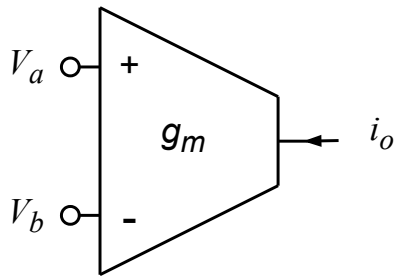


Figure 4.1. The OTA Symbol.

The operation of OTA is given as

$$i_o = g_m(V_a - V_b) \tag{4.1}$$

where i_o is the output current of the OTA, V_a and V_b are the voltages at the input of the OTA and g_m is the transconductance of the OTA. The circuit schematic of proposed NGD is given in Figure 4.2. The transfer function of the given circuit is shown in Figure 4.2, is given as

$$H(s) = \frac{V_o}{I_{in}} = \frac{1}{g_{m2}} \frac{g_{m2} + sC}{g_{m1} + sC}. \tag{4.2}$$

Note that the pole and zero as well as the gain can be adjusted independently by modifying g_{m1} and g_{m2} values. This allows control of these values and permits easy design.

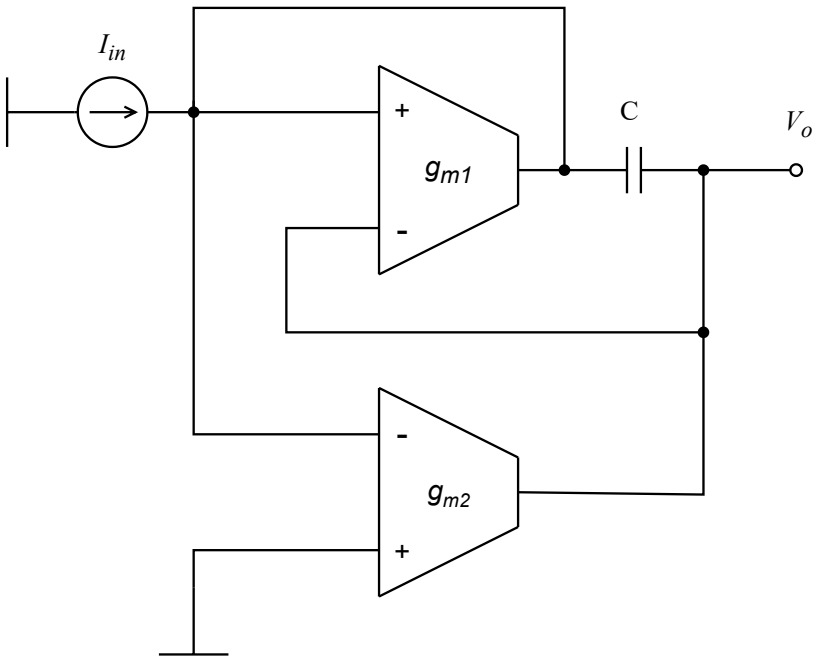


Figure 4.2. The OTA Based NGD Circuit Schematic.

The phase response and the group delay response of the circuit are given as

$$\phi(\omega) = arctan\{\frac{Im[Y(j\omega)]}{Re[Y(j\omega)]}\} - arctan\{\frac{Im[X(j\omega)]}{Re[X(j\omega)]}\} \cong \frac{\omega C}{g_{m2}} - \frac{\omega C}{g_{m1}} \tag{4.3}$$

where X and Y are input and output signal's Laplace transform, respectively. Moreover, group delay is given as

$$\tau_g(\omega) = -\frac{d\phi(\omega)}{d\omega} = C(\frac{1}{g_{m1}} - \frac{1}{g_{m2}}). \tag{4.4}$$

The condition of transconductance values for a NGD is written as

$$g_{m1} > g_{m2}. \tag{4.5}$$

(4.4) shows when condition (4.5) is satisfied NGD can be achieved, where the transconductance values are positive. The gain of the system in the low frequency region and high frequency region is given as

$$|H(\omega = 0)| = \frac{1}{g_{m1}} \tag{4.6}$$

and

$$|H(\omega = \text{inf})| = \frac{1}{g_{m2}} \tag{4.7}$$

respectively. Equations (4.6) and (4.7) show that amplitude change is possible maintaining the NGD operation of the circuit. Moreover, changing g_{m2} without changing g_{m1} provides us to adjust group delay without changing the gain significantly in the low frequency region.

The constant gain in the NGD region provides an easy and a flexible design of a NGDC where the output of the circuit differs from the input signal in terms of group delay but not in terms of amplification or attenuation. Therefore, the same circuit is usable for different desired NGD values without making a drastic changes in the design part.

The ideal model [28], of the circuit with controlled sources is given in Figure 4.3, where the input and the parasitic capacitances of OTAs are ignored since their values are expected to be low, [25]. The output resistances of the MOSFETs, r_o, and the output capacitances add high frequency pole expressed as

$$f_t = \frac{1}{2\pi RC}. \tag{4.8}$$

Therefore, low output capacitances and expected high output resistances of the MOSFETs do not disturb the operation range NGD calculations significantly.

The circuit is built using 2 OTA blocks as shown in Figure 4.4. The circuit is constructed with 13 transistors and a single capacitor. The first and the second blocks are formed by the transistors $M_{1-4,6}$ and $M_{9-12,7-8,13}$, respectively.

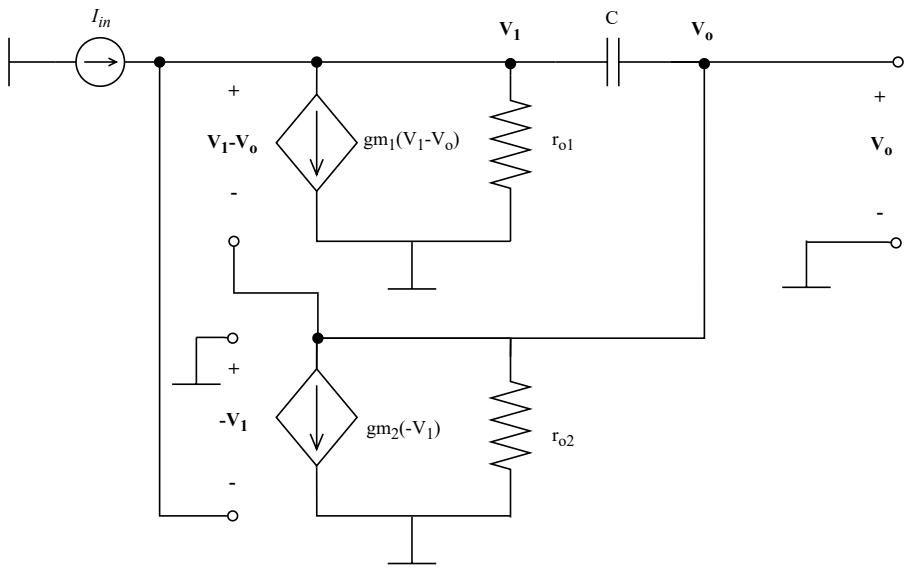


Figure 4.3. The Design of the Circuit with Ideal VCCSs.

The aspect ratios of the 2nd block transistors with respect to the 1st block transistors are given as

$$\frac{W_{2ndBlock}}{L_{2ndBlock}} = \alpha \frac{W_{1stBlock}}{L_{1stBlock}}. \tag{4.9}$$

The complete schematic of the circuit is given in 4.4. The first stage of the schematic sources the IREF to the first block and the second block.

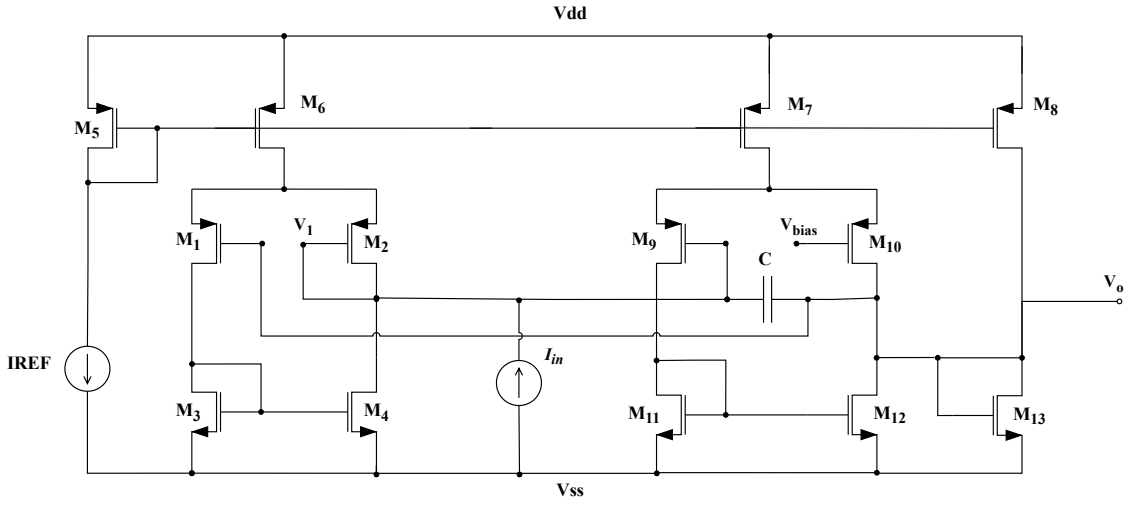


Figure 4.4. The Schematic of the OTA-C Based NGD.

The overdrive voltages (V_{ov}) of the transistors are selected to be in the range of 0.2-0.3V. (3.6) is used to calculate the g_m values of the transistors, [25, 28].

IREF in Figure 4.4 is selected as $100\mu A$. To keep the first block transistors V_{ov} values about 0.2V range the transistor sizes are selected as in considering the current equation of the MOSFET in the saturation region in (3.7). The equation (4.4) shows that increasing the g_m difference between the first and second OTA blocks maximize the NGD value of the circuit. To increase the g_m difference between the first block and the second block, the second block current source is decreased. To achieve that the current mirror formed by M_7 and M_6 is used. The second block's transistor aspect ratios are reduced including the transistor M_7.

Reducing the aspect ratio of the transistor M_7 in the form of (4.9), decreases the current by the same ratio since the gate voltages of M_6 and M_7 is same. (4.9), (3.6) and (3.7) show that the transconductance of the second block is dependent to α in the form of

$$g_{m9} = \alpha g_{m1} \tag{4.10}$$

where α is a positive number smaller than 1. In this design IREF as selected as 100 μA. Therefore, to achieve a 10 μA current flowing to the second block, the α is limited to be at least 0.1. That limits proportionally the minimum input current. In addition to that, the maximum possible input current is limited by the IREF/2 which is the differential pair tail's current in the first block.

Table 4.1. Parameters of the transistors in OTA-C NGD.

Reference	**Value**
V_{DD}	1.8V
V_{SS}	0 V
I_{REF}	100 µA
V_{bias}	0.6 V
V_{THON}	0.371 V
V_{THOP}	–0.395 V
μ_{n}	276.47 cm^2/Vs
μ_{p}	118.02 cm^2/Vs
T_{ox}	$4.1{\cdot}10^{-9}$ m
L	0.36 µm
$W_{1,2}$	14.4 µm
$W_{3,4}$	3.6 µm
$W_{5,6}$	28.8 µm
$W_{9,10}$	$\alpha{\cdot}14.4$ µm
$W_{11,12}$	$\alpha{\cdot}3.6$ µm
$W_{7,8}$	$\alpha{\cdot}28.8$ µm
W_{13}	$\alpha{\cdot}7.2$ µm

Parameters of the transistors and other values related to the circuit are given in Table 4.1. The first stage transistors, M_5 and M_6, of the circuit is sized as 80L, and the transistors that formed the differential pair, $M_{1,2}$ and $M_{3,4}$ are sized as 40L and 10L, respectively. The second block is sized as in the equation (4.9).

Finally, another stage is added to the second block to reduce the band of the high frequency operation where the gain is higher, (4.7) and where the group delay is positive, the frequency band is outside the NGD operation range.

The capacitor C is connected between V_o and V_1 node, M_2 drain. For the circuit to function, the capacitor's current flow is crucial. The current flowing from M_2 drain to M_4 drain is expected to be equal because of the transistor size choices. The input current is given from that node and connected to the capacitor C. To flow current through that capacitor, M_8 and M_{13} is added to the second OTA block. In addition to that M_{13} transistor size is selected smaller than the transistor size of M_8. Therefore, a current flowing from drain of the transistor M_8 will flow to the M_{13} drain and the capacitor C.

The transistor M_{13} size is selected as the $1/4th$ of the M_8 so that the circuit is not effected from the output load significantly. The ratio of the last stage is selected as

$$\frac{W_{13}}{W_{12}} = 2\frac{W_8}{W_7}, \tag{4.11}$$

considering the DC offset at the output [25].

The gate and the drain of M_{13} is shorted, forms a load that keeps DC level at the output node V_o close to the DC level at the node V_1. The second differential pair works if M_9 and M_{10} transistors are in the saturation region. The gate voltages of M_2 and M_9 are equal. Therefore, DC bias (V_{bias}) is given according to the expected DC offset at V_1 node, which is selected as 0.6V to obtain 0.2V to 0.3V V_{ov} for the transistors M_1, M_2, M_9 and M_{10}. The first block and the second block g_m values are equal to the g_m value of the transistor M_1 and M_9 ignoring the mismatches between the transistors, respectively. Using (3.6), (4.10) and parameters in Table 4.1 give the first transconductance as $453\mu A/V$ and the second transconductance as α $453\mu A/V$.

4.3. Design Example and Simulation Results

Rearranging the equation (4.4) considering (4.10), the group delay can be written as

$$\tau_g(\omega) = \frac{C}{g_{\mathrm{m1}}} \frac{\alpha - 1}{\alpha}. \tag{4.12}$$

The calculated group delay values with expected g_{m} values and alpha is compared with the simulation. Using the three capacitor values and alpha, group delay is calculated as shown in Figure 4.5.

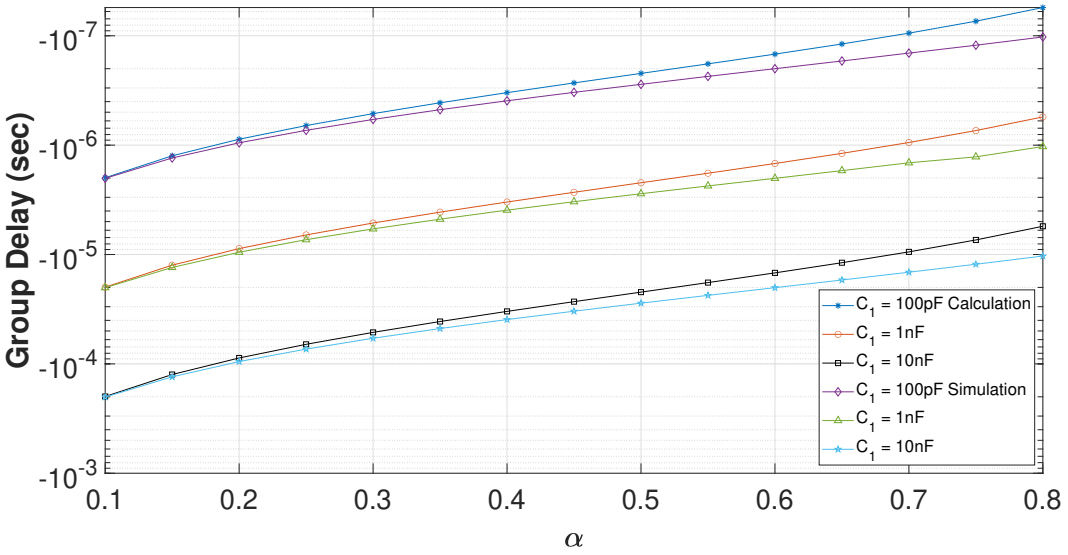


Figure 4.5. Alpha vs. Group Delay, with C=0.1,1,10 nF.

In Figure 4.5 calculated group delay and simulation values are in good match in the range of 0.1 to 0.8 α values.

In addition to the ideal VCCS model of the circuit, there are output parasitic capacitors of the transistors. These capacitors values are not expected to affect the group delays significantly since their values are low. However, they affect -3dB point at high frequencies.

As seen in Figure 4.2 and 4.3, there are two OTA blocks which have a capacitor connected between the output of them. The second OTA block transistor sizes are scaled with α which is a positive number smaller than 1. Therefore, the transistor gate to drain or gate to source capacitors of the second block are expected to be lower than the first OTA block. That leading us the bigger capacitor value at the output will determine the dominant pole of the system at high frequencies, which is the output capacitor of the first block. Thus, the high frequency pole is formed by the first block's output stage.

The input current signal is connected to the drain of M_2 and M_4. It is also connected to the M_9 gate. There are 3 capacitor values that is connected to that node which are the three transistors' parasitic capacitors. The M_9 parasitic capacitors are negligible since the transistor size is scaled with α. Remaining two capacitors are given by capacitors between the gate-source of the transistor M_2 and gate-drain capacitor of the transistor M_4, parallel to each other.

The gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) capacitors of the first OTA stage are given by (4.13), the technology values of the gate to drain and gate to source capacitances are $7.9{\cdot}10^{-10}$ F/m and $6.34{\cdot}10^{-10}$ F/m for the n-channel and p-channel transistors, respectively. To achieve a realistic model of the circuit the output capacitor of the first stage, [25], is given as

$$\begin{aligned} C_{\mathrm{gs2}} &= C_{\mathrm{gs0_p}}{\cdot}W_2 \\ C_{\mathrm{gd4}} &= C_{\mathrm{gd0_n}}{\cdot}W_4 \\ C_{\mathrm{o1}} &= C_{\mathrm{gs2}} + C_{\mathrm{gd4}}. \end{aligned} \tag{4.13}$$

The output capacitors of the first and second OTA are given as

$$\begin{aligned} C_{\mathrm{o1}} &\cong 9.13 \text{ fF} + 2.84 \text{ fF} = 11.97 \text{ fF} \\ C_{\mathrm{o2}} &\cong \alpha{\cdot}(9.13 \text{ fF} + 2.84 \text{ fF}) = \alpha{\cdot}11.97 \text{ fF} \end{aligned} \tag{4.14}$$

respectively.

The output capacitance of the first block is parallel with the output resistance of the first OTA block, which is formed by the transistors M_2 and M_4 output resistances, given as

$$R_{o1} = r_{o2} \parallel r_{o4}. \tag{4.15}$$

Hence, the transfer function in (4.2) can be expressed as

$$H(s) = \frac{V_{\mathrm{o}}}{I_{\mathrm{in}}} = \frac{1}{g_{\mathrm{m9}}} \frac{g_{\mathrm{m9}} + sC}{g_{\mathrm{m1}} + sC} \frac{1}{1 + sR_{o1}C_{o1}}. \tag{4.16}$$

The NGD value and the operation range are expected to be inversely proportional to each other as mentioned in the Chapter 2. To determine the negative group delay operation range the dominant zero of the system is calculated. In the transfer function (4.16), there are one zero and pole and one additional pole at high frequencies because of the parasitic capacitances. The zero exists at lower frequency than the pole. In that value of frequency the gain is increased by 3 dB. Therefore, the dominant zero of the system does not determine the group delay value change from negative to positive. However, that value determines the NGD value change approximately 10% compared to the NGD value at low frequency of the system. Therefore, when α is 0.125 the dominant zero is calculated as

$$f_{\mathrm{NGD}_{cross}} = \frac{g_{\mathrm{m9}}}{2\pi C} = 8.95kHz \tag{4.17}$$

to represent the NGD operation range of the circuit. On the other hand, the dominant pole of the system determines the 3 dB gain drop of the system, indicated as

$$f_{3dB} = \frac{g_{m1}}{2\pi C} = 71.6kHz \tag{4.18}$$

while the gain value beyond this frequency is given by (4.7). The dominant capacitance of the system is equal to C. Note that the output resistance of the first OTA is approximately 75 kΩ, which is equal to $r_{o2} \parallel r_{o4}$ given in equation (4.15).

The capacitor values of the OTA_1 are given in (4.14), the high-frequency pole of the NGD circuit can be calculated as

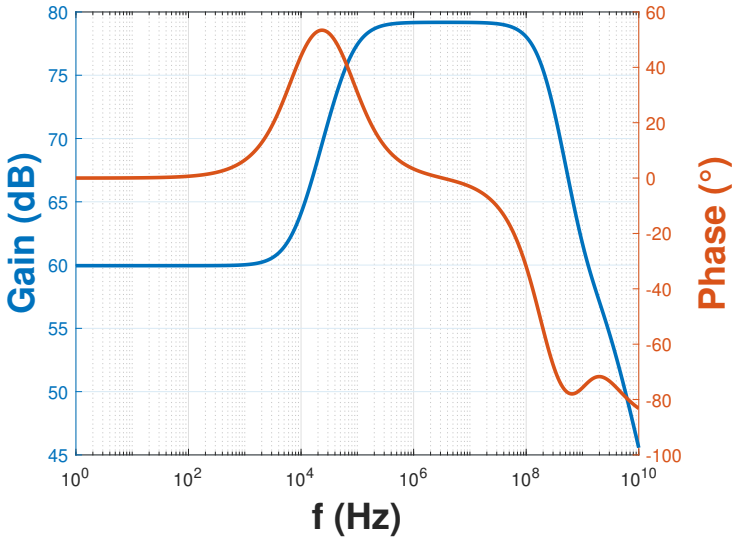
$$f_{-3\mathrm{dB}_{hf}} = \frac{1}{2\pi C_{\mathrm{o1}} \times 75 \cdot 10^3} = 178 \text{ MHz}. \tag{4.19}$$

The transfer function at low frequency is given as

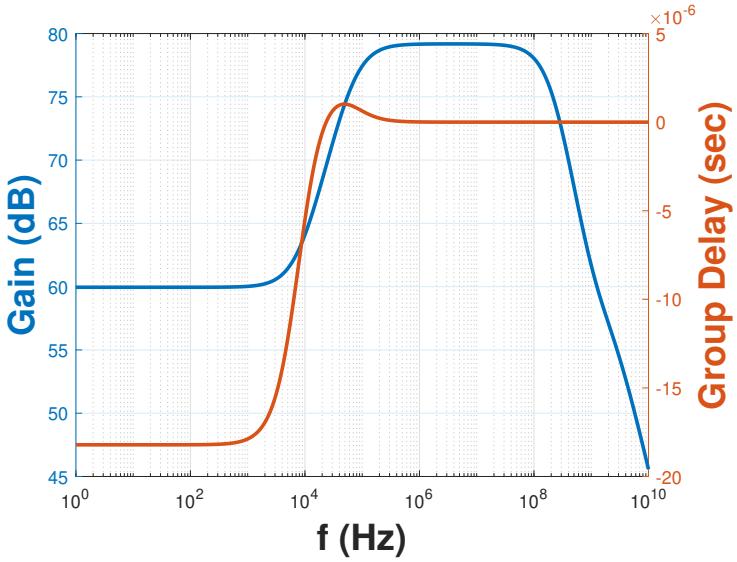
$$\frac{V_o}{I_{in}} = \frac{1}{g_{m9}} \frac{g_{m9} + sC}{g_{m1} + sC}. \tag{4.20}$$

To test the circuit with $C = 1$ nF, $\alpha = 0.125$, and using the parameter in Table 2.4, the group delay is calculated to be -15.50μs. The dominant zero of the system determines the group delay change of the system, as indicated in (4.17).

The AC response of the system with selected parameters are given in Figure 4.6. The group delay is seen to increase at frequencies higher than 1kHz and the value is negative until about 10kHz. The flatness of the group delay is important in terms of distortion of the input signal as mentioned in the previous chapters. Therefore, the time domain analysis is done using an input signal at 1kHz. After the group delay becomes positive the gain increase is seen in the Figure 4.6.



(a)



(b)

Figure 4.6. Simulated (a) magnitude and phase-frequency responses, (b) Transimpedance magnitude gain and group delay-frequency responses for $C = 1$ nF and $\alpha = 0.125$.

The time domain simulation is done with a single tone current input @1kHz and 1ms delay. The end of the cycles a small oscillation may occur at the output, [5]. To show that the signal that is given to the system is opened 1ms after the simulation started, 4.7, 4.8. A voltage bias of value 0.6V is used for the circuit to keep the second block transistors in the saturation region. Figure 4.7 shows that a DC offset of 730mV exists at the output due to the not symmetrical supply voltages.

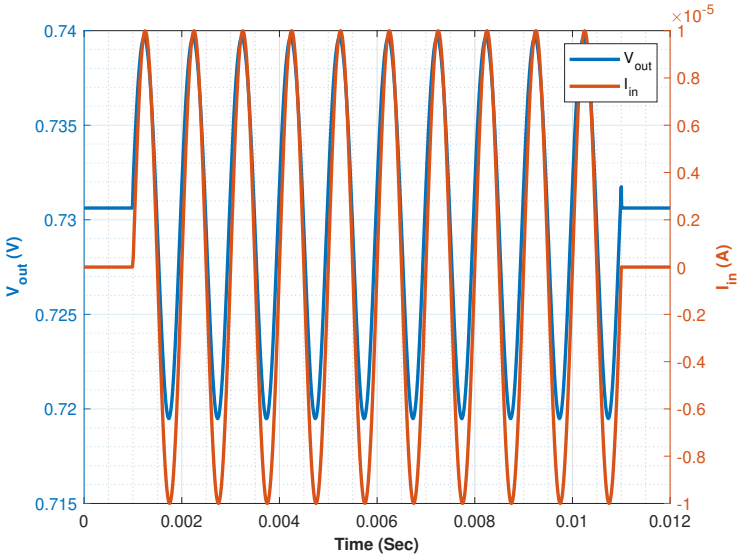


Figure 4.7. Time Domain Simulation V_{out} and I_{in}, f=1kHz.

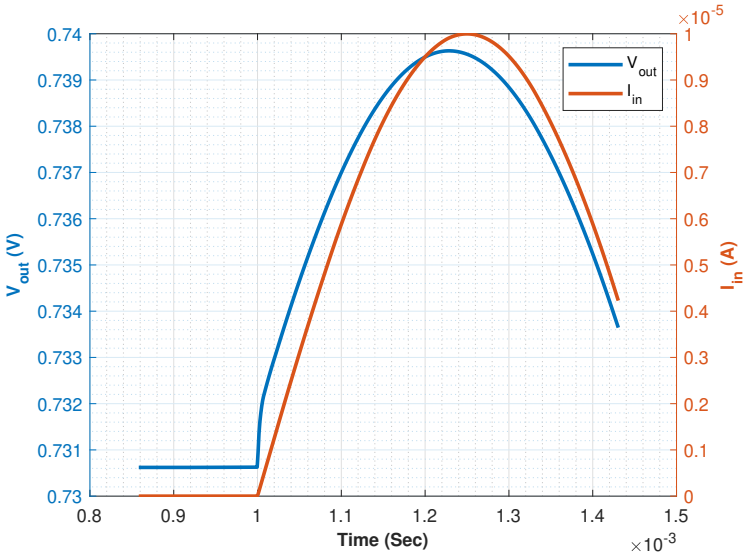


Figure 4.8. Time Domain Simulation V_{out} and I_{in}, Zoomed version of above Figure between 0.8-1.5ms.

The zoomed plot is shown to visualize NGD better in Figure 4.8. The post-layout results can be seen in 4.9 and 4.10. 4.10 shows a gain difference between the pre-layout simulation and the post-layout simulation about 5dB. In addition to that, the gain difference after the NGD operation region is 10dB. The post-layout shows a better result in terms of the gain and positive group delay gain difference. The layout of the circuit is given in 4.11, for the design α is selected as 0.125. The MOSFET dimensions used in Spice and Layout are given in Table 4.2.

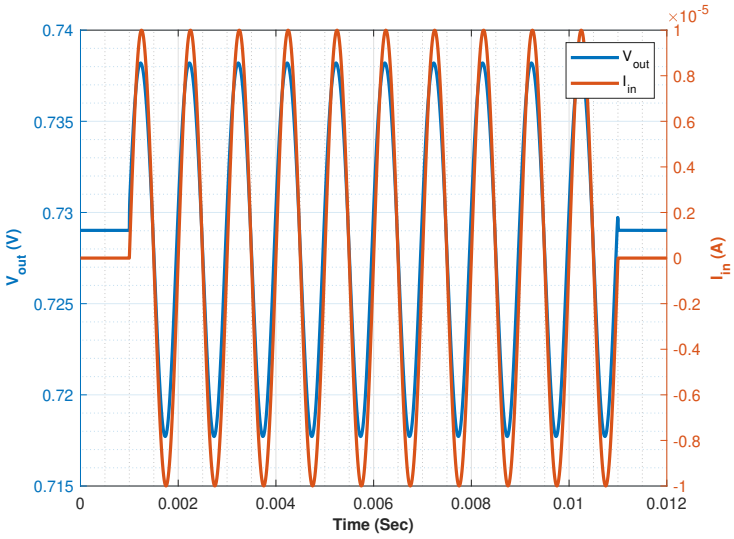


Figure 4.9. Time Domain Simulation V_{out} and I_{in}.

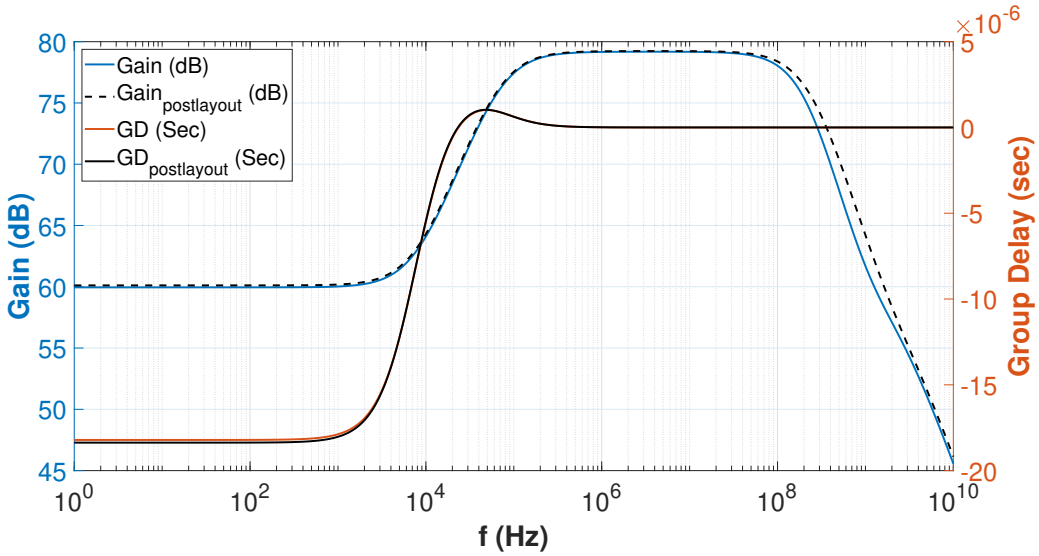


Figure 4.10. AC Response Comparison.

Moreover, the results are summarized and given in Table 4.3.

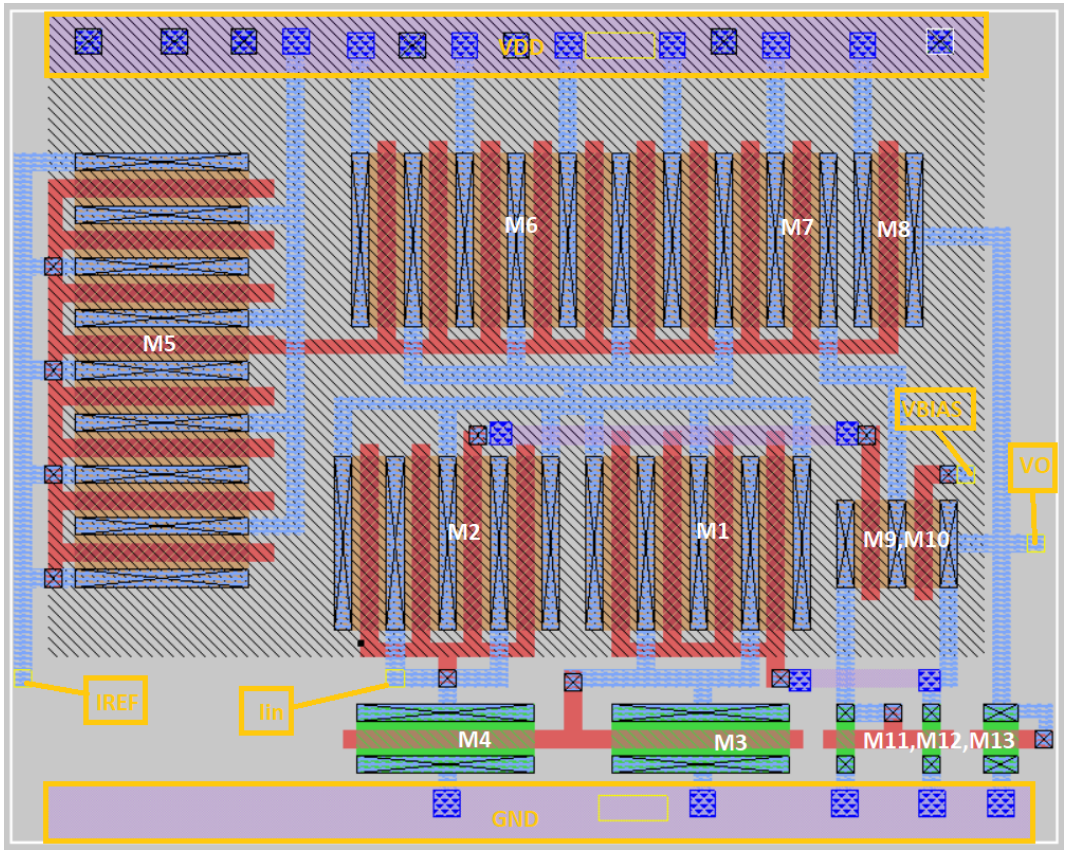


Figure 4.11. The layout of the designed NGD with the dimension of 21.6 µm × 17.1 µm.

Table 4.2. The Transistor Dimensions.

Transistors	W	L	W/L
$M_{1,2}$	$14.4\mu m$	$0.36\mu m$	40
$M_{3,4}$	$3.6\mu m$	$0.36\mu m$	10
$M_{5,6}$	$28.8\mu m$	$0.36\mu m$	80
$M_{9,10}$	$1.80\mu m$	$0.36\mu m$	5
$M_{11,12}$	$0.36\mu m$	$0.36\mu m$	1
$M_{7,8}$	$3.60\mu m$	$0.36\mu m$	10
M_{13}	$0.72\mu m$	$0.36\mu m$	2

4.3.1. Audio Processing

To give a real life example to the study an example audio record is given to the system as an input to test to circuit with different input other than sinusoidal.

Table 4.3. Brief comparison of the simulation results.

$\alpha = 0.125$	**GD** (µs)	**NGD Operation Range** (kHz)	$f_{-3dB_{hf}}$ (MHz)	**Transimpedance Gain at the NGD Operation Frequencies** (dB)
Calculation	–15.50	8.95	178	66.88
LTspice pre-layout simulation	–18.21	7.05	173	59.95
Magic post-layout simulation	–18.37	7.73	210	60.11

The time domain results are given in 4.12 and 4.13. The audio record is band-limited @7kHz to be inside the negative group delay operation range. This is achieved by using a digital filter without the LPF circuit in Figure 2.14. The signals are normalized without the offset.

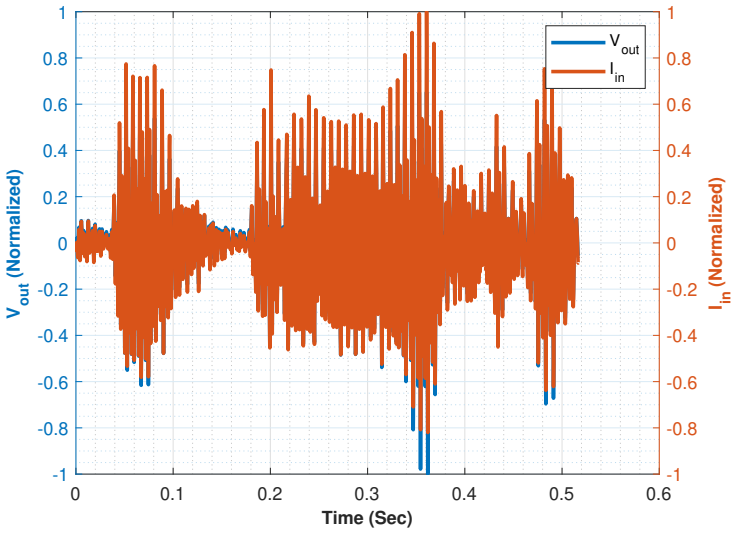


Figure 4.12. Time Domain Simulation V_{out} and I_{in} for Audio Input.

4.3.1.1. Cross-Correlation and RMSE. The calculated RMSE for normalized audio signal is 0.0470 using the equation (1.10).

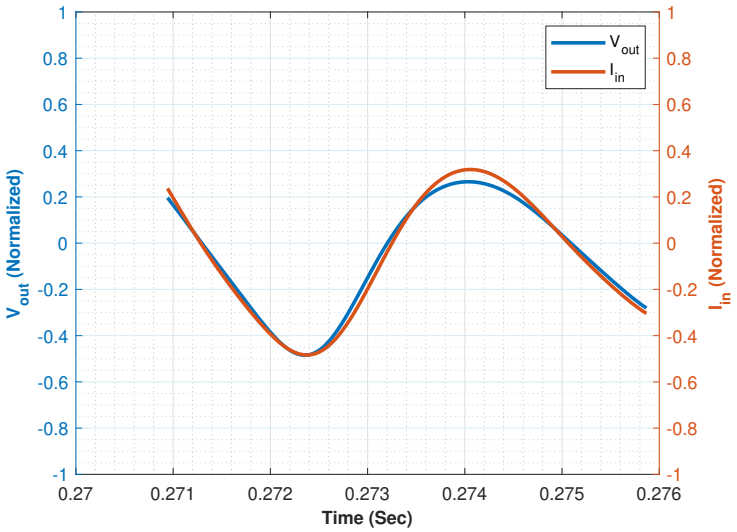


Figure 4.13. Time Domain Simulation V_{out} and I_{in}, Time Advancement, Zoom.

Moreover, the cross-correlation of the output of the NGD and the input is investigated to confirm the NGD value and the show the correlation [22]. The result is shown in Figure 4.14.

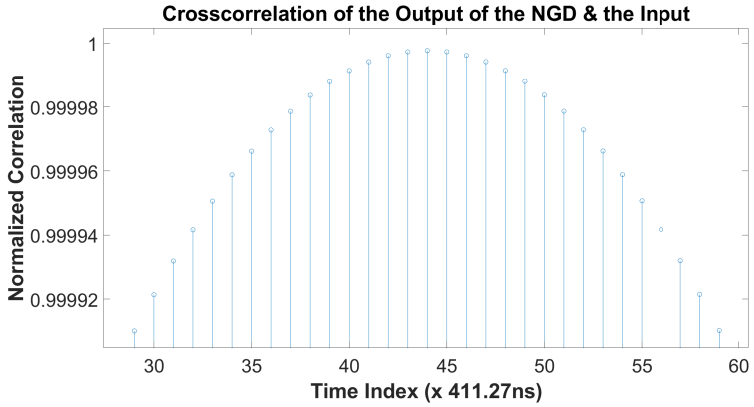


Figure 4.14. The Audio input and output of the NGDC Cross-correlation Calculation, 44x411.27ns, 18.08μs Time Advance on the Output.

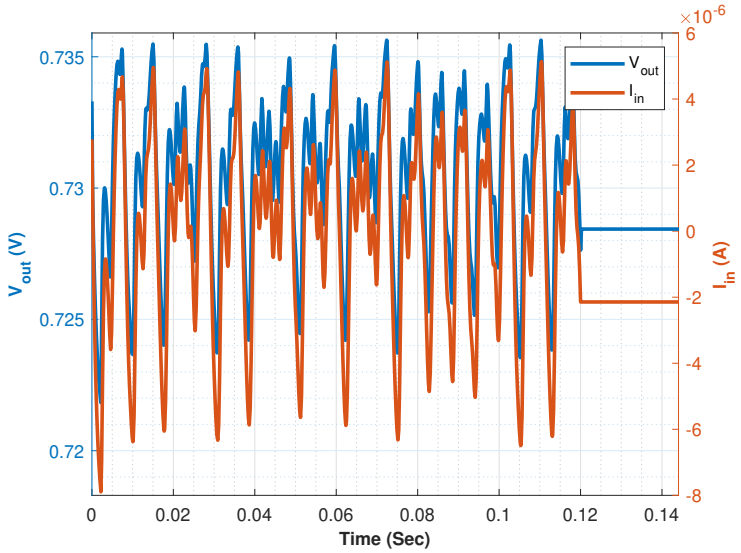
4.3.2. Mackey-Glass Discrete Time Series Analysis

The Mackey-Glass equations are used in several biological models. In addition to an audio signal and single tone sinusoidal to the NGD circuit, a discrete time Mackey-Glass input data is constructed to test the circuit similar to the study [20]. The Mackey-Glass equation [20] is given as

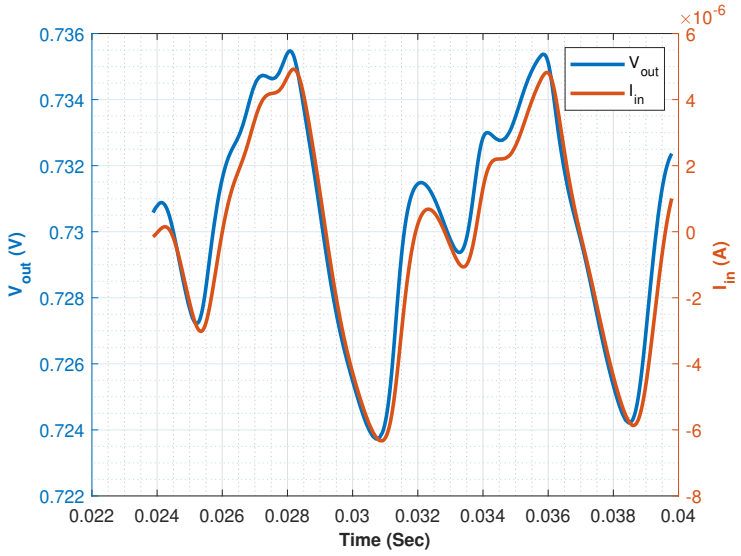
$$\frac{dx(t)}{dt} = \frac{ax(t-\tau)}{1+x(t-\tau)^{10}} - bx(t). \tag{4.21}$$

The parameters for selected to test the circuit are $a = 0.22$, $b = 0.1$, $\tau = 22$, where the τ is delay constant. The time steps are used to test circuit is 10μs. And the initial condition is selected as $1.2\text{x}10^{-6}$, to be in the current input limit in the range of tens of μA. The Time domain analysis of the circuit is given in Figure 4.15.

4.3.2.1. Cross-Correlation and RMSE. The calculated RMSE for the Mackey-Glass is 0.0331. The cross-correlation is seen in Figure 4.16. The time advance is 164μs which is well-correlated the time advance calculation using the equation (4.12) which gives 155μs with $C = 10nF$.



(a)



(b)

Figure 4.15. Simulated (a) Mackey-Glass Time Series Input to the System $C = 10nF$, (b) Zoomed Time Advance.

4.3.3. Comparison of Operation Ranges

The NGD value and the NGD circuit's operation frequency limit are inversely proportional. As a result, the F.O.M is calculated in the same way as in the study [19], given in the equation (2.21). The product of the operation range and the NGD value is given in Table 4.4. A more negative number indicates better F.O.M.

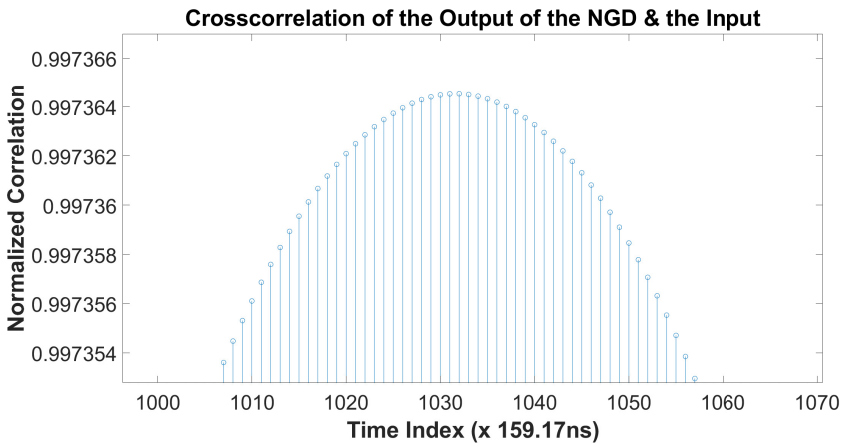


Figure 4.16. Cross-correlation of Mackey-Glass Time Series, 1032x159.17ns, 164.26μs Time Advance on the Output.

The comparison of several NGD studies are summarized in Table 4.4. [1]

Table 4.4. Comparison of the NGD Studies.

Study	**GD (µs)**	**NGD Operation Range (kHz)**	**F.O.M**	**Circuit Structure**
[6]	–74.5	3.95	-294·10^{-3}	Passive RL-RC Network
[21]	–12000	0.010 [1]	-120·10^{-3}	OA Based Active Filter
[19]	–100	1	-100·10^{-3}	Passive RL-RC Network
[10]	–0.8	10	-8·10^{-3}	Cascaded CFOA Based Active Filter
This Study	–18.37	7.73	-142·10^{-3}	OTA-C Based Active Filter

[1]The study [21] based on a Gaussian-like pulse input, the pulse width is approximately 100ms

5. EXPERIMENTAL VERIFICATION

The setup in Figure 2.14 is built with a LPF and NGDC to show NGD value is in conformity with the simulations. For the setup, Circuit 8 in Figure 2.10 is used with one AD844AN, one OP200 for LPF, a signal generator AFG3032C Tektronix, a signal analyzer MDO3104 Tektronix and a dual voltage supply SPD-3606 GW INSTEK. For the supply of the CFOA's 12V,-12V is used. The component values used for the 4th order LPF and for NGDC are given in Table 5.1 and 5.2, respectively. The given passive component values are belong to the circuit schematic in Figure 2.14.

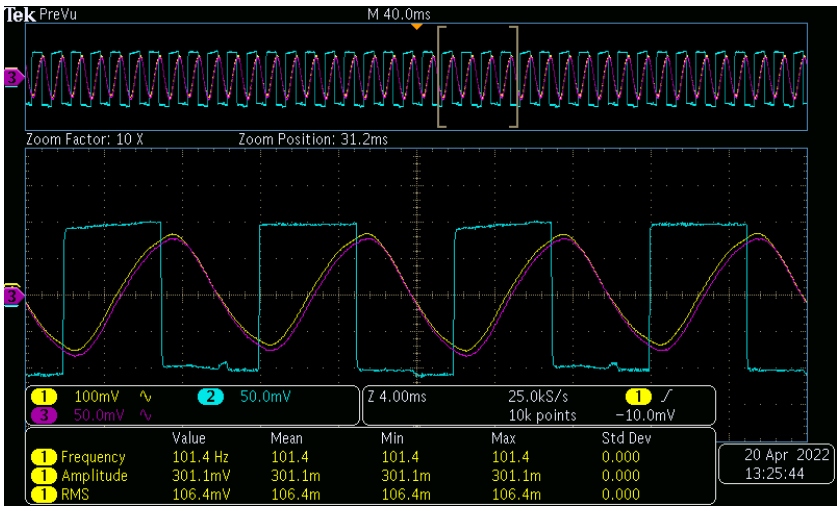
Table 5.1. The Component Values of LPF.

Components	Value
R_{1s1}	9.64 kΩ
R_{2s1}	11.76 kΩ
C_{1s1}	116 nF
C_{2s1}	100 nF
R_{1s2}	5.71 kΩ
R_{2s2}	6.57 kΩ
C_{1s2}	262 nF
C_{2s2}	95 nF

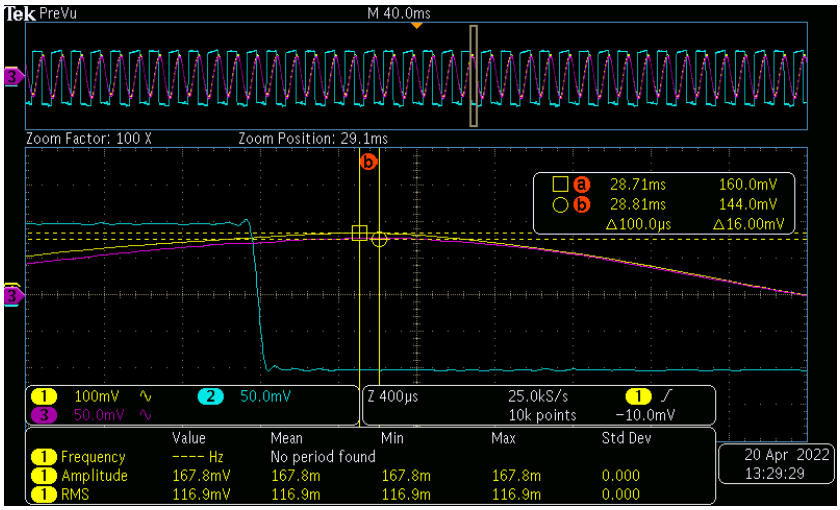
Table 5.2. The Component Values of NGDC.

Components	Value
R_1	9.8 kΩ
R_2	10.26 kΩ
R_3	9.8 kΩ
C_1	22 nF
C_2	22 nF

Moreover, to show NGDC operation range change with respect to capacitor, a single tone sinusoidal input is given to the system with 2 different set of the capacitor values. Test 1 is done with $C_1 = C_2 = 2.2$ nF, Test 2 is done with $C_1 = C_2 = 22$ nF, shown in Figure 5.2, 5.3 respectively.



(a)



(b)

Figure 5.1. (a)The input pulse signal and the output of the LPF and NGDC, (b) about 100μs NGD value, Yellow is the output of the NGDC, Purple is the output of the LPF, Blue is the input square wave.

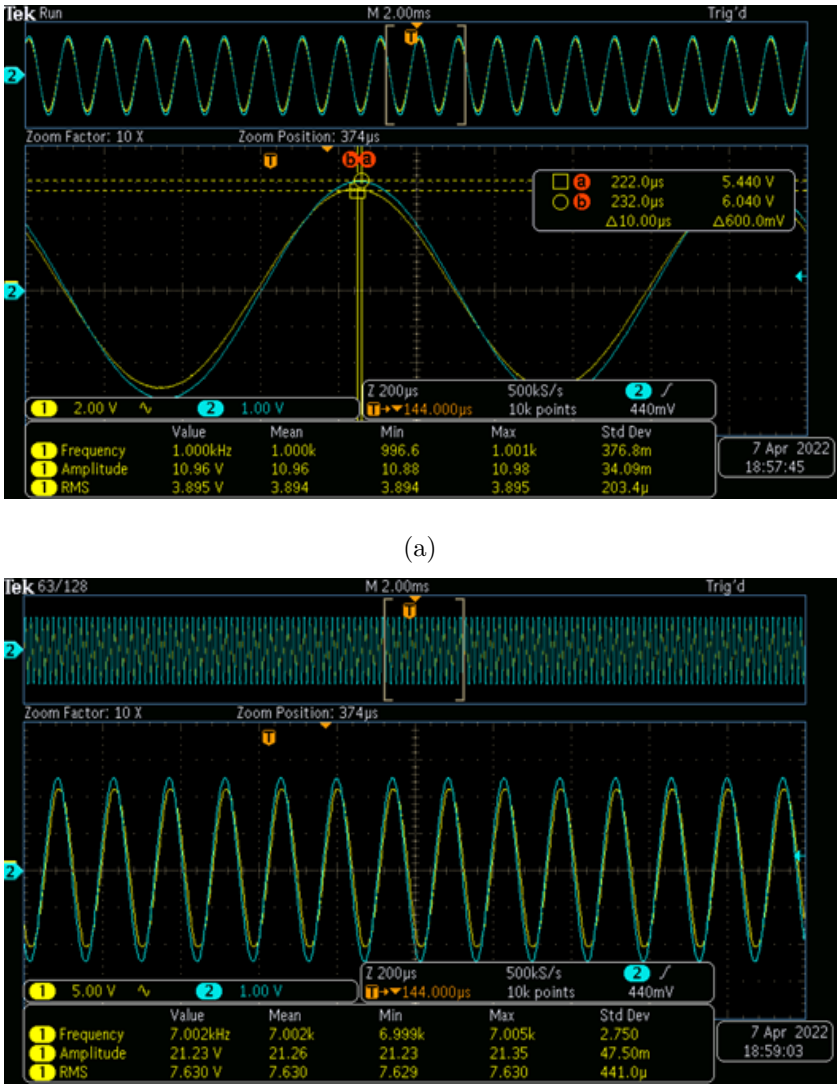
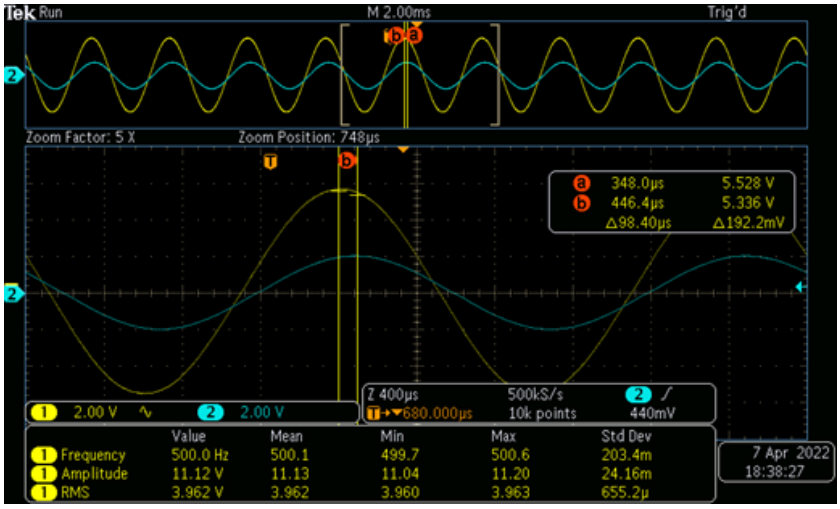
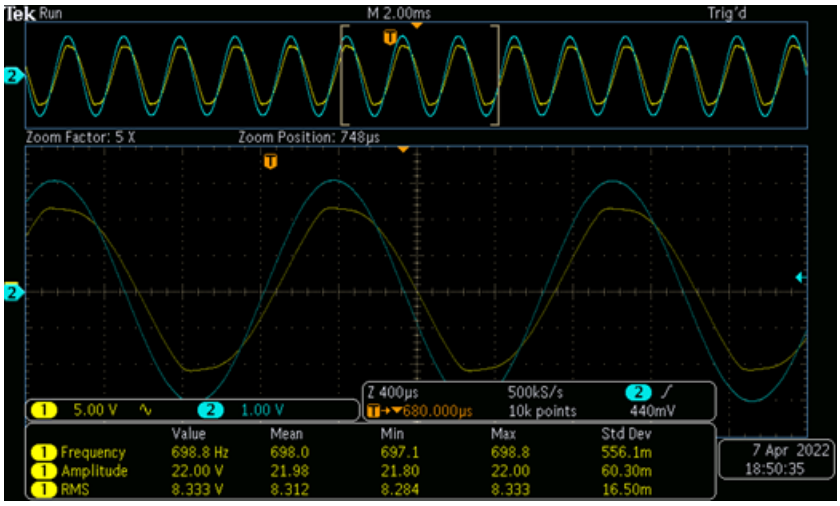


Figure 5.2. (a) 10μs NGD Result for Test 1, (b) The NGD Break at 7kHz, Yellow is the output of the NGDC, Blue is the input of the NGDC.

Applying the equation (1.10) gives us the following results summarized in Table 5.3. The comparison of error between this study and two studies are given in Table 5.4.



(a)



(b)

Figure 5.3. (a) 98.40μs NGD for Test 2, (b) The NGD Break at 700Hz, Yellow is the output of the NGDC, Blue is the input of the NGD.

Table 5.3. The Circuit 8 Results.

	Calculation	Simulation	Test 1	Test 2
NGD	108μs	101.6μs-112.5μs	10μs	98.40μs
Flat Group Delay Range	1Hz-650Hz	1Hz-650Hz	7kHz	700Hz

Table 5.4. The Comparison of Errors.

Reference	This Study	[10]	[19] (a)
NGD	100μs	800ns	100μs
Flat Group Delay Range	650Hz	10kHz	$\cong$150Hz*
RMSE (Single Tone)	0.0086	0.0674	0.0013
RMSE (Audio Record)	0.0154	0.0012	0.0053

*The NGD operation range is 1kHz [19]

6. CONCLUSION

In this thesis, a mathematical model for NGD design is established while taking into consideration earlier discoveries in the literature. The design process is described for active analog NGD circuits. A variety of application cases' functionality is also shown through simulation and experimental verification. The NGD is tested using a single sinusoidal input in the voltage and current modes for one of the CFOA-based circuits and the OTA-C-based circuit. Examples of time series and audio processing are given for the NGD circuits being discussed. It has been demonstrated that these NGD circuits provide a solution to time delay issues in electronic systems. The application areas of NGD can be summarized as in Figure 6.1.

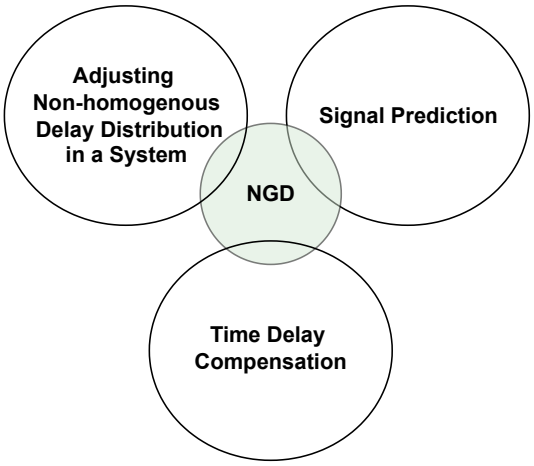


Figure 6.1. The NGD Application Areas.

6.1. Discussion

In the thesis first and second order single CFOA based new NGD topologies are introduced, giving a design methodology. The simulation results show that this kind of active NGD circuits are suitable for low frequency signals. In the range of 1 Hz – 650 Hz a [-108μs - (-112)μs], group delay is achieved with proposed component values. With this kind of active NGD circuit topologies it is shown that without gain dependency a certain NGD value can be achieved with a specific NGD operation frequency range.

Advantages and disadvantages of CFOA based active NGD circuit:

- Easy to design
- NGD value is independent from gain
- Requiring higher area compared to other studies, requires passive components
- Adjusting NGD depends on the passive component values
- Low quality and poor choice of passive components may result oscillations at the output

Furthermore a first order NGD circuit is presented which is suitable for voltage controllable NGD application areas. An example design is included to show time advance depending on the controlled voltage value.

Advantages and disadvantages of MOSFET realization of the NGD circuit:

- Easy to design
- NGD value is not directly dependent to gain
- Requiring lower area compared to other studies
- NGD is easy to adjust with voltage
- NGD operation frequency range and the NGD value is lower compared to other studies

Moreover, an OTA-C Based active NGDC is introduced without resistors. A flexible NGD value is achievable with varying capacitor values, -200 μs to -100 ns. The NGDC chip area is small compared to most other active NGDC studies. This kind of study will be suitable for a current output sensor delay compensation as the simulations show.

Advantages and disadvantages of OTA-C based transimpedance-mode NGD circuit:

- Complex design compared to other studies
- NGD value is obtained with integrated circuit
- NGD value is independent from gain
- Requiring lower area compared to other studies
- Adjusting NGD depends on the transistor sizes
- Designing a linearly distributed parallel NGD array is complex compared to other studies
- More flexible compared to other active NGD filter studies

6.2. Possible Future Applications

A NGD circuit can be utilized in a system with a temperature or pressure sensor to anticipate the input signal in addition to the examples that have been shown. A single NGD structure was also used in this study to assess the NGD value. A parallel array of the introduced circuits may provide multiple input delay compensation in later research for a system needs varying NGD values for the different specific inputs.

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APPENDIX A: AD844AN Spice Model

* AD844A SPICE Macro-model 7/91, Rev. A * JCB / PMI * * * This version of the AD844 model simulates the worst case * parameters of the 'A' grade. The worst case parameters * used correspond to those in the data sheet. * * Copyright 1991 by Analog Devices, Inc. * * Refer to "README.DOC" file for License Statement. Use of this model * indicates your acceptance with the terms and provisions in the License Statement. * * Node assignments * non-inverting input * — inverting input * — — positive supply * — — — negative supply * — — — — output * — — — — — compensation node * — — — — — — .SUBCKT AD844A 1 2 99 50 28 12 * * INPUT STAGE * R1 99 8 1E3 R2 10 50 1E3 V1 99 9 6.6 D1 9 8 DX V2 11 50 6.6 D2 10 11 DX I1 99 5 200E-6 I2 4 50 200E-6 Q1 50 3 5 QP Q2 99 3 4 QN Q3 8 6 30 QN Q4 10 7 30 QP R3 5 6 300E3 R4 4 7 300E3 C1 99 6 8.8E-15 C2 50 7 8.8E-15 * * INPUT ERROR SOURCES * GB1 99 1 POLY(1) 1 22 400E-9 150E-9 GB2 99 30 POLY(1) 1 22 450E-9 160E-9 VOS 3 1 300E-6 LS1 30 2 1E-8 CS1 99 2 1E-12 CS2 50 2 1E-12 * EREF 97 0 22 0 1 * *GAIN STAGE and DOMINANT POLE * R5 12 97 2.2E6 C3 12 97 5.5E-12 G1 97 12 99 8 1E-3 G2 12 97 10 50 1E-3 V3 99 13 5.3 V4 14 50 5.3 D3 12 13 DX D4 14 12 DX * * POLE AT 70 MHZ * R8 17 97 1E6 C4 17 97 3.18E-15 G4 97 17 12 22 1E-6 * * POLE AT 300 MHZ * R12 21 97 1E6 C8 21 97 0.318E-15 G8 97 21 17 22 1E-6 * * OUTPUT STAGE * ISY 99 50 6.1E-3 R13 22 99 16.7E3 R14 22 50 16.7E3 R15 27 99 30 R16 27 50 30 L2 27 28 6E-8 G9 25 50 21 27 33.33E-3 G10 26 50 27 21 33.33E-3 G11 27 99 99 21 33.33E-3 G12 50 27 21 50 33.33E-3 V5 23 27 0.5 V6 27 24 0.5 D5 21 23 DX D6 24 21 DX D7 99 25 DX D8 99 26 DX D9 50 25 DY D10 50 26 DY * * MODELS USED * .MODEL QN NPN(BF=1E9 IS=1E-15) .MODEL QP PNP(BF=1E9 IS=1E-15) .MODEL DX D(IS=1E-15) .MODEL DY D(IS=1E-15 BV=50) .ENDS

APPENDIX B: Transistor Spice Models

*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8 * DATE: Jul 29/05 * LOT: T55U WAF: 3003 * Temperature parameters=Default .MODEL nfet NMOS (LEVEL = 8 +VERSION = 3.1 TNOM = 27 TOX = 4.1E-9 +XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.3719233 +K1 = 0.5847845 K2 = 1.987508E-3 K3 = 1E-3 +K3B = 3.846051 W0 = 1.00001E-7 NLX = 1.66359E-7 +DVT0W = 0 DVT1W = 0 DVT2W = 0 +DVT0 = 1.616073 DVT1 = 0.4422105 DVT2 = 0.0205098 +U0 = 276.4769418 UA = -1.287181E-9 UB = 2.249816E-18 +UC = 5.695845E-11 VSAT = 1.050018E5 A0 = 1.8727159 +AGS = 0.4223855 B0 = -8.460618E-9 B1 = -1E-7 +KETA = -6.583564E-3 A1 = 0 A2 = 0.8925017 +RDSW = 105 PRWG = 0.5 PRWB = -0.2 +WR = 1 WINT = 0 LINT = 1.509138E-8 +XL = 0 XW = -1E-8 DWG = -3.993667E-9 +DWB = 1.211844E-8 VOFF = -0.0926198 NFACTOR = 2.4037852 +CIT = 0 CDSC = 2.4E-4 CDSCD = 0 +CDSCB = 0 ETA0 = 2.64529E-3 ETAB = -1.113687E-5 +DSUB = 0.0107822 PCLM = 0.7114924 PDIBLC1 = 0.1861265 +PDIBLC2 = 2.341517E-3 PDIBLCB = -0.1 DROUT = 0.708139 +PSCBE1 = 8E10 PSCBE2 = 9.186022E-10 PVAG = 5.128699E-3 +DELTA = 0.01 RSH = 6.5 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11 +KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 +UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 +WL = 0 WLN = 1 WW = 0 +WWN = 1 WWL = 0 LL = 0 +LLN = 1 LW = 0 LWN = 1 +LWL = 0 CAPMOD = 2 XPART = 0.5 +CGDO = 7.9E-10 CGSO = 7.9E-10 CGBO = 1E-12 +CJ = 9.604799E-4 PB = 0.8 MJ = 0.3814692 +CJSW = 2.48995E-10 PBSW = 0.8157576 MJSW = 0.1055989 +CJSWG = 3.3E-10 PBSWG = 0.8157576 MJSWG = 0.1055989 +CF = 0 PVTH0 = -4.358982E-4 PRDSW = -5 +PK2 = 2.550846E-4 WKETA = 1.466293E-3 LKETA = -7.702306E-3 +PU0 = 23.8250665 PUA = 1.058432E-10 PUB = 0 +PVSAT = 1.294978E3 PETA0 = 1.003158E-4 PKETA = -3.857329E-3) * .MODEL pfet PMOS (LEVEL = 8 +VERSION = 3.1 TNOM = 27 TOX = 4.1E-9 +XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.3955237 +K1 = 0.5694604 K2 = 0.0291529 K3 = 0.0997496 +K3B = 13.9442535 W0 = 1.003165E-6 NLX = 9.979192E-8 +DVT0W = 0 DVT1W = 0 DVT2W = 0 +DVT0 = 0.5457988 DVT1 = 0.2640392 DVT2 = 0.1

+U0 = 118.0169799 UA = 1.591918E-9 UB = 1.129514E-21 +UC = -1E-10 VSAT = 1.545232E5 A0 = 1.6956519 +AGS = 0.3816925 B0 = 4.590751E-7 B1 = 1.607941E-6 +KETA = 0.0142165 A1 = 0.4254052 A2 = 0.3391698 +RDSW = 168.2822665 PRWG = 0.5 PRWB = -0.5 +WR = 1 WINT = 0 LINT = 3.011839E-8 +XL = 0 XW = -1E-8 DWG = -4.05222E-8

+DWB = 4.813652E-9 VOFF = -0.099839 NFACTOR = 1.8347784 +CIT = 0 CDSC = 2.4E-4 CDSCD = 0 +CDSCB = 0 ETA0 = 0.201776 ETAB = -0.1409866 +DSUB = 1.0474138 PCLM = 1.4195047 PDIBLC1 = 2.422412E-4 +PDIBLC2 = 0.022477 PDIBLCB = -1E-3 DROUT = 1.228009E-3 +PSCBE1 = 1.245755E10 PSCBE2 = 3.598031E-9 PVAG = 15.0414628 +DELTA = 0.01 RSH = 7.5 MOBMOD = 1 +PRT = 0 UTE = -1.5 KT1 = -0.11 +KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 +UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 +WL = 0 WLN = 1 WW = 0 +WWN = 1 WWL = 0 LL = 0 +LLN = 1 LW = 0 LWN = 1 +LWL = 0 CAPMOD = 2 XPART = 0.5 +CGDO = 6.34E-10 CGSO = 6.34E-10 CGBO = 1E-12 +CJ = 1.177729E-3 PB = 0.8467926 MJ = 0.4063096 +CJSW = 2.417696E-10 PBSW = 0.851762 MJSW = 0.3387253 +CJSWG = 4.22E-10 PBSWG = 0.851762 MJSWG = 0.3387253 +CF = 0 PVTH0 = 1.406461E-3 PRDSW = 11.5261879 +PK2 = 1.718699E-3 WKETA = 0.0353107 LKETA = -1.277611E-3 +PU0 = -1.4642384 PUA = -6.79895E-11 PUB = 1E-21 +PVSAT = 50 PETA0 = 1.003152E-4 PKETA = -3.103298E-3) *