SIGMA-DELTA DITHERING BASED FREQUENCY SYNTHESIS AND MODULATION FOR DCS-1800

by

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ABSTRACT

SIGMA-DELTA DITHERING BASED FREQUENCY SYNTHESIS AND MODULATION FOR DCS-1800

Today cell phone industry tends to increase the capabilities of the cell phones and at the same time minimize the cost. This trend reflects itself to frequency synthesizer design. Hence, a cheap and efficient way of designing such a frequency synthesizer is suggested in this thesis. The design aims to meet DCS-1800 specifications. The designed frequency synthesizer is based on digital circuits as much as possible. To design such a synthesizer, some different synthesizer and modulation topologies are studied at system level. After deciding on the topology, circuit level design was performed and a full CMOS frequency synthesizer using standard 0.18 μm technology was obtained.

ÖZET

DCS-1800 İÇİN SIGMA-DELTA KARARSIZLIĞI BAZLI FREKANS SENTEZLEYİCİ VE MODULASYONU

Günümüzde cep telefonu endüstrisi, cep telefonlarının maliyetini düşürmeye çalışmanın yanında yüksek veri transfer hızlarını da hedeflemektedir. Dolayısıyla bu yaklaşım frekans sentezleyiciler için de geçerlidir. Bu projede böyle bir frekans sentezleyici tasarlamak için ucuz ve verimli bir yol önermeye çalıştık. Tasarıma DCS1800 standartına uygun olacak şekilde başlandı. Tasarlanan frekans sentezleyici günümüz teknolojisinin el verdiği ölçüde sayısaldır. Böyle bir frekans sentezleyici tasarlamak için sistem seviyesinde farklı frekans sentezleme yöntemleri denendi. Yönteme karar verilince, çalışmalar transistor seviyesinde devam etti ve tümüyle 0.18 μm CMOS olan bir frekans sentezleyici tasarlandı.

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LIST OF SYMBOLS/ABBREVIATIONS

A	Amplitude
f	frequency
f_{ref}	Reference frequency
I_{in}	Input current to the loop filter
K_{pd}	Gain of the PFD
K_{vco}	Gain of the VCO
m	Order of the Σ-Δ modulator
N	Number
V_{out}	Ouput voltage of the loop filter
ωt	Omega in radians
Φ	Phase symbol
Φsd	Phase contribution of the Σ-Δ modulator
Φout	Output phase
ΣΔ	Sigma-Delta

ADS	Advanced Design System
BW	Band-width
CMOS	Complementary Metal Oxide Semiconductor
dBc/Hz	dB with respect to carrier per hertz
DCO	Digitally Controlled Oscillator
DPA	Digital Power Amplifier
EDGE	Enhanced Data Rates for Global Evolution
FCW	Frequency Command Word
FM	Frequency Modulation
gm	Transconductance
GMSK	Gaussian Minimum Shift Keying
G(s)	Open Loop gain of the system
H(s)	Closed loop gain of the system
LO	Local Oscillator

NMOS	N type Metal Oxide Semiconductor
PFD	Phase Frequency Detector
PMOS	P type Metal Oxide Semiconductor
ppm	piece per million
PVT	Process-Voltage-Temperature
PLL	Phase Locked Loop
PM	Phase Modulation
QAM	Quadrature Amplitude Modulation
RMS	Root mean square
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	Wireless Local Area Network
VCO	Voltage Controlled Oscillator
Z(s)	Response of the filter
8PSK	8 Phase Shift Keying

1. INTRODUCTION

Modern handsets are designed to handle high data rates. However, for battery powered handsets it is hard to preserve battery charge for a long time while transmitting and receiving intense data. Standards such as WiMAX and WLAN are data intensive standards. Although these are the fundamental objectives, it is hard to design a system without dividing the problem into smaller blocks. In these blocks, one of the most challenging parts is the low power transmitter design. Standards mentioned above use complex modulation schemes (e.g. 64 QAM) where both the amplitude and the phase of the signal carry the information, hence both are modulated. In such a case, a linear power amplifier whose efficiency is very low (%20) has to be used to amplify the modulated signal. As this scheme is not efficient, a linear power amplifier cannot be used in such a design.

In 2005 R. Staszewski et al. [1] introduced a more robust polar loop transmitter for 8PSK (EDGE) using a fully digital amplitude and phase modulator. In the architecture, there are mainly a Digitally Controlled Oscillator (DCO), and a Digitally Controlled Power Amplifier (DPA). A high speed 225 MHz Σ-Δ dithering is implemented to improve the DCO resolution to less than 1 KHz. DPA is saturated near-class-E amplifier. The biggest advantage of this architecture is the fully digital nature of both frequency and amplitude modulations. This architecture is more robust to process-voltage-temperature (PVT) variations and delay mismatches between the different modulation paths.

As that mentioned above, the modulation scheme in WLAN is 16-QAM or 64-QAM, which means that both amplitude and phase are modulated. To do phase and envelope simulation at same design is a very hard task, because bandwidth of such a design is very wide. Thus, it is better to start with only phase modulation, which is the objective of this thesis and investigate the extension to WLAN in a second stage.

Hence, the objective of this thesis is to design a frequency synthesizer that meets DCS-1800 specifications. These specifications are well known and documented. The frequency synthesizer is based on digital circuits as much as possible. To design such a synthesizer, some different synthesizer and modulation topologies were studied at the system level. After deciding on the topology, then studies were continued on the circuit level.

1.1. Frequency Synthesis in Radio

In every radio transmitter and receiver there is a local oscillator (LO) independent of the architecture. LO is necessary in transmitter path to up-convert the signal and in receiver path to down-convert the signal. LO has to be tunable because modern communication channel systems have to cover the entire band, not only the channel. For example, in our target standard DCS 1800 there are up to 885 channels [2]. And the frequency grid that the synthesized frequency has to be placed on should be very dense and cover the channel spacing. Hence, the frequency synthesizer is used as LO in radio and it may be the most critical block in the entire mobile communication systems.

1.2. Frequency synthesizer topologies

There are three generalized synthesizer topologies. These are:

- Direct Analog
- Direct Digital
- Indirect or Phase Locked Loop based

Direct analog technique was used in 1920's and this is not used anymore except instrumentation because it needs many analog filters. The outputs of these filters are combined together, multiplied, subtracted, so on to generate the expected frequency. This method costs hundreds of thousands of dollars.

For the technique known as Direct Digital, direct means there is no feedback, meaning that there is no error correction.

Indirect or Phase Locked Loop (PLL) based technique uses the idea of feedback. The output signal is fed back to the reference signal and an error signal is generated. By trying to minimize the error, the required frequency is synthesized. In this thesis, this technique is used, which is the most common topology of modern frequency synthesizers.

1.3. Reasons for why PLL based frequency synthesizer is chosen

To understand why PLL is chosen among the others, the design criteria must be analyzed and the mathematical background of the frequency synthesis idea must be understood.

1.3.1. Phase Noise in Oscillators

An ideal oscillator would have an ideal sinusoidal waveform which can be written as:

$$V(t) = A\sin(\omega t + \Phi)$$

However, in real world there is nothing that can generate ideal sinusoidal waveform. Both amplitude and phase are corrupted by noise. The mathematical formula of the actual waveform can be written as:

$$V(t) = A(t)\sin(\omega t + \Phi(t))$$

The amplitude noise is not a severe problem. It can be removed easily by hard filtering or thresholding methods; however, this is not the case for phase noise. Once phase of a signal is corrupted by noise, the waveform loses its periodicity. In Figure 1.1, voltage vs time graph can be seen. Because signal is corrupted by the phase noise it loses

its periodicity and timing jitter is seen. The spectrum of an ideal oscillator and of a practical one can also be seen in Figure 1.2.

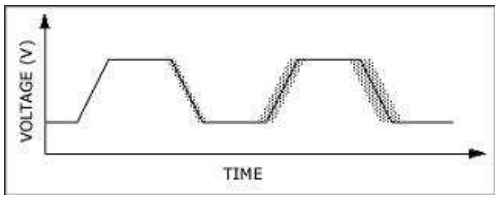


Figure 1.1. Clock jitter [3]

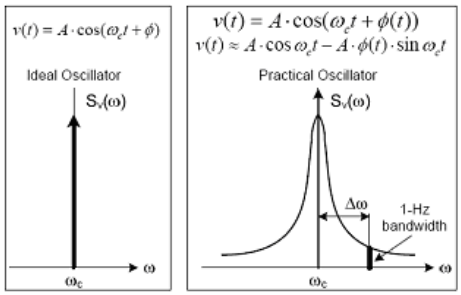


Figure 1.2. Phase noise [4]

If our synthesizer were built for only one radio signal, phase noise would not be the most important criterion, because there would be only one transmitter and only one receiver. However, in today's world, there are lots of transmitters and receivers. Even in a single handset, communicating in duplex manner, transmittion and reception occur at the same time. This example is illustrated in Figure 1.3. Assume that there are two transmitters and one receiver. The frequency of wanted signal is ω_{c2} whereas the interferer's is ω_{c1}. As it is seen in the figure, the desired signal has smaller amount of power than interferer has. Also, assume that the desired signal has a perfect noise profile. On the other hand, phase profile of the output of the interferer transmitter does not lay in the communication specifications. If this is the scenario, the skirt of the interferer signal may destroy the desired signal or even cut the communication.

The example shown in Figure 1.3 was for unideal transmitter noise profile. If our receiver has a bad noise profile, then what happens? The next figure illustrates this scenario. Assume again that there are two transmitters whose noise profiles are perfect; however our receiver has a bad phase noise profile like in the Figure 1.4. In

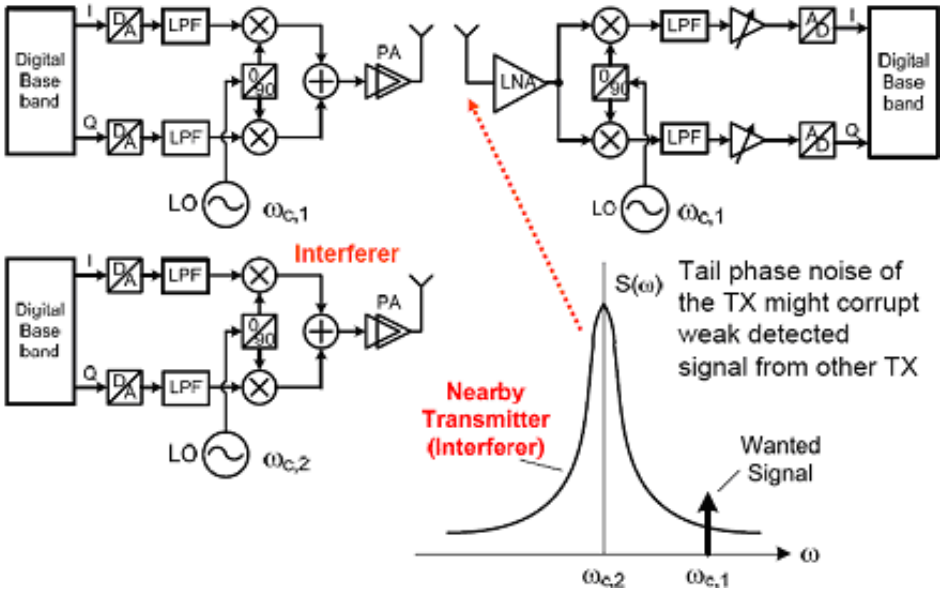


Figure 1.3. Phase noise transmitter side [4]

this scenario, again desired signal is weaker than the interferer. After passing through the LNA, the interferer and the desired signal are convolved with the spectrum of the receiver LO output, and results somehow like in the figure. Hence signal due to conversion of the interferer corrupts the desired signal.

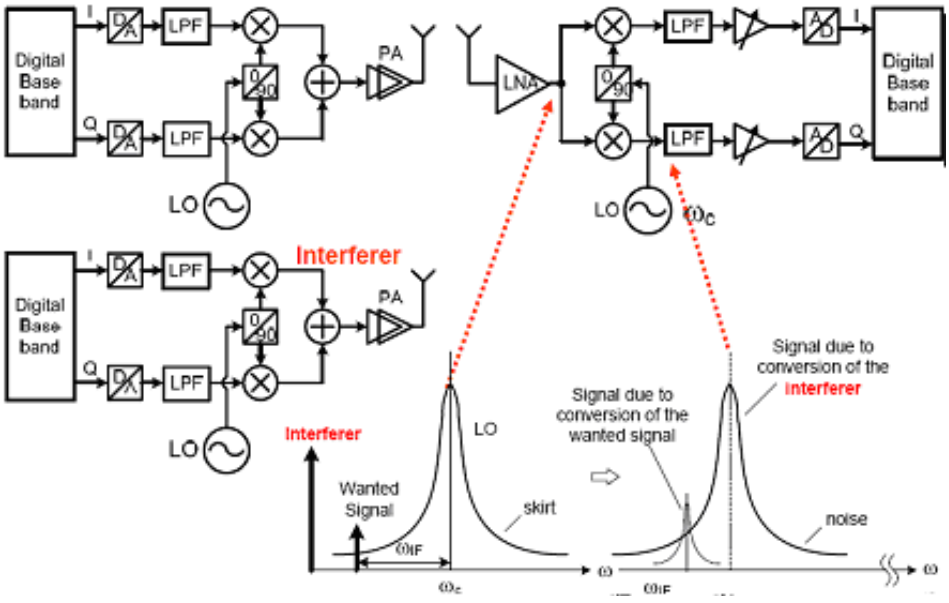


Figure 1.4. Phase noise receiver side [4]

These examples are to explain why wireless communication systems impose stringent phase noise requirements. Seeing that phase noise is a serious problem, one should

find a way to remove this error. However, as mentioned above, this is a difficult task. Unless there is some kind of feedback to correct phase error, we had to live with that error. In fact this is the answer of why we have chosen the PLL based topology.

In the next chapter, how a PLL works is explained to have an idea about the essence of the design.

2. HOW DOES A PLL WORK?

It is better to explain how a PLL works briefly before going ahead through the necessary calculations for the design. First of all, there must be a reference signal source for the PLL to work. PLL cannot generate the needed frequency from nothing. This reference frequency is one input of the phase/frequency detector (PFD). The other input of the PFD is the divided synthesized frequency. The PFD generates pulses according to the difference between these two signals. These pulses control the charge pump afterwards. Charge pump changes the tune voltage of the voltage controlled oscillator (VCO) by injecting plus and minus currents to the loop filter. The frequency at the output of the VCO is controlled via this tune voltage. This output frequency is the needed synthesized frequency. This frequency is divided by a number N. Through this division, it is possible to carry out most operations in low frequency. This divided frequency is then supplied to the PFD. Hence, the loop is closed. In Figure 2.1, the overall system can be seen.

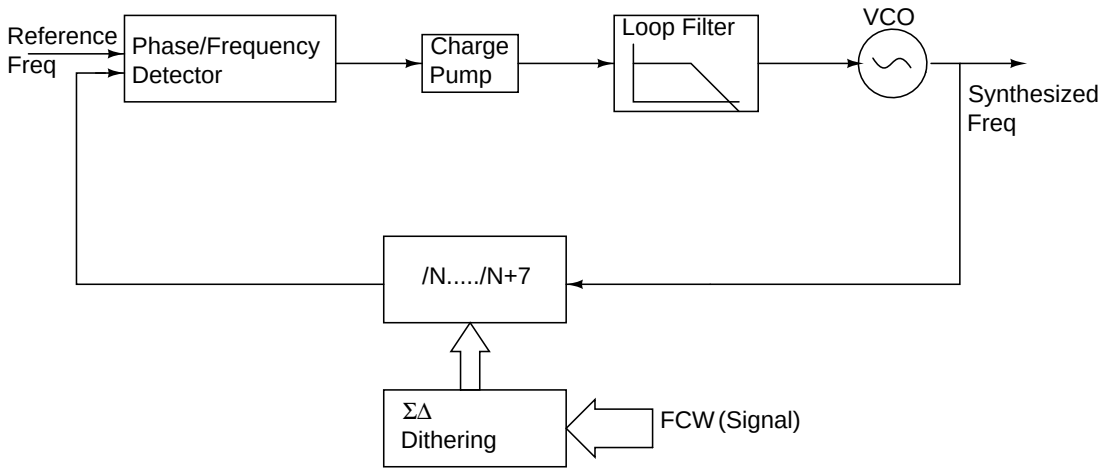


Figure 2.1. Overall PLL

For example, if the frequency of the divided signal is higher than the reference frequency, the PFD generates down pulses. These down pulses sink current from the loop filter. So the tune voltage of the VCO decreases. Hence, the synthesized frequency decreases if the gain of the VCO is positive. The divided frequency is also decreased. The pulses generated by the PFD become narrower. This continues until the reference

signal and the divided frequency are locked to each other. If the gains of the blocks are not chosen well, then stability problems occur. These calculations are done in the following chapter.

If a design is only capable of dividing the output signal to an integer number N, then the synthesized frequency is the integer multiple of the reference frequency. However if the division ratio can be somehow changed, then generated signal has a finer resolution. This operation can be achieved by using fractional-N PLL. This can be explained roughly as the following. For example division ratio can be chosen as N or N+1. By choosing division ratio as N for constant cycle and N+1 for another constant cycle, then any fraction can be obtained between these two integers. Hence the synthesized frequency is calculated as N+fraction times the reference frequency. However this approach generates undesired spurs in the spectrum of the output. An effective method to solve the generation of the spurs problem is to use a $\Sigma\Delta$ modulator [5] to randomize the channel-selection bits. $\Sigma\Delta$ modulator pushes the phase noise and the spurs to higher frequencies, which are suppressed by the loop filter.

As it was mentioned in the introduction, frquency synthesizers are used as local oscillators (LO). For phase modulation (PM) or frequency modulation (FM), baseband signal has to be upconverted to the higher bands, which is also the case for GMSK modulation. There are different topologies to upconvert the baseband signal. One technique is to use analog mixers, the other technique is to inject the signal directly as voltage source to VCO, or changing the input of the $\Sigma\Delta$ modulator , which is called as frequency command word (FCW). The last technique is also called direct modulation.

The system level design of the mentioned above is explained in Chapter 3.

3. DESIGN

3.1. Specifications and Requirements of the DCS1800 Standard

The aim for the design is to meet the specifications of the DCS 1800 which are:

- Frequency Band (DCS): 1710.2 MHz 1784.8 MHz
- Channel spacing: 200 KHz
- Tolerated Frequency Error: 0.1 ppm
  - Crystal frequency: 10 ppm + (calibrated with base station)
- RMS Phase error: 3°
- Phase Noise:-112dBc/Hz@400Khz and -154 dBc/Hz@20MHz
- Settling Time 245 s
- Data Rate ($1/T_b$): 270.833 Kbit/s
- GMSK Modulation :
  - Gaussian filter BW: BT_b=0.3
  - Frequency Modulation: 67.708 KHz

To meet these specifications, two different topologies in the Figure 3.1 and Figure 3.2 are chosen to start with. In fact, for the frequency synthesizer part they are same, however they modulate the phase in different manners. In the topology in Figure 3.1, signal is given only as frequency command word (FCW) whereas in the topology in Figure 3.2, signal is given from two different ways, as FCW and directly to VCO.

To decide which topology will be used, specifications should be checked and system simulations should be done. Modulating only from $\Sigma\Delta$ block is easier to design in circuit level, whereas two point modulation gave better results which will be clear after seeing some results. Although both topologies were analyzed, the former topology was chosen to start with, because the system simulations indicate that the simpler solution yields sufficient results.

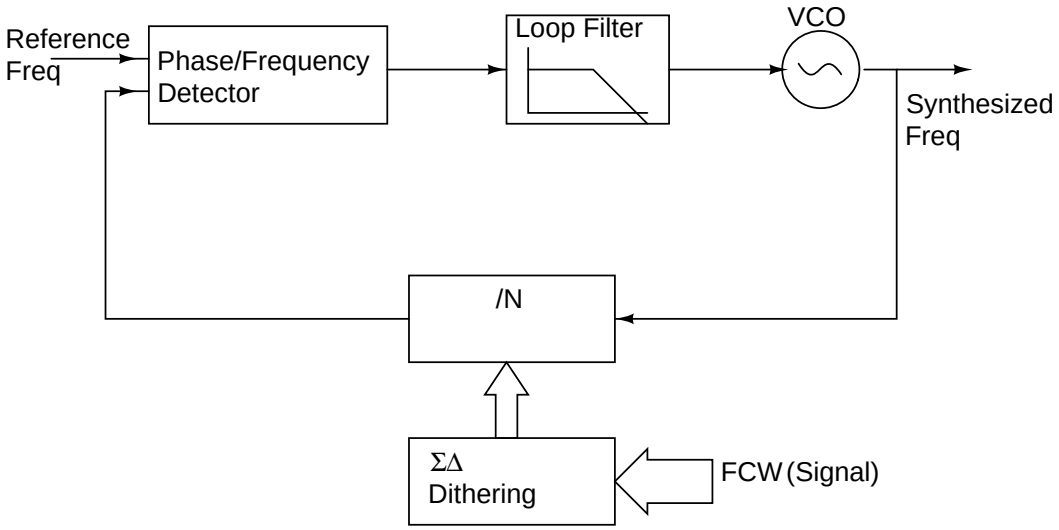


Figure 3.1. Fractional-N frequency synthesizer

After deciding the topology, one should determine the bandwidth of the PLL. To determine the bandwidth, first of all, rms phase error and phase noise should be considered. For our case RMS phase error is 3° and the needed cutoff frequency of the PLL is given by the following equation [6]:

$$f_c < \left[\left(\frac{\varphi_{rms}}{\sqrt{2}} \right)^2 \frac{m + 0.5}{(2\pi)^{2m}} \right]^{1/(2m-1)} \cdot f_{ref}$$

where:

- m: is the order of the sigma-delta
- f_c: cut off frequency of the PLL
- φ_{rms}: rms phase error
- f_{ref}: reference frequency and it is chosen to be 26 MHz for our case

According to this formula

- If m=2; f_c should be smaller than 338 kHz
- If m=3; f_c should be smaller than 984 kHz

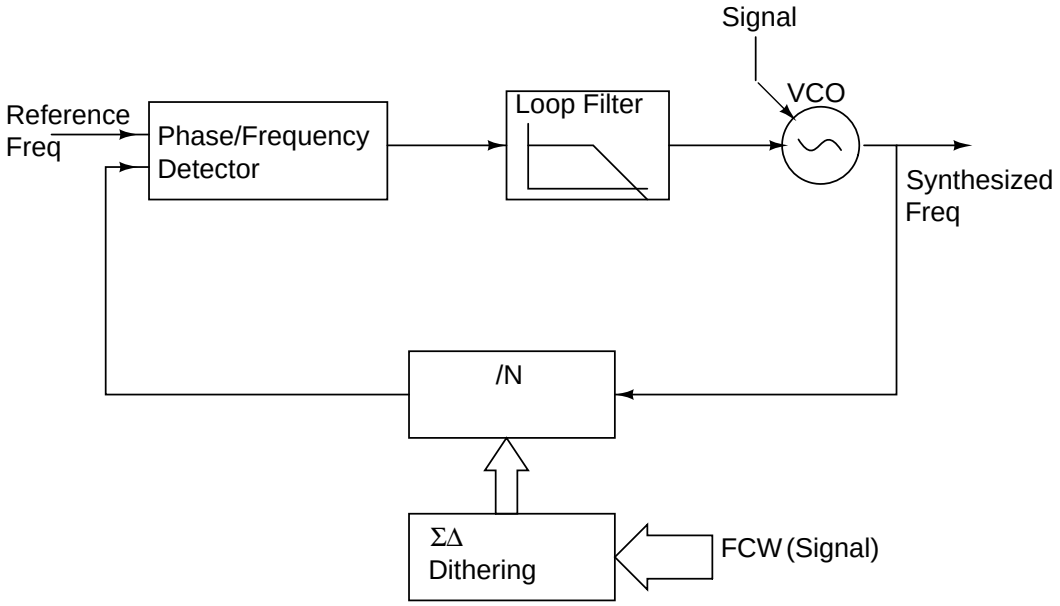


Figure 3.2. Fractional-N frequency synthesizer capable of two point modulation

Also, GSM uses GMSK modulation technique and typically normalized bandwidth for GMSK modulation, which is given as BT. For DCS1800 standart it is 0.3 and 1/T is 270.833 Kbits/sec. Typically cutoff frequency of the PLL is chosen bigger than B, for process-voltage-temperature variations (PVT) as described in many references. So, if f_cT is chosen as 0.5, then f_c should be 145 kHz. Usually jitter peaking is a problem so f_c is better to be chosen as 200 kHz which is still far below than the necessary frequency according to rms phase error calculation.

To decide the order of the filter phase noise specifications should be checked. Phase Noise is defined as the following formula [1]:

$$L\left(\Delta\omega\right) = 10\log 10\left\{\frac{\text{noise power in a 1 Hz bandwidth at frequency } \omega c + \Delta\omega}{\text{carrier power}}\right\}$$

and given by the following formula [7] at wanted frequency f:

$$L(f) = 10\log\left(\frac{1}{12}\frac{f_{ref}}{f^2}\left[2\sin\left(\frac{\pi f}{f_{ref}}\right)\right]^{2m}|H(s)|^2\right)$$

where:

- f_{ref}: Reference frequency
- |H(s)|: Magnitude of closed loop transfer function of the PLL at that frequency

The linear model of the PLL can be seen in Figure 3.3. By considering the model H(s) can be written as

$H(s) = \frac{\Phi out}{\Phi sd}$ (Φ_{sd} is phase contribution of SigmaDelta)

where:

G(s) is the open loop transfer function of the PLL and given by

$$G(s) = \frac{Kvco(s) \times Kpd \times Z(s)}{N}$$

where Z(s) is the transfer function of the loop filter and is obtained by finding V_{out} / I_{in}. V_{out} is the tuning voltage of the VCO and I_{in} is the phase frequency detector output current.

As it was mentioned above, the closed loop transfer function $H(s) = \frac{\Phi out}{\Phi sd}$ (Φsd is phase contribution of SigmaDelta) is:

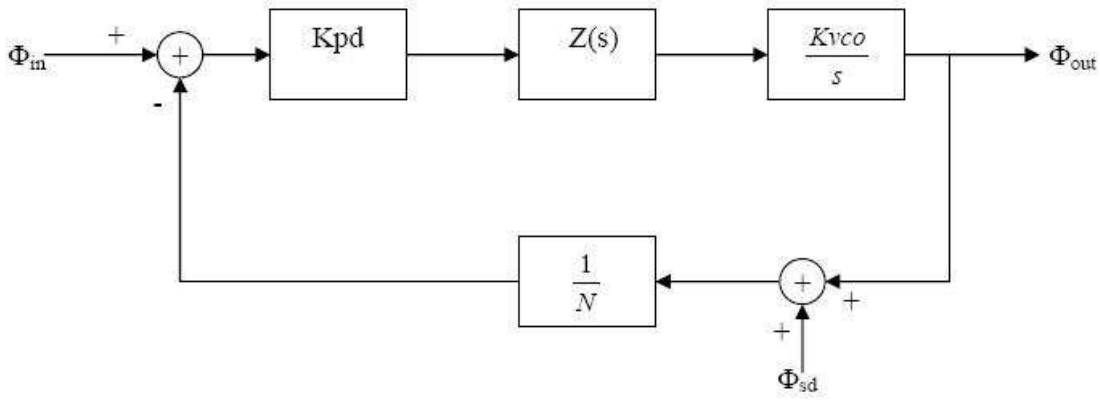


Figure 3.3. Linear model of the PLL

$$= \frac{G(s)}{1+G(s)}$$

To simplify the calculations it can be assumed that G(s) is much smaller than 1. So closed loop transfer function becomes:

$$\mathrm{H(s)} \approx \mathrm{G(s)}$$

Typically first order filters such as the one in Figure 3.4 are employed in PLL's.

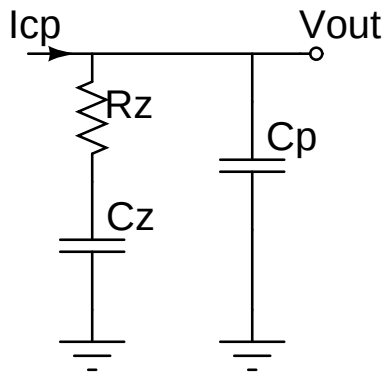


Figure 3.4. A first order filter

$Z(s) = \frac{Vout}{Iin}$ of 1^{st} order filter is found as:

$$Z(s) = \frac{1 + sRzCz}{sCz + sCp + s^2CzCpRz}$$

For the design, gain of the Voltage Control Oscillator (K_{vco}) is chosen to be 20π MHz/Volt

$$Kvco(s) = \frac{Kvco}{s}$$

Gain of the phase frequency detector (K_{pd}) is chosen to be 1 mA/2π

$$Kpd = \frac{Ipd}{2\pi}$$

Open Loop gain of the PLL is then given by:

$$G(s) = \frac{Kvco \times Ipd \times Z(s)}{2\pi \times N \times s}$$

Z(s) can also be written as follows:

$$Z(s) = \frac{(1 + s/\omega_z)}{A_0 s(1 + s/\omega_p)} with \rightarrow A_0 = C_z + C_p \& \omega_z = \frac{1}{C_z R_z} \& \omega_p = \frac{C_z + C_p}{C_z R_z C_p} \approx \frac{1}{R_z C_p}$$

for $\omega >> \omega_p \& C_z >> C_p$ $|Z(s)| \approx \left|\frac{1}{jC_p\omega}\right|$. Open loop cross over frequency ω_c is given by $\omega_c = \frac{K_{pd}K_{vco}R_z}{N}$. The closed loop transfer function can be assumed to be equal to the open loop transfer function, H(s) $\approx$ G(s).

$$|H(j\omega)| \approx |G(j\omega)| = \left|\frac{Kvco \times Kpd}{N \times j\omega \times j\omega C_p}\right| = \frac{\omega_c \times \omega_p}{\omega^2}$$

For hand calculation, the formula above is very efficient to use for phase noise constraint calculation. Hence phase noise formula becomes:

$$L(f) = 10 \log \left(\frac{f_{ref}}{12 f^2} \times \left[\sin(\frac{2f\pi}{f_{ref}}) \right]^{2m} \times \left[\frac{\omega_c \times \omega_p}{(2f\pi)^2} \right]^2 \right)$$

For f << f_{ref}

$$\sin(\frac{2\pi f}{f_{ref}}) \approx \frac{2\pi f}{f_{ref}}$$

and if m = 3 :

$$L(f) = 10 \log \left(\frac{f_{ref}^{-5} \times (2\pi)^2}{12} \times (\omega_c \times \omega_p)^2 \right)$$

For our case f_{ref} = 26 MHz. To obtain 1,742 GHz, N = 67, ω_c should be around $2\pi f_c$ where f_c is found above to be 200 kHz. For phase margin $\omega_p > 2\omega_c$ for f = 20 MHz => L(f) = -110 dB

and if m = 2 :

$$L(f) = 10 \log \left(\frac{f_{ref}^{-3}}{12 \times f^2} \times (\omega_c \times \omega_p)^2 \right)$$

For our case f_{ref} = 26 MHz for f = 20 MHz => L(f) = -129.3 dB

L(f) is found to be -110 dB, which is not sufficient for GSM specifications. So higher order filters should be tried. Higher order filters need higher number of components which means that high noise contribution of passive elements. So it is better to lower the order of the filter as much as possible. Like this analysis, third order filter analysis is as follows:

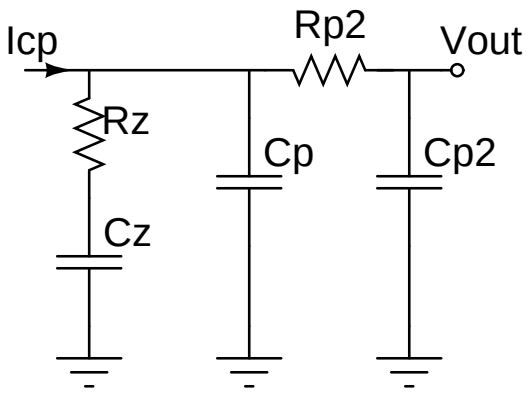


Figure 3.5. A second order filter

Gains of every block are same in the linear model in Figure 3.3, except the gain of the loop filter block whose transfer function is given as

$$Z(s) = \frac{Vout}{Iin}$$

$$Z(s) = \frac{1 + sRzCz}{denom}$$

$$denom = denom1 + denom2 + denom3$$

$$denom1 = s(Cp + Cz + Cp_2)$$

$$denom2 = s^2(CzCp_2Rz + CzCp_2Rp_2 + CpCzRz + CpCp_2Rp_2)$$

$$denom3 = s^3CzCpCp_2RzRp_2$$

This term can be rewritten as:

$$Z(s) \approx \frac{(1 + s/\omega_z)}{C_{tot}s(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \text{only valid if } \omega_z << \omega_{p1} << \omega_{p2}$$

$$with\ C_{tot} = C_z + C_p + C_{p2}; \omega_z = 1/R_zC_z\ ,\ \omega_{p1} \approx C_{tot}/R_zC_zC_p \quad and \ \ \omega_{p2} \approx 1/R_{p2}C_{p2}$$

for $\omega >> \omega_p \& \omega_{p2}$ and $C_z >> C_p \& C_{p2}$ $\longrightarrow$ $|\mathrm{Z(s)}| \approx \left|\frac{\omega_{p2}}{\mathrm{jC_p}\omega^2}\right|$

$$G(s) = \frac{K_pZ(s)K_{vco}}{sN}$$

$$\omega_\mathrm{c} = \frac{K_pK_{vco}R_z}{N} \ \ ; \ \ Kp = \frac{I_{cp}}{2\pi}; \qquad |\mathrm{H(s)}| = \left|\frac{G}{1+G}\right| \approx |G(s)| = \frac{\omega_\mathrm{c}\omega_p\omega_{p2}}{\omega^3}$$

Phase noise formula becomes:

$$L(f) = 10\log\left(\frac{f_{ref}}{12f^2} \times \left[\sin(\frac{2f\pi}{f_{ref}})\right]^{2m} \times \left[\frac{\omega_c \times \omega_p \times \omega_{p2}}{(2f\pi)^3}\right]^2\right)$$

For f << f_{ref}

$$\sin(\frac{2\pi f}{f_{ref}}) \approx \frac{2\pi f}{f_{ref}}$$

If m = 3 :

$$L(f) = 10\log\left(\frac{f_{ref}^{-5}}{12 \times f^2} \times (\omega_c \times \omega_p \times \omega_{p2})^2\right)$$

for phase margin $\omega_p = 2\omega_c$ and $\omega_{p2} = 6\omega_c$ then for f = 20 MHz => L(f) = -140 dB

If m = 2 :

$$L(f) = 10\log\left(\frac{f_{ref}^{-3}}{12 \times f^4 \times (2\pi)^2} \times (\omega_c \times \omega_p \times \omega_{p2})^2\right)$$

for phase margin $\omega_p = 2\omega_c$ and $\omega_{p2} = 6\omega_c$ then for f = 20 MHz => L(f) = -154 dB

It is seen that 2^{nd} order filter is not also sufficient for phase noise requirements, so it is needed to calculate for 3^{rd} order filter.

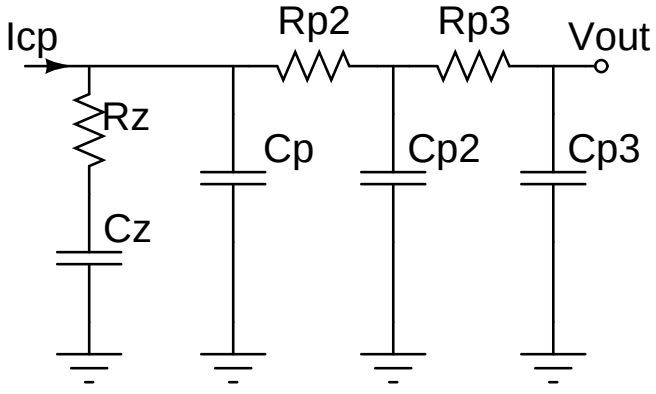


Figure 3.6. A third order filter

In Figure 3.6 a typical 3^{rd} order filter can be seen. The analysis is as follows:

$$Z(s) = \frac{1 + sRzCz}{denominator}$$

$$denominator = denom1 + denom2 + denom3 + denom4$$

$$denom1 = s(Cp + Cz + Cp_2 + Cp_3)$$

$$denom2\_1 = s^2(CzCp_2Rz + CzCp_3Rz + Cp_2Cp_3Rp_3 + CpCp_3Rp_3 + CzCp_3Rp_3)$$

$$denom2\_2 = s^2(CpCp_2Rp_2 + CpCp_3Rp_2 + CzCp_3Rp_2 + CzCpRp + CzCp_2Rp_2)$$

$$denom3\_1 = s^3(CzCp_2Cp_3RzRp_3 + CzCpCp_3RzRp_3 + CpCp_2Cp_3Rp_2Rp_3)$$

$$denom3\_2 = s^3(CzCp_2Cp_3Rp_2Rp_3 + CzCpCp_2RzRp_2 + CzCpCp_3RzRp_2)$$

$$denom4 = s^4CzCpCp_2Cp_3RzRp_2Rp_3$$

This term can be rewritten as the following

$$Z(s) \approx \frac{(1 + s/\omega_z)}{C_{tot}s(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3})} \text{only valid if } \omega_z << \omega_{p1} << \omega_{p2} << \omega_{p3}$$

$$with\ C_{tot} = C_z + \sum_i C_{pi};\ \omega_z = 1/R_zC_z\ ,\ \omega_{p1} \approx C_{tot}/R_zC_zC_{p1}$$

and

$$\omega_{pi} \approx 1/R_{pi}C_{pi} \; for \; i = 2 \; or \; 3$$

for $\omega >> \omega_{pi}$ and $C_z >> C_{pi}$ $\longrightarrow$ $|\mathrm{Z(s)}| \approx \left|\frac{\omega_{p2}\omega_{p3}}{\mathrm{jC_p}\omega^3}\right|$

$$G(s) = \frac{K_p Z(s) K_{vco}}{sN}$$

$$\omega_c = \frac{K_p K_{vco} R_z}{N} \;\; ; \;\; Kp = \frac{I_{cp}}{2\pi}; \qquad |\mathrm{H(s)}| = \left|\frac{G}{1+G}\right| \approx |G(s)| = \frac{\omega_c \omega_p \omega_{p2} \omega_{p3}}{\omega^4}$$

Phase noise formula becomes:

$$L(f) = 10\log\left(\frac{f_{ref}}{12f^2} \times \left[\sin(\frac{2f\pi}{f_{ref}})\right]^{2m} \times \left[\frac{\omega_c \times \omega_p \times \omega_{p2} \times \omega_{p3}}{(2f\pi)^4}\right]^2\right)$$

For f << f_{ref}

$$\sin(\frac{2\pi f}{f_{ref}}) \approx \frac{2\pi f}{f_{ref}}$$

and if m = 3 :

$$L(f) = 10\log\left(\frac{f_{ref}^{-5}}{12 \times f^4 \times (2\pi)^2} \times (\omega_c \times \omega_p \times \omega_{p2} \times \omega_{p3})^2\right)$$

for phase margin $\omega_p = 2\omega_c$ and $\omega_{p2} = 6\omega_c$ and ω_{p3} =$6\omega_c$ then for f = 20 MHz => L(f) = -164 dB and if m = 2 :

$$L(f) = 10\log\left(\frac{f_{ref}^{-3}}{12 \times f^6 \times (2\pi)^4} \times (\omega_c \times \omega_p \times \omega_{p2} \times \omega_{p3})^2\right)$$

for phase margin $\omega_p = 2\omega_c$ and $\omega_{p2} = 6\omega_c$ and ω_{p3} =$6\omega_c$ then for f = 20 MHz => L(f) = -178 dB. Then, what about the resolution? As it was mentioned tolerated frequency error is 0.1 ppm. This is important to decide the number of bits of $\Sigma\Delta$ modulator.

0.1 ppm of 1.7 GHz is 170 Hz. With a ΣΔ modulator of 18 bits, resolution is 99 Hz, which is calculated as reference frequency over $2^{\#ofbits}$. So ΣΔ modulator word length should be 18 bits.

3.2. System Level Design

The analysis above is simulated by using Advanced Design System® at EPFL. As it is seen in the linear model of PLL in Figure 3.3, every block is modeled. In fact there were example designs about PLLs in the database. The suitable one for our case was chosen and modified. The top level model is seen in Figure 3.7.

The best way to explain the overall system is to keep Figure 3.7 in mind. In this model, main blocks are Phase Locked Loop with programmable divider, SD_Modulator (ΣΔ modulator) and GMSK_out (Gaussian Minimum Shift Keying modulator) block. In fact, GMSK modulator is not about the synthesizer; however, it is important to see if the model is working well. Because the reason is that GMSK modulation is used in the DCS1800 standard. All blocks will be explained in detail both in system level and in transistor level.

In this model, a constant fraction is given as an input to SD_Modulator to synthesize the necessary frequency. This constant number depends on the word length of SD_Modulator.

Synthesized Frequency = (N + Fraction) x RefFreq

$$\text{Fraction} = \frac{\text{Offset}}{2^{\Sigma\Delta \text{ bits}}}$$

By an example it can be explained easily. Reference frequency (RefFreq) is 26 MHz and N (division ratio) is 67. For example, if the desired frequency is 1.763 GHz, 67 + fraction = 1.763 GHz / 26 MHz = 67.807692307 Thus the fraction is 0.807692307, and the offset becomes 211732.

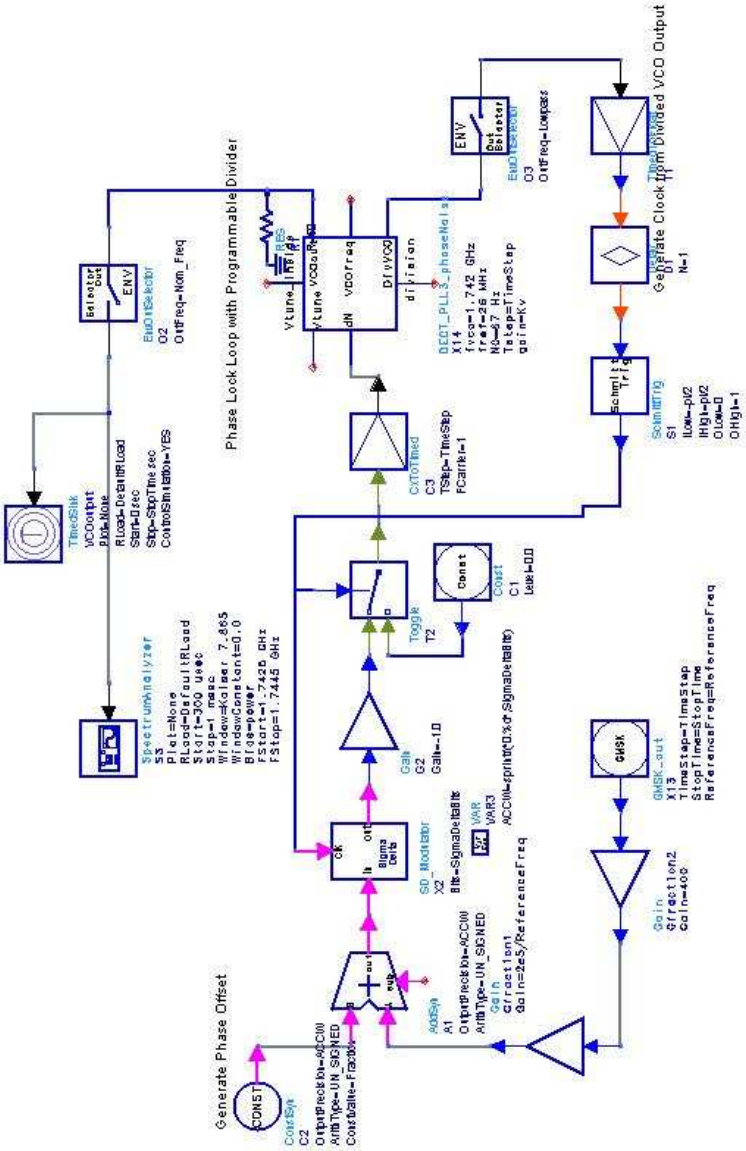


Figure 3.7. System level design in ADS

3.2.1. Blocks and their operations

ΣΔ modulator output is given to PLL with programmable divider as an input. PLL with programmable divider outputs the synthesized frequency. Now it is better to analyze these blocks starting with the SD_Modulator block.

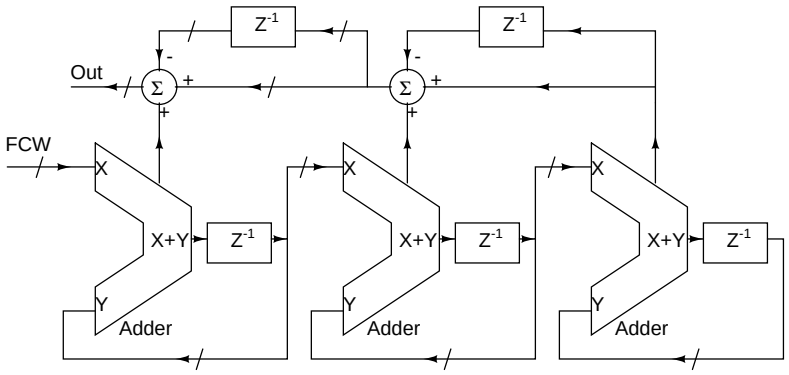


Figure 3.8. ΣΔ block level

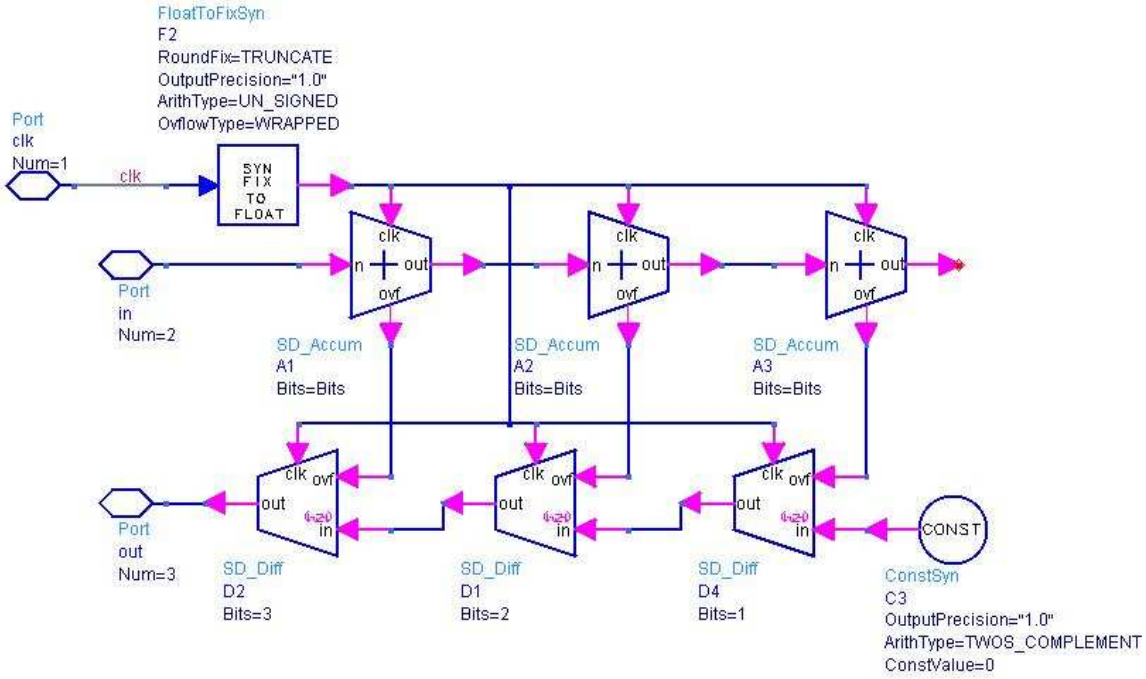
3.2.1.1. ΣΔ Modulator Block. This block consists of digital accumulators, subtractors and delay elements. ΣΔ modulators are typically used as analog to digital and digital to analog converters. However, for our case, it is purely in digital domain. Its input is 18 bits unsigned number as mentioned above. This 18 bits number enters an accumulator whose symbol and schematic can be seen in Figure 3.9.

The number is delayed by one cycle and then added with the next number. Hence, the number is always accumulated. If there is an overflow, overflow takes the value "1", otherwise its value is "0". It also outputs 18 bits sum. This sum enters the second accumulator block. The output of the second one enters the third one.

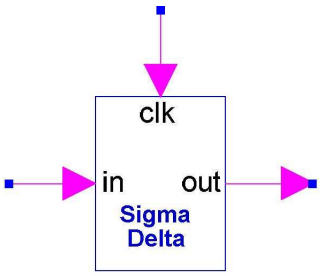
While 18 bits numbers are added in three different accumulators, they output overflow bits. Every overflow output is one bit length. As it is seen in Figure 3.2, overflow bit value of third accumulator block is added to overflow bit value of the second accumulator and the delayed overflow value is subtracted from this number. Same calculation is also done for first and second accumulators.

Although overflow bits are one bit length, the output of the ΣΔ modulator is 4 bits. This will be clear when circuit level implementation is seen.

3.2.1.2. Phase Locked Loop with Programmable Divider. This is the block where most of the operation is done. Necessary calculations have been performed for this block on the previous pages. Symbol and schematic of this block are seen in Figure 3.10.



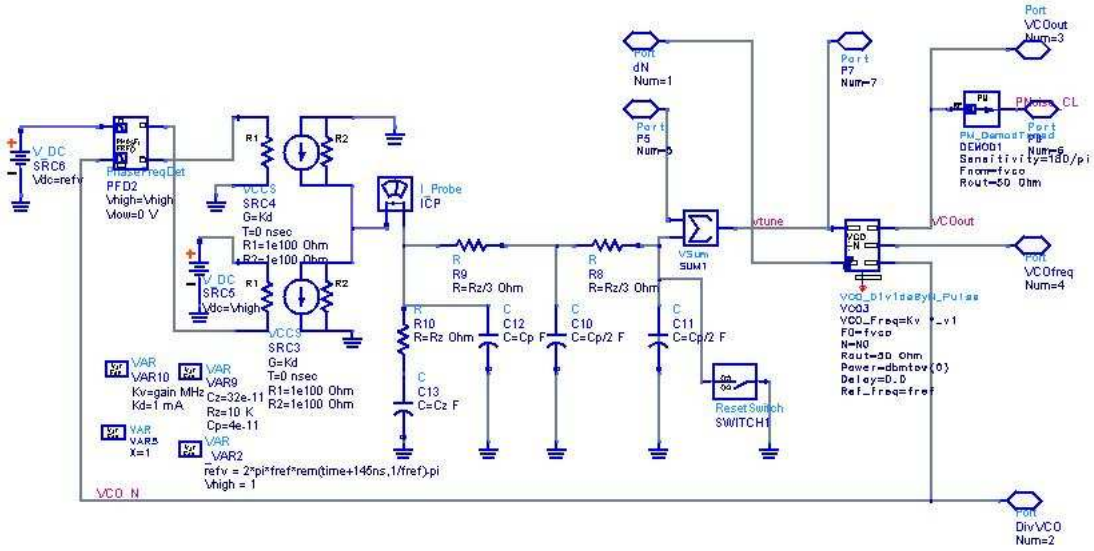
(a) ΣΔ Modulator



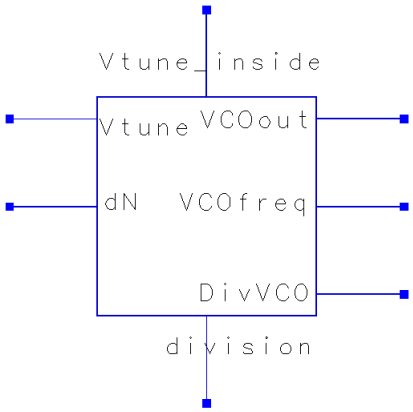
(b) ΣΔ Modulator Symbol

Figure 3.9. ΣΔ modulator (a) schematic and (b) symbol

As it can be seen from Figure 3.10, in this block there are phase/frequency detector (PFD), charge pump, loop filter, and voltage controlled oscillator block also capable of dividing by N. PFD detects the difference between reference frequency and the synthesized frequency divided by N. It outputs up and down pulse trains. These pulses control the switches of the charge pump which pump current to loop filter or sink from it. By pumping or sinking current, the tune voltage of the voltage controlled oscillator (VCO) is set. As it was mentioned while deciding on the order of the filter, PFD and charge pump gain together is decided to be $1mA/2\pi$. The loop filter was decided to be passive, and as calculated there are 3 resistors and 4 capacitors. One of those capacitors is very big, hence it is thought to be off-chip. The gain of the VCO is chosen to be 20π MHz/Volt. This means that for every millivolt change in the tune



(a) PLL with programmable divider



(b) PLL with programmable divider symbol

Figure 3.10. PLL with programmable divider (a)schematic and (a) symbol

voltage will result a 20π kHz frequency change at the output frequency. It should also be mentioned that nominal frequency of the VCO is 1,742 GHz which is the result of multiplication of reference frequency (26 MHz) and the division number N (67). This VCO block outputs the synthesized frequency, divided version of it to be fed back.

With the gain values chosen above, one needs to decide the values of loop filter components. To decide these values:

$$\omega_c = \frac{K_{pd} K_{vco} R_z}{N}$$

$$\omega_c = \frac{1 \times 10^{-3} \times 20\pi \times 10^6 \times Rz}{2\pi \times 67} = 200 \times 2\pi \times 10^3 rad$$

then Rz is equal to 8.4k, it can be chosen as 10k to be on the safe side, then

$$\omega_c = \frac{1 \times 10^{-3} \times 20\pi \times 10^6 \times 10k}{2\pi \times 67} = 1.5Mrad$$

then fc = 237 kHz which is around as the constraint

$$\omega_z = 1/R_z C_z = \omega_c/4 \quad \Rightarrow \quad C_z = 4/(10^4 \times 2\pi 200.\ 10^3) = 320pF$$
$$\omega_{p1} = 1/R_z C_{p1} = \omega_c \times 2 \quad \Rightarrow \quad C_{p1} = 1/(10^4 \times 2 \times 2\pi 200.\ 10^3) = 40pF$$
$$\omega_{p2} = \omega_{p3} = 6\omega_{p1} \Rightarrow C_{p2} = C_{p3} = C_{p1}/2 = 20pF$$
$$and\ R_{p2} = R_{p3} = R_z/3 = 3.3K\Omega$$

3.2.1.3. GMSK modulator. The other block is the GMSK modulator whose symbol can be seen in Figure 3.11 The schematic of this block is seen in Figure 3.12.

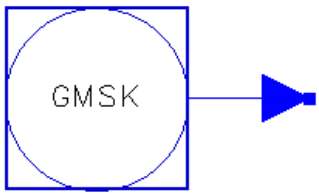


Figure 3.11. GMSK out

There is no input for this block. This block generates bit sequences and modulates these sequences by using Gaussian Minimum Shift Keying [8]. After settlement of the frequency this output is given to our design of PLL.

There are two different ways to give this output to PLL. One is directly modulating the frequency command word (FCW) of ΣΔ modulator. The other way, which is called two point modulation is to give this signal to PLL by modulating the tune voltage of the VCO, at the same time modulating the FCW of the ΣΔ modulator. Each method has some advantages. The output of the two point modulator is better

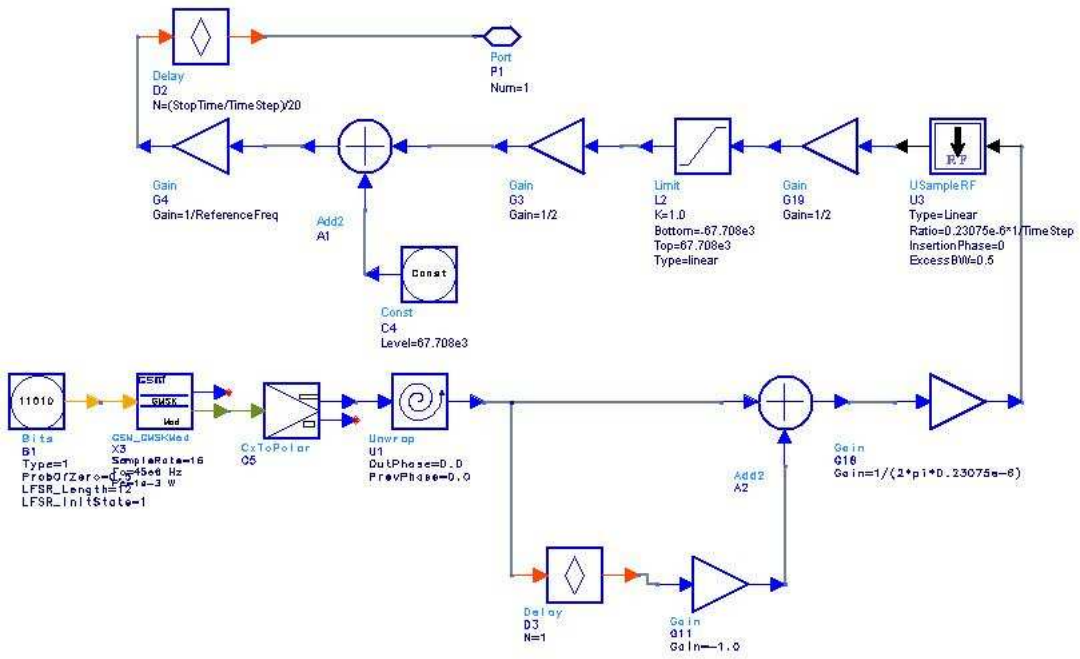


Figure 3.12. GMSK out schematic

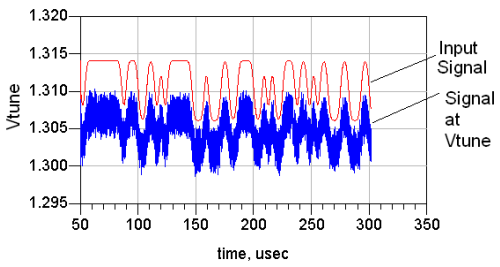
than modulating only FCW, while the latter is easier to implement in circuit level, because the former one needs a fine analog design of VCO.

3.2.2. Simulation Results

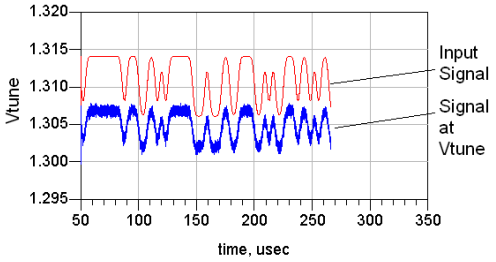
Some examples of the input and output signals can be seen in Figure 3.13(a), 3.13(b) and 3.13(c).

As it is seen from the waveforms, the higher the order of loop filter, the better the output signal. In Figure 3.14(a), input and output waveforms are obtained by modulating the frequency only from $\Sigma\Delta$ modulator. It can be seen that there is a peaking in sharp changes. This peaking is easily seen in Figure 3.14(b), where input, output of two point modulation and the output of $\Sigma\Delta$ modulation are plotted together.

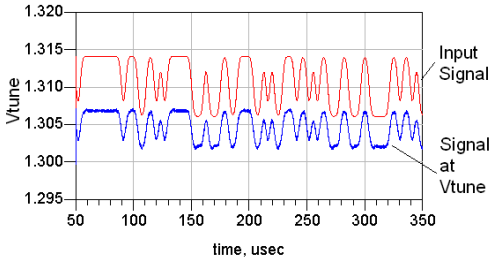
After choosing precisely the values of those components in the loop filter, the modulation method with only $\Sigma\Delta$ modulation gave sufficient results. While designing the loop filter, usually zero frequency (ω_z) is chosen to be $\omega_c/3$ and pole frequency (ω_p)



(a) 2 Point Modulation with 1^{st} order filter and 3^{rd} order $\Sigma\Delta$ modulator



(b) 2 Point Modulation with 2^{nd} order filter and 3^{rd} order $\Sigma\Delta$ modulator

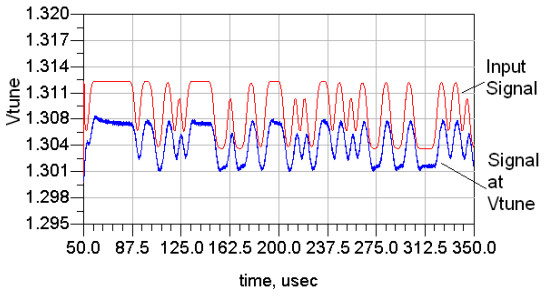


(c) 2 Point Modulation with 3^{rd} order filter and 3^{rd} order $\Sigma\Delta$ modulator

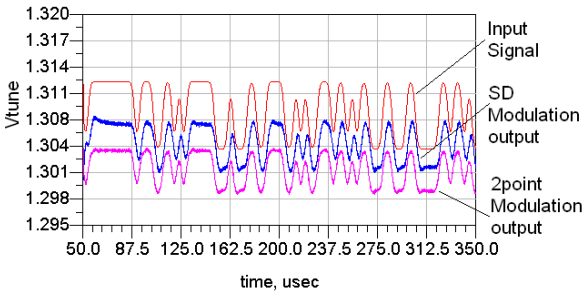
Figure 3.13. 2 point simulation results

is chosen to be $3\omega_c$ for sufficient phase margin in the response of open loop transfer function. In some designs, such as our case, first order filter is not sufficient. Additional one or two poles should be added (Figure 3.15). Usually, they are sufficiently far away not to disturb the phase margin.

However one should also check the closed loop response of the system. For example, a peak is seen at the output signal in our case which is called jitter peaking. This can also be seen in the closed response magnitude graph in Figure 3.16 and mod-



(a) $\Sigma\Delta$ modulation with 3^{rd} order filter



(b) Difference between 2 point modulation and only $\Sigma\Delta$ modulation

Figure 3.14. $\Sigma\Delta$ modulation and differences

ulation output graphs (Figure 3.14(b)). In the magnitude and phase graph peaking is measured as 5.53 dB.

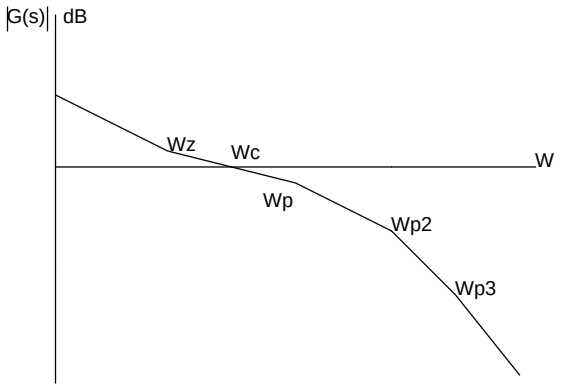


Figure 3.15. Poles

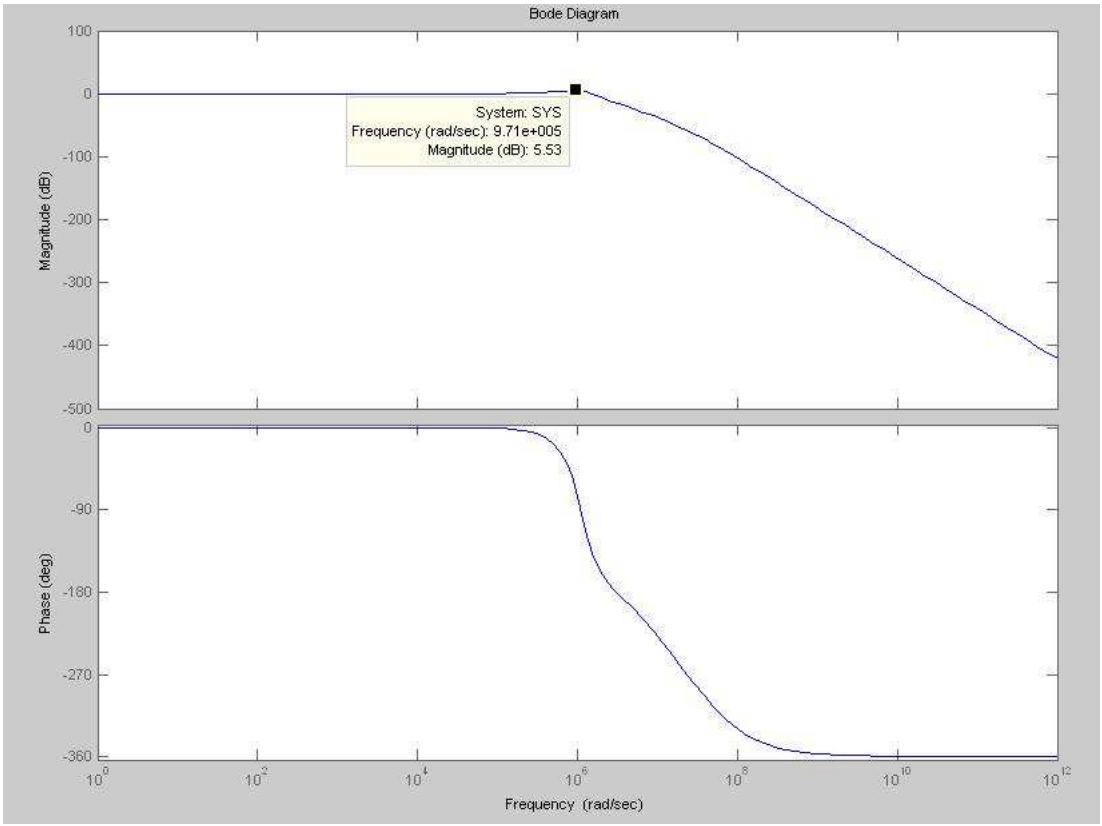


Figure 3.16. Closed loop bode plot of the system

As it is expected, the peaking in the modulated frequency in Figure 3.14(b) is because of the peak before cutoff frequency in the response of the PLL. The frequency of the change is calculated as approximately 144 kHz. This corresponds a 5,3 dB

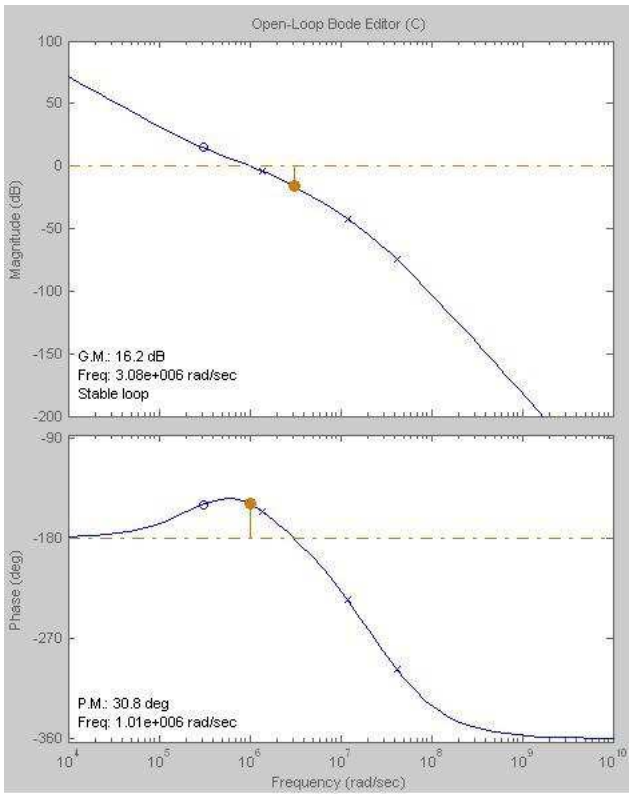


Figure 3.17. Open loop bode plot of the system

increase in the signal. To eliminate this peaking, one should consider to cancel the zero which cause this peak by shifting the pole.

After cancellation of the zero, jitter peaking is only max 1,51 dB with enough phase margin (Figure 3.18).

Modulating the signal by using this revised filter gave better results which can be seen in the Figure 3.21(b). However we have to pay from phase noise performance as it can also be seen in Figures 3.19 and 3.20.

At this point, it can be considered that by flattening the response, efficient bandwidth is increased, so we can decrease the cut-off frequency to increase the noise performance. A nice trial is also shown with I_{pd} (current of the phase frequency detector) 0,6 mA. As it is seen in Figures 3.19, 3.20 and 3.21(a) noise performance is distinguishable between 1 mA and 0,6 mA cases. However, when current is smaller, delay time is higher as seen in the figure.

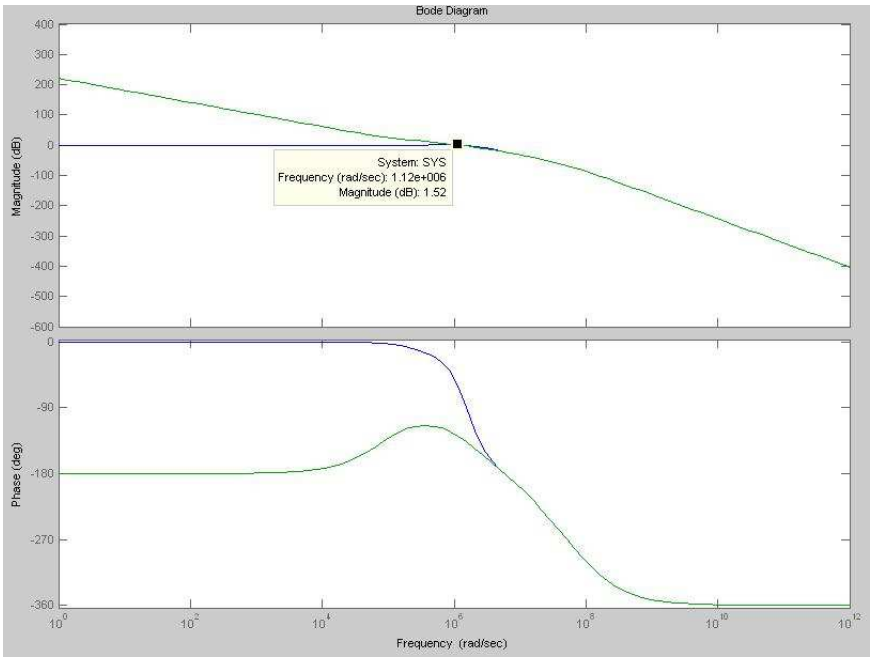


Figure 3.18. Closed loop bode plot of the modified system

In the next chapter, circuit level implementations of the blocks that are used in system level simulations are explained.

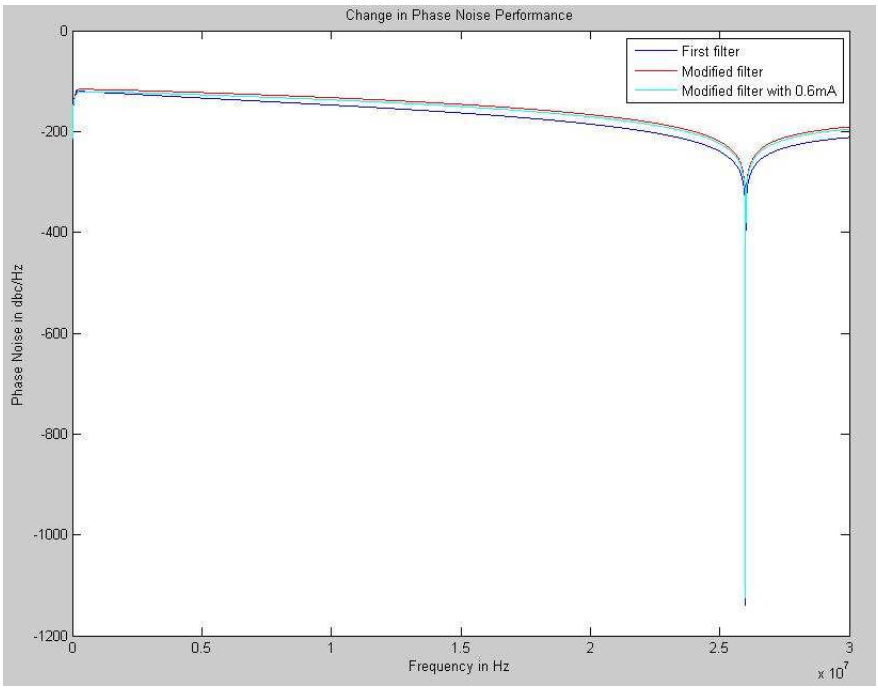


Figure 3.19. Phase noise performance difference

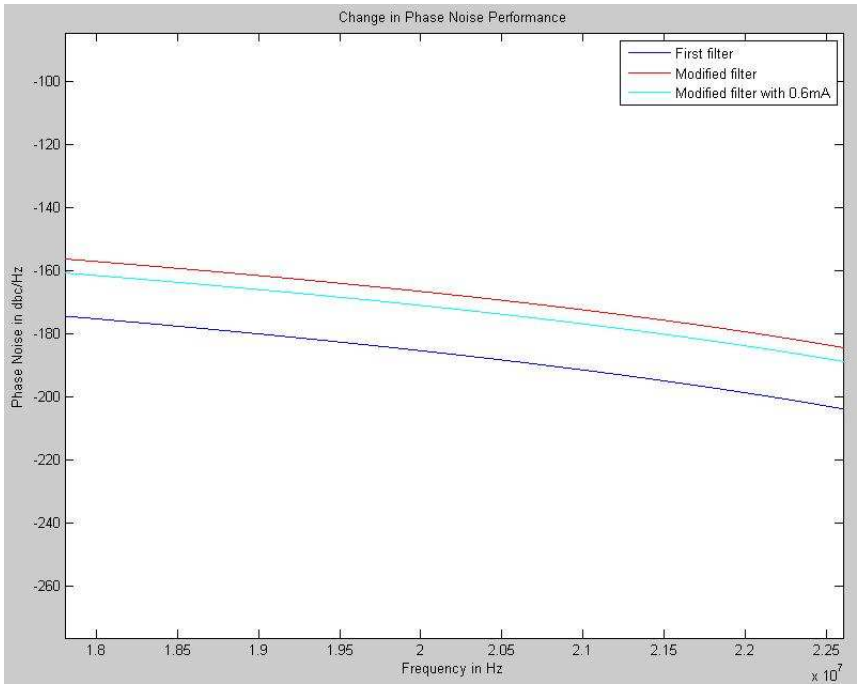
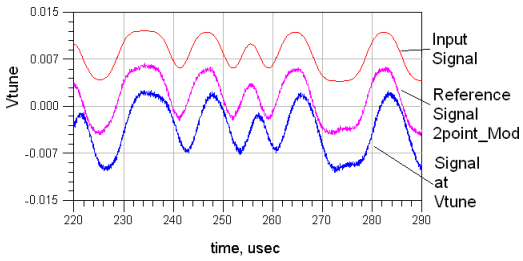
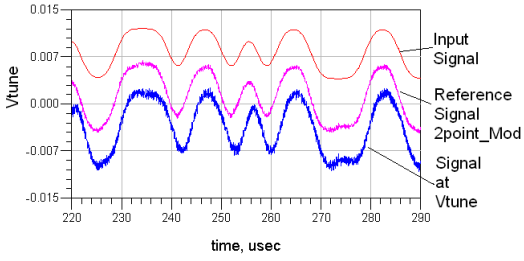


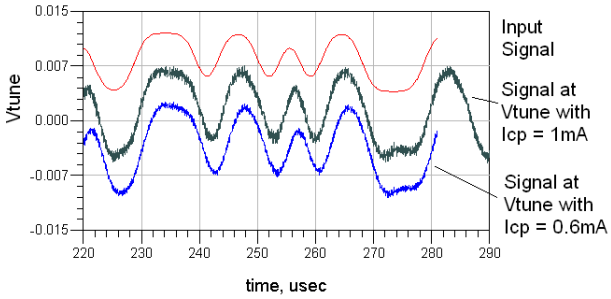
Figure 3.20. The zoomed in version of phase noise performance difference



(a) ΣΔ modulation with modified 3^{rd} order filter with I_c=0.6mA



(b) ΣΔ modulation with modified 3^{rd} order filter with I_c=1mA



(c) Difference between ΣΔ modulation with modified 3^{rd} order filter with I_c=1mA and I_c=0.6mA

Figure 3.21. ΣΔ modulation with modified loop filter

4. LOW LEVEL DESIGN

Blocks that are used in system level are designed by using Mentor Graphics®. The process is standard 0.18 μm CMOS process. In Figure 4.1, system with all blocks can be seen and these blocks are explained one by one. There may be several implementations of this work, however this design is influenced by the proposed design by Craninckx and Steyaert [9]. The output of the VCO is first divided by fast prescalers. At the output of these prescalers, 4 signals with 90° phase shift are generated. The frequencies of these signals are 1/4 of the synthesized frequency. One of these shifted signals is chosen by 4to1 multiplexer according to output of the $\Sigma\Delta$ modulator. The frequency is divided first by 4 then by 16. Thus the overall signal is divided by 64. This is valid only if the output of the 4 to 1 multiplexer is tied to a specified input. However, if the inputs of 4 to 1 mutiplexer are selected, then some of the periods are swallowed, which leads to different division ratios. 90° phase shift at the output of the 4 to 1 multiplexer means swallowing one pulse, so divisor is increased by one [10]. By selecting appropriate inputs, the synthesized frequency can be 64 to 71 times of the reference frequency. As it is calculated, the resolution depends on the number of bits of the $\Sigma\Delta$ modulator. The word length is chosen as calculated above as 18. Thus, the resolution is 99Hz. With a 26.6 Mhz reference frequency, frequency synthesis range of the PLL is 1.703 GHz to 1888.6 GHz. However because of the topology that we have chosen as $\Sigma\Delta$ modulator, which is mash 1-1-1 (Figure 3.2), the average of the output of the $\Sigma\Delta$ modulator is always between 0 and 1. So the range can be only as much as the reference frequency. To increase the range, a different $\Sigma\Delta$ modulator topology or a higher reference frequency can be choosen. If reference frequency is chosen higher, then to provide the same resolution, the bit length of the $\Sigma\Delta$ modulator would be also increased. The blocks that are used in the design and overall schematic can be seen in Figure 4.1. However for 50 μsec, transient simulation takes one week if all of the circuit is simulated together. So, efficient methods for simulation are sought. Simulating the circuit part by part is a good solution. However, to divide the circuit, the reference frequency source should be chosen as the clock of the $\Sigma\Delta$ modulator. In the literature, it is written that choosing the divided signal as the clock gives better results; however,

for practical purposes, the circuit is divided and simulated. By doing so, simulation time for 50 μsec becomes 30 hours.

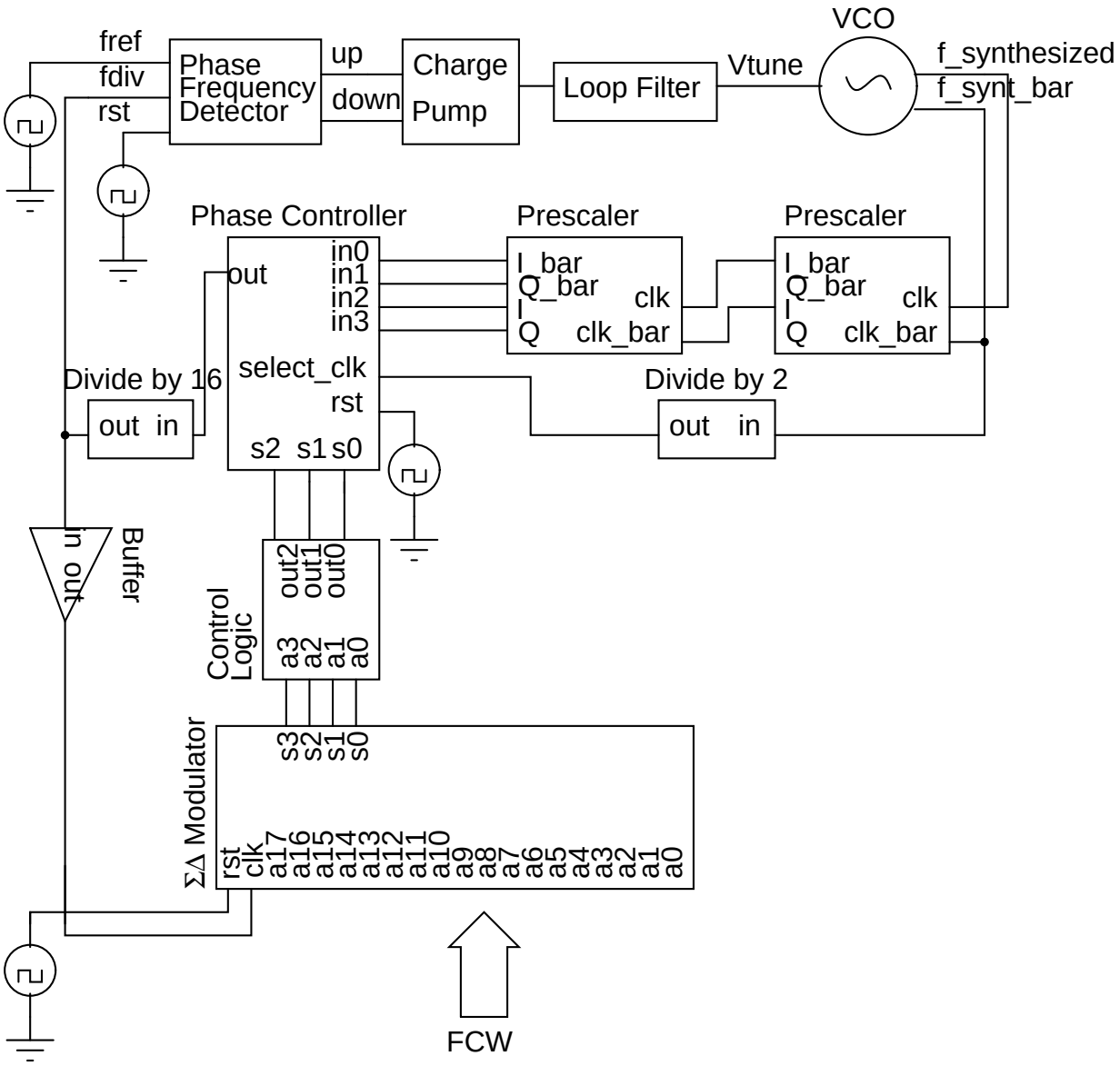


Figure 4.1. Block schematic of the low level design

4.1. ΣΔ Modulator

This block is the implementation of the ΣΔ model in Figure 3.2. It is an all-digital block. The schematic of this block can be seen in Figure 4.2. As they can be seen, there are only adders and registers. Registers are delay elements and adders are for subtraction and addition operations. Subtraction is done by taking two's complement

of the binary number.

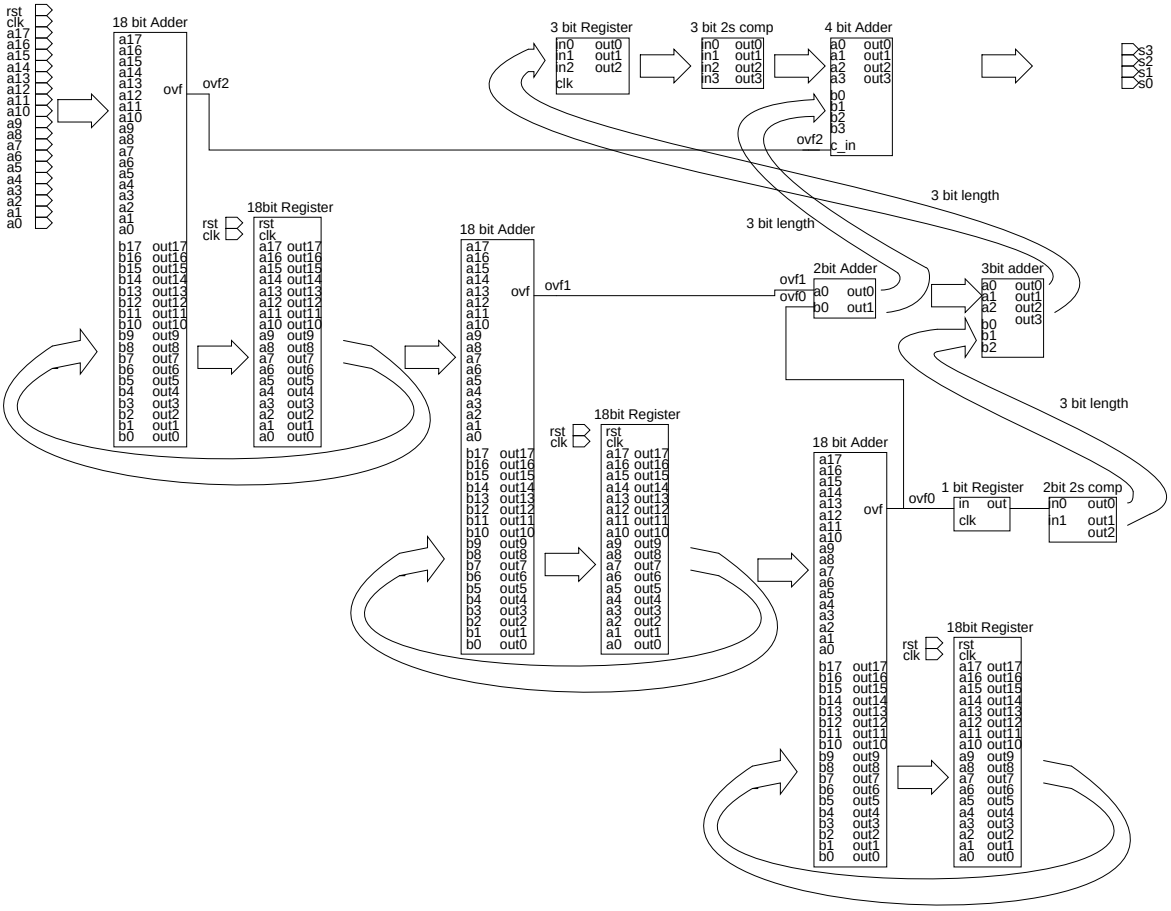


Figure 4.2. $\Sigma\Delta$ modulator inside

Maybe the most important fact about the implementation is to decide how to handle overflow bits of the accumulators. Every overflow outputs of the accumulators is one bit length. These binary numbers are to be added and subtracted. The overflow of the 3^{rd} accumulator is added to overflow of the 2^{nd} accumulator. At the same time, it is written into the register and delayed one cycle. The output of the register is subtracted from the summation of overflow bits of 3^{rd} and 2^{nd} accumulators. This subtraction is done by taking the 2's complement of the binary number and adding this number to the minuend afterwads. The difference is written into register and added to current overflow bit of the first accumulator. The minuend of the first stage of the previous cycle is subtracted form this result. Resulting number is the output of the $\Sigma\Delta$ modulator.

4.2. Voltage Controlled Oscillator

The design of a VCO that is capable of spanning all the specified frequency band in a limited tune voltage range with a maximal allowed phase noise, is a hard task. Consider the LC tanks in Figure 4.3. An LC tank can be considered as a band-pass filter, whose angular center frequency can be calculated as [11]:

$$\omega_c = \frac{1}{\sqrt{LC}}$$

As inductors are not ideal, they have a non-zero resistance which shown as Rs in Figure 4.3. The representation of the LC tank in the left hand side of the figure can be transformed to the right one with using the following statement [11]

$$Rp = \frac{Ls}{CRs}$$

With appropriate L and C, the needed nominal frequency of the VCO can be obtained. However capacitor value is not the value that is used in the design. In fact it consits of parasitic capacitance of the inductor, capacitance of the active devices (CMOS devices) and the capacitance of the load devices (prescalers). It is better to choose a coarse value of the capacitance and fine tune afterwards. An active element which is represented

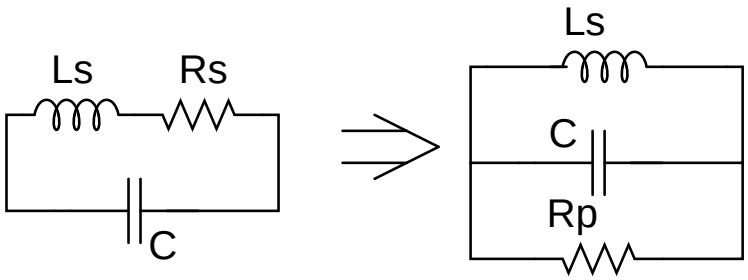


Figure 4.3. LC tanks

as negative resistance (-R) in Figure 4.4 should be in the design to compansate the losses of the parasitic resistance of the inductor and capacitor (R_L and R_C), so that the system would fulfil the Barkhausen oscillator creterion [12]. The active element used in LC-VCOs are cross coupled MOS transistors, whose effective resistance seen from their drains is equal to -2/gm (Figure 4.5).

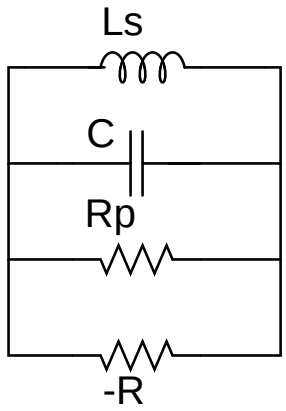


Figure 4.4. LC tank negative R

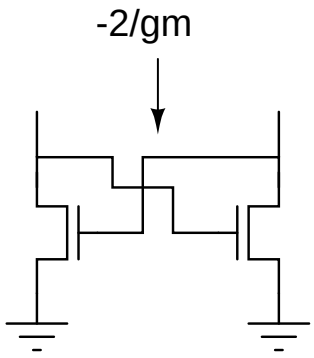
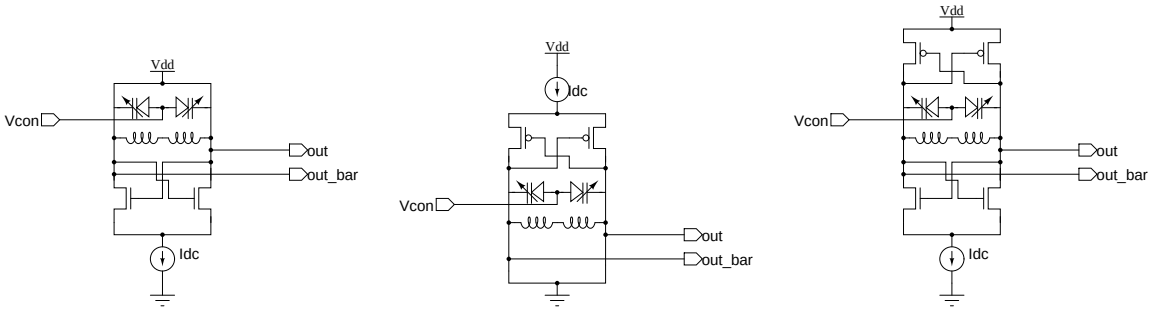


Figure 4.5. -R is equal to -2/gm

Roughly speaking, there are three different LC VCO topologies which can be seen in Figure 4.2. In this design, the one that contains both PMOS and NMOS transistors is chosen, because that topology consumes less power and has a better phase noise behavior [11]. The amplitude of the output swing is limited by VDD and ground, however in the other designs amplitude can be as large as technology limits can tolerate.

As it was mentioned phase noise is very important. There are many publications on the issue of predicting the phase noise of VCOs. The phase noise model of Abidi [13] is mainly considered among three main phase noise models [14], [9], [13]. Abidi states:



(a) NMOS only (b) PMOS only (c) CMOS

Figure 4.6. Different LC VCO topologies (a)only NMOS, (b)only PMOS and (c)both NMOS and PMOS

$$L(\omega_m) = \frac{4FkTR}{V_0^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2$$

and

$$F = 2 + \frac{8\gamma R I_T}{\pi V_0} + \gamma\frac{8}{9}g_{mbias}R$$

According to this formula, if V_0 increases phase noise decreases and if I_T increases, as a consequence V_0 increases, hence phase noise decreases, on the other hand, phase noise is also inversely proportional to I_T. As seen in Figure 4.7 increasing tail current causes V_0 to rise until limited by the supply voltage. Then increasing I_T increases phase noise. In the design, the I_T value which makes V_0 as large as possible should be chosen.

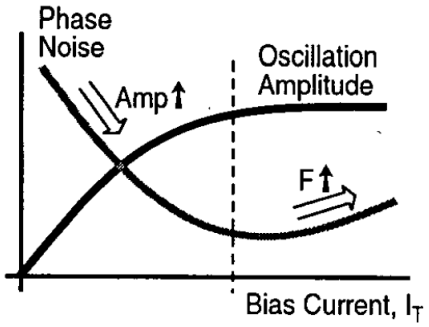


Figure 4.7. Phase noise [13]

To decrease the phase noise, L_s/R_s and L_s/C should be maximized [11]. Maximization of L_s/R_s is limited by the technology. To maximize L_s/C, C should be chosen as low as possible, however with low capacitance gain of the VCO is limited. In addition, as it was mentioned, C consists of parasitic capacitances which leads to nonlinear gain of the VCO. To linearize the gain as much as possible varactor capacitance should be as large as possible. On the other hand, varactors have bad noise profiles, so choosing a large varactor decreases the noise performance.

In the light of above discussions VCO in Figure 4.8 is designed with the given transistor values in Table 4.1. I_{dc} is chosen as 1,5 mA, which makes oscillation amplitude maximum. The value of I_{dc} is also important when VCO is loaded which is known as pulling in literature. When VCO is loaded the oscillation frequency also changes because of the capacitance of the load. Hence it is better to design VCO with the loads. The inductor used in the design is a planar CMOS inductor with a value of 6,598 nH with 4,5 turns. The diameter of the inductor is 286 μm and the width of the metal is 10 μm. These values are also tabulated in Table 4.2. The on chip capacitance and varactor values are given in Table 4.3. C3 and C4 are varactors whose capacitances are 488 fF with no bias voltage.

Table 4.1. Device sizes of VCO

Devices	**M1**	**M2**	**M3**	**M4**
Sizes(in μm)	60	60	10	10

Table 4.2. Parameters of inductors

L	**NT**	**Do**	**W**
6.598 nH	4,5	286μm	10μm

Table 4.3. Capacitor values

C1	**C2**	**C3**	**C4**
271 fF	271 fF	488 fF	488 fF

Altough design focuses on the DCS1800 standard and necessary effort is made, the

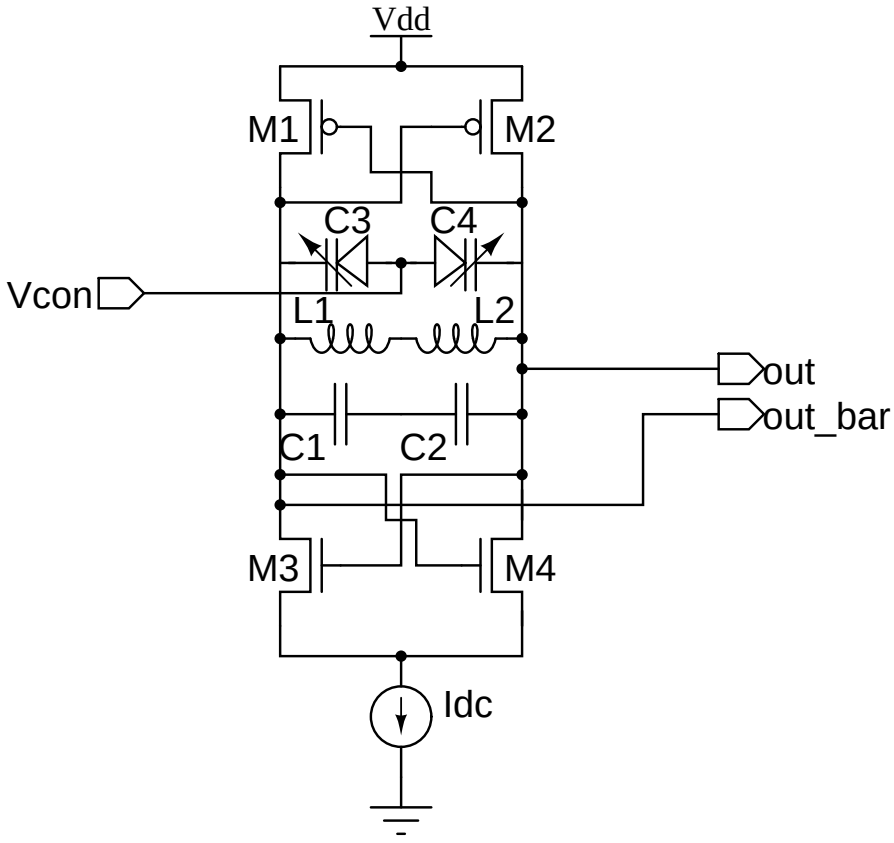


Figure 4.8. VCO

designed VCO could not meet the requirements. The phase noise of the designed VCO is -151 dBc/Hz at 20 Mhz offset (Figure 4.9). But this is in circuit stage, if its layout would be drawn then it would increase more. Altough its phase noise performance is not that good, its gain is quite sufficient to span the band, which is 88Mhz/V as it can be calculated form Figure 4.10.

As a future work, there are some kind of tricks to decrease the phase noise. One trick is to design the VCO that has a center frequency of double center frequency of this design and then divide it by '2'. The other trick is to use a differential center tap inductor, which was not avaliable in our design kit.

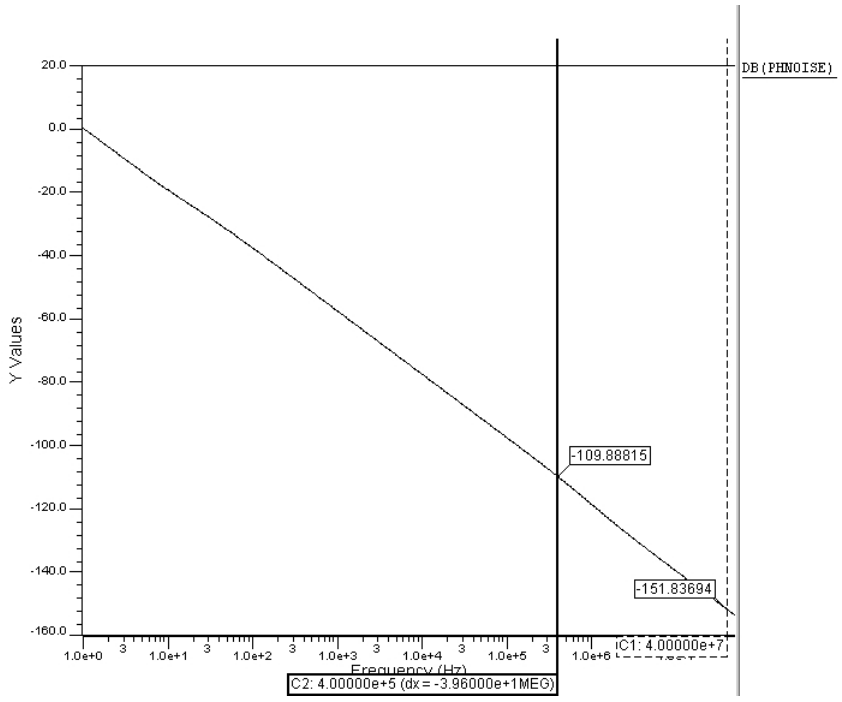


Figure 4.9. Phase noise of the VCO

4.3. High Speed Prescaler

The high speed prescaler topology seen in Figures 4.11(a) and 4.11(b) is taken from Wang [15]. However device sizes are different. Sizes can be seen in table 4.4. Instead of this prescaler, TSPC based prescalers could be used, however for this PLL topology, four signals with 90° phases difference are needed. The operation of the block can be explained as following. When CLK is high, M1, M2 and M5 conduct. Assume that D is high for this example, then Q_bar becomes 0. So M6 does not conduct and Q becomes high, M7 also helps M3 and M5 against M1 to pull Q_bar to ground. Q_bar output of the above flip flop is the D input of the below one. Because CLK was high and the clock inputs of the below flip flop are tied inversely, transistors M1, M2 and M5 of the below one do not conduct when CLK is high. So, the states of Q and Q_bar depend on their previous values. When CLK_bar becomes high, M1, M2 and M5 of the below DFF conduct. So Q_bar of the below DFF becomes high, so as the D_bar of the above DFF. For one period of the clock, outputs keep their states, hence the frequency is divided by 2. As it is clear from this analysis output changes when CLK or CLK_bar become high, in other words in the rising edge. Because clk signal is tied inversely for below flip flop with respect to the above one, there is one clock pulse

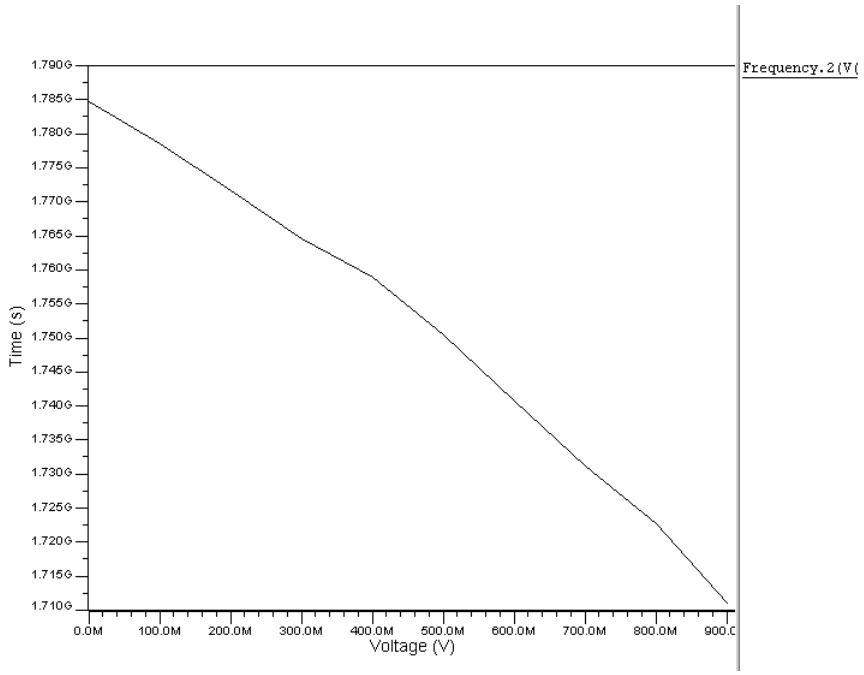
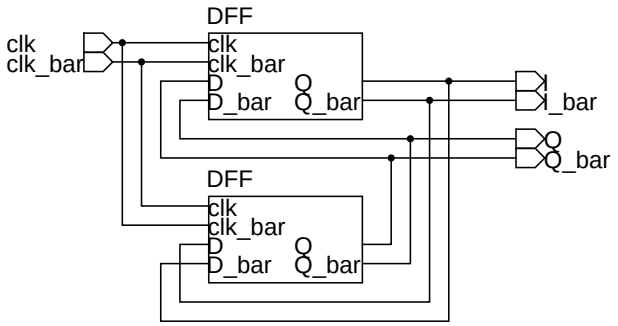


Figure 4.10. The gain of the VCO

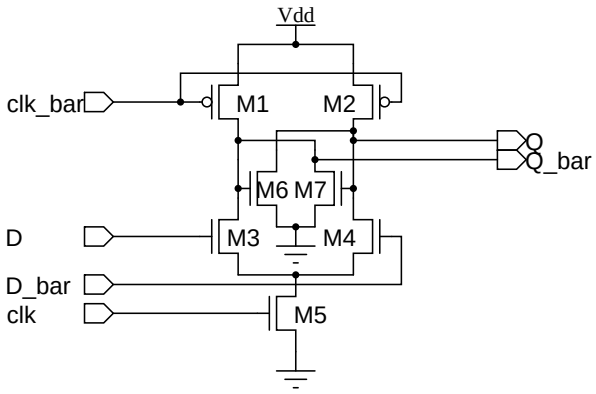
phase difference between the outputs of above and below flip flops. One clock pulse difference means 90° phase shift. And because there are two inverse pairs, there are four 90° phase shifted divided by 4 signals which can be seen in Figure 4.12.

Table 4.4. Device sizes of prescaler

Devices	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**
Sizes (in μm)	1.8	1.8	1.8	1.8	1.8	5.4	5.4



(a) Prescaler inside



(b) DFF

Figure 4.11. High speed prescaler (a) flip-flop connections and (b) design of the flip-flops

4.4. Phase Frequency Detector

The Phase Frequency Detector (PFD) detects the phase difference of two clock sources. The inputs of this block are the output of the reference frequency source and the divided output frequency. It detects the difference between these pulses and generates up or down pulses according to which of the input lags or leads. The width of these pulses depends on the time difference between low to high transitions of these input signals. The duration of the pulse determines how long to pump current to the loop filter or sink current from it. There are different kinds of PFDs. The most common one in the literature is tri-state PFD [16], which is used in this design also. It can be seen in Figure 4.13 which is based on two registers. The clock of the upper register is connected to reference frequency (f_{ref}), and the clock of the lower register is connected to feedback frequency (f_{div}). If f_{ref} leads f_{div} then output of the upper register becomes '1' before the lower register. When the output of the lower register also becomes '1'

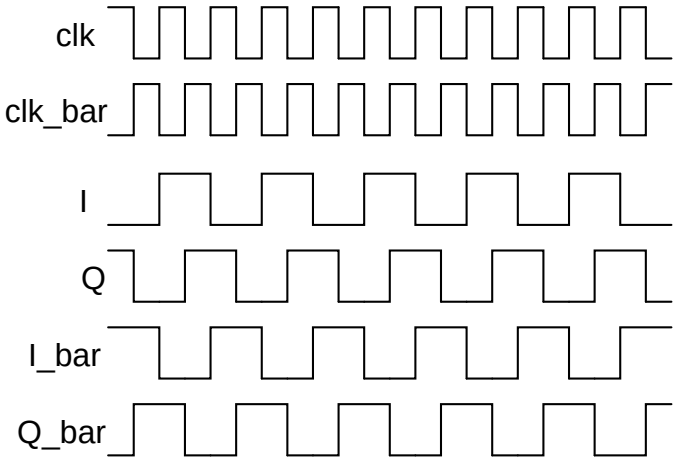


Figure 4.12. Signals at the output of high speed prescalers

reset inputs of the registers become '0'. So ouputs of the both registers become '0'. If f_{ref} lags f_{div}, then down pulse is wider then the up pulse.

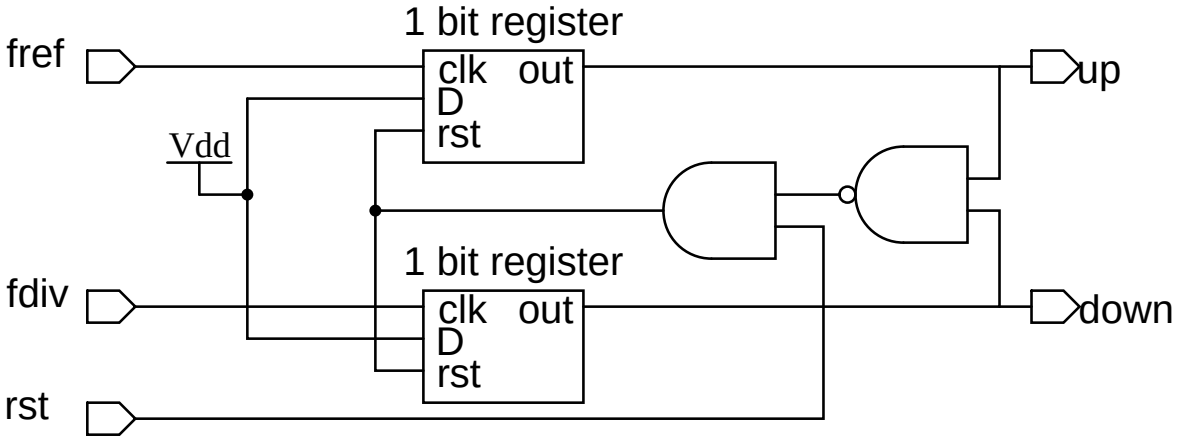


Figure 4.13. PFD

The "and gate" in the reset path is to reset the registers from outside and to delay the reset signal. This delay is important to eliminate the "dead zone" (undetectible phase difference range). Because of this delay, a pulse is seen at the outputs of both registers, independent of which signal leads which.

And & nand gates are minimum sized simple gates, while the 1 bit register is multiplexer based positive edge triggered register (Figure 4.15).

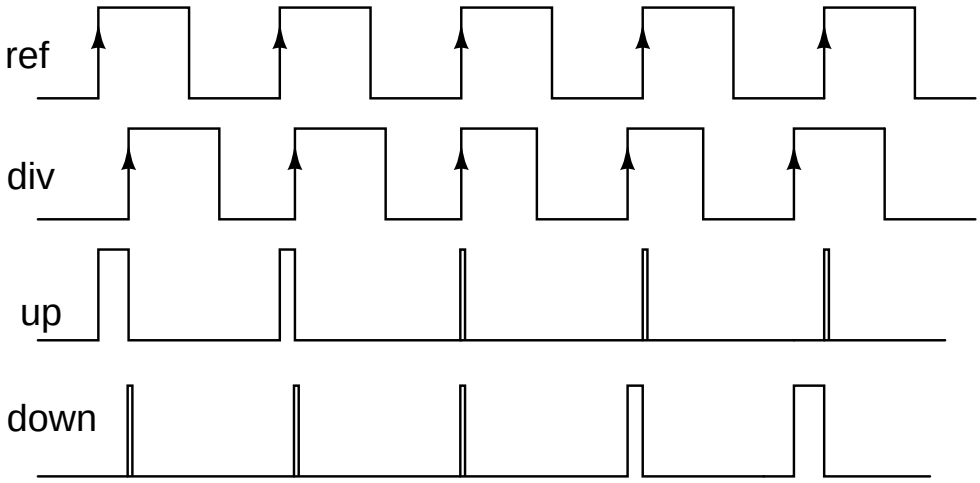


Figure 4.14. Up and down pulses

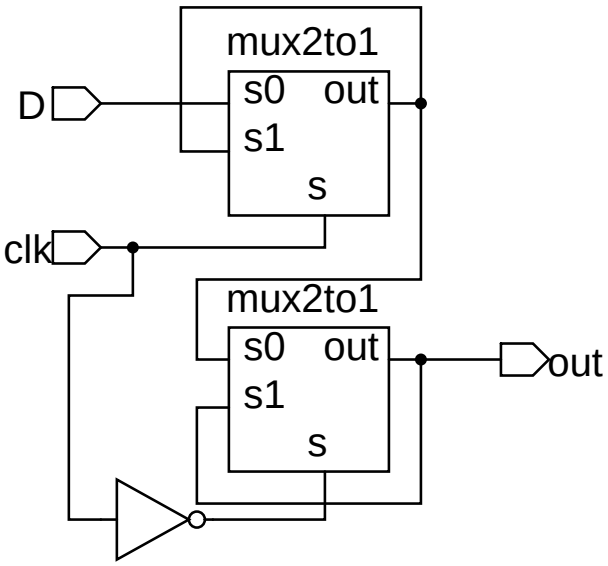


Figure 4.15. 1 bit register

4.5. Charge Pump

The function of the charge pump is to deliver current to loop filter as it was mentioned above. It transfers phase difference to current. This transformation is done by depending on the duration of the up and down pulses of the PFD via constant current. The up and down pulses of the PFD opens or closes M3 or M11 respectively. Hence if M11 conducts, the charge pump sinks current from loop filter; and if M3 conducts, it pumps current to the loop filter. The amount of this constant current is very important in stability analysis. The difference between pump and sink currents are also important in terms of generating spurs, which is undesirable. Altough the

magnitude of the current is determined by the above analysis, after starting low level design, it is seen that it is better to design the VCO first, then gain of the charge pump should be determined according to the gain of the VCO. As it was mentioned the gain of the designed VCO is 88 Mhz/V, however in the analysis it was chosen as 10 Mhz/V and the charge pump current was 1 mA. As it is clear from the above analysis, if the multiplication of gain of the VCO and the gain of the charge pump is constant, they can take every different pair of values whose multiplication give the same constant value. So if the gain of the VCO increased by 8.8 times, so the sink and pump current should be decreased by 8.8. Hence the current is chosen to be 114 μA. Although there are better charge pump circuits in the literature, this circuit was chosen. M5, M6 & M7 are to bias the pull down circuit and M1, M2, M8 & M9 are to bias the pull up circuit. Pull up and pull down currents are determined as 114 μA by choosing appropriate device sizes for M3, M4, M11 and M10.

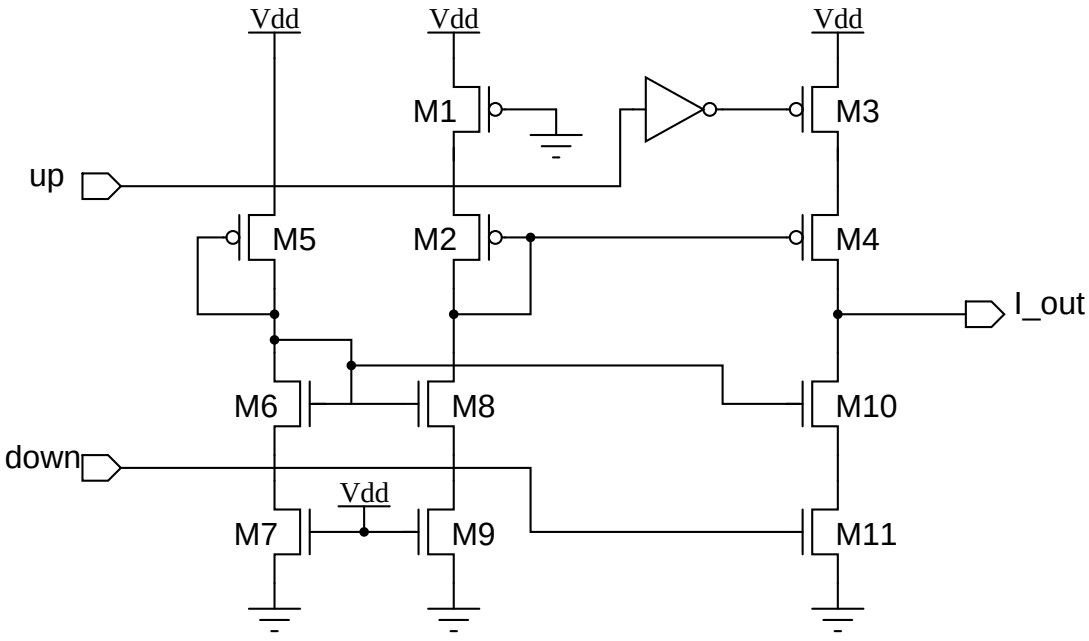


Figure 4.16. Charge pump

Table 4.5. Device sizes

Devices	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**	**M9**	**M10**	**M11**
Sizes (in μm)	0.48	0.48	2.22	2.22	0.48	0.24	0.24	0.24	0.24	1.32	1.32

4.6. Loop Filter

Loop filter consists only passive elements. Component values were calculated previously and these values are also used in transistor level implemantation.

4.7. 4 to 1 Multiplexer

Multiplexer is based on transmission gate logic. 4 to 1 multiplexers are created by using three 2 to 1 multiplexers. In Figure 4.18, 2 to 1 multiplexer can be seen. Device sizes are $0.24\mu m$ for all nmos transistors and $0.48\mu m$ for all pmos devices. Inverters at the output are to recover the loss of drain to source voltage. To design a glitch free multiplexer, an additional 2 to 1 multiplexer is added to the second select bit path as seen in Figure 4.17

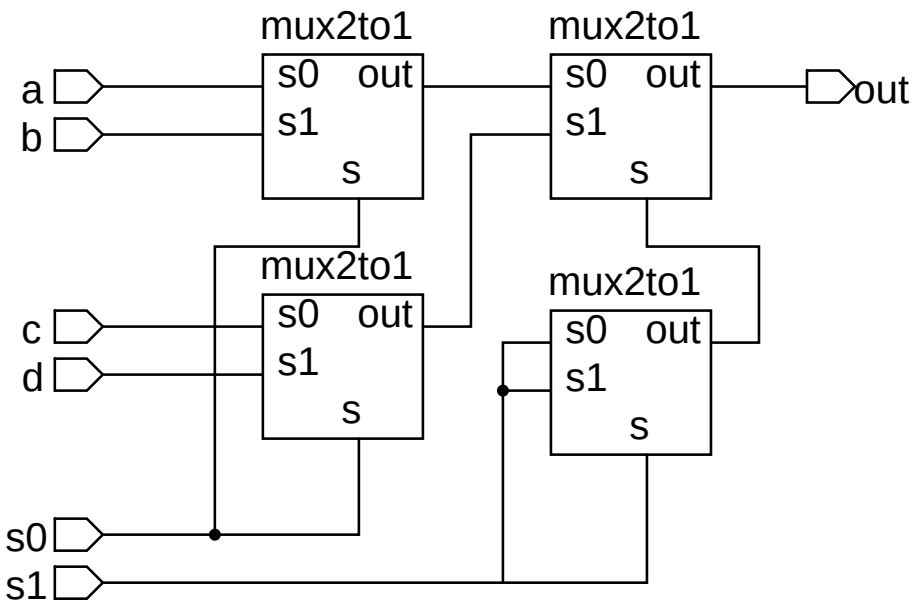


Figure 4.17. Synchronized 4 to 1 multiplexer

4.8. Division by 16 block

In this block there are 4 equal sub blocks, whose schematic can be seen in Figure 4.19. This design is taken from [17]. All nmos transistors are $0.24\mu m$ and all pmos transistors are $0.48\mu m$. TSPC based logic is very fast and its operation can be explained

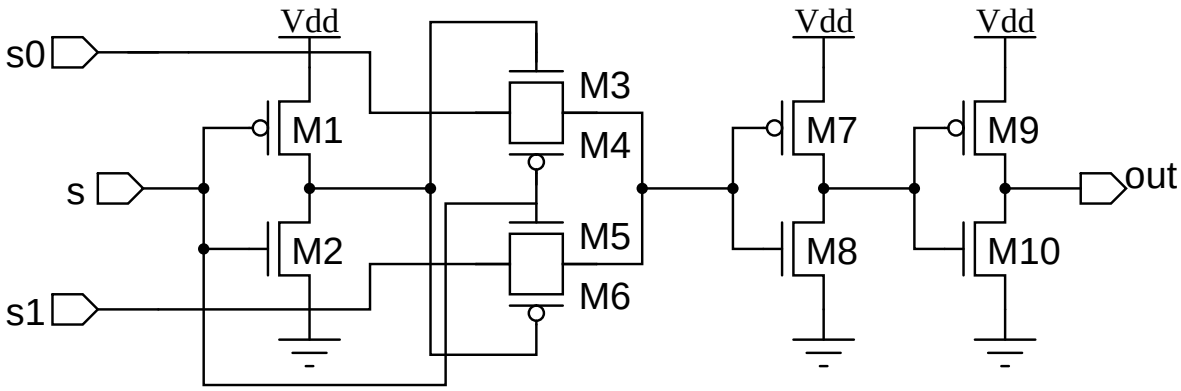


Figure 4.18. 2 to 1 multiplexer

as follows. Assume that *out* is high. For *out* to be high, M7 should conduct. If M7 conducts, then M9 does not conduct. For M7 to conduct M4 should not conduct, but M5 & M6 should conduct. For M6 to conduct, *in* should be high, and as we assumed that *out* is high, then M3 also conducts. When *in* becomes low, then M4 conducts and M7 opens, however because *in* is low M8 is also open so out states as it was. When *in* becomes high again, because M9 was conducting, *out* is pulled down to ground by M8 immediately. When *out* becomes low, then M3 stops conducting, becuse *in* is high, M2 also does not conduct. So the gate of the M5 states as it was. And again if *in* becomes low the gate of M5 is pulled up immediately by M1 & M2, and this operation goes on. Hence for one period of the input output preserves its state. So the signal is divided by two. As it was mentioned there are 4 blocks one driving the other. So clock is divided by 16 at the output of 4 blocks.

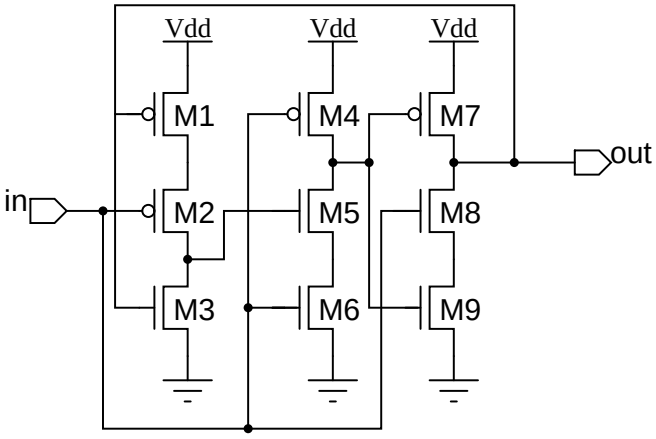


Figure 4.19. TSPC DFF

4.9. Buffer

It is still better to explain this block, altough this block becomes unnecessary after dividing the circuit for fast simulation purpose. Division by 16 block has to drive the clock pin of ΣΔ modulator, which consists of edge triggered function blocks. So this buffer is essential because of large fan-out of division by 16 block and it consists of two inverters. Inverters are sized for fast transition times. The device sizes are tabulated in table 4.6.

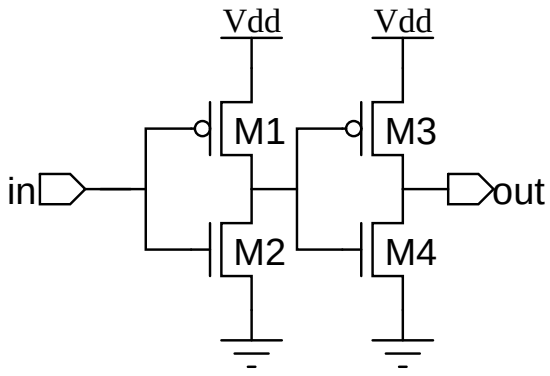


Figure 4.20. Buffer

Table 4.6. Device sizes of buffer

Devices	**M1**	**M2**	**M3**	**M4**
Sizes (in μm)	0.48	0.24	2.84	1.92

4.10. Control Logic

The output of the ΣΔ modulator is 4 bit signed number changing from -3 to 4. The output of the 3 bit adder in Figure 4.2, can only take -1,0,1 and 2. So the output of the modulator can take -3 to 4. These 8 different numbers can be represented by 3 bits. This control logic block is to map the numbers between -3 to 4, to the numbers between 0 to 7. This is achieved just adding 3 to the output of ΣΔ modulator by using a 3 bit adder. 3 bit adder is enough because sign bit is unnecessary.

In addition, because of the delay, select bits are not synchronized. To synchronize

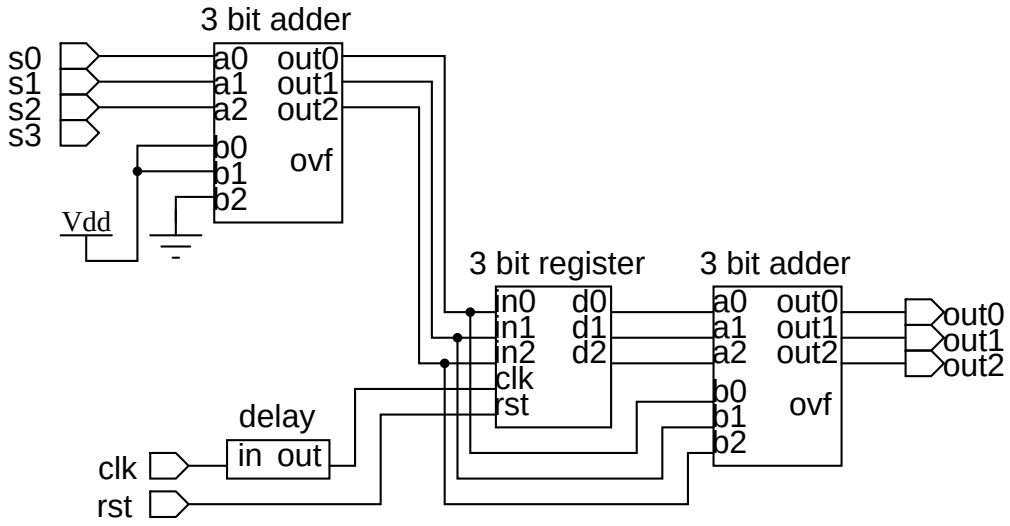


Figure 4.21. Control logic

these bits, a positive edge triggered three bit register is used. The clock of this register is the same clock as the clock of the $\Sigma\Delta$ modulator, however it is delayed by 3.63 nsec.

4.11. Phase Controller

To change the division factor, special cautions should be taken. While switching between pulse trains whose phases are different, glitches may occur. These glitches lead to wrong division factors. So by inspiring from [10] a different phase switching topology is designed. As it was mentioned above, in this topology, there are 4 signals with 90° phase difference. The frequency of these signals are same and 1/4 of the synthesized frequency. As it was mentioned division factor can range between 64 to 71. How could it be if there are 4 different signals? This may be explained as ascending the steps one by one instead of higher step sizes. In Figure 4.22, the clock signal, four different signals, and the signal at the output of the multiplexer are seen. As it is seen in the figure, four different signals at the output of the prescaler are in an order. The topology can be explained best by giving an example. Assume that the output of the $\Sigma\Delta$ modulator is 6, then division factor shoud be 70. Pulses are swallowed one by one, by choosing the next input at every positive edge of the half of the clock. In any time, the next increasing the divider operation starts from the current input. For example assume that the division factor is 66, and the next division factor is 64. So for division to 66 starting from in0, firstly in1 is chosen then in2 is chosen, so division becomes

66. Then to divide 64, there should be no switching operation, and as in2 was chosen, it continues as it is. This operation is achieved by adding the current division factor difference to the previous one.

The block schematic can be seen in Figure 4.23. As it is seen there is a counter whose clock should be chosen with speacial care. Before mentioning why selection of the counter is important, it is better to continue to explain the operation of the block. The change at the output of the $\Sigma\Delta$ modulator makes counter to start to count. In every increament of the counter, the next phase is selected by the 4 to 1 multiplexer. This selection continues until the output of the counter is equal to the output of the $\Sigma\Delta$ modulator. So as it is explained occurance of the glitches is eliminated. However if the clock of the counter is chosen as seen in Figure 4.22, then while switching from in1 to in2 and from in3 to in4 glitches are expectable to occur. Beacuse selection starts in the falling edge of the selected signal and because there is a delay in the selection operation, a glitch occurs. To prevent this to be happened, appropriate clock should be chosen. In fact in the design there are many clock candidates, however there is only one suitable clock, which is the clock_bar of the VCO divided by TSPC based flip flop. By choosing it as the clock, glitch free output is obtained.

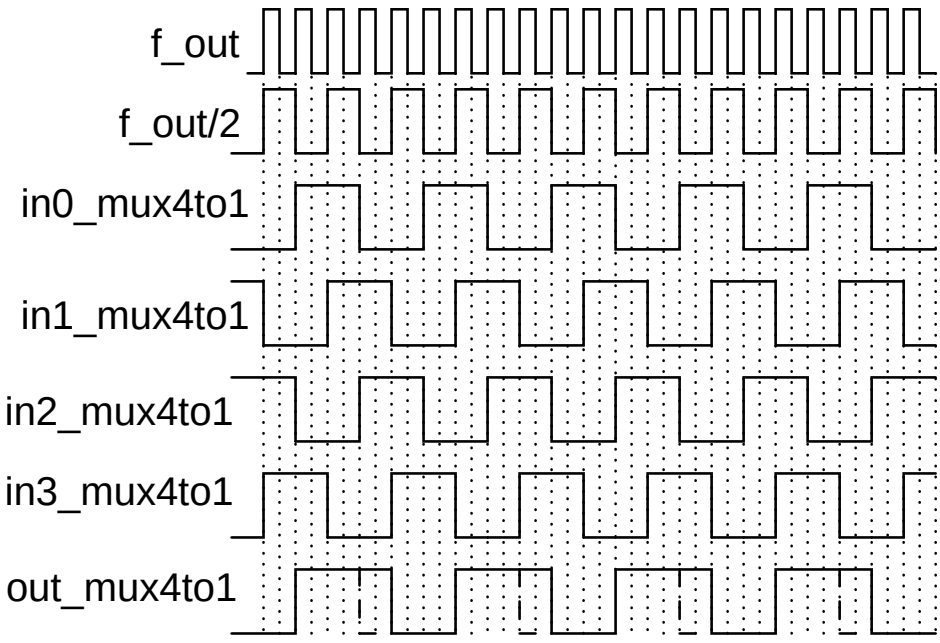


Figure 4.22. Division by 5

Altough the clock problem is solved, counter in the design is problematic. This problem can be seen in Figure 4.26. As it is seen, altough S01 should be high, when in the falling edge of S00, S01 does not become high when the first transition occurs. So phase controller selects one of the previous signals instead of selecting the next phase. So undesirable glitch occurs. This problem should be solved to obtain the expected results.

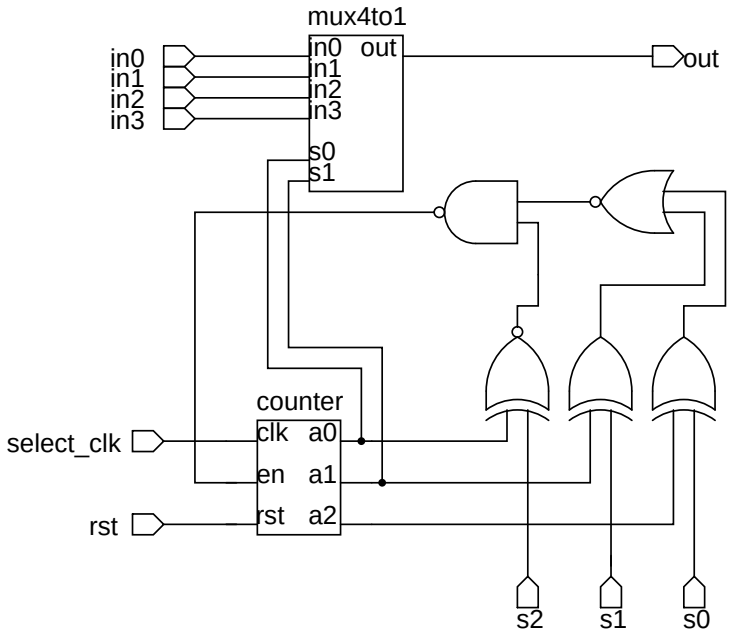


Figure 4.23. Phase controller

4.12. Simulation Results of Low Level Design

Altough in every design steps blocks are simulated to see whether they are working or not, not all of the results could find suitable places for themselves. Here only the overall design results are seen. For example in Figure 4.27 the control voltage of the VCO is seen before adding the $\Sigma\Delta$ modulator. Here it is seen that tune voltage of the VCO is converged to a point. That voltage value corresponds to the voltage that is needed to synthesize the frequency whose division is equal to the reference frequency. This frequency match can also be seen in Figure 4.28. As it is seen, settling time is very low with respect to the specifications. The output of the charge pump can also be seen in Figure 4.29. The pump durations are easily seen. Those sudden pulses are supressed by the loop filter, so they do not generate spurs. In addition, the tune

Figure 4.24. The delay in the counter

voltage is not clear as it was expected. Because it is the voltage of two varactors in the VCO design and because there is a huge swing at the other ports of the varactors.

In Figure 4.30 another simulation result of the tune voltage of the oscillator is seen, however this design is also without $\Sigma\Delta$ modulator. In Figure 4.31 the matching of the divided signal and the reference signal is seen.

After seeing that PLL is working, $\Sigma\Delta$ modulator is added to synthesize the expected frequency. However, as it is seen in Figure 4.32 the tune voltage could not converge to a value. In fact it should be as above simulation results. This is because of the counter design as it was mentioned. In Figure 4.33 frequencies of the divided signal and the reference signal are seen. Altough everything seems good by looking that figure, that is the divided signal lingers around 26 MHz, a look to the Figure 4.34 shows the problem. In that figure the frequency of the output of the phase controller is seen. It is expected to be below 440 MHz. However there are some points that is much higher than that value. This problem is because of the counter and it was mentioned above.

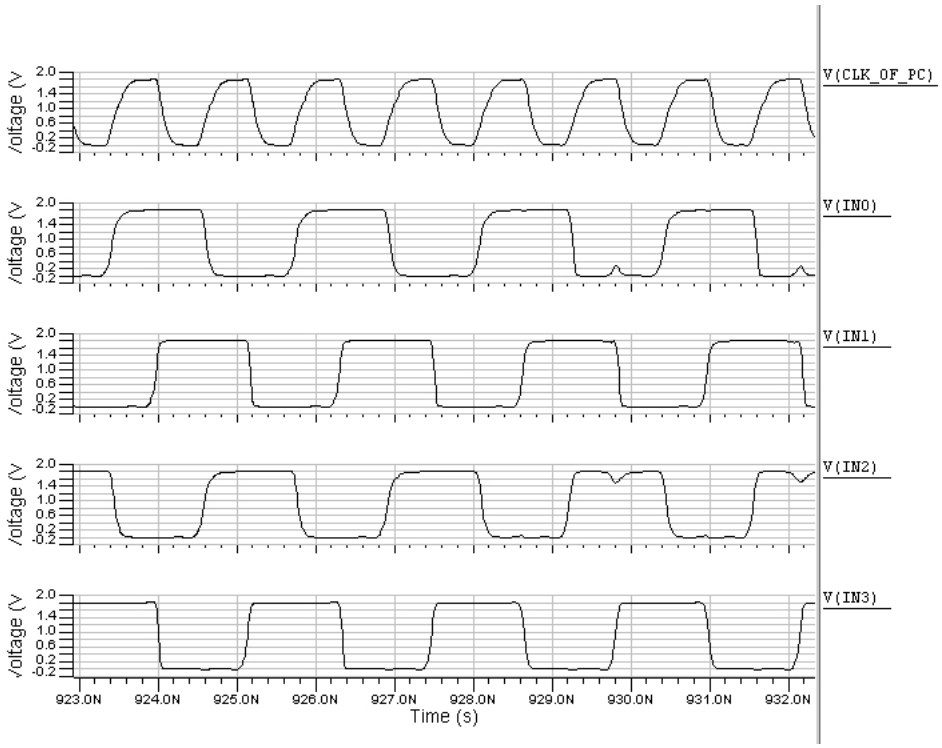


Figure 4.25. The clock of the phase controller

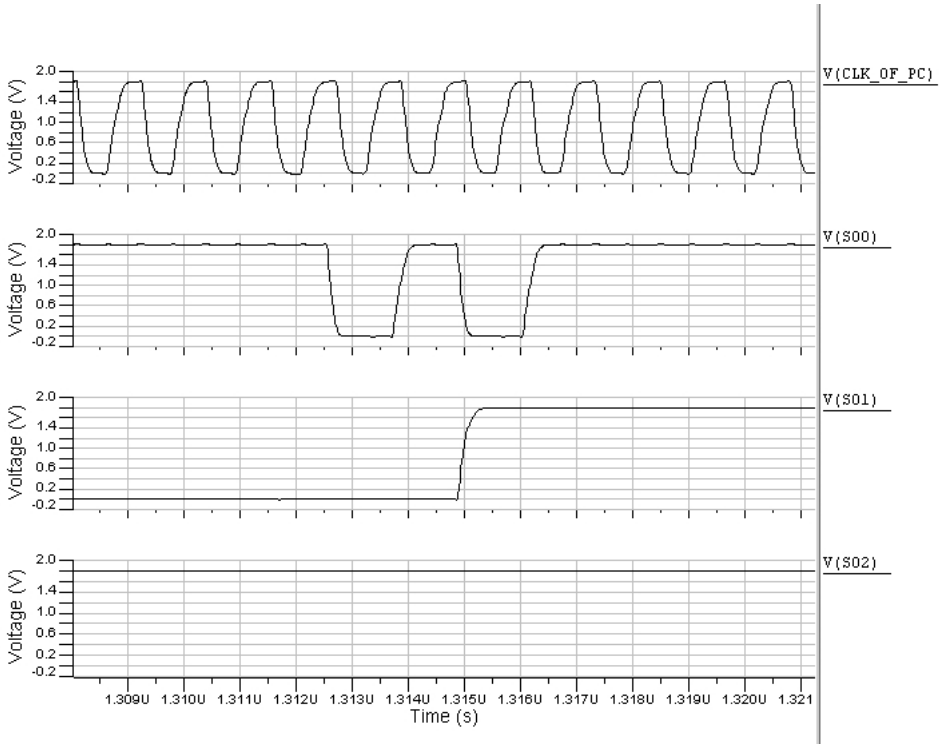


Figure 4.26. Problem at counter

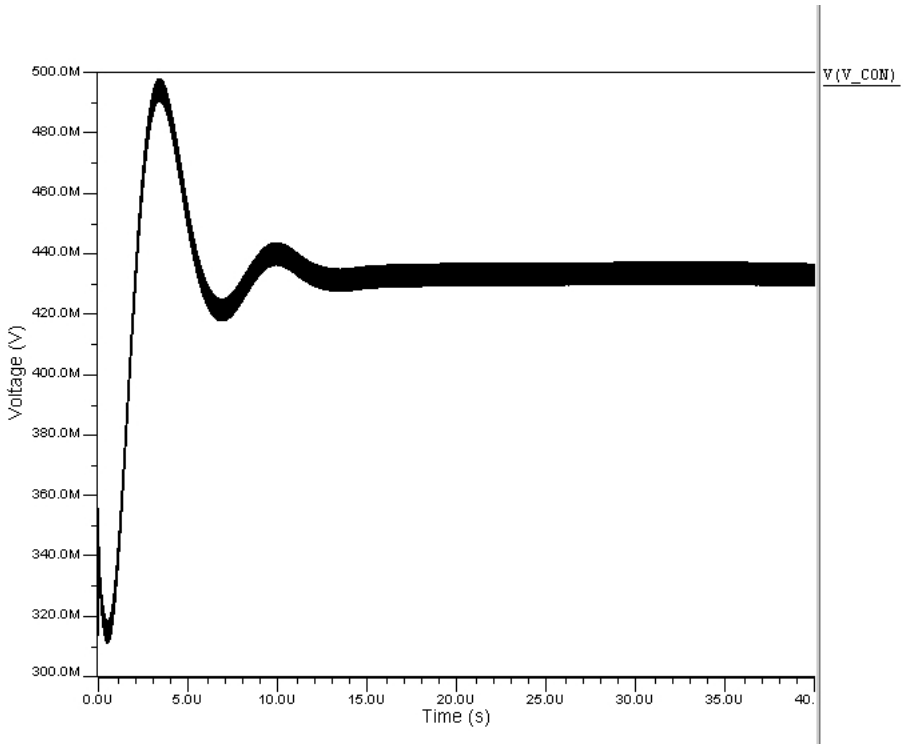


Figure 4.27. Without ΣΔ modulator

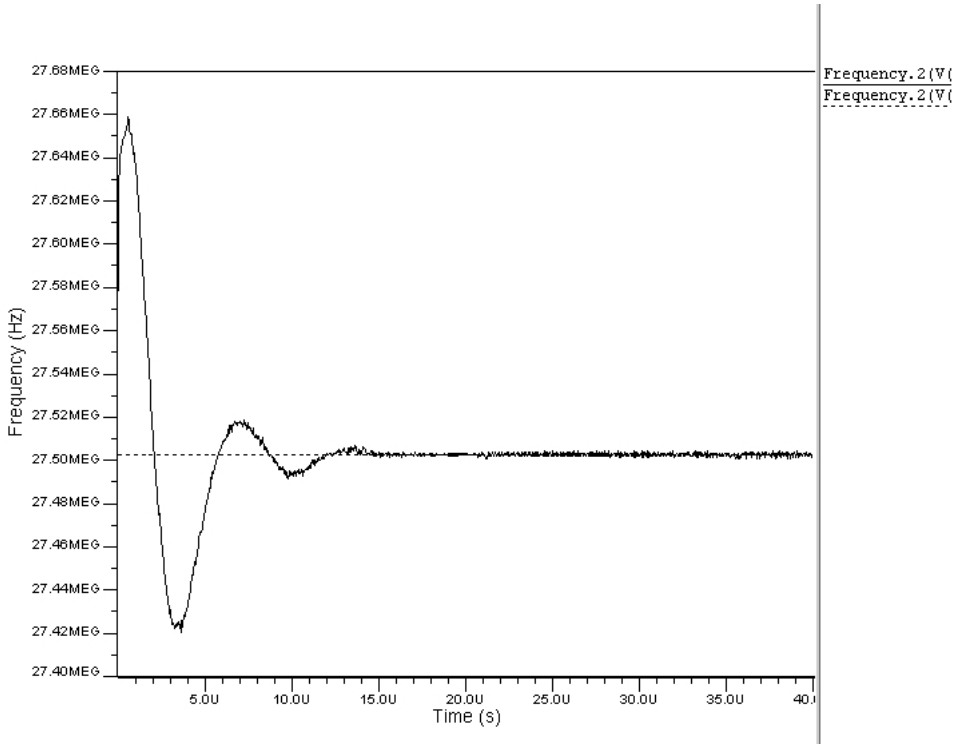


Figure 4.28. Frequency match

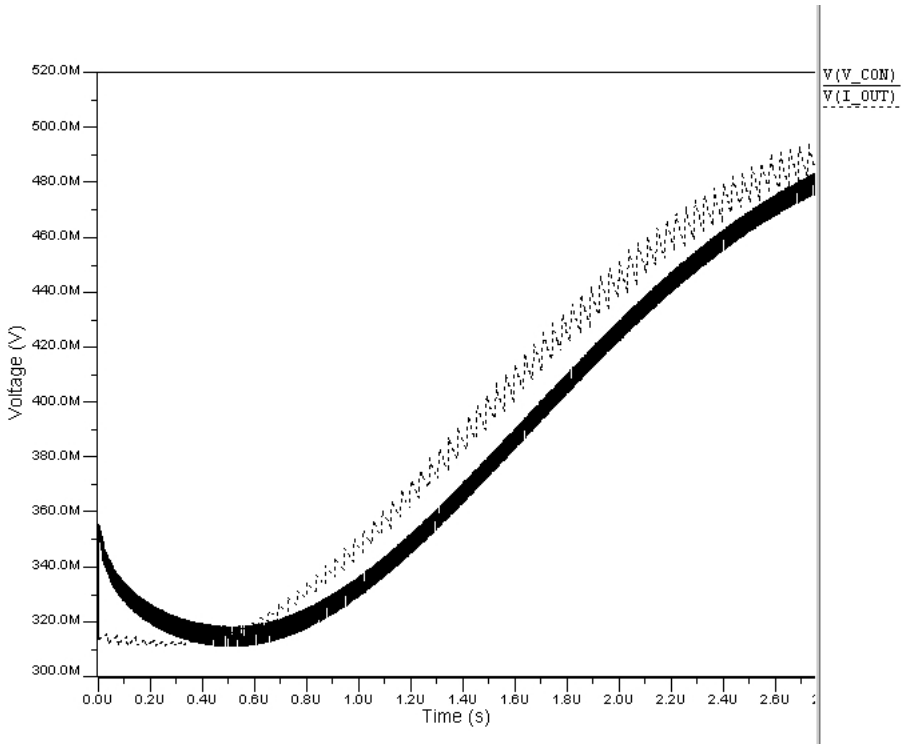


Figure 4.29. Charge pump out

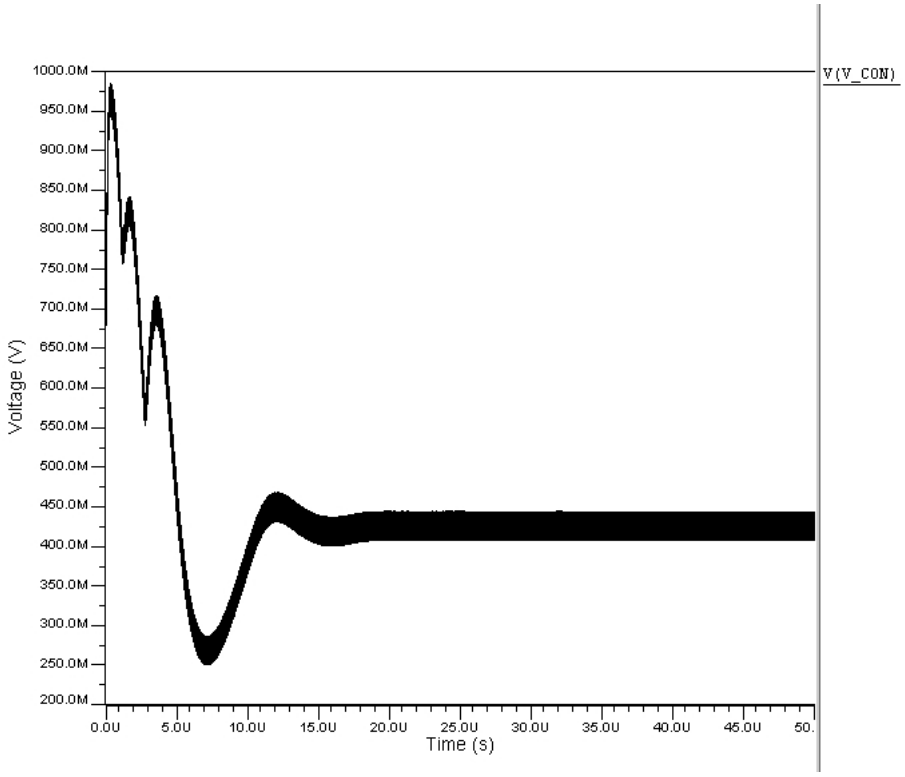


Figure 4.30. A different simulation result without $\Sigma\Delta$ modulator

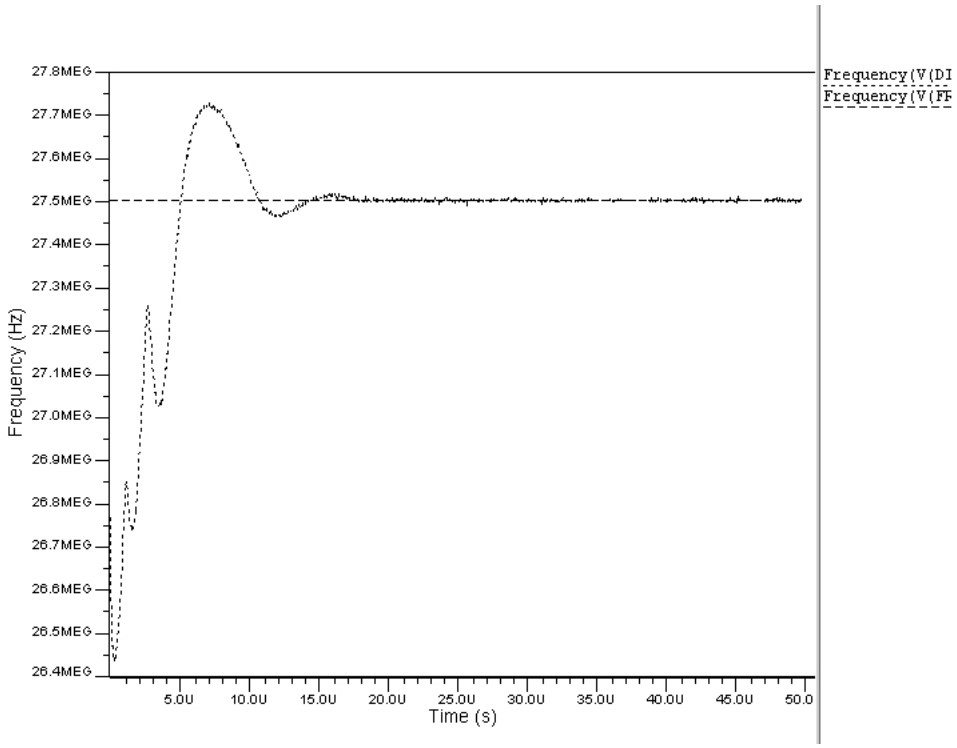


Figure 4.31. Frequency match for the second simulation

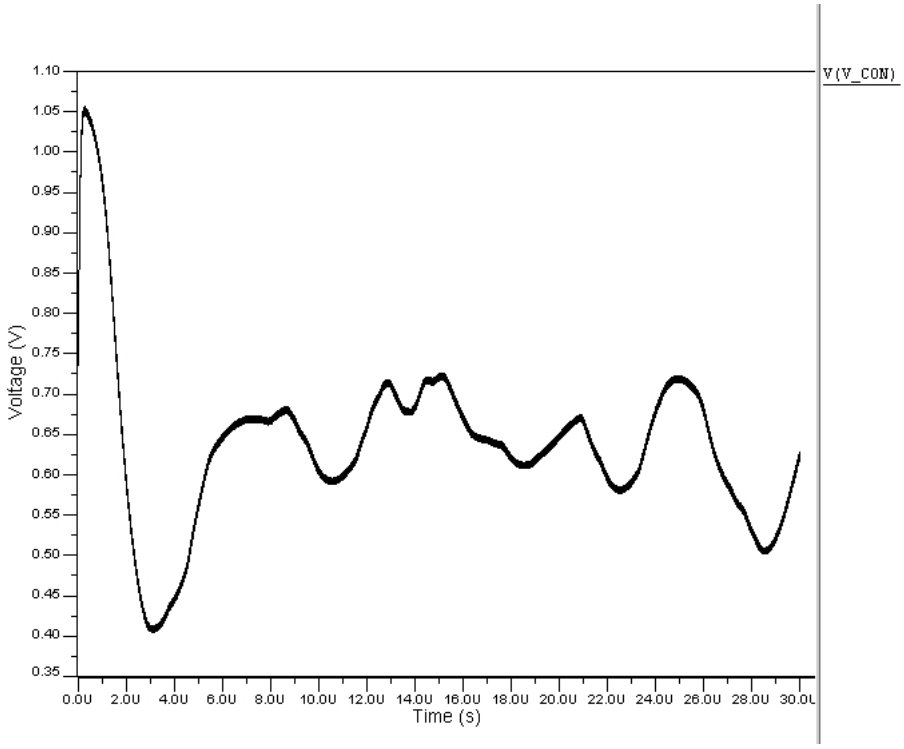


Figure 4.32. With $\Sigma\Delta$ modulator

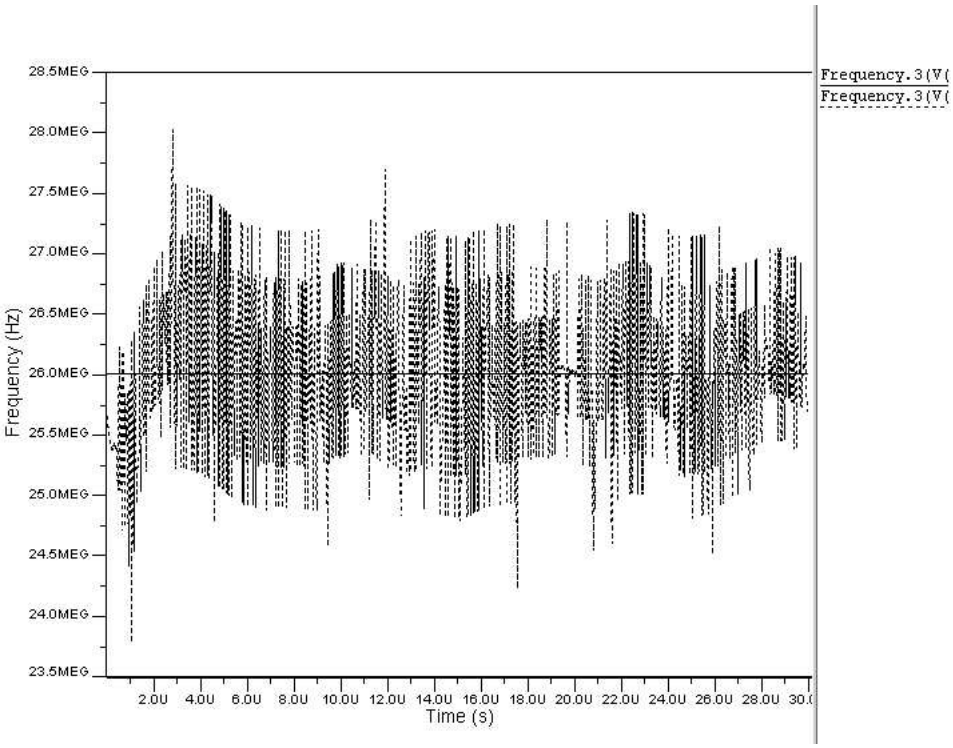


Figure 4.33. With $\Sigma\Delta$ frequency match

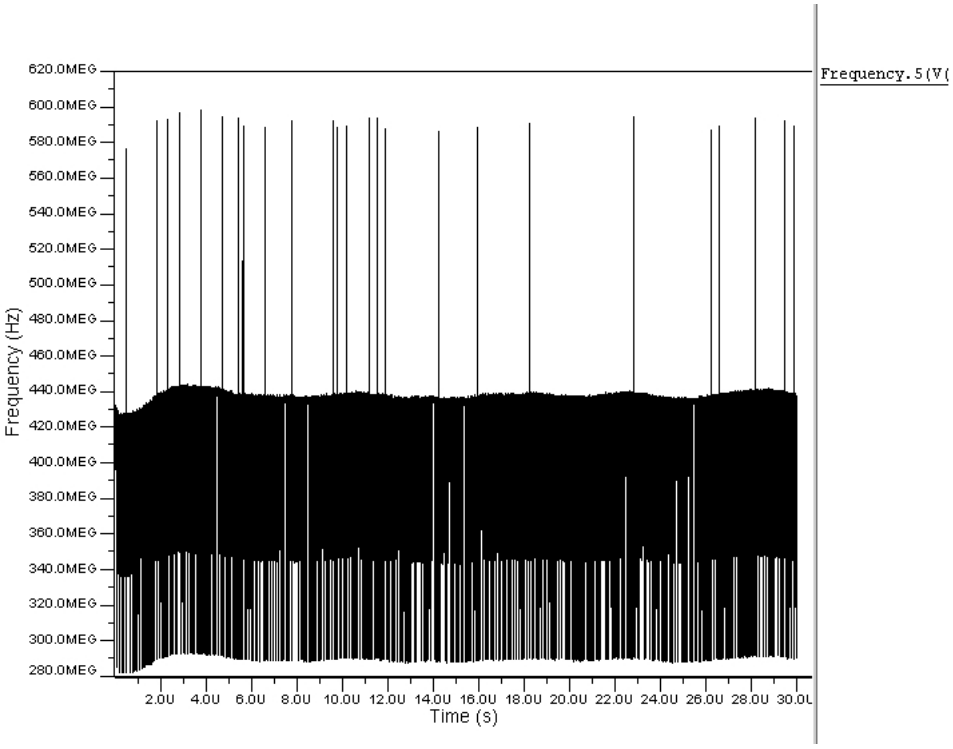


Figure 4.34. Phase select error

5. CONCLUSIONS

In this thesis, a fractional N phase locked loop with $\Sigma\Delta$ modulator for DCS1800 is designed starting from the system level to the end of its ciruit design. In system level design, everything was fine and the designed PLL was capable of synthesing the necessary frequency and modulating the incoming data. System level design was performed at EPFL in Lausanne by using Advanced Design System (ADS). In system level, all specifications of the DCS1800 were met. Although system level design is one of the steps of a bigger project, the design was continued by circuit level implementation at Boğaziçi University. In circuit level design, some problems occured, which are left as future work. These are mentioned in section 4.

In system level, according to the requirements of DCS1800, the topology of the PLL, the modulation topology, the type of $\Sigma\Delta$ modulator, the loop filter order, the location of the poles and the zeroes of the filter response were decided. How these decisions were made is explained in section 3.

After deciding to the parameters above, tests were started at system level. Between the two modulation topologies, direct modulation topology was chosen instead of two point modulation. The reason is that in direct modulation topology, modulation is done directly by modulating the frequency command word of the $\Sigma\Delta$ modulator, whereas in two point modulation, in addition to modulating the FCW, VCO is also modulated by the input analog signal. As it is understood, direct modulation is more digital, and it does not need fine analog VCO design. Tests are done and it was seen that direct modulation also was giving sufficient results. These are all explained in section 3.

Then design continued at circuit level. At this design level, the job was to implement circuits of all of the blocks used in the system level. For example PFD was a black box in system level with certain behaviour, however in circuit level that behaviour should be realized by circuit components. At this level this was done exactly.

Every block at system level was searched in the literature and the suitable ones were chosen and implemented. At this level the task was easy, but at the same time it was complicated, because there were many different implementations. It took time to decide which implementation was suitable for our application. The implementation of all the blocks are explained in section 4.

The tests done at circuit level were very time consuming. Thus the circuit was changed a little for simulation. It is worth to explain it here because sometimes, a little change in a circuit can shorten the simulation. For example while the clock of the $\Sigma\Delta$ modulator was the divided signal, simulation time was 4 times slower. By choosing one of the outputs, as an input at somewhere in the design creates a feedback loop. So this slows down the simulation drastically. The tests were done by breaking that feedback, altough it affected the performance of the circuit.

There are many tasks remaining as future work, when this research is finished. Some of these are mentioned in the text; however, it is better to mention all of them here again. The topology of the $\Sigma\Delta$ modulator should be changed because all of the band is not spanned with the topology used in the design. Or to span all of the band, reference frequency should be chosen as the width of the band or even higher. If this is done then to obtain the same resolution the width of the FCW should be chosen appropriately.

The designed VCO could not meet the phase noise requirments, it should be designed with a better technology or the tricks to increase the noise performance mentioned in the VCO design section should be considered and tried.

Finally, the counter in the phase controller block should be designed for the worst case scenario.

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