LOW-VOLTAGE LOW-POWER DESIGN AND IMPLEMENTATION OF CURRENT-MODE CIRCUITS

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ABSTRACT

LOW-VOLTAGE LOW-POWER DESIGN AND IMPLEMENTATION OF CURRENT-MODE CIRCUITS

Low-voltage and low-power analog and digital circuits are needed to realize battery-optimized, reliable and low-cost electronic devices for many applications. Example applications include remote environmental monitoring, medical diagnostics and consumer products. The need for design techniques to allow circuits to maintain an acceptable level of performance when the supply voltages are decreased is immense.

This work is focused on the issues associated with the novel design techniques of current-mode circuits for the applications which require low-power consumption. Firstly, different types of building blocks suitable for low-voltage and low-power operation are proposed, designed and simulated. Then, these building blocks are used to implement current-mode active elements such as current differencing buffered amplifiers (CDBA), operational transresistance amplifiers (OTRA) and current differencing transconductance amplifiers (CDTA). Finally, various analog filters are designed by using the proposed active elements in order to demonstrate the efficiency and usefulness of the proposed circuits. HSPICE tool along with UMC 0.18 μm twin-well CMOS technology is used in this work for schematic capture, simulation and measuring the noise performance. The proposed circuits are translated to their corresponding layouts using Cadence Virtuoso Layout Editor.

ÖZET

DÜŞÜK BESLEME GERİLİMLİ DÜŞÜK GÜÇ TÜKETEN AKIM-MODLU DEVRELERİN TASARIMI VE GERÇEKLENMESİ

Bugün birçok uygulamada gerekli olan düşük güç sarfiyatlı, güvenilir ve düşük maliyetli elektronik ürünlerin tasarlanabilmesi için düşük besleme gerilimleriyle çalışabilen analog ve sayısal devrelere ihtiyaç vardır. Düşük güç ihtiyacı gerektiren en önemli uygulamalar uzaktan izleme sistemleri, tıbbi teşhis cihazları ve tüketici elektroniği olarak sıralanabilir. Besleme gerilimleri düşürüldüğünde kabul edilebilir bir seviyede performans elde etmek için yeni devre tasarımı tekniklerine duyulan ihtiyaç büyüktür.

Bu tez düşük besleme gerilimi ile çalışan ve düşük güç tüketen uygulamalar için kullanılabilecek güvenilir akım modlu devrelerin tasarımı ve tasarlanan devrelerin uygulanabilirliği üzerine odaklanmıştır. İlk olarak düşük besleme geriliminde çalışmaya uygun değişik devre blokları tasarlanmış ve simüle edilmiştir. Daha sonra tasarlanan bu bloklar yardımıyla değişik akım modlu aktif elemanlar gerçekleştirilmiştir. Tasarlanan aktif elemanlar sırasıyla akım farkı alan tamponlanmış kuvvetlendirici (CDBA), işlemsel geçiş direnci kuvvetlendiricisi (OTRA) ve akım farkı alan geçiş iletkenliği kuvvetlendiricisidir (CDTA). Son olarak tasarlanan aktif elemanların uygulanabilirliğini göstermek amacıyla değişik süzgeç devreleri önerilmiştir. Tasarlanan devrelerin performansı HSPICE programı yardımıyla test edilmiştir. Simulasyonlarda UMC firmasına ait 0.18 μm CMOS teknoloji parametreleri kullanılmıştır. Önerilen devrelerin serimleri (layout) Cadence Virtuoso Layout Editor ile yapılmıştır.

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f_{CLK}	Clock frequency
f_T	Transition frequency
I_{SC}	Short-circuit current
k	Boltzman constant
P_D	Dynamic power consumption
P_{SC}	Short-circuit power consumption
P_{STAT}	Static power consumption
Q	Quality factor
R_m	Transresistance of an OTRA
S	Sensitivity
V_{DD}	Positive power supply voltage
V_{SS}	Negative power supply voltage
α_p	Current transfer ratio between terminals p and z
α_n	Current transfer ratio between terminals n and z
β_v	Voltage transfer ratio between terminals z and w
ε_p, ε_n	Current tracking errors
ε_v	Voltage tracking error
ω_o	Angular resonant frequency
ASIC	Application Specific Integrated Circuit
CC	Current Conveyor
CCI	First Generation Current Conveyor
CCII	Second Generation Current Conveyor
CCIII	Third Generation Current Conveyor
CDBA	Current Differencing Buffered Amplifier
CDTA	Current Differencing Transconductance Amplifier
CFOA	Current-Feedback Operational Amplifier
CMOS	Complementary Metal-Oxide Semiconductor
DO-OTA	Dual-Output Operational Transconductance Amplifier

DVCC	Differential Voltage Current Conveyor
ECCII	Electronically Controlled Current Conveyor
FHSS	Frequency Hopping Spread Spectrum
FTFN	Four-Terminal Floating Nullor
GBP	Gain-Bandwidth Product
IC	Integrated Circuit
IRN	Input Referred Noise
ISM	Industrial Scientific Medicine Band
MOS	Metal-Oxide Semiconductor
NMOS	N-type Metal-Oxide Semiconductor
opamp	Operational amplifier
OTRA	Operational Transresistance Amplifier
PMOS	P-type Metal-Oxide Semiconductor
THD	Total Harmonic Distortion
VLSI	Very Large Scale Integration

1. INTRODUCTION

Low-voltage signal processing is one of the most important aims of today's analog designers. With the advent of the portable electronic and mobile communication systems low-voltage and low-power circuit design has gained importance. For the operation of cell-phones, hearing aids etc, batteries are the main source of power. They need low-power dissipation in order to have long battery life. Figure 1.1 illustrates the International Technology Roadmap for Semiconductors [1].

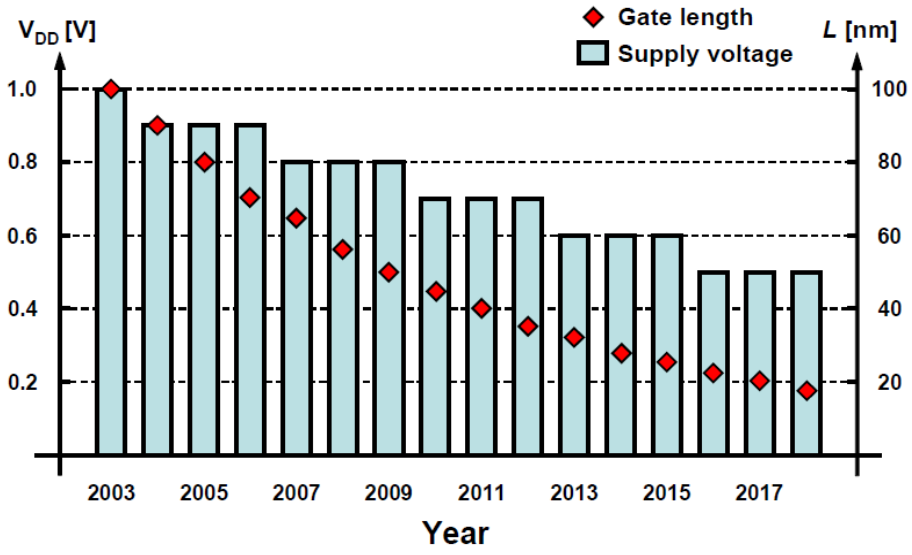

Figure 1.1. Semiconductor Industry Association (SIA) forecast of CMOS voltage supply

Another reason for the low-voltage operation is today's advanced submicron technology. Smaller feature sizes result in larger local electrical fields as high as 5 MV/cm. Hence, the supply voltage has to be reduced in order to ensure device reliability.

The lowest supply voltage can be obtained by biasing MOS transistors in weak-inversion since this gives the smallest gate to source voltage for a given transistor. However, for high frequency applications, transistors should be biased in strong inversion rather than in weak-inversion. This increases the gate to source voltage of a device and therefore the minimum supply voltage. In addition to that, the power consumption per unit area has been increased due to the large integration. In order to reduce the power

dissipation, supply voltages have to be reduced since the dynamic power consumption of digital circuits is proportional to the square of the power supply. However, a reduction in the supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing.

At moderate low-voltages many of the proven circuit design techniques can be directly used as before or with little sacrifice of circuit performance [2]. However, scaling the supply voltage down to this range presents a formidable challenge to the design of analog circuits. This challenge comes from the fact that the threshold voltages of MOSFET devices are relatively high for the given supply voltage ranges [3]. Scaling down the threshold voltage of MOSFETs reduces the performance loss somewhat, but it has its own disadvantages, i.e. the increase in the static power dissipation. Performance of digital circuits is improved by scaling, but the analog cells benefit marginally because minimum size transistors cannot be used due to noise and offset requirements.

In today's design techniques the aim is to achieve high speed and high integration on-chip with a large dynamic range. One of the factors which affect these parameters is power dissipation in the circuit. There are three major sources of power dissipation [4];

- Dynamic power dissipation
- Static power dissipation
- Short-circuit power dissipation

Dynamic power dissipation is given by;

$$P_D = \alpha C_L f_{CLK} V_{DD}^2 \tag{1.1}$$

where α is called the switching activity. C_L is the load capacitance and f_{CLK} is the clock frequency. It can be easily seen in (1.1), the most efficient method in order to reduce power dissipation is to reduce the power supply voltage. Due to increased demands on the system performance, the clock frequency goes up. Power dissipation can be minimized by reducing the switching activity and the output load capacitance. The switching activity can be reduced by using proper circuit and system designs and the load capacitance can be

reduced by using small device dimensions. However, the reduction in power dissipation is the most effective when V_{DD} is lowered. The static power consumption can be written as;

$$P_{STAT} = I_{STAT} V_{DD} \tag{1.2}$$

During switching in CMOS, both NMOS and PMOS are simultaneously active for a short period of time and an instantaneous short-circuit current (I_{SC}) flows from the power supply directly to ground. The power consumption due to I_{SC} is given by;

$$P_{SC} = I_{SC} V_{DD} \left(\frac{t_{SC}}{T} \right) \tag{1.3}$$

Thus, the total power consumption can be written as;

$$P_{TOT} = P_D + P_{STAT} + P_{SC} = \alpha C_L f_{CLK} V_{DD}^2 + I_{STAT} V_{DD} + I_{SC} V_{DD} \left(\frac{t_{SC}}{T} \right) \tag{1.4}$$

Lowering power dissipation is also important for a high-performance system. An increase in power dissipation increases the ambient temperature which worsens the electro-migration reliability problems. The low-voltage operation complicates the design of the circuits. The current-mode design technique is a good choice for the low-voltage and high performance analog design. The main advantage of the current-mode design is that it offers voltage independent high-bandwidth analog circuits. The designer deals with current levels for the operation of the circuits in current-mode design.

However, in voltage-mode, performance of the circuits is determined by voltage levels at various nodes. Voltage-mode circuits suffer from the following disadvantages;

- The output voltage can not change instantly when there is a sudden change in the input voltage due to stray and other circuit capacitances.
- There is a trade-off between the gain and bandwidth.
- Slew-rate is dependent on the time-constants associated with the circuit.

- Circuits do not have high voltage swings.

Therefore, voltage-mode circuits are not suitable for high frequency applications. In current-mode circuits, voltage levels are not important in determining the circuit performance. The nodes have low impedance and voltage swings across them are small. The low means low time-constant and thus the bandwidth will be higher compared to voltage-mode circuits. Slew-rate is also high if the rate of the output change is high**.**

1.1. Motivation

Low-voltage design of current-mode circuits has become an increasingly interesting subject as many applications switch to portable battery powered operations. The need for design techniques to allow circuits to maintain an acceptable level of performance when the supply voltages are decreased is immense.

The main objective of this thesis is to investigate the feasibility of reliable current-mode circuit design techniques in standard CMOS processes for low-voltage operation. Different types of building blocks suitable for low-voltage and low-power operation are proposed, designed and simulated. These building blocks are used to implement current-mode active elements such as current differencing buffered amplifiers (CDBA), operational transresistance amplifiers (OTRA) and current differencing transconductance amplifiers (CDTA).

The following methodology is used to attain the main objective;

- Overview of past and current research status to cover the existing design techniques for low-voltage and low-power circuits.
- Investigation of challenges imposed by the restriction of low supply voltage.
- Development of building blocks in the design of current-mode circuits for low-voltage operation.
- Application of completed current-mode active elements to demonstrate the efficiency and performance of the proposed circuits.
- Results, comments and discussion with further development.

1.2. Thesis Outline

In Chapter 2, challenges and issues in low-voltage deep-submicron CMOS analog design with the limitations imposed by the reduced supply voltage are addressed. Also different kinds of design techniques suitable for low-voltage operation are examined.

Chapter 3 covers the most important specifications of current-mode building blocks. In addition, main current-mode structures reported in the literature are surveyed.

In Chapter 4, we propose three current differencing buffered amplifier (CDBA) circuits. Then detailed simulation results for the proposed CDBAs are presented. Performances of the proposed circuits are demonstrated on various design examples. A comprehensive performance comparison of the CDBAs is also included in this chapter.

In addition, another active element called operational transresistance amplifier (OTRA) is designed in Chapter 4. Then a voltage-mode multi-function filter configuration is presented to show the usefulness of the proposed OTRA. A detailed comparison of the OTRAs in the literature is also included in this chapter. Moreover, two different types of current differencing transconductance amplifiers (CDTA) with simulation results are proposed. Design examples and performance comparison on tabular format are also given in Chapter 4.

Finally, continuous-time Chebyshev-type low-pass filters for Bluetooth applications are designed in order to show performances of the proposed active elements and a detailed performance comparison is given in Chapter 5.

2. LOW-VOLTAGE DESIGN TECHNIQUES

In this chapter after a brief introduction to the MOSFET operation, different kinds of low-voltage design techniques suitable for analog circuit structures are examined.

2.1. Operation of MOSFET

One of the most important electrical properties of the MOS transistor is the gate to source voltage. It determines the minimum supply voltage at which the amplifier is able to operate. Since the MOS transistor is a voltage driven device, the required transconductance determines the gate to source voltage of a transistor.

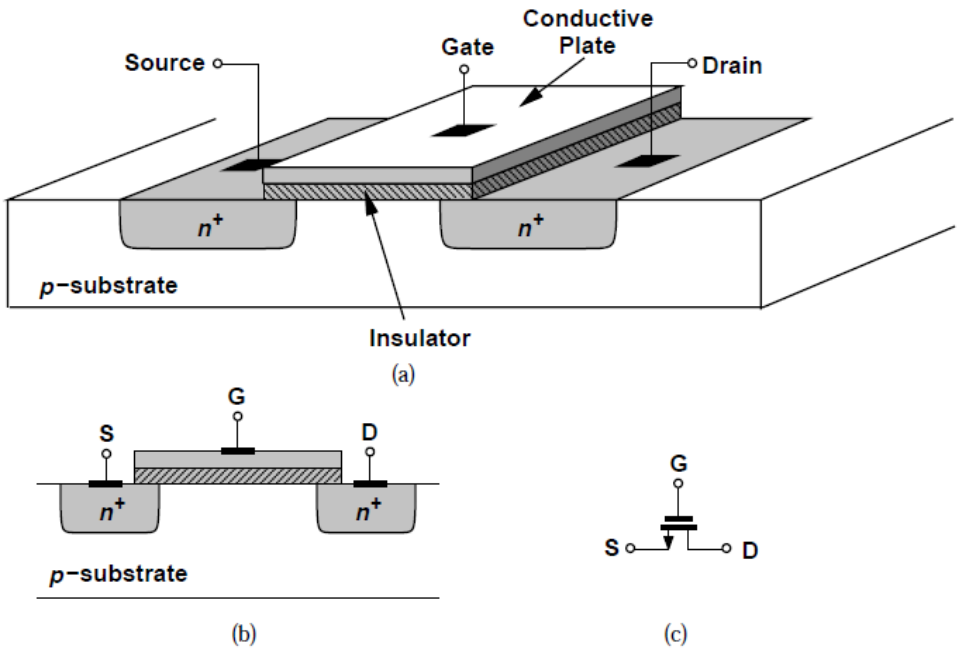

Figure 2.1. (a) Structure of NMOS (b) side view (c) circuit symbol

Two types of MOSFET devices can be defined. NMOS devices consist of n^+ source and drain regions in a p-substrate, while PMOS devices have p^+ source and drain regions in an n-substrate. In the operation of MOSFET, it is concentrated on the NMOS device shown in Figure 2.1. If the gate to source voltage (V_{GS}) of the NMOS transistor is smaller than its threshold voltage (V_T), no channel exists and the NMOS device will be off and in that

case, the drain to source current (I_{DS}) will be zero regardless of the value of the drain to source voltage (V_{DS}).

2.1.1. Strong Inversion ($V_{GS}>V_T$)

When the gate to source voltage (V_{GS}) is greater than the threshold voltage (V_T), a channel is established between the drain and source. In other words, the NMOS device is in strong inversion when the channel is strongly inverted.

2.1.1.1. Linear (Triode) Region. On the other hand, assume that $V_{GS} > V_T$ and that a small voltage is applied between the drain and source, the NMOS device will be on and $I_{DS} > 0$. In that case, the NMOS device is in linear or triode region. In that region $V_{DS} < V_{GS} - V_T$ and the output current for long-channel NMOS devices is given in (2.1);

$$I_{DS}(\text{lin}) = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^{\,2}\right] \tag{2.1}$$

where μ_n is the mobility, W is the channel width and L is the channel length of the NMOS device. C_{ox} stands for the capacitance per unit area introduced by the gate oxide and it equals;

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.2}$$

where ε_{ox} is the oxide permittivity and t_{ox} is the thickness of the oxide. The threshold voltage can be expressed by;

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right) \tag{2.3}$$

where V_{SB} is the source to bulk voltage and V_{T0} is the threshold voltage for $V_{SB} = 0$. ϕ_F is the Fermi potential and the parameter γ (gamma) is called the body-effect coefficient. For

NMOS devices, the threshold voltage is positive, while it is negative for PMOS devices. It is clear that the threshold voltage increases when the source to bulk voltage grows. Therefore, in low-voltage design, the source to bulk voltage should be kept as low as possible.

2.1.1.2. Saturation Region. If V_{GS} voltage is kept constant and $V_{DS} > V_{GS} - V_T$, the NMOS device goes into the saturation region. Figure 2.2 depicts I_{DS}-V_{DS} characteristic of the NMOS device.

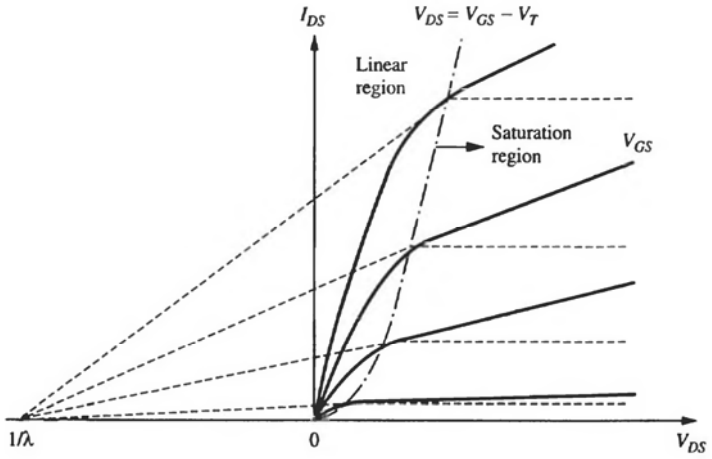

Figure 2.2. I_{DS}-V_{DS} characteristic of the NMOS device

By taking the channel-length modulation into consideration, the output current for long-channel NMOS devices can be expressed by;

$$I_{DS}(\text{sat}) = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{2.4}$$

where λ is called the channel-length modulation coefficient which is an empirical parameter. λ is inversely proportional to channel length and it is more effective in short-channel devices. For low-voltage design, most of the transistors in the amplifier operate on the edge of saturation. Transconductance (g_m) of a transistor can be expressed as;

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T) \tag{2.5}$$

If we want to increase g_m, it may not be possible to increase V_{GS} since this would require a higher supply voltage. Therefore better way to increase g_m is to increase both W/L and I_D.

2.1.1.3 Velocity Saturation. The model derived above is no longer valid for the short-channel devices. The main reason is that the velocity of the carriers is proportional to the electrical field and independent of the value of that field for the linear model [5]. However, as the electrical field increases, it reaches a critical value ξ_c and velocity of the carriers saturates. This effect is called velocity saturation and it is illustrated in Figure 2.3.

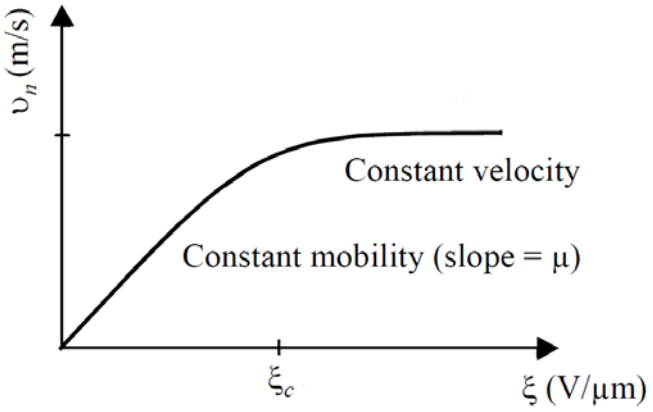

Figure 2.3. Velocity saturation effect

Velocity saturation has some important impacts on the operation of the device. Short-channel devices have an extended saturation region since they enter saturation before V_{DS} reaches $V_{GS}-V_T$, as is illustrated in Figure 2.4. Another important impact is that relationship between I_{DS} and V_{GS} for short-channel devices is linear unlike the long-channel devices which have a quadratic relationship between I_{DS} and V_{GS}. For short-channel devices, modified expression of the drain current in linear region is given by;

$$I_{DS}(\text{lin}) = \kappa(V_{DS})\mu_n C_{ox}\frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}{V_{DS}}^2\right] \tag{2.6}$$

$$\kappa(V) = \frac{1}{1+\left(\frac{V}{\xi_c L}\right)} \tag{2.7}$$

where κ is a measure of the degree of velocity saturation. For long-channel devices, κ approaches 1, while it is smaller than 1 for short-channel devices. As V_{DS} increases, electrical field reaches the critical value and the device becomes velocity saturated. The drain current in the velocity saturation can be expressed by;

$$I_{DS}(\text{sat}) = \kappa(V_{DSAT})\mu_n C_{ox}\frac{W}{L}\left[(V_{GS}-V_T)V_{DSAT}-\frac{1}{2}{V_{DSAT}}^2\right] \tag{2.8}$$

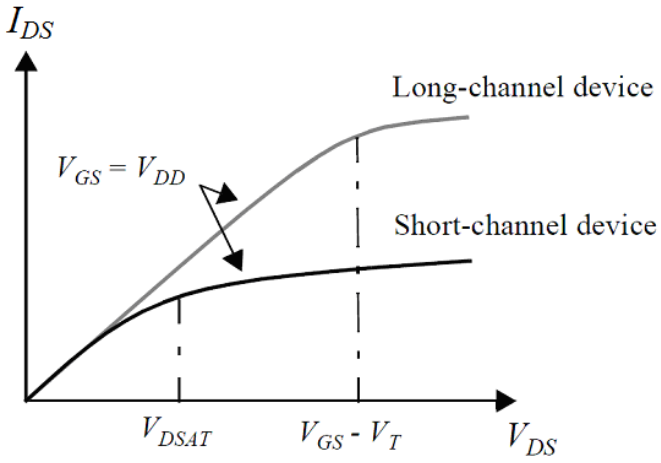

Figure 2.4. I_{DS}-V_{DS} characteristic with velocity saturation effect

For 0.18 μm NMOS device, effects of the velocity saturation are shown in Figure 2.5 and Figure 2.6. V_{DS} and V_{GS} are swept from 0 to 1.8 V.

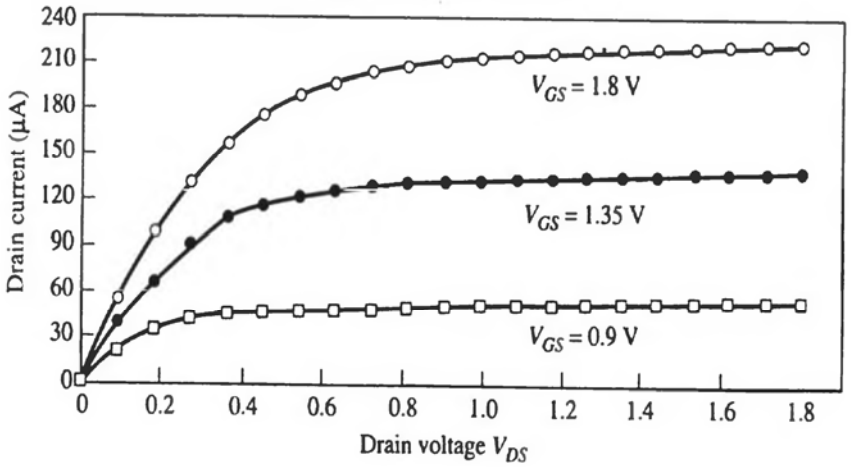

Figure 2.5. I_{DS}-V_{DS} characteristic for 0.18 μm NMOS device

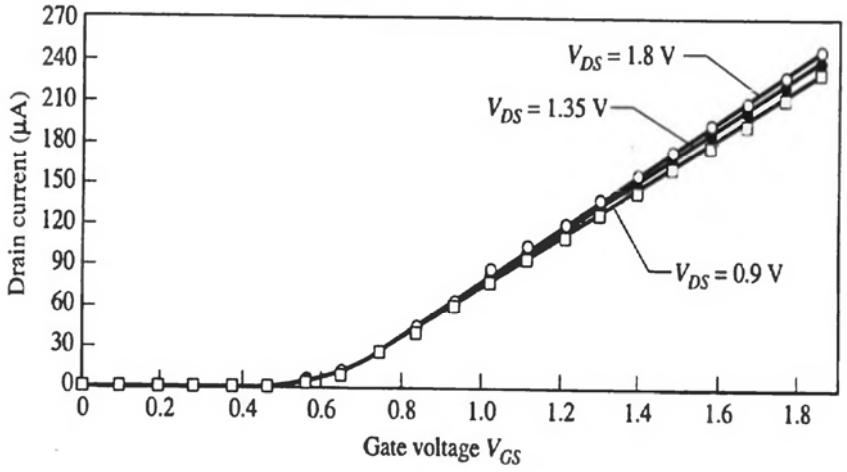

Figure 2.6. I_{DS}-V_{GS} characteristic for 0.18 μm NMOS device

Linear relationship between I_{DS}-V_{GS} and extended saturation region can be clearly seen from Figure 2.6 [6].

2.1.2. Weak-Inversion (V_{GS}<V_T)

So far we have assumed that I_{DS} current goes to zero when V_{GS} voltage drops below the threshold voltage. However, it is obvious from Figure 2.7 that the current does not drop abruptly to zero and the device is partially conducting when V_{GS} equals the threshold voltage. This effect is called weak-inversion conduction.

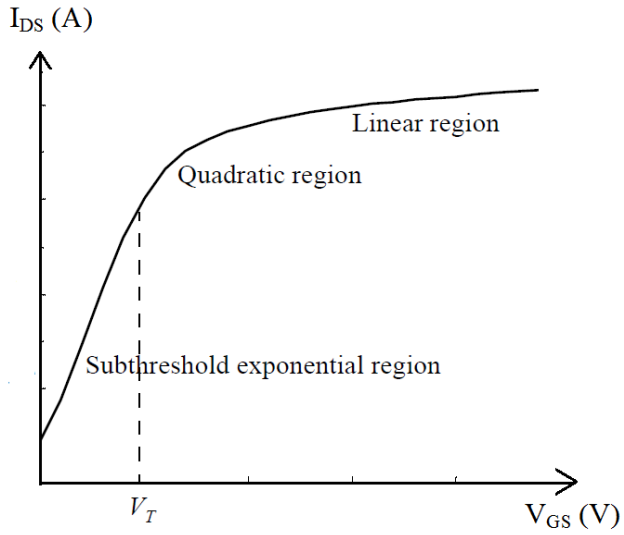

Figure 2.7. I_{DS}-V_{GS} characteristic for the NMOS device (on logarithmic scale)

An NMOS transistor operates in weak-inversion region when $V_{GS} < V_T$. In this mode, the transistor saturates when $V_{DS} > 3$ or 4 V_{TH}. $V_{TH} = \frac{kT}{q}$ is called the thermal voltage which is about 25 mV at room temperature.

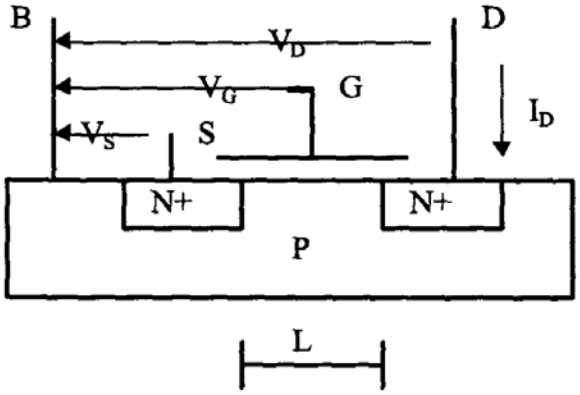

Figure 2.8. Side-view of the NMOS transistor

By looking at the cross-sectional view of the NMOS transistor given in Figure 2.8, I_{DS} current (subthreshold current) for weak-inversion region is expressed by;

$$I_{DS} = I_{D0} e^{\frac{V_G}{nV_{TH}}} \left(e^{\frac{-V_S}{V_{TH}}} - e^{\frac{-V_D}{V_{TH}}} \right) \tag{2.9}$$

$$I_{D0} = 2n\mu_n C_{ox} \frac{W}{L} V_{TH}^2 e^{\frac{-V_{T0}}{nV_{TH}}} \tag{2.10}$$

where

k	Boltzman constant (1.38×10^{-23} J/^{o}K)
T	Temperature in degrees Kelvin
q	Charge of an electron
n	Slope factor = $(C_{ox} + C_{dept}) / C_{ox} \approx 1.5$
C_{ox}	Oxide capacitance
C_{dept}	Surface depletion capacitance
I_{D0}	Characteristic current

According to (2.9) and (2.10), the subthreshold current increases exponentially as the threshold voltage scales down with the technology. Figure 2.9 shows how the subthreshold current scales with the technology [7-8].

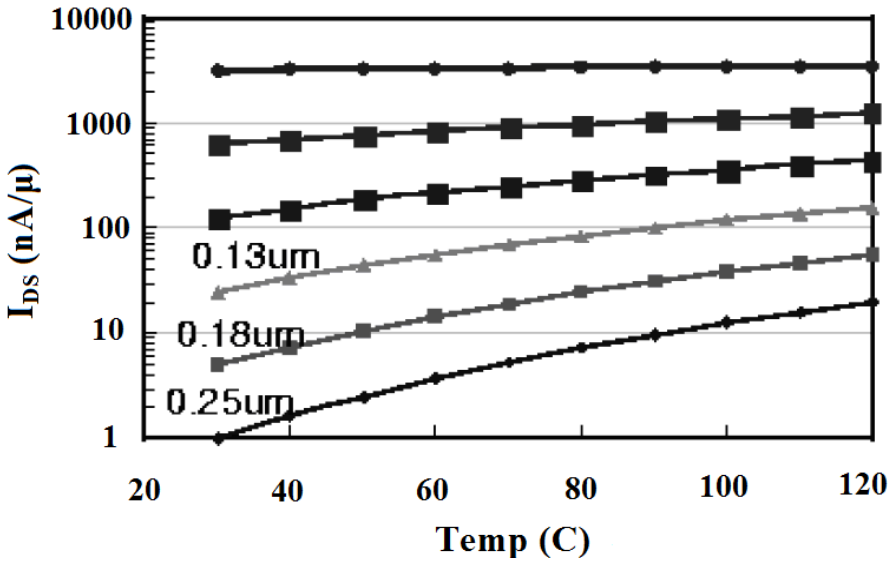

Figure 2.9. Subthreshold current variation with temperature

Because of the exponential relationship in (2.9), devices operating in weak-inversion region are useful for low-voltage and low-frequency applications. One of the application areas is nonlinear systems such as oscillators [9], phase detectors [10] and phase-locked loops [11]. Another application is log-domain filters which rely on the voltage companding principle [12-14]. Moreover, in weak-inversion region, MOSFETs have low saturation voltages (≈ 100 mV), which gives larger voltage swings at low supply voltage even in cascoded MOSFET structures due to exponential dependence of I_{DS} upon V_{GS}.

In weak-inversion region, if source and bulk (substrate) terminals are tied together and grounded ($V_S = V_B = 0$) and $V_{DS} > 3$ or 4 V_{TH}, (2.9) can be simplified as;

$$I_{DS} = I_{D0} e^{\frac{V_{GS}}{nV_{TH}}} \tag{2.11}$$

Transconductance of the NMOS device in weak-inversion region can be easily derived from (2.11) [15];

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}} = \frac{I_{\mathrm{DS}}}{nV_{\mathrm{TH}}} \tag{2.12}$$

From (2.12), it is obvious that g_m is independent of geometry and has a linear dependence with I_{DS} in weak-inversion region. In addition to that, output conductance (g_{ds}) given in (2.13) has a linear relationship with I_{DS}. Thus, a MOS device in weak-inversion region achieves the highest gain and that gain is independent of I_{DS}.

$$g_{\mathrm{ds}} = \frac{I_{\mathrm{DS}}}{V_{\mathrm{E}}} \tag{2.13}$$

where V_E is the early voltage. On the other hand, devices operating in weak-inversion region have several limitations. In order to obtain higher gain, large area for biasing the device is required, which means larger capacitance and higher manufacturing cost [16]. Next, linearity is quite poor in weak-inversion region. Furthermore, frequency response is also quite poor as shown in (2.14).

$$f_{\mathrm{T}} \cong \frac{\mu V_{\mathrm{TH}}}{2\pi L^2} \tag{2.14}$$

where f_T is the transition frequency. (2.14) also shows that in weak-inversion region f_T is independent of the overdrive voltage unlike the case in strong inversion without velocity saturation, but similar to the case with velocity saturation [17]. Another drawback of MOS transistors operating in weak-inversion region is that drain and source to substrate currents associated with the reverse biased diffusion to substrate junction are not negligible compared to the weak-inversion drain current.

2.2. Challenges in Low-Voltage Design in Deep-Submicron

There are numerous challenges in the design of analog circuits in deep-submicron CMOS technology, especially for low-voltage analog circuit design. The threshold voltage is not reduced at the same rate as the power supply drops in standard CMOS technology. Figure 2.10 illustrates the relationship between maximum supply voltage and and threshold

voltage for Intel processes [18]. Using multi-threshold process technology may be a solution to the problem, but unfortunately it is more expensive [19].

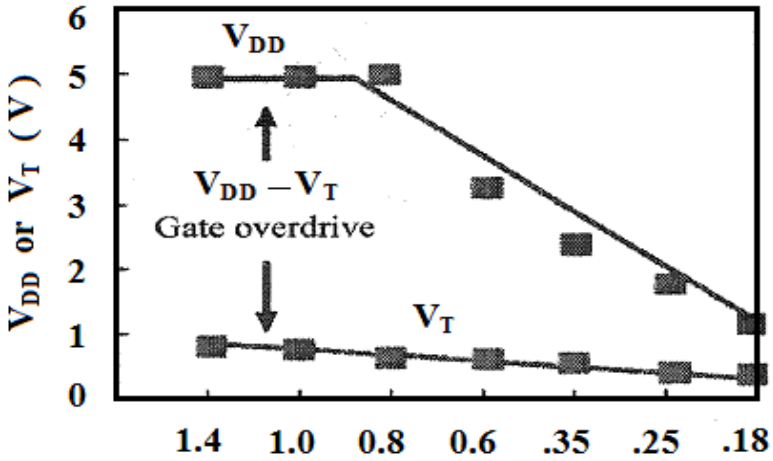

Figure 2.10. Supply voltage and threshold voltage versus technology generation (courtesy from Intel)

Another issue for low-voltage design is the output resistance (r_o). Output resistance is a critical parameter especially in analog circuit design since it determines the intrinsic gain ($g_m r_o$) of a device and the performance of current mirrors and sources. As the technology scales down, output resistance decreases.

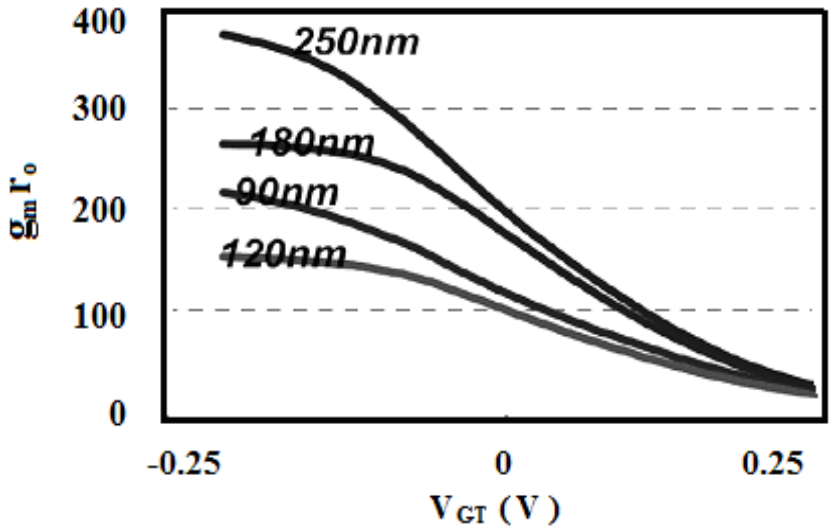

Figure 2.11. Gain versus overdrive voltage with V_{DS}=0.3 V and L=1 μm for different technologies

Figure 2.11 depicts gains of transistors as a function of the overdrive voltage for different technologies. As the voltage swing decreases, performance of the transistors degrades. One way of increasing the output resistance is to use stacking transistor structures, but they are not always compatible with the low supply voltage.

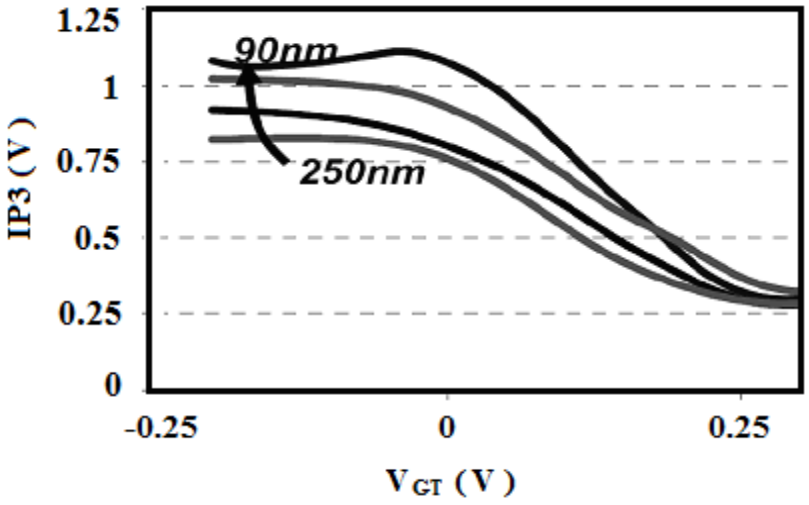

Figure 2.12. Output IP3 versus overdrive voltage with V_{DS}=0.3 V and L=1 μm for different technologies

Linearity is the other important issue in low-voltage design. Third-order intercept point (IP3) is a measure for nonlinear systems and devices. Variations of IP3s with the overdrive voltage for different technologies are shown in Figure 2.12. As the supply voltage goes down, linearity degrades.

One of the most important issues in low-voltage design is the dynamic range degredation. Dynamic range is defined as the ratio of maximum allowable signal voltage swing (or power) under some distortion specifications over the noise floor [19]. The dynamic range is degraded because of the lower allowable signal swing and the larger noise voltages that arise as a result of the smaller bias currents. In order to increase the dynamic range, a low-voltage amplifier needs signal voltages that extend from rail-to-rail.

Matching is another issue in low-voltage design. As supply voltages scale down, maximum voltage swing decreases. In order to maintain the same dynamic range, mismatch errors should be reduced [20]. Threshold voltage (V_T) mismatch of MOS devices

is determined by measuring the difference among the thresholds of many couples of nominally identical devices [21]. The V_T distribution is given in (2.15);

$$\sigma\left(\Delta V_T\right) = \frac{A_{VT}}{\sqrt{WL}} \tag{2.15}$$

where the term A_{VT} is a constant for a given technology. Power supply development according to the Semiconductor Industry Association (SIA) roadmap [22] is shown in Figure 2.13. Bottom line in the figure indicates the matching of a pair of minimum size transistors, while the matching coefficients for different technologies are represented by the crosses [23].

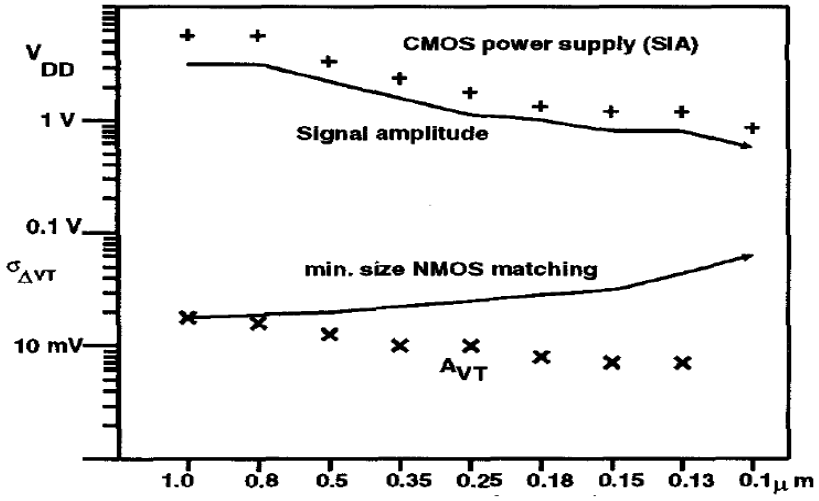

Figure 2.13. Development of power supply voltage and A_{VT} through various process generations

Noise is also a problematic issue in low-voltage analog circuit design. As the size of the devices scales down, the noise increases. Additionally, digital noise coupling comes into play in submicron devices. Switching activity in digital part results in a noise which can easily propagate to the analog part of the circuit through the substrate. Although some measures can be taken such as using separate power supply and careful routing, common substrate is still a conductive path between digital and analog parts of the circuit. Digital noise coupling mechanism is depicted in Figure 2.14 [24]. So far some digital noise coupling reduction methods have been reported in the literature [25-29].

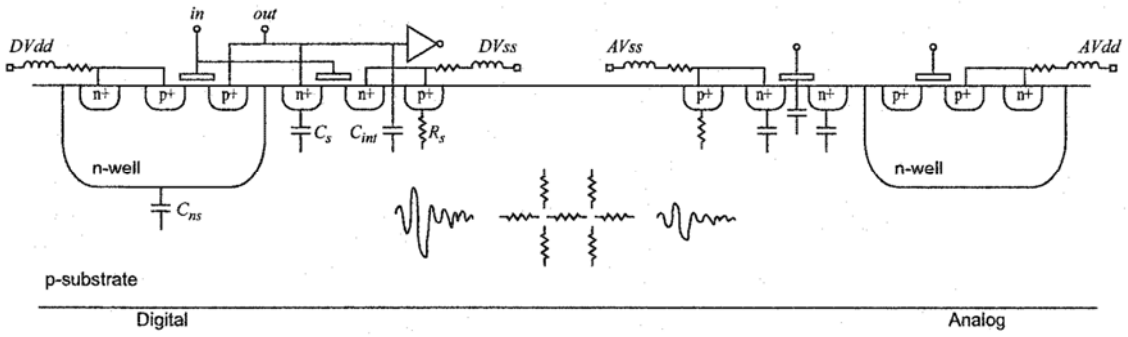

Figure 2.14. Noise coupling path

Gate leakage is a relatively new effect and can not be ignored in deep-submicron devices. Gate leakage current is very dependent on the oxide thickness and this dependency can be seen in Figure 2.15.

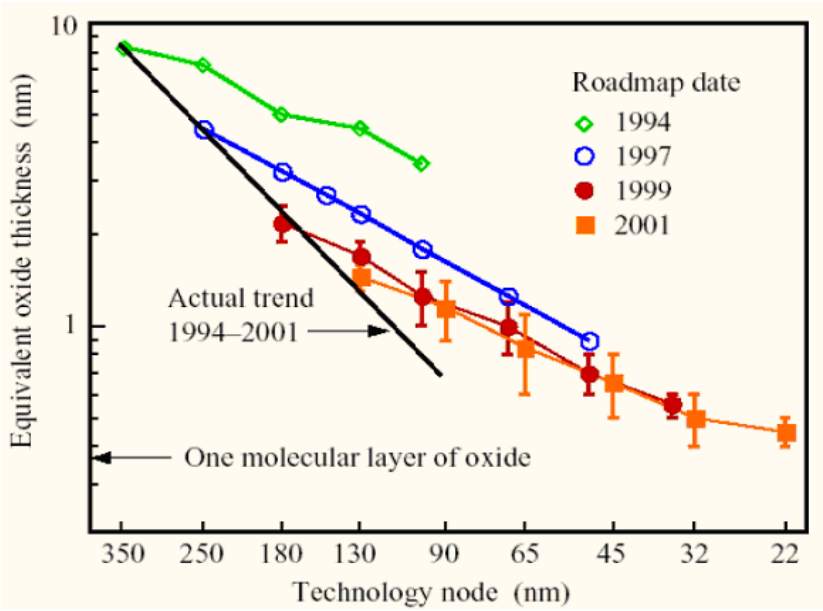

Figure 2.15. Oxide thickness for different CMOS technologies

In addition to that, it depends on V_{GS}, V_{DS} and the gate area. Figure 2.16 illustrates the graph of the gate leakage current versus V_{GS}. For this graph all W/L ratios are selected as 100 µm / 0.13 µm except for 0.18 µm technology whose W/L ratio is 100 µm / 0.18 µm [30]. It is clear that as the technology scales down, gate leakage current increases. The impacts of the gate leakage current can be investigated by using the circuit given in Figure 2.17 where i_c depends on frequency, while i_{tunnel} does not.

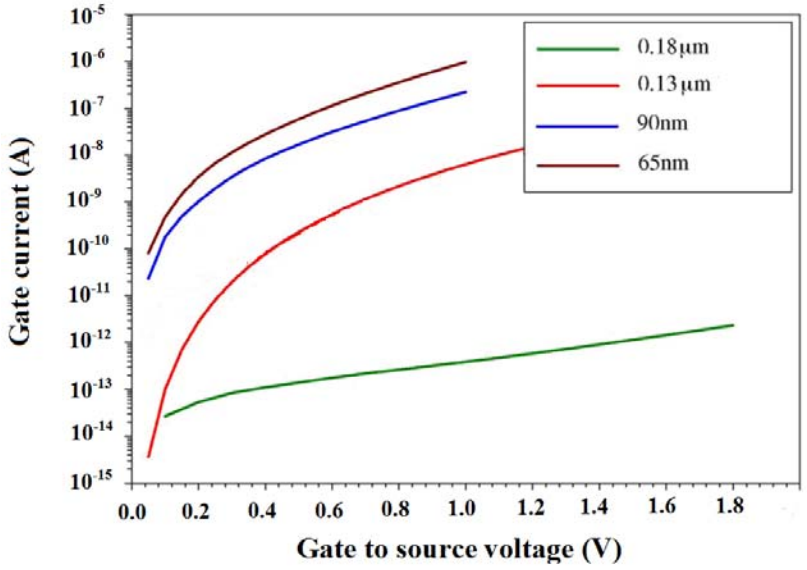

Figure 2.16. Gate leakage current for different CMOS technologies

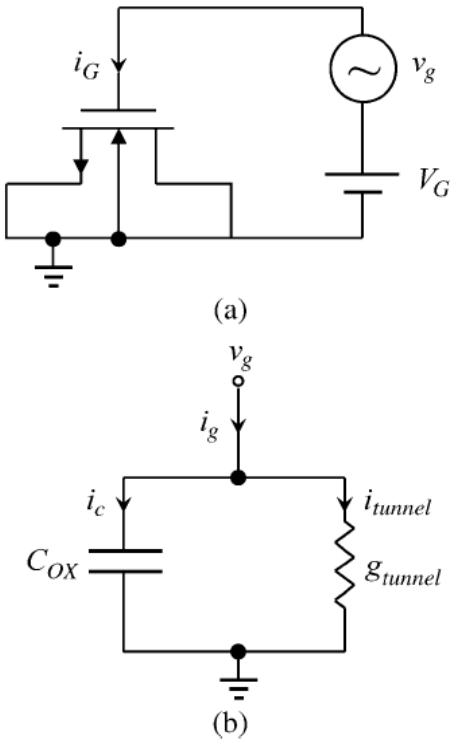

Figure 2.17. (a) Test circuit for gate leakage current (b) its small-signal equivalent

Using the small-signal equivalent model, frequency f_{gate} where the two currents have equal magnitude is determined;

$$f_{\text{gate}}(V_{\text{GS}},V_{\text{DS}}) = \frac{g_{\text{tunnel}}}{2\pi C_{\text{ox}}} \tag{2.16}$$

where g_{tunnel} is called tunnel conductance. For frequencies lower than f_{gate}, the input impedance is resistive; above f_{gate} it is capacitive and the gate behaves as a conventional MOSFET gate. Figure 2.18 represents the behavior of f_{gate} as a function of $V_{GS}-V_T$ for different CMOS technologies with various W/L ratios. Gate leakage current is especially important in low-frequency applications such as PLL loop filters and hold circuits with long time-constants [31]. Because of the resistive behavior for low frequencies, MOS capacitors can not be used in these applications. Input bias currents, gate leakage mismatch and shot noise are the other effects of gate leakage [32].

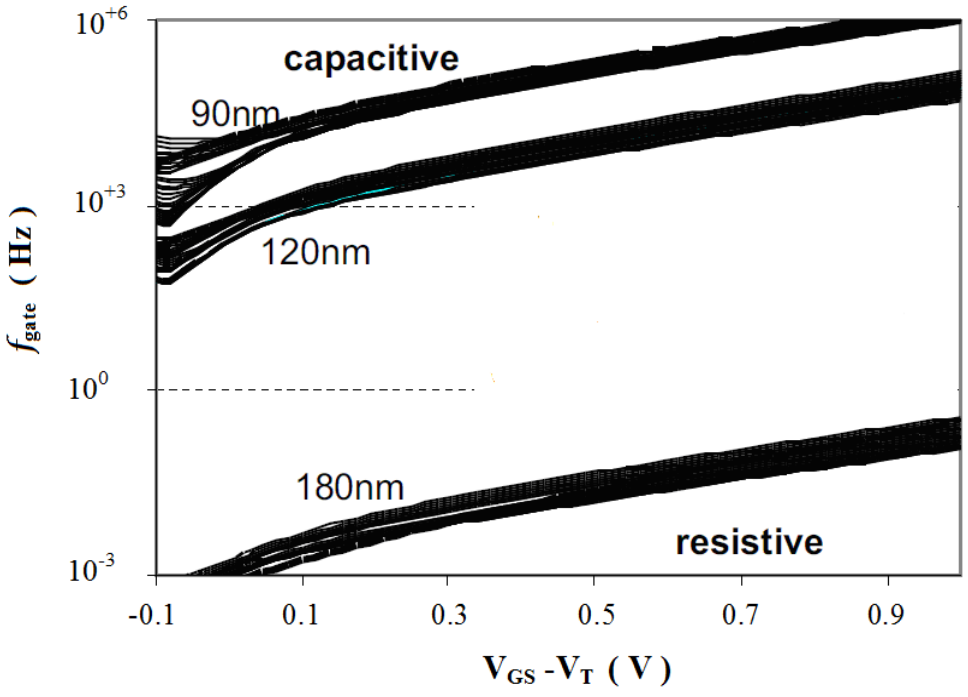

Figure 2.18. f_{gate} versus V_{GS}–V_T for different CMOS technologies

2.3. Design Techniques for Low-Voltage Analog Circuits

So far numerous design techniques for low-voltage analog circuits have been reported in the literature. Most important ones can be enumerated as bulk-driven MOSFETs, self-cascode MOSFETs, floating-gate MOSFETs and current-mode circuits.

2.3.1. Bulk-Driven MOSFETs

Bulk-driven MOS transistor concept was proposed by Guzinski *et al.* in 1987 [33]. Then a software-programmable CMOS telephone circuit was realized by using that concept in 1991 [34]. Blalock *et al.* adopted this technique for low-voltage analog circuits in 1998 [35]. The bulk-driven MOSFET actually is just a standard MOSFET. The difference between the bulk-driven MOSFET and standard MOSFET is the way of using it. Bulk-driven MOSFET technique is based on driving the bulk terminal of the transistors instead of the gate terminal [35]. The cross-sectional view of the NMOS device is shown in Figure 2.19 (a). In this method by applying a sufficient voltage to the gate of the transistor, a channel is formed between the drain and source terminals. Then an input signal is applied to the bulk terminal. The current flowing in the channel is modulated by the reverse bias on the bulk-channel and we obtain a JFET-like transistor given in Figure 2.19 (b).

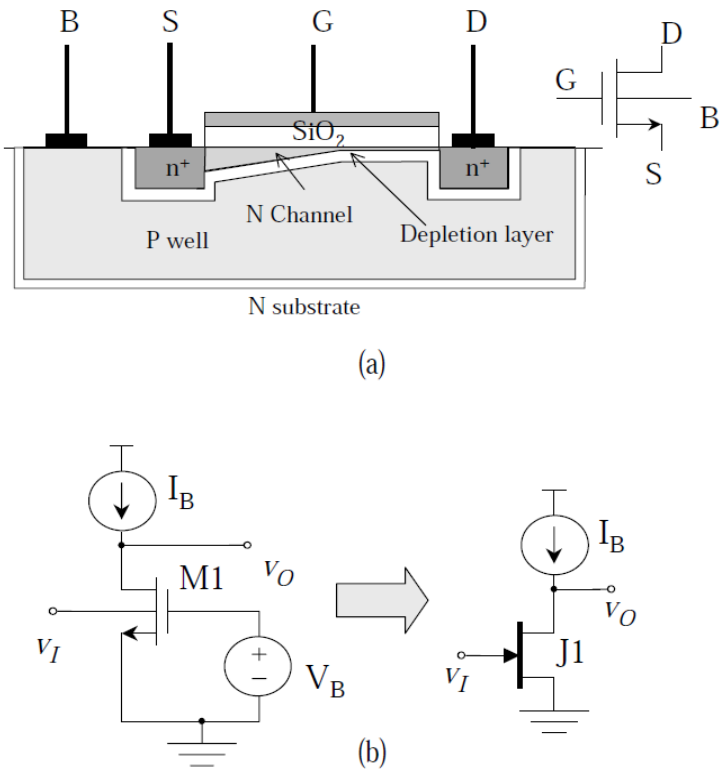

Figure 2.19. (a) Cross-section and symbol of the NMOS (b) equivalent circuit

In typical n-well processes, only PMOS devices can be used for this purpose. The way of using the bulk terminal of NMOS devices is to use modern CMOS processes such

as buried deep n-well process and triple-well process. Cross-sectional views [36] of these devices are given in Figure 2.20.

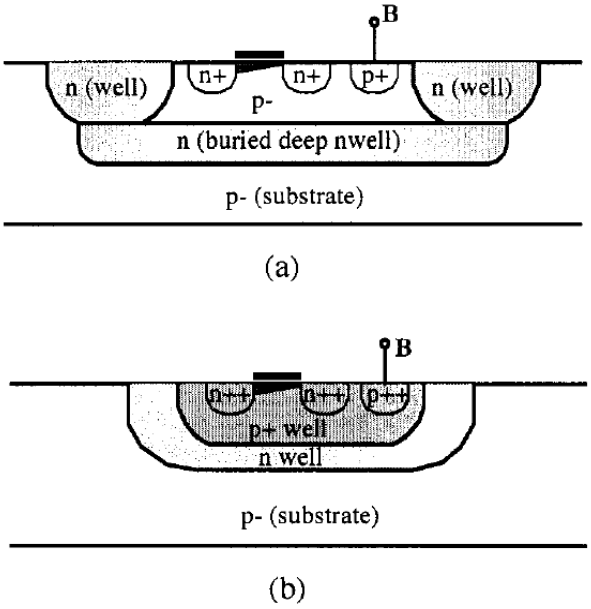

Figure 2.20. NMOS device (a) with buried deep n-well layer (b) in a triple-well

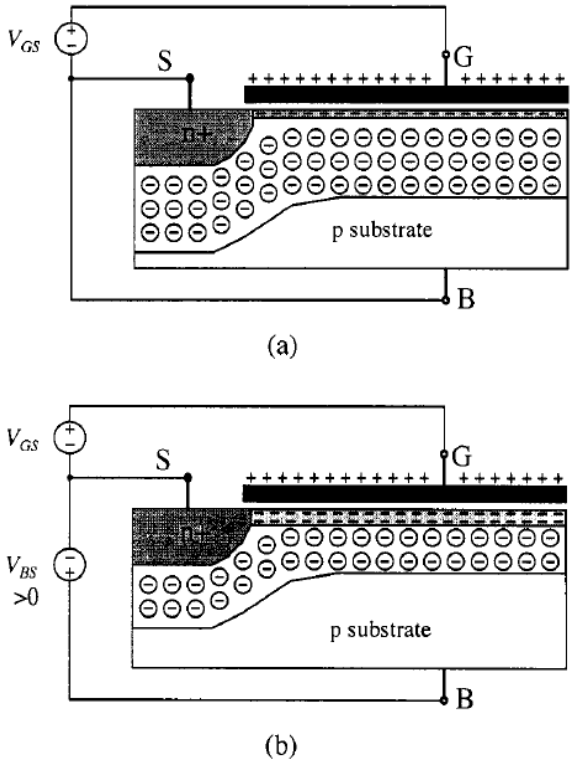

Figure 2.21. Effect of V_{BS} on V_T (a) with V_{BS}=0 (b) with V_{BS}>0

Figure 2.21 explains the effect of bulk terminal on the threshold voltage (V_T). If $V_{GS}>V_T$, a channel is formed under the gate. When bulk and source terminals are tied together, there is a depletion region between source and bulk terminals. As the bulk to source voltage (V_{BS}) increases, the depth of the depletion region decreases, which causes the charge in the depletion region to reduce. As a result, V_T decreases for the same V_{GS}. Variation in V_T as a function of V_{BS} [36] is depicted in Figure 2.22.

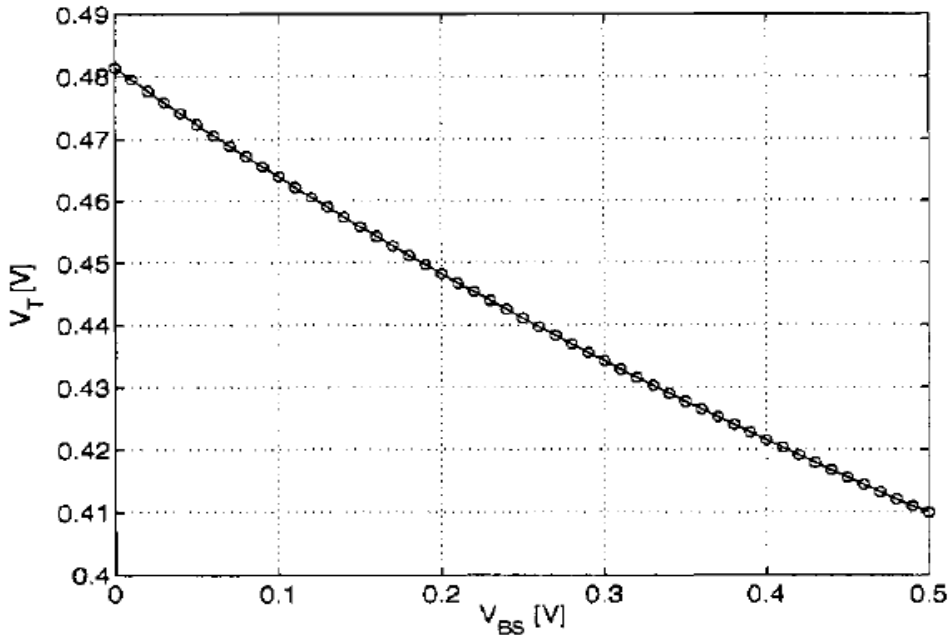

Figure 2.22. V_T versus V_{BS} for 0.18 μm CMOS technology

One of the advantages of the bulk-driven MOSFETs is their large input common-mode range. In addition to that, it removes the threshold voltage requirements and the device can be operated at low supply voltages. Due to depletion characteristics zero, negative and even small positive values of bias voltage can be applied to get the desired DC currents. Moreover, the small-signal transconductance (g_{mb}) can be larger than the MOSFET's transconductance (g_m) if $V_{BS} \geq 0.5$ V. However, there will be appreciable current flowing in the bulk to source junction under these conditions.

Beside lots of advantages, bulk-driven MOSFETs have some drawbacks too. One drawback of the bulk-driven MOSFETs is its input capacitance. The gate-driven MOSFET's frequency response capability is described by its transition frequency (f_T);

$$f_{T_{gate-driven}} \approx \frac{g_m}{(2\pi C_{gs})} \tag{2.17}$$

where C_{gs} is the gate to source capacitance. For the bulk-driven MOSFETs, transition frequency can be expressed as shown in (2.18);

$$f_{T_{bulk-driven}} \approx \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub})} = \frac{\eta g_m}{2\pi(C_{bs} + C_{bsub})} \tag{2.18}$$

where η is the ratio of g_{mb} to g_m and is in the range of 0.2 to 0.4, C_{bs} is the bulk to source capacitance and C_{bsub} is the well to substrate capacitance. The capacitance of (C_{bs} + C_{bsub}) is usually larger than that of the gate-driven.

Another drawback of the bulk-driven MOSFETs is noise. Obviously, the channel noise current is the same as for the gate-driven MOSFETs. However, the bulk (or well) sheet resistance of the bulk-driven MOSFETs can cause additional thermal noise [35] which can be reduced by careful layout. Furthermore, bulk-driven MOSFETs require special CMOS processes such as buried deep n-well process and triple-well process.

Final drawback is the polarity of the bulk-driven MOSFETs which is based on the process. For p-well processes, only n-type bulk-driven MOSFETs are available and for n-well processes, only p-type MOSFETs are available. Therefore, it is impossible to use bulk-driven MOSFETs in CMOS structures where both n-type and p-type MOSFETs are required.

2.3.2. Self-Cascode MOSFETs

Self-cascode is a new technique which is suitable for low-voltage operation. It provides high output impedance with a larger voltage swing than the conventional cascode structures. As a result, it is useful in low-voltage design. As shown in Figure 2.23, a self-cascode MOSFET consists of two transistors which can be treated as a composite single transistor.

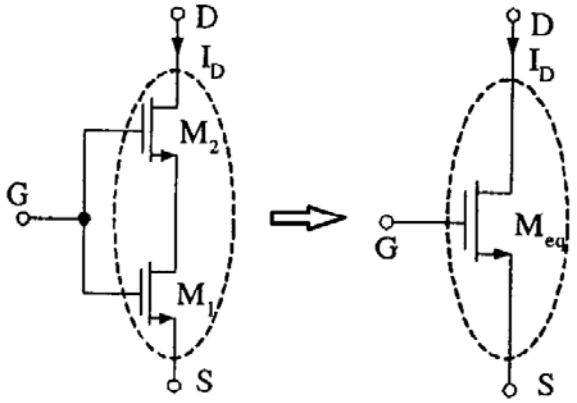

Figure 2.23. Self-cascode NMOS transistor and its equivalent

The lower transistor (M_1) operates in triode region and V_{DS1} is quite small. M_1 is equivalent to a resistor whose value is dependent on the input. Depending on the operation mode of the top transistor (M_2) and assuming that threshold voltages are the same, drain to source current [37] can be expressed by;

$$I_{DS} = \begin{cases} \mu_n C_{ox}\left(\frac{W}{L}\right)_{eq}\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}{V_{DS}}^2\right].....M_2-\text{lin.} \\ \\ \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{eq}(V_{GS}-V_T)^2.....M_2-\text{sat.} \end{cases} \tag{2.19}$$

From (2.19), the equivalent aspect ratio for the composite transistor can be found as;

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{W}{L}\right)_1\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1+\left(\frac{W}{L}\right)_2} \tag{2.20}$$

For optimal operation, the W/L ratio of M_2 is kept larger than that of M_1. In this case $\left(\frac{W}{L}\right)_{eq} \approx \left(\frac{W}{L}\right)_1$. The composite structure has larger effective output impedance which is equal to $g_{m2}r_{ds1}r_{ds2}$.

2.3.3. Floating-Gate MOSFETs (FGMOS)

One of the low-voltage design techniques is the floating-gate MOSFETs (FGMOS). FGMOS is suitable for low-voltage analog applications because of its threshold voltage programmability [38]. Floating-gate devices were first proposed in 1967 [39]. So far they have been used for digital memory applications such as erasable programmable read-only memory (EPROM), electronically erasable programmable read-only memory (EEPROM) [40] and flash memory [41]. However, analog applications of FGMOS such as analog memories [42], trimming circuits [43], multipliers [44], D/A converters [45], filters and amplifiers [46-48] started to appear after the late 1980s.

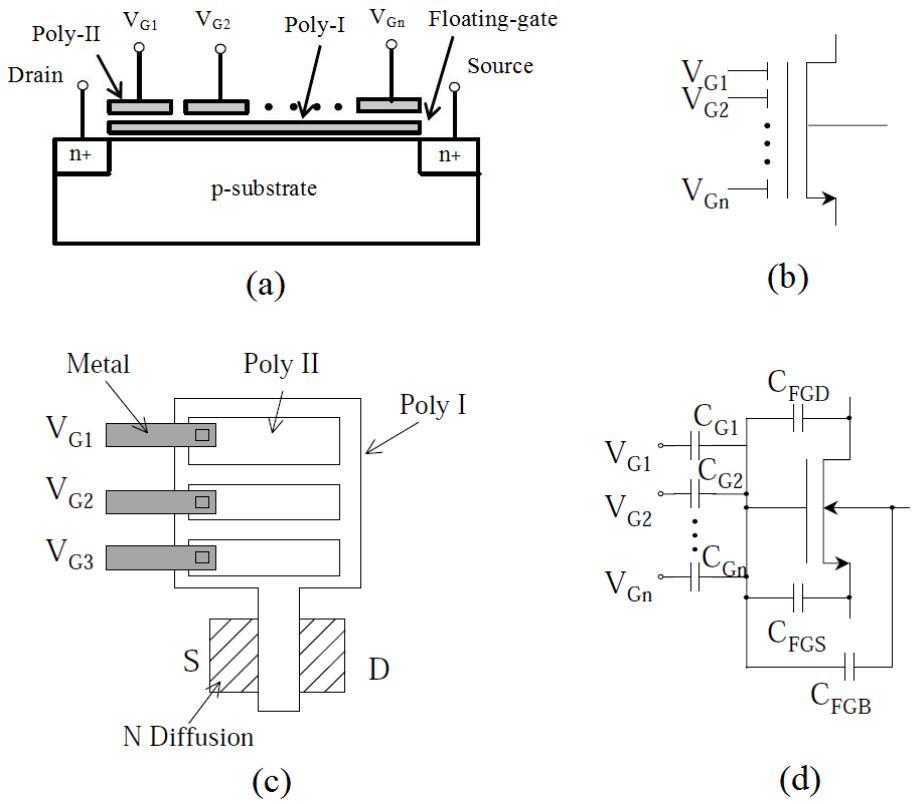

Figure 2.24. Floating-gate MOSFET (a) cross-sectional view (b) symbol (c) layout (d) equivalent circuit

Figure 2.24 depicts cross-sectional view, symbol, layout and equivalent circuit of the floating-gate MOSFETs. This technique requires a standard double poly-silicon CMOS process. The first poly-silicon forms the floating-gate (FG) over the channel, while the

other one forms multiple-input control gates (MIG). The FG is located between MIG and the channel of the transistor.

The major difference between floating-gate MOSFETs and standard MOSFETs is that the floating-gate of a FGMOS is controlled by the coupled signals through capacitors. Using the charge conservation law, the floating-gate voltage can be expressed as;

$$\sum_{i=1}^{n} C_{Gi}(V_{Gi} - V_{FG}) + C_{FG,D}(V_D - V_{FG}) + C_{FG,S}(V_S - V_{FG}) + C_{FG,B}(V_B - V_{FG}) = 0 \qquad (2.21)$$

where C_{Gi} represents the coupling capacitances between the FG and the ith control gate and V_{Gi} represents the gate voltage. $C_{FG,D}$, $C_{FG,S}$ and $C_{FG,B}$ denote the coupling capacitances from FG to the drain, source and bulk, respectively [38]. If we restrict our analysis to a two-input FGMOS, the voltage on floating-gate with $V_S = V_B = 0$ can be expressed as;

$$V_{FG} = \frac{C_{G1}}{C_T} V_{G1} + \frac{C_{G2}}{C_T} V_{G2} + \frac{C_{FG,D}}{C_T} V_D \qquad (2.22)$$

where $C_T = C_{G1} + C_{G2} + C_{FG,D} + C_{FG,S} + C_{FG,B}$ is the total FG capacitance. The drain current of the FGMOS in saturation region (assuming that C_{G1}, $C_{G2} >> C_{FG,D}$, $C_{FG,S}$, $C_{FG,B}$) can be expressed as;

$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(\frac{C_{G1}}{C_T} \right) \left(V_{G1} + \frac{C_{G2}}{C_{G1}} V_{G2} - \frac{C_T}{C_{G1}} V_T \right)^2 \qquad (2.23)$$

From (2.23), the effective threshold voltage ($V_{T,eff}$) is equal to;

$$V_{T,eff} = V_T + \frac{C_{G2}}{C_{G1}} (V_T - V_{G2}) \qquad (2.24)$$

This equation shows that it is possible to make the effective MOSFET threshold voltage very small or even negative. However, floating-gate MOSFETs have some drawbacks such as low gain, low output impedance and degraded frequency response.

2.3.4. Current-Mode Circuits

Current-mode circuits process signals in the form of current. They are suitable for low-voltage operation and therefore, they have been receiving a great deal of interests as an alternative to voltage-mode circuits especially for analog signal processing applications [49]. In addition to low-voltage operation, popularity of current-mode circuits can be attributed to some other features such as larger dynamic range, low power consumption and higher speed. All of them mainly stem from the fact that these circuits have low impedance levels. Furthermore, they do not need high voltage gain [50]. There are a lot of active elements which are able to function in current-mode such as current conveyors, operational transresistance amplifiers (OTRA), current differencing buffered amplifiers (CDBA), current operational amplifiers (COA) and current differencing transconductance amplifiers (CDTA).

3. CURRENT-MODE CIRCUITS FOR LOW-VOLTAGE OPERATION

The threshold voltage is not reduced at the same rate as the power supply drops in standard CMOS technology, which imposes many critical challenges on the design of CMOS current-mode circuits [51]. These challenges are small dynamic range, reduced effective gate to source voltage, poor DC accuracy, increased device mismatches and high sensitivity to biasing conditions. They also severely affect the performance of many existing CMOS current-mode circuits. In order to overcome these difficulties, numerous novel current-mode circuits have emerged so far. An in-depth and comparative study of these circuits is given in this chapter. Some important parameters for low-voltage CMOS current-mode circuits including input and output impedances, bandwidth, noise and dynamic range are also examined in this chapter.

3.1. Characteristics of Current-Mode Circuits

3.1.1. Input Impedance

Low input impedance is essential for current-mode circuits. It reduces the loading effect to the preceding stage and it increases the bandwidth of the front-ends of Gbit/s receivers [52]. The normalized load-induced current error is defined as;

$$\frac{\Delta i_o}{i_o} = \frac{Z_{in}}{Z_{in} + Z_o} \tag{3.1}$$

where $\Delta i_o = i_o - i_{o2}$, Z_o and Z_{in} are the output impedance of the driving stage and the input impedance of the driven stage, respectively. Figure 3.1 depicts the loading effect of current-mode circuits.

Input impedance of a basic current amplifier can be lowered by increasing the biasing current, but this gives rise to an increase in power consumption and a decrease in bandwidth. Another way to obtain lower input impedance is to use current amplifiers with

negative feedback such as active current amplifiers, low-input impedance current amplifiers and current amplifiers with current-current feedback. Additionally, bootstrapped current amplifiers and high-bandwidth current amplifiers can be used to decrease the input impedance.

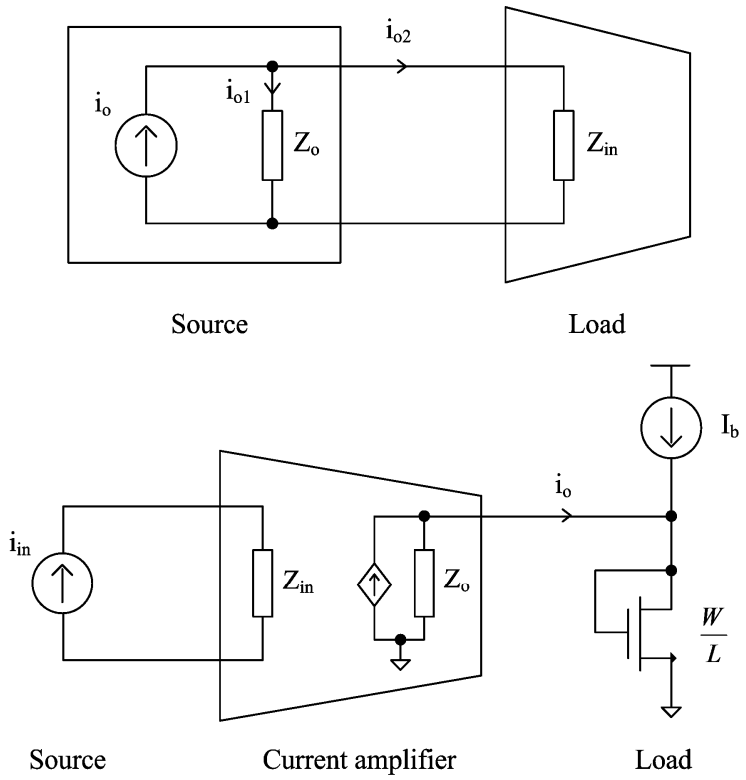

Figure 3.1. Loading effect of current-mode circuits and configuration for frequency response simulation

3.1.2. Output Impedance

In order to minimize the loading effect in current-mode circuits, large output impedance is highly desirable. Due to the strong channel-length modulation effect in deep-submicron CMOS devices, output impedance of current-mode circuits is small [53]. Output impedance can be boosted by increasing the channel length. However, increasing the channel length leads to a decrease in bandwidth. Another way to increase the output impedance is to use the cascode configuration, but it is not attractive for low-voltage design. Bootstrapped current amplifiers can also be used to obtain high output impedance, but they also require bootstrapped biasing circuitry. To boost the output impedance without

using complex bootstrapped configuration, pseudo-cascode current amplifiers can be the other solution.

3.1.3. Bandwidth

Bandwidth is also a key design parameter for current-mode circuits. Bandwidth of the basic current amplifier is given by;

$$\omega_{\mathrm{b,BASIC}} = \frac{g_{\mathrm{m1}}}{C_{\mathrm{gs1}} + C_{\mathrm{gs2}}} \tag{3.2}$$

Bandwidth can be increased either by supplying more biasing current or reducing the width of the transistors. The former causes high power consumption whereas the latter reduces the current gain. Additionally, current-current feedback can be used to increase the bandwidth.

3.1.4. Dynamic Range

Dynamic range is another important design parameter for current-mode circuits. For current amplifiers, the lower bound of the dynamic range is set by the power of the input-referred noise current generators, while the upper bound is determined by the level of the harmonic distortion allowed at the output.

3.1.5. Noise

Thermal and flicker noise are the main noise contributions in MOS transistors. Thermal noise is also called white noise since its spectral density is constant over a given frequency [50]. Spectral density of flicker noise is inversely proportional to frequency and it is dominant at low frequencies, so it is also known as 1/f noise. The intersection between flicker and white noise is called 1/f noise corner. In MOS devices, thermal noise is inversely proportional to its transconductance and flicker noise is inversely proportional to WL product. Therefore, the choice of transistor sizes is significant to lower noise and has to be done according to the working frequency of the circuit [54].

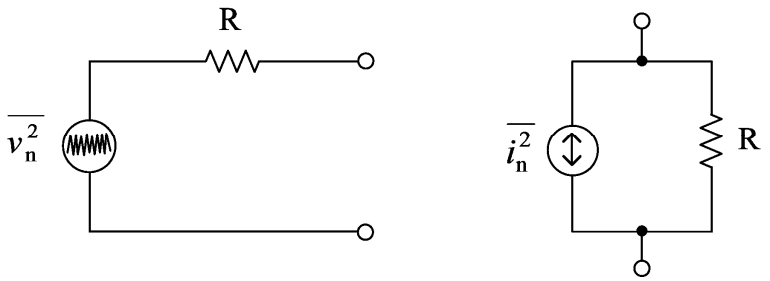

Figure 3.2. Noisy resistance equivalent models

From a classical point of view, a noisy resistor R can be modeled as an ideal (noise-free) resistance and an equivalent noise source as shown in Figure 3.2. The noise expressions are given both in terms of voltage and current spectral densities as follows;

$$\frac{\overline{v_n^2}}{\Delta f} = 4kTR \quad \left(\frac{V^2}{Hz}\right) \tag{3.3}$$

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R} \quad \left(\frac{A^2}{Hz}\right) \tag{3.4}$$

being k the Boltzmann constant (k = 1.38×10^{-23} J/°K) and T the absolute temperature, expressed in Kelvin degrees. A MOS transistor can be regarded as a voltage controlled resistance, so its noisy model could be an ideal MOS having in parallel a current noise source dependent on the channel conductance (g_{DO}).

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_{DO} \quad \left(\frac{A^2}{Hz}\right) \tag{3.5}$$

In (3.5), γ has a value dependent on the operating region of the transistor. Its value is 1 for a transistor in saturation and 2/3 when its drain to source voltage approaches zero. In saturation region, this equation becomes;

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_m \quad \left(\frac{A^2}{Hz}\right) \tag{3.6}$$

The equivalent noise source can be considered at the input terminal. This can be done by dividing it by g_m^2. Thus, the voltage spectral density can be written as;

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{4kT\gamma}{g_m} \quad \left(\frac{V^2}{Hz}\right) \tag{3.7}$$

Shot noise has been observed especially in all those situations where a current is controlled by a voltage, for example, the gate of a MOS transistor. Its formula is;

$$\frac{\overline{i_s^2}}{\Delta f} = 2qI_G \quad \left(\frac{A^2}{Hz}\right) \tag{3.8}$$

where q is the electronic charge of the electron and I_G is the gate current.

In a MOS transistor, 1/f noise can be modeled by a noise current generator, $\overline{i_f^2} = \frac{A_f}{f}$ placed in parallel with the drain to source impedance. Alternatively, it can be modeled by a series voltage generator, connected to the gate terminal, $\overline{v_f^2} = \frac{K_f}{f}$. The values of K_f and A_f depend numerically on the technology;

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{KFI_D}{fC_{ox}L^2} \quad \left(\frac{A^2}{Hz}\right) \tag{3.9}$$

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{KF}{2fC_{ox}WLK'} \quad \left(\frac{V^2}{Hz}\right) \tag{3.10}$$

where KF (different from K_f) and K' are specific constants, C_{ox} is the gate oxide capacitance per unit area, W is the channel width and L is the channel length. Small-signal model for a MOS transistor is shown in Figure 3.3. Noise effects have not been included in this model. This can be done by adding the noise generators as shown in Figure 3.4.

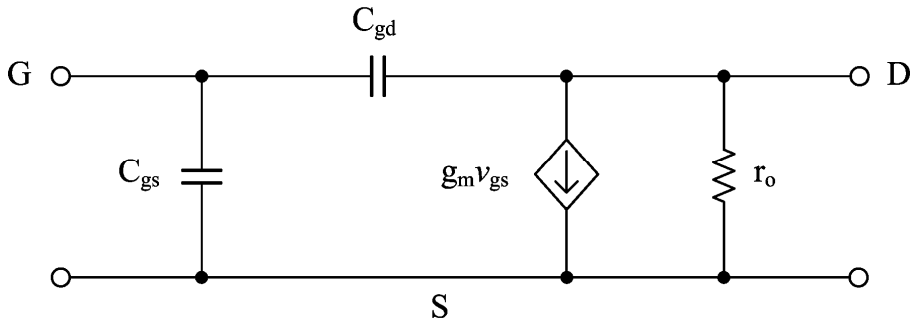

Figure 3.3. Small-signal model of a MOS transistor

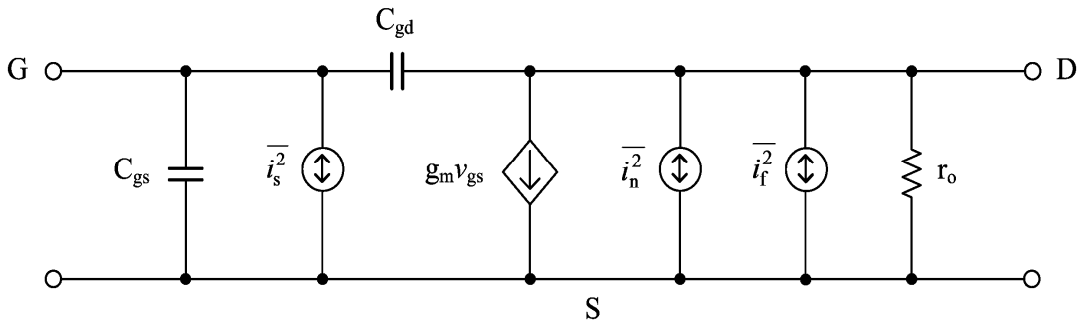

Figure 3.4. Small-signal noisy model of a MOS transistor

It is also possible to obtain an equivalent model of the noisy transistor having all the noise sources at its input as shown in Figure 3.5.

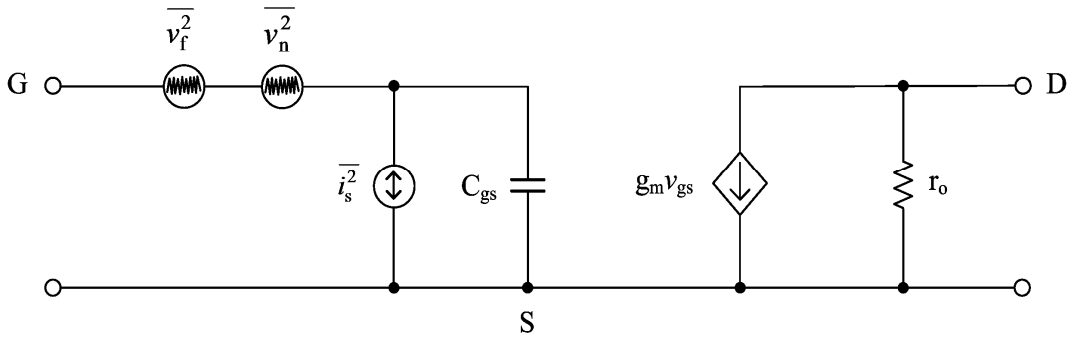

Figure 3.5. Small-signal noisy model of a MOS transistor having all noise sources at input

Figure 3.6 depicts a more simplified model which has only an equivalent input voltage generator ($\overline{v_T^2}$) or an equivalent output current generator ($\overline{i_T^2}$).

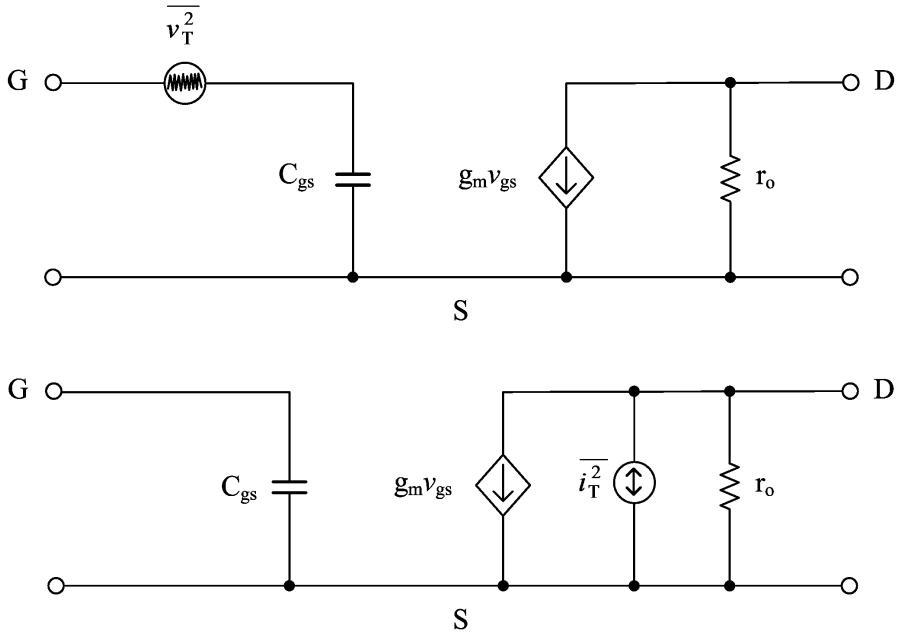

Figure 3.6. Simplified small-signal noisy models of a MOS transistor

3.2. Low-Voltage Current Amplifiers

3.2.1. Basic Current Amplifiers

Schematic of the basic current amplifier is given in Figure 3.7. When only the gate to source capacitance (C_{gs}) is considered, input impedance of the basic current amplifier is given by;

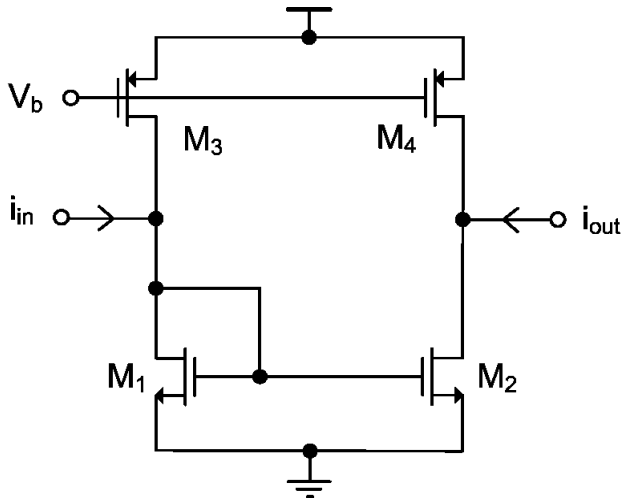

Figure 3.7. Basic current amplifier

$$Z_{\text{in},\text{BASIC}} \approx \frac{1}{g_{\text{m1}}\left(1+\frac{s}{\omega_{\text{b1}}}\right)} \tag{3.11}$$

where g_{m1} is the transconductance of M_1 and $\omega_{\text{b1}} = \frac{g_{\text{m1}}}{\left(C_{\text{gs1}} + C_{\text{gs2}}\right)}$ is the –3dB frequency of the amplifier.

3.2.2. Active Current Amplifiers

The active current amplifier is shown in Figure 3.8. It makes use of a local negative voltage feedback to decrease the input impedance [55-56]. Input impedance of the active current amplifier can be expressed by;

$$Z_{\text{in},\text{ACTIVE}} \approx \frac{1}{Ag_{\text{m1}}\left(1+\frac{s}{\omega_{\text{b2}}}\right)} \tag{3.12}$$

where A is the voltage gain of the auxiliary amplifier, $\omega_{\text{b2}} = A\left(g_{\text{m1}} / C_{\text{in}}\right)$ and C_{in} is the input capacitance of the auxiliary amplifier.

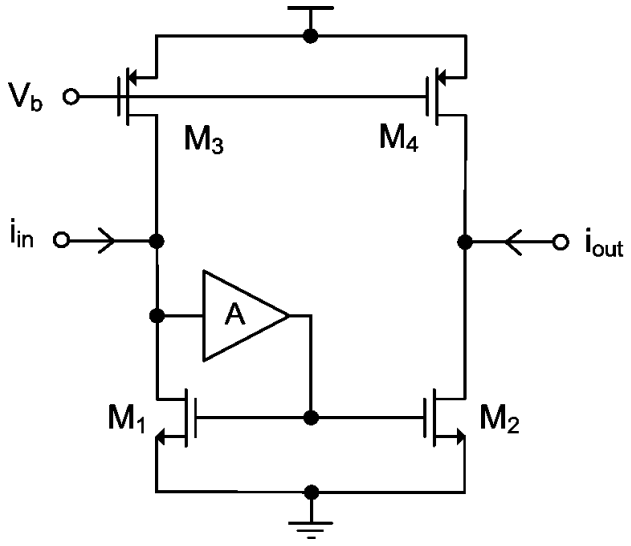

Figure 3.8. Active current amplifier

It is clear in (3.12) that the auxiliary amplifier isolates the input node from the dominant capacitor at the gate of M_1 and M_2. Thus, the dominant capacitor has no effect on the input impedance. The auxiliary amplifier can be realized by using common-gate configurations shown in Figure 3.9 to take the advantage of their immunity from the Miller effect.

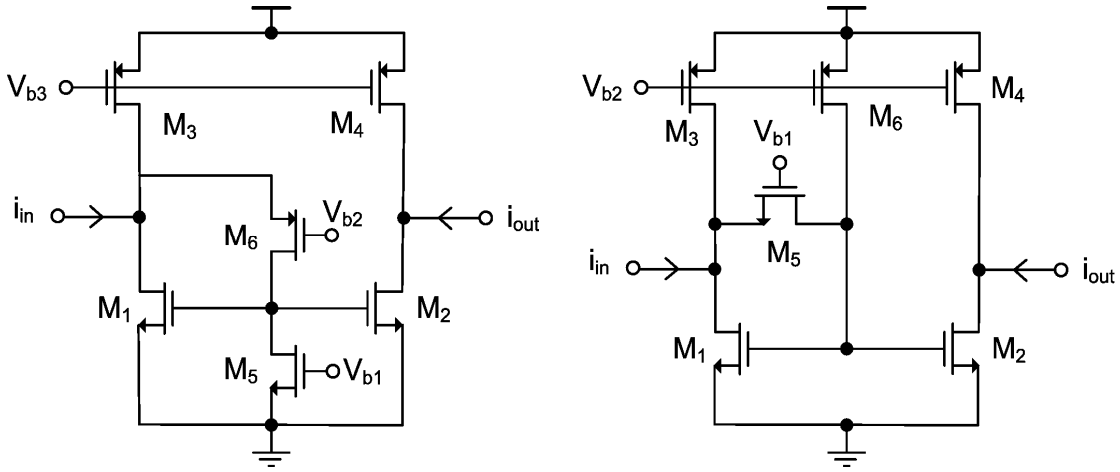

Figure 3.9. Current amplifiers with common-gate active feedback (CGFB)

3.2.3. Bootstrapped Current Amplifiers

Figure 3.10 illustrates bootstrapped current amplifiers reported in [57-59]. They are usually used for V_{DS}-mismatch compensation and output impedance boosting.

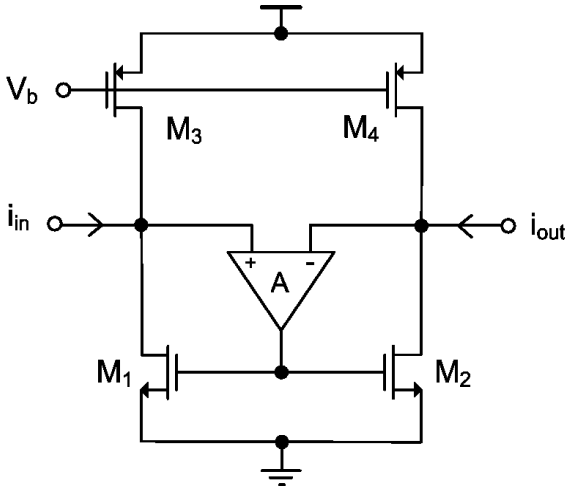

Figure 3.10. Bootstrapped current amplifier

This configuration also offers low input impedance. On the other hand, it has stability problem especially at high frequencies.

3.2.4. High-Bandwidth Current Amplifiers

The high bandwidth current amplifier is shown in Figure 3.11. It utilizes a source follower to suppress the effect of the C_{gs} of M_1 and M_2 on the input impedance [60]. However, it requires a high supply voltage. The minimum supply voltage of the amplifier is given by $V_{DD\,(min)} = 2V_T + V_{DSAT}$ where $V_{TN} = |V_{TP}| = V_T$ is the device threshold voltage and V_{DSAT} is the pinch-off voltage.

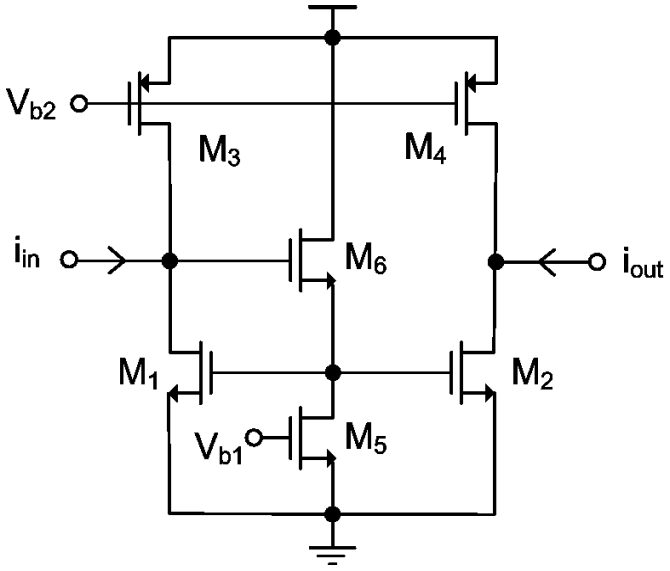

Figure 3.11. High-bandwidth current amplifier

3.2.5. Low Input Impedance Current Amplifiers

Low input impedance current amplifier shown in Figure 3.12 can be used to lower the input impedance. The amplifier reduces the input impedance by means of a local negative voltage feedback. In that case, the input impedance can be expressed by;

$$Z_{\text{in,LOWIMP}} \approx \frac{1}{g_{\text{m1}}\left(g_{\text{m5}} r_{\text{o5}}\right)} \tag{3.13}$$

where g_{m5} is the transconductance of M_5 and r_{o5} is the output resistance of M_5 [61]. Note that this amplifier is useful for low-voltage operation. Minimum supply voltage of this amplifier is $V_{DD\ (min)} = V_T + V_{DSAT}$. A drawback of this amplifier is the reduced input dynamic range.

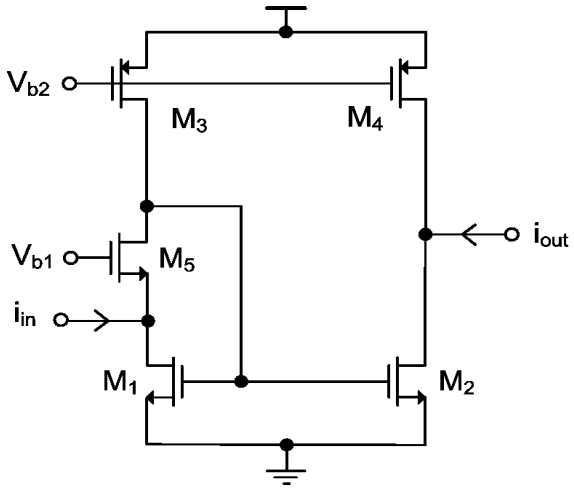

Figure 3.12. Low input impedance current amplifier

3.2.6. Current Amplifiers with Current-Current Feedback

Negative current-current feedback requires a current-sensing element, usually a resistor, in the output loop to sample the output current, resulting in a large DC voltage drop, subsequently a smaller dynamic range [62].

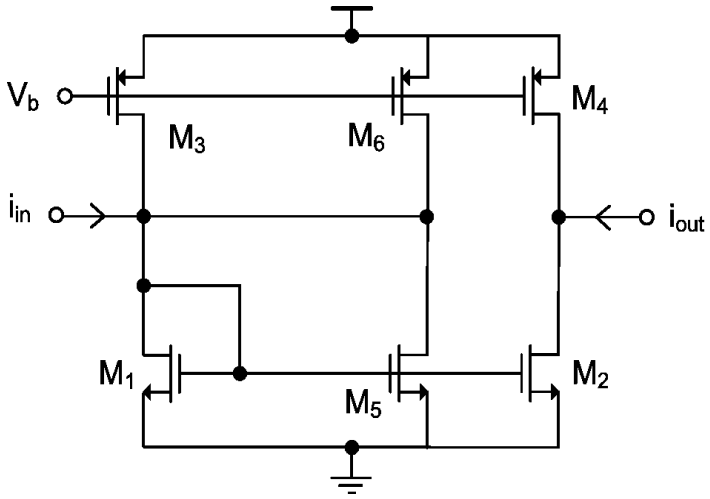

Figure 3.13. Current amplifier with current-current feedback

Figure 3.13 shows the current amplifier with current-current feedback. This topology offers low input impedance which is given by;

$$Z_{\text{in},\text{CCFB}} \approx \frac{1}{g_{\text{m1}}\left(1 + Af\right)} \tag{3.14}$$

where $A = (W/L)_2 / (W/L)_1$ is the forward path gain and $f = (W/L)_f / (W/L)_2$ is the feedback path gain. Another important advantage of this configuration is its low minimum supply voltage given by $V_{DD\,(min)} = V_T + V_{DSAT}$.

3.2.7. Pseudo-Cascode Current Amplifiers

Pseudo-cascode current amplifiers shown in Figure 3.14 are used to avoid using complex bootstrapped configurations. Output impedance of the pseudo-cascode current amplifier at low frequencies is given by;

$$Z_{\text{o,PSEUDO}} \approx r_{\text{o2}}\left(g_{\text{m5}} r_{\text{o5}}\right) \tag{3.15}$$

The pseudo-cascode configuration eliminates the drawback of a bootstrapped current amplifier that the output impedance largely depends on that of the biasing current source. The number of transistors between the power and ground rails of the pseudo-cascode amplifier is only three. Therefore, it is suitable for low-voltage operation. In addition, it offers large bandwidth and low power consumption.

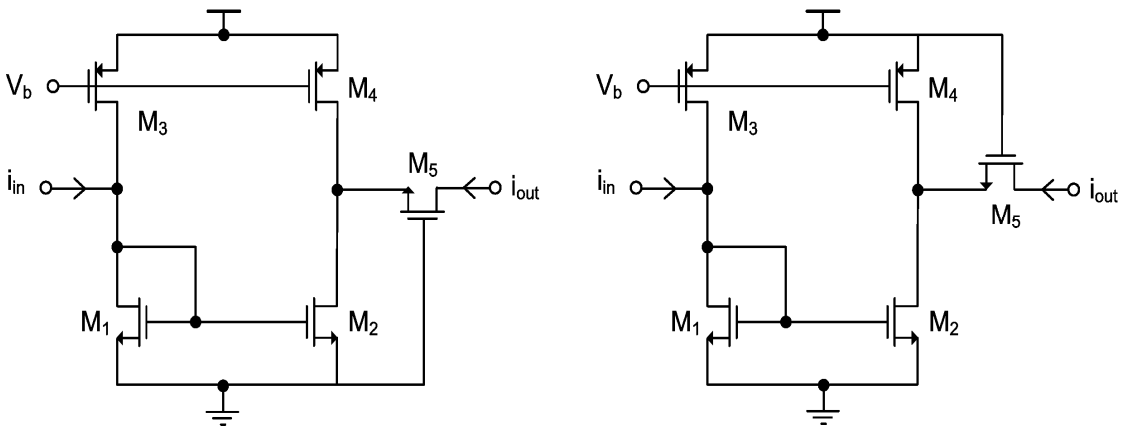

Figure 3.14. Pseudo-cascode current amplifiers

4. DESIGN OF CURRENT-MODE ACTIVE ELEMENTS FOR LOW-VOLTAGE OPERATION

The search for a most versatile and general active element is still going on. Simultaneously, however, new circuit configurations are proposed employing already known elements. The obvious advantage is accumulated knowledge, work and even commercial availability in integrated circuit form. As an active building block, operational amplifier played a predominant role in the last two decades and an enormous number of publications exist in the literature on various circuit examples so that the design engineer can choose the appropriate one. However, opamp-based circuits exhibit several drawbacks in their performance arising from the limited bandwidth and slew-rate of these active elements. Therefore, current-mode approach has been increasingly recognized as a way to overcome the opamp drawbacks and to realize high speed systems.

In the last decade and especially in recent years new current-mode active building blocks like second generation current conveyors (CCII+ and CCII–) [63-67] and current-feedback opamps (CFOA) [68-69] received considerable attention due to their larger dynamic range and wider bandwidth. In addition, different types of active elements like electronically controlled current conveyors (ECCII) [70], differential voltage current conveyors (DVCC) [71], differential difference current conveyors (DDCC) [72], third generation current conveyors (CCIII) [73], four-terminal floating nullors (FTFN) [74] and dual-output operational transconductance amplifiers (DO-OTA) [75] are presented in the literature.

One relatively old active element is the operational transresistance amplifier (OTRA) [76-81], a three port element like the opamp or OTA, but with low input impedance. Although the operational transresistance amplifier is commercially available from several manufacturers under the name of current differencing amplifier or Norton amplifier, it has not gained attention until recently. These commercial realizations do not provide internal ground at the input port and they allow the input current to flow in one direction only. The other active element, current differencing buffered amplifier (CDBA) [82-86], was introduced by Acar and Ozoguz to provide further possibilities in the circuit synthesis.

Recently, a new active element named current differencing transconductance amplifier (CDTA) has been proposed [87] and some applications have also been presented [88-91]. The proposed CDTA element with two current inputs and two current outputs enables an easy implementation of multiple input current integrators. It also exhibits the ability of tuning by the help of transconductance parameter. All these advantages together with the advantages of current-mode operation make the CDTA a promising building block of current-mode filters.

In this chapter, some of the active elements mentioned above are examined, which are namely current differencing buffered amplifier (CDBA), operational transresistance amplifier (OTRA) and current differencing transconductance amplifier (CDTA). After specifications for these active elements are given, low-voltage and low-power versions of them are designed.

4.1. Current Differencing Buffered Amplifier (CDBA)

The current differencing buffered amplifier was initially introduced by Acar and Ozoguz. Block diagram and equivalent circuit of an ideal CDBA are shown in Figure 4.1. A CDBA basically consists of two fundamental building blocks namely the current subtractor and voltage follower.

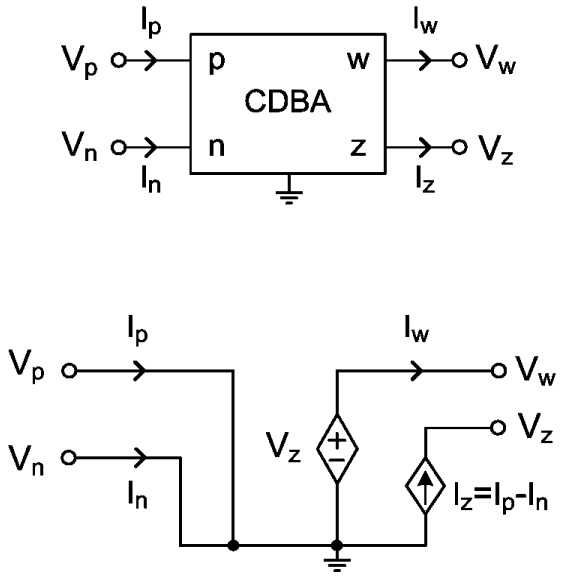

Figure 4.1. Symbol and equivalent circuit of an ideal CDBA

Current and voltage characteristics of an ideal CDBA can be described by the following matrix equation;

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_w \\ I_p \\ I_n \end{bmatrix} \tag{4.1}$$

According to the above matrix equation and equivalent circuit in Figure 4.1, the current through terminal-z is the difference of the currents through terminal-p and terminal-n, hence terminal-z is called current output; terminal-p and terminal-n are non-inverting and inverting input terminals, respectively. Since the voltage at terminal-w follows the voltage at terminal-z, it is called voltage output. Note that input terminals through which I_p and I_n flow are internally grounded. It is clear that terminal-p and terminal-n are current-mode input terminals and they should have ideally zero impedance. Terminal-z is defined as the current output and it has ideally infinite impedance. Since terminal-w is the voltage output, it should have zero impedance. In reality, port relations of a CDBA can be described by the following matrix;

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & \alpha_p & -\alpha_n \\ \beta_v & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_w \\ I_p \\ I_n \end{bmatrix} \tag{4.2}$$

where α_p and α_n are the current transfer ratios and β_v is the voltage transfer ratio. They should equal to unity in ideal case. In practice, they can be expressed as $\alpha_p = 1 - \varepsilon_p$, $\alpha_n = 1 - \varepsilon_n$, $\beta_v = 1 - \varepsilon_v$ with $|\varepsilon_p| \ll 1$, $|\varepsilon_n| \ll 1$ and $|\varepsilon_v| \ll 1$. ε_p and ε_n denote the current-tracking errors and ε_v denotes the voltage-tracking error.

A CDBA can operate in both current-mode and voltage-mode, which provides flexibility. Moreover, it is free from many parasitic capacitances and appropriate for high frequency operation. A CDBA can be designed in different ways. One possible realization is based on the use of the current-feedback operational amplifier (CFOA). There are also

other implementations which are suitable for bipolar technology. Several CMOS implementations of the CDBA have already been reported in the literature [82-86]. Unfortunately, terminal resistances of the CMOS-based CDBAs are quite high, in the order of several hundred ohms. In addition, their voltage and current transfer ratios are much smaller than one. Furthermore, most of the existing CDBAs are operated at high supply voltages and they have high power consumption.

4.1.1. Realization of the CDBA Using AD844

Two AD844 current-feedback opamps from Analog Devices [92] shown in Figure 4.2 are used to simulate the CDBA.

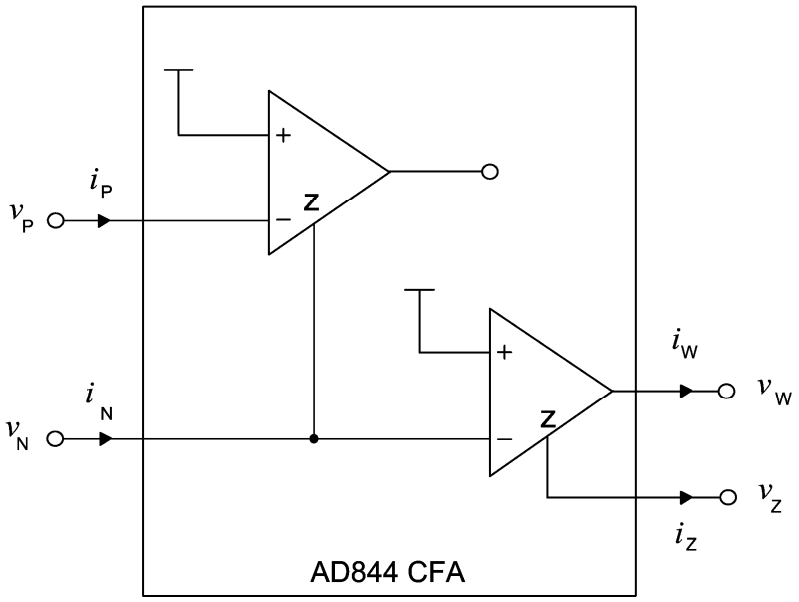

Figure 4.2. CDBA realization using AD844

Terminal-p and terminal-n inputs of the CDBA are unconditionally grounded. The ideal element is therefore very suitable for current-mode circuits if very low input resistances are desired. The implementation in Figure 4.2, however, employs AD844 which presents an equivalent resistance of about 60 Ω at the inverting input terminal. Other implementations of the CDBA may also have some parasitic input resistances which may be denoted as r_p and r_n. Similarly, the output resistance at terminal-z is finite for practical CDBA realizations.

4.1.2. First Proposed Low-Voltage CDBA

Figure 4.3 and Figure 4.4 show the complete schematic and layout of the proposed low-voltage CDBA circuit which is based on the use of the current differencing circuit (M_1-M_8) and voltage buffer (M_9-M_{14}). The proposed circuit is supplied by the voltages of ±0.6 V. For the simulations, UMC 0.18 μm CMOS technology is used. Aspect ratios of the transistors are reported in Table 4.1. Bias currents I_{B1} and I_{B2} are selected as 56 μA and 84 μA, respectively.

Table 4.1. Aspect ratios

Transistor	**W/L [μm/μm]**
M_1, M_2, M_3, M_4	3.6/1.80
M_5, M_6	180/1.80
M_7, M_8	180/1.80
M_9	45/0.36
M_{10}	240/0.36
M_{11}	72/0.36
M_{12}	240/0.36
M_{13}	72/0.36
M_{14}	240/0.36

The current subtractor circuit is based on the flipped voltage follower current sources (FVFCS) which give rise to very low input resistances at input terminals [93]. Schematic of the FVFCS is shown in Figure 4.5. The input resistance of the FVFCS looking at node-X can be expressed by;

$$R_x \cong \frac{\frac{1}{g_{m2}}\left(1+\frac{r_b}{r_{o2}}\right) /\!/\ r_{o1}}{g_{m1}\left(r_b /\!/\ g_{m2} r_{o1} r_{o2}\right)} \tag{4.3}$$

where r_b is the output resistance of the current source, r_o is the output resistance and g_m is the transconductance of the transistors. For a simple current source ($r_b = r_{o2}$), the resistance at node-X in (4.3) is changed to;

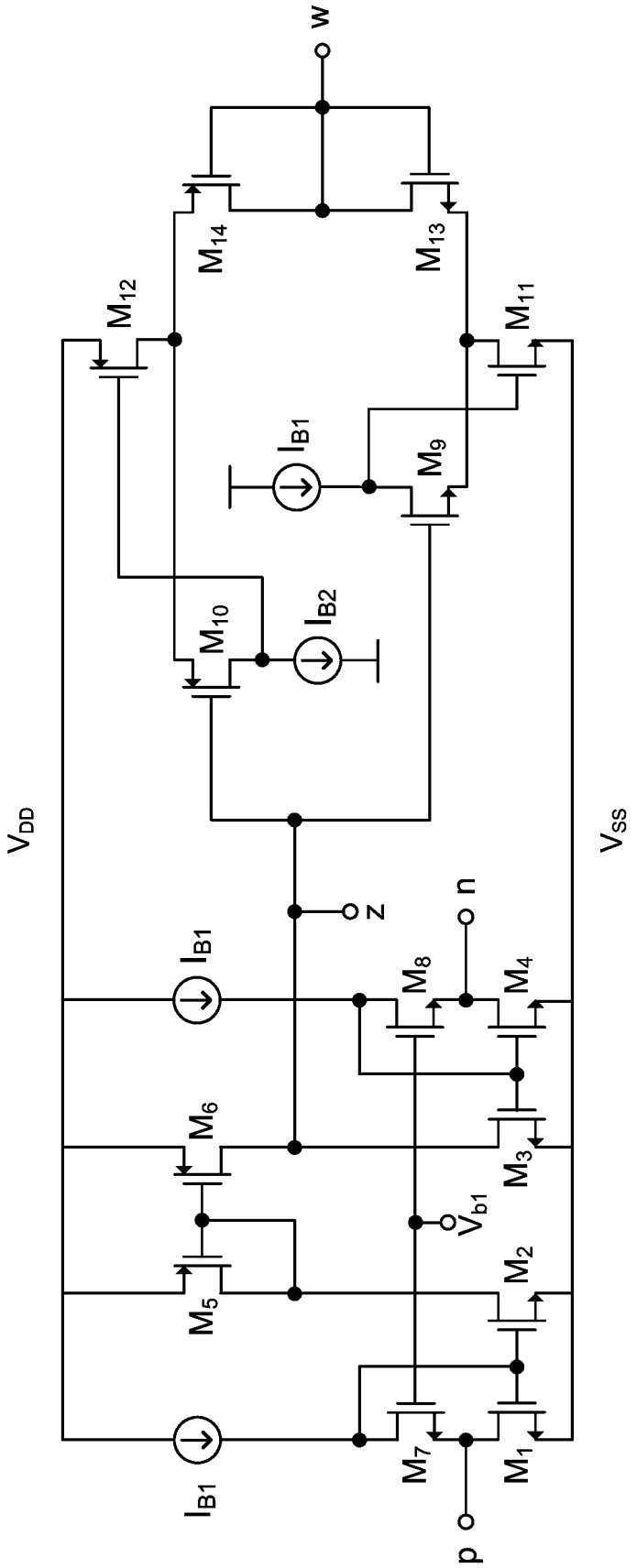

Figure 4.3. First proposed CDBA

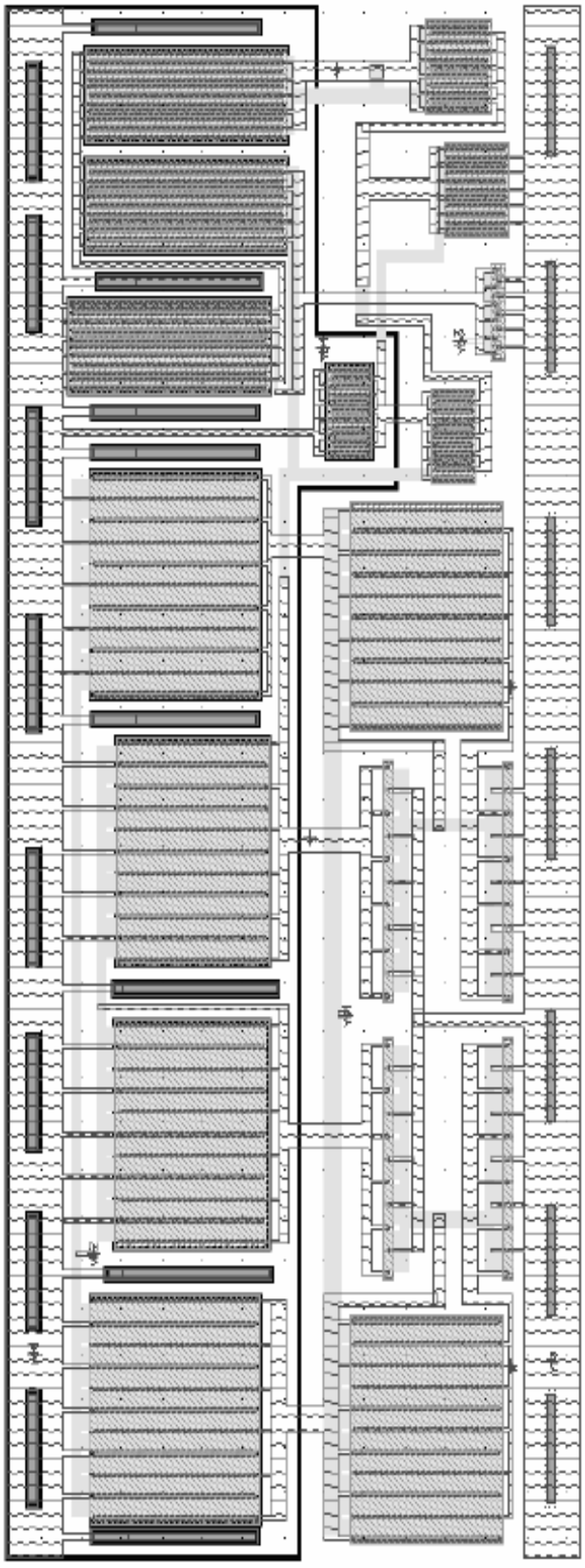

Figure 4.4. Layout of the proposed CDBA

$$R_x \cong \frac{2}{g_{m1} g_{m2} r_{o2}} \tag{4.4}$$

The current subtractor circuit shown in Figure 4.6 consists of the transistors M_1 to M_8. The current at terminal-z follows the difference of the currents at terminal-p and terminal-n. Hence, we name terminal-z as the current output.

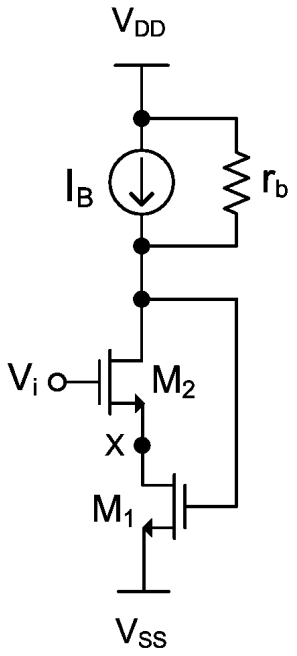

Figure 4.5. Flipped voltage follower current source (FVFCS)

Assuming that each group of transistors (M_1-M_4), (M_5-M_6) and (M_7-M_8) is matched and all transistors operate in saturation region, the circuit operates as follows; the current source I_{B1} forces equal currents of 56 μA in transistors (M_1-M_4). Thus, the gate to source voltages of these transistors will be equal to each other and this equality in the gate to source voltages forces the voltages of the two input terminals to be zero. Figure 4.7 shows that impedances at terminal-p and terminal-n are equal to 56.4 Ω for a wide frequency range. Since terminal-z is defined as the current output, it should ideally have infinite impedance. The resistance looking at terminal-z is equal to;

$$R_z = \frac{r_{o3} r_{o6}}{r_{o3} + r_{o6}} \tag{4.5}$$

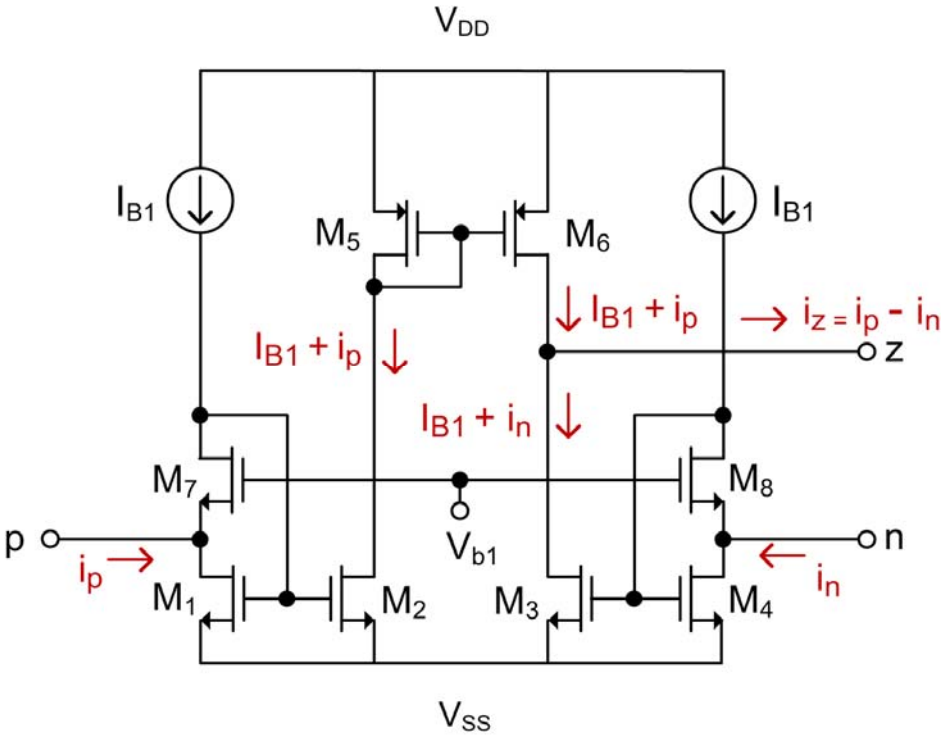

Figure 4.6. Current subtractor circuit

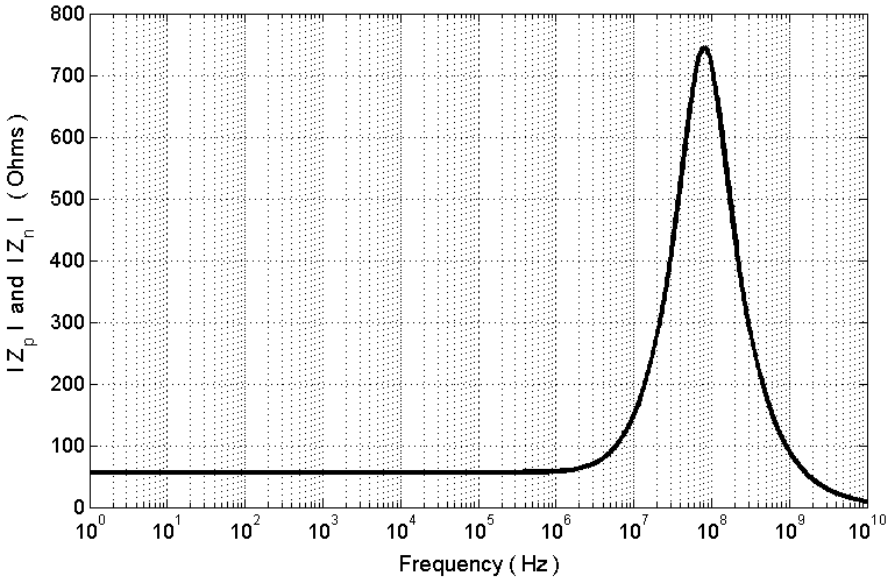

Figure 4.7. Frequency variation of input impedance magnitudes

Figure 4.8 shows the variation of terminal-z impedance magnitude with frequency. The proposed CDBA yields a value of 157 kΩ at frequencies up to 1 MHz. Figure 4.9 displays DC current transfer characteristic of the proposed CDBA. It can be easily seen

that this CDBA has a high linearity over the entire dynamic range (I_{B1}=56 μA). Also, offset current at terminal-z is 0.05 μA.

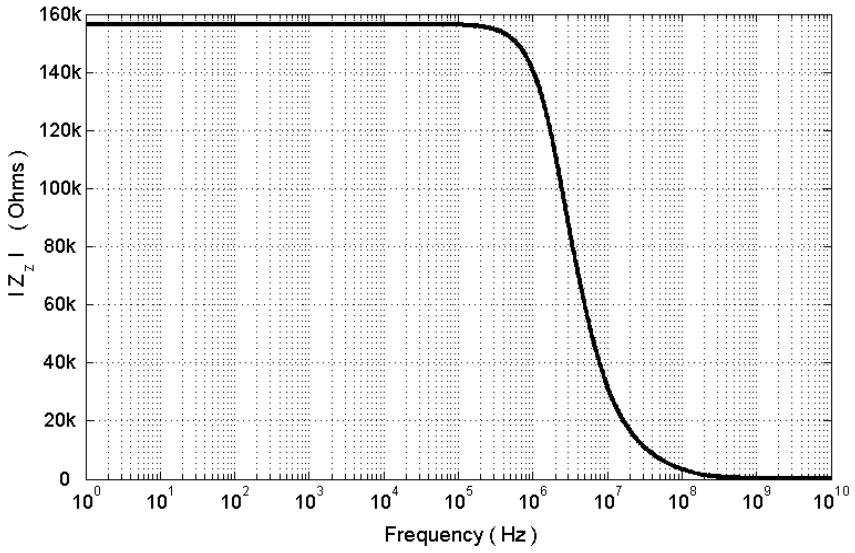

Figure 4.8. Frequency variation of terminal-z impedance magnitude

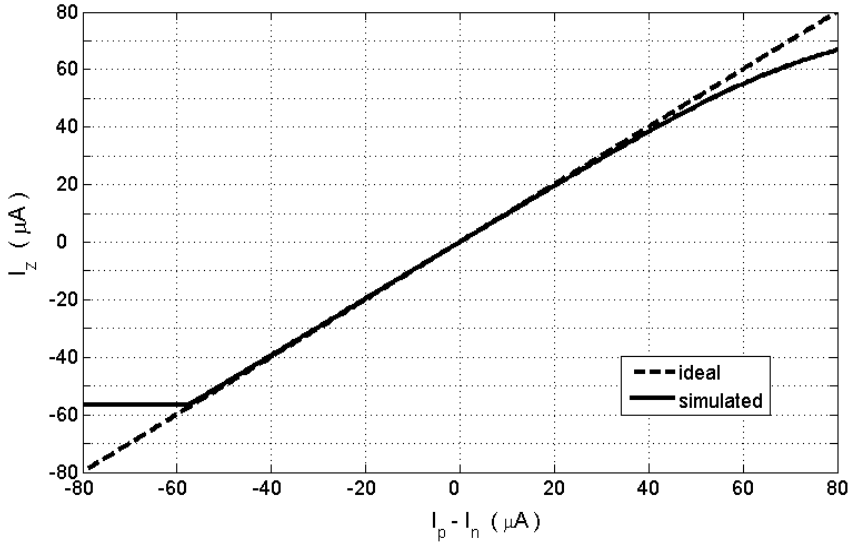

Figure 4.9. DC current transfer characteristic

The output stage of the proposed CDBA is based on the differential flipped voltage follower (DFVF) [94] which is shown in Figure 4.10. The impedance at node-Y is very low and its voltage remains approximately constant for large currents through transistor M_3.

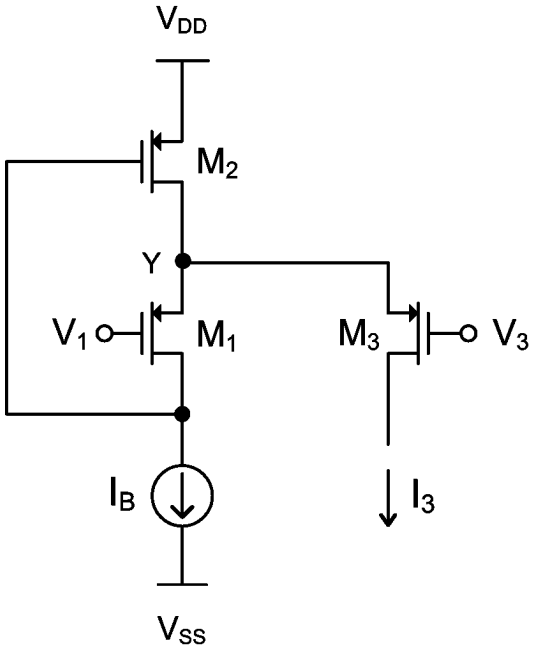

Figure 4.10. Differential flipped voltage follower (DFVF)

If we consider the quiescent conditions when $V_1=V_3$ and assuming the same transistor sizes for M_1 and M_3, the condition of $I_1=I_3=I_B$ is satisfied. A differential voltage of V_1-V_3 generates current variations in M_3 that follow the MOS square law. Another important characteristic of the DFVF is that it can also be operated with a very low supply voltage. The minimum supply voltage is found as $V_{DD\,(min)} = V_{TP} + 2V_{DSAT}$.

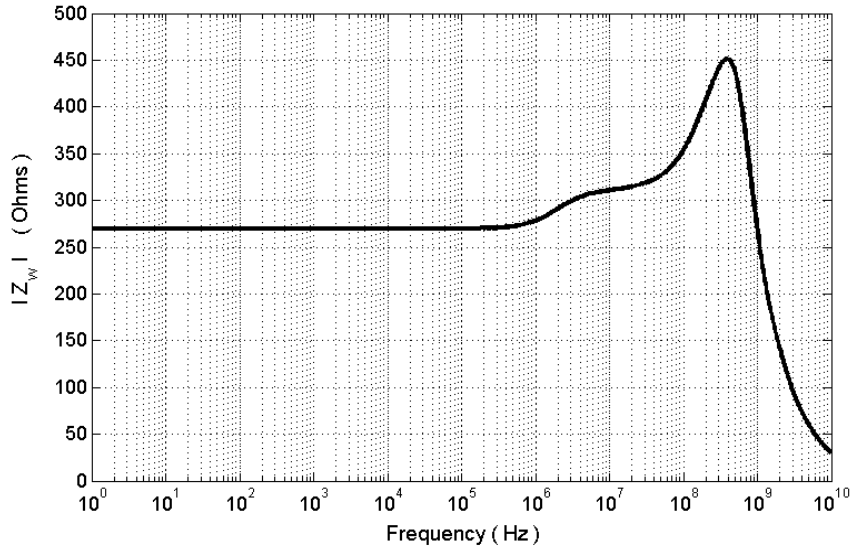

Figure 4.11. Frequency variation of terminal-w impedance magnitude

The complete schematic of the output stage can be seen in Figure 4.3. It offers low output impedance and a moderate output voltage swing. In fact, this circuit is a class-AB voltage buffer which uses two complementary DFVF cells (M_{10}-M_{12}) and (M_9-M_{11}) with current sources I_{B1} and I_{B2}. The frequency characteristic of terminal-w impedance magnitude is shown in Figure 4.11.

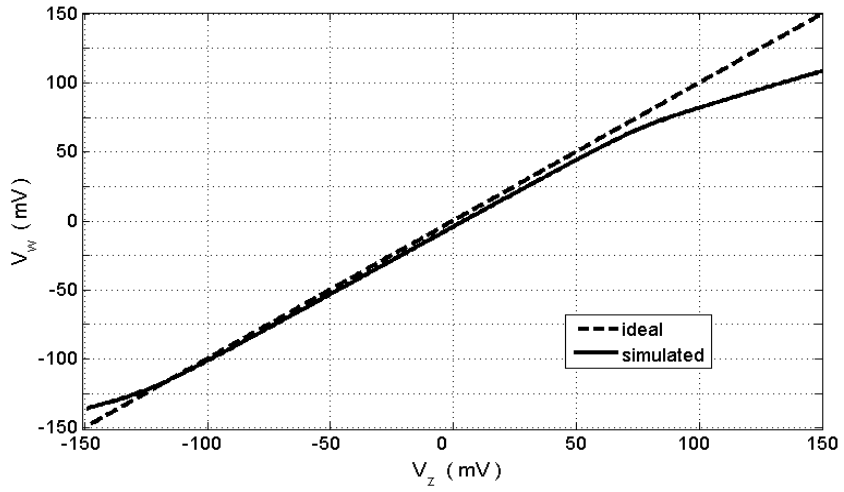

Figure 4.12. DC voltage transfer characteristic

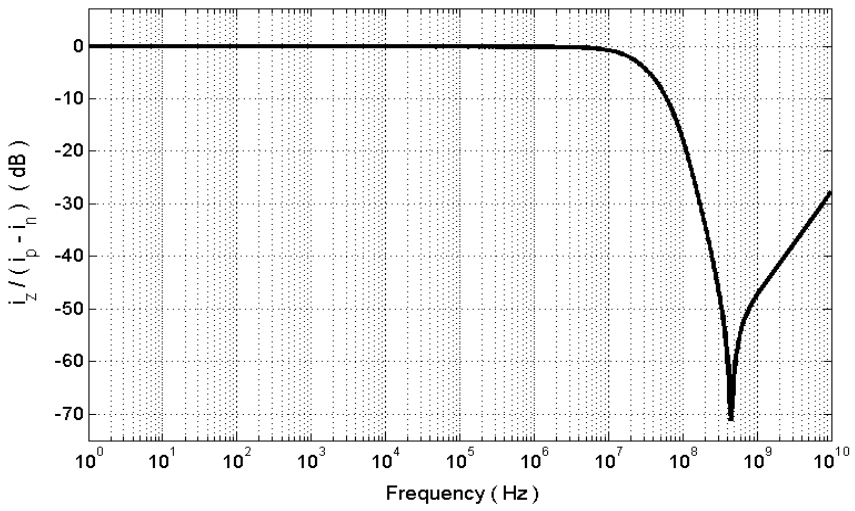

Figure 4.13. Frequency response of the current transfer ratio

DC voltage transfer characteristic of the CDBA is given in Figure 4.12 which shows the output voltage V_w against V_z. From Figure 4.12, it is seen that voltage transfer error tends to increase for V_z values greater than ±100 mV.

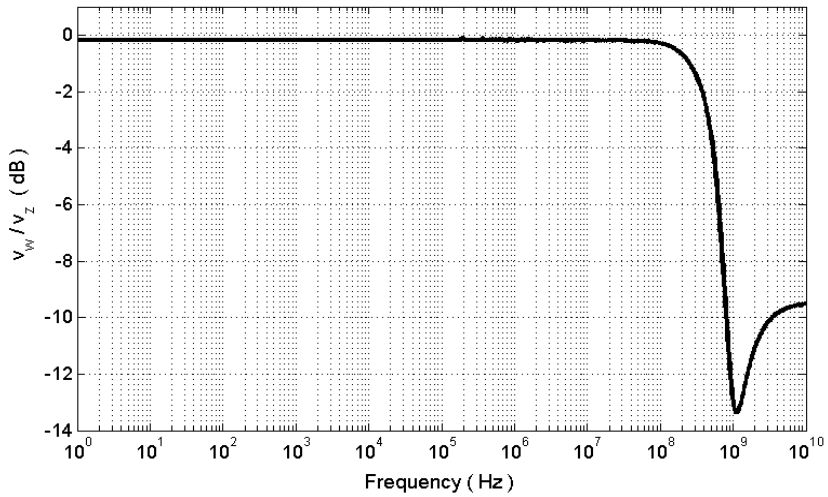

Figure 4.14. Frequency response of the voltage transfer ratio

Figure 4.13 and Figure 4.14 illustrate AC transfer characteristics of the proposed CDBA. Current transfer ratios (α_p, α_n) and the voltage transfer ratio (β_v) are found to be 0.981, 0.981 and 0.978, respectively. It can be observed that the –3dB frequencies of I_z/I_p, I_z/I_n and V_w/V_z are approximately equal to 25 MHz, 25 MHz and 474 MHz, respectively. Schematic and post-layout simulation results are summarized in Table 4.2. To illustrate the effects of parameter variations on the proposed circuit, Monte-Carlo simulations are done. W, L and V_{T0} parameters of each transistor are varied by using values supplied by UMC. Simulation results are given in Figure 4.15 and Figure 4.16. Variations on the current and voltage transfer ratios are 1% and 0.5%, respectively.

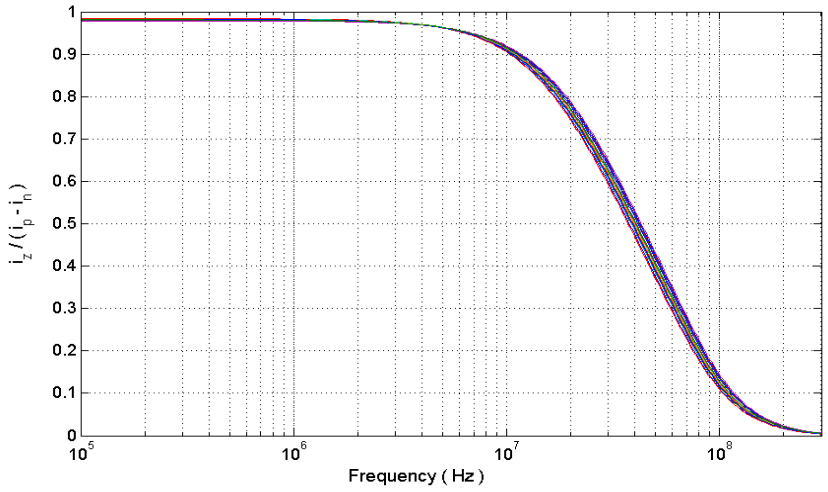

Figure 4.15. Monte-Carlo analysis of the current transfer ratio

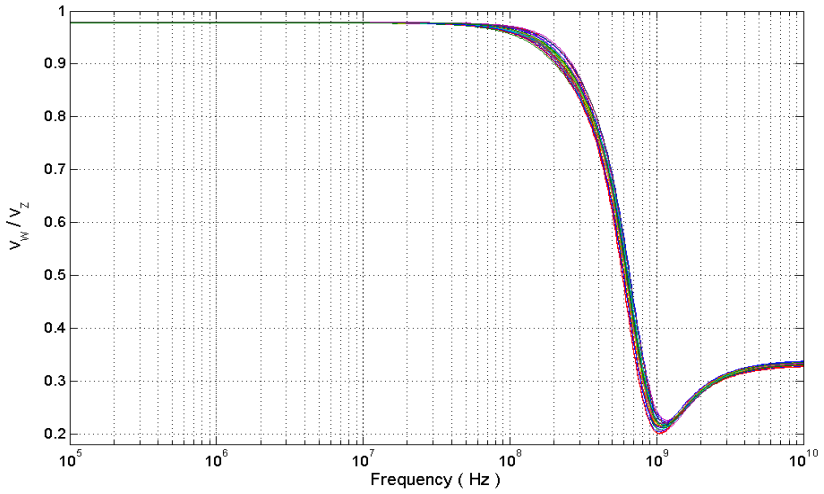

Figure 4.16. Monte-Carlo analysis of the voltage transfer ratio

Table 4.2. Performance of the proposed CDBA

Simulation Results		
Parameter	**Schematic**	**Post-layout**
Power supply	±0.6 V	±0.6 V
Power dissipation	565.25 µW	560 µW
Bias voltage, V_{B1}	0.45 V	0.45 V
Bias current, I_{B1}	56 µA	56 µA
Bias current, I_{B2}	84 µA	84 µA
Current transfer ratio, $\alpha_p = I_z / I_p$	0.981	0.980
Current transfer ratio, $\alpha_n = I_z / I_n$	0.991	0.990
Current transfer BW of α_p	25 MHz	24.6 MHz
Current transfer BW of α_n	74.8 MHz	74 MHz
Voltage transfer ratio, $\beta_v = V_w / V_z$	0.978	0.977
Voltage transfer BW	474 MHz	401 MHz
Terminal-p resistance	56.4 Ω	56.55 Ω
Terminal-n resistance	56.4 Ω	56.55 Ω
Terminal-z resistance	157 kΩ	153 kΩ
Terminal-w resistance	270 Ω	295 Ω
Input current linear range	(−56 µA)-(+56 µA)	(−55 µA)-(+55 µA)
Offset current at terminal-z	0.05 µA	0.08 µA

4.1.2.1. Design Example. To demonstrate the performance of the proposed CDBA, a novel second-order filter configuration shown in Figure 4.17 is proposed. The proposed configuration contains only one active element (CDBA), three resistors and two capacitors.

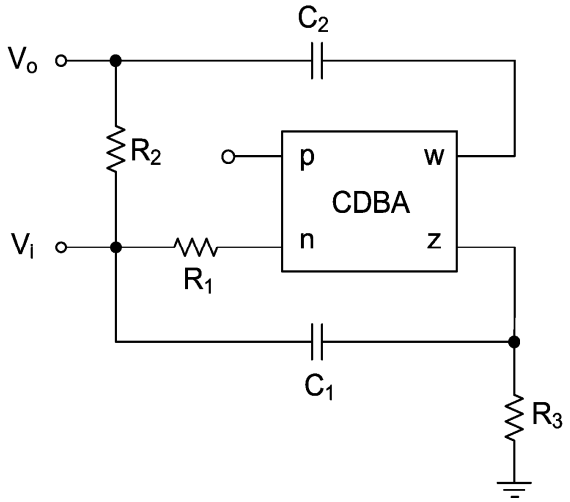

Figure 4.17. Voltage-mode second-order all-pass/notch filter configuration

This configuration can realize all-pass and notch filter responses depending on the matching condition of its passive elements. The general transfer function between V_o and V_i can be written as;

$$\frac{V_o}{V_i} = \frac{s^2 + s\left(\frac{1}{C_2R_2} - \frac{1}{C_1R_1}\right) + \frac{1}{C_1C_2R_2R_3}}{s^2 + s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}} \tag{4.6}$$

If $\frac{1}{C_1R_1} = \frac{2}{C_2R_2} + \frac{1}{C_1R_3}$, a second-order all-pass filter is obtained and the equation in (4.6) is modified to;

$$\frac{V_o}{V_i} = \frac{s^2 - s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}}{s^2 + s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_3}\right) + \frac{1}{C_1C_2R_2R_3}} \tag{4.7}$$

The angular resonant frequency (ω_o) and quality factor (Q) for the filter can be expressed as;

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_2 R_3}} \tag{4.8}$$

$$Q = \frac{\sqrt{C_1 C_2 R_2 R_3}}{C_1 R_3 + C_2 R_2} \tag{4.9}$$

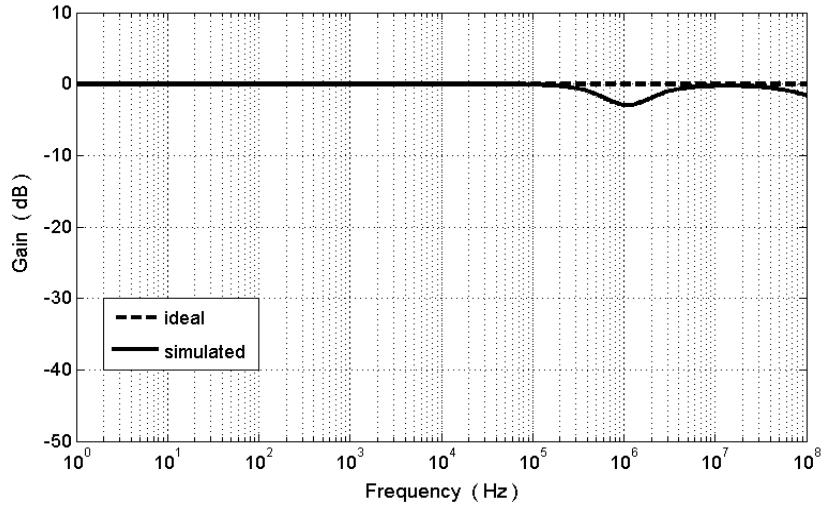

Figure 4.18. Gain response of the proposed all-pass filter

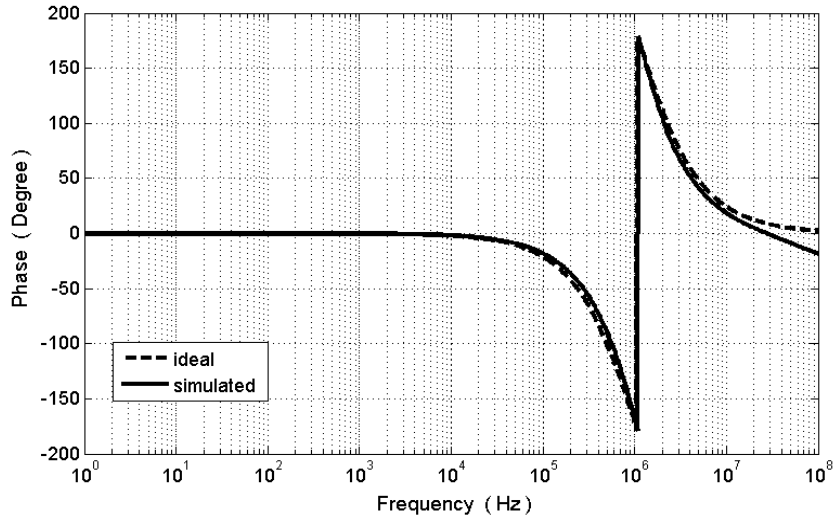

Figure 4.19. Phase response of the proposed all-pass filter

To verify the theoretical analysis, this filter is simulated by using UMC 0.18 μm CMOS process parameters. Figure 4.18 and Figure 4.19 show both ideal and simulated gain and phase responses of the all-pass filter. By taking the matching condition into consideration, external component values are chosen as R_1=2 kΩ, R_2=6 kΩ, R_3=6 kΩ, C_1=25 pF and C_2=25 pF. Then the center frequency of the circuit is found as f_c=1.08 MHz which is in close agreement with the theoretical one.

If we satisfy the matching condition of $C_1R_1 = C_2R_2$ in (4.6), a second-order notch filter is obtained and transfer function of the notch filter can be written as;

$$\frac{V_o}{V_i} = \frac{s^2 + \dfrac{1}{C_1C_2R_2R_3}}{s^2 + s\left(\dfrac{1}{C_2R_2} + \dfrac{1}{C_1R_3}\right) + \dfrac{1}{C_1C_2R_2R_3}} \tag{4.10}$$

It can be observed from (4.11) that the proposed filter is suitable for low Q applications. Sensitivity analysis of the proposed filter with respect to passive elements yields;

$$S_{R_2}^{Q} = \frac{1}{2}\frac{C_1R_3 - C_2R_2}{C_1R_3 + C_2R_2}$$

$$S_{R_3}^{Q} = -\frac{1}{2}\frac{C_1R_3 - C_2R_2}{C_1R_3 + C_2R_2}$$

$$S_{C_1}^{Q} = -\frac{1}{2}\frac{C_1R_3 - C_2R_2}{C_1R_3 + C_2R_2}$$

$$S_{C_2}^{Q} = \frac{1}{2}\frac{C_1R_3 - C_2R_2}{C_1R_3 + C_2R_2}$$

$$S_{R_2}^{\omega_o} = S_{R_3}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2} \tag{4.11}$$

The gain and phase responses of the notch filter for the ideal and simulated cases are illustrated in Figure 4.20 and Figure 4.21. If the component values are chosen as R_1=10 kΩ, R_2=10 kΩ, R_3=2 kΩ, C_1=20 pF and C_2=20 pF, then the center frequency of the circuit is found as f_c=1.8 MHz.

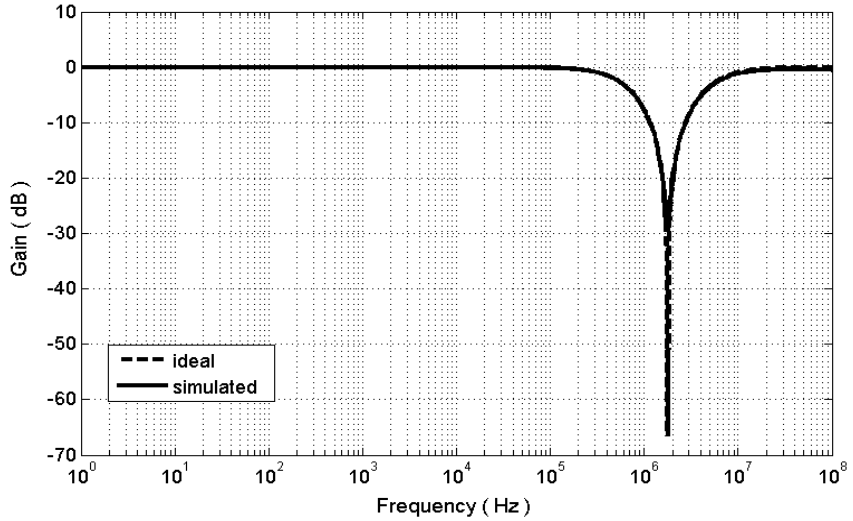

Figure 4.20. Gain response of the proposed notch filter

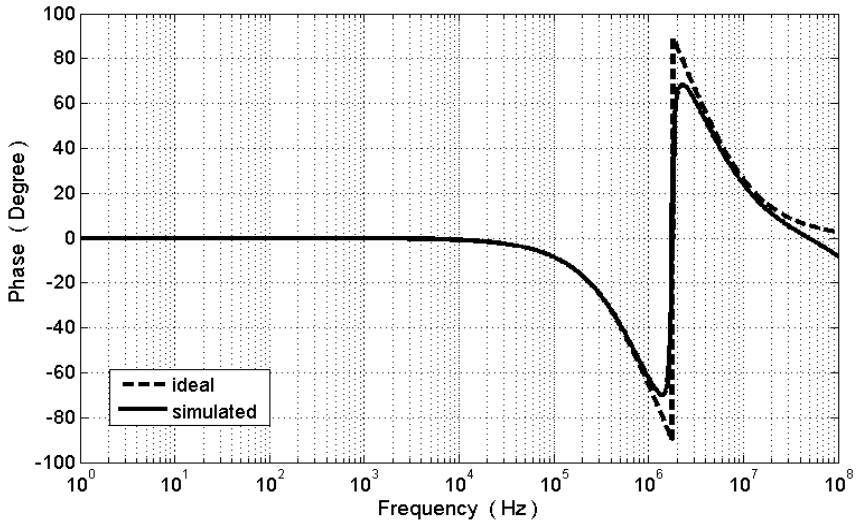

Figure 4.21. Phase response of the proposed notch filter

Finally, total harmonic distortion (THD) of the proposed notch filter is simulated by applying 1 MHz sinusoidal input signal with various amplitudes to the input of the filter. According to Figure 4.22, THD is less than 6% over the input range of ±0.5 V.

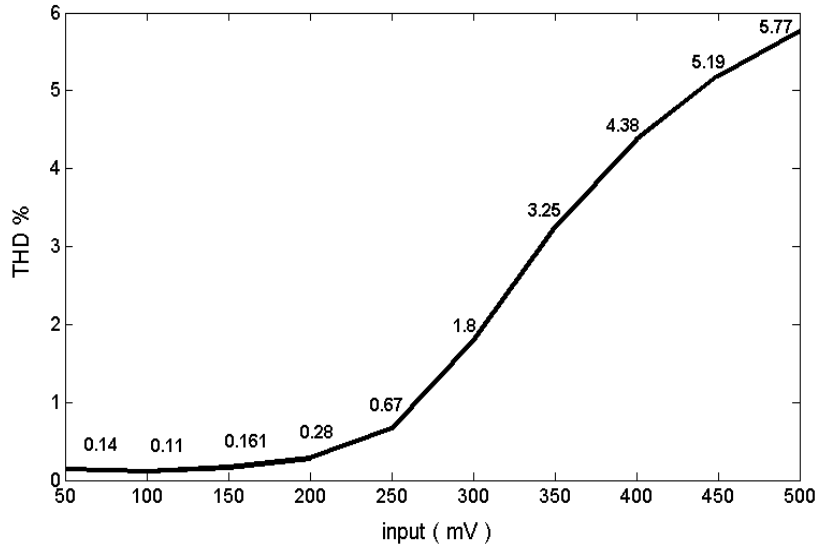

Figure 4.22. Output harmonic distortion versus input voltage of 1 MHz

4.1.3. Second Proposed Low-Voltage CDBA

A low-voltage, high-swing CMOS current differencing buffered amplifier (CDBA) is proposed. The proposed circuit operates with the power supplies of ±0.6 V and consumes low-power. For the simulations, 0.18 μm CMOS technology provided by UMC is used. Aspect ratios of the transistors used are shown in Table 4.3.

Table 4.3. Aspect ratios

Transistor	**W/L [μm/μm]**
M_1, M_2, M_3, M_4	2.7/0.90
M_5, M_6	99/1.80
M_7, M_8	63/0.90
M_9, M_{10}	63/0.90
M_{11}, M_{12}	4.5/0.36
M_{13}	36/0.90
M_{14}	52/0.90
M_{15}, M_{16}	18/0.36
M_{17}, M_{18}	4.5/0.36
M_{19}	180/0.90
M_{20}	180/0.36

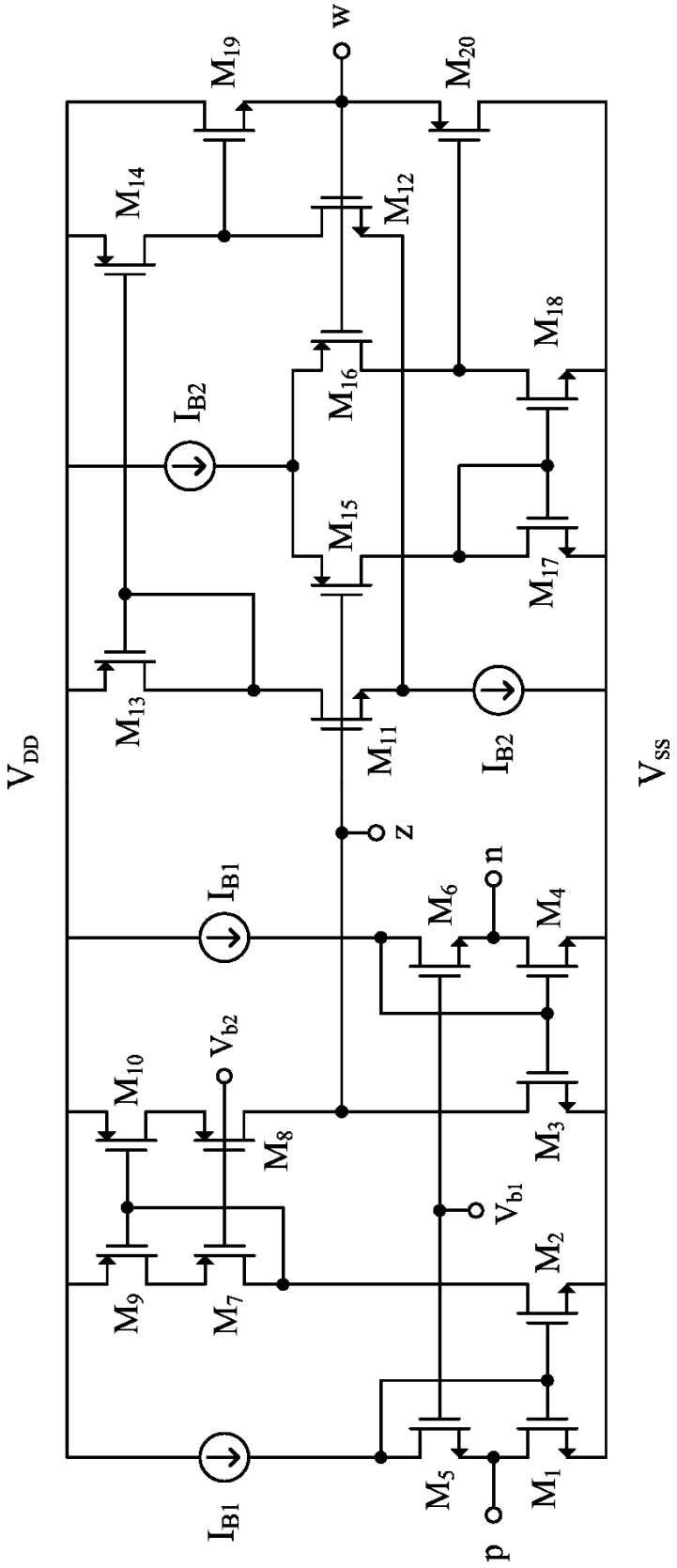

Figure 4.23. Second proposed CDBA

Schematic of the proposed low-voltage CDBA circuit is given in Figure 4.23. It mainly consists of two fundamental building blocks namely the current subtractor and voltage follower. The current subtractor circuit is formed by the transistors M_1 to M_{10}. This circuit exploits flipped voltage follower current sources (FVFCS). A FVFCS is characterized by very low supply requirements and low impedance (tens of ohms) at input terminals. Input resistances of the circuit can be expressed as;

$$R_{\mathrm{p}} \cong \frac{2}{g_{\mathrm{m1}} g_{\mathrm{m5}} r_{\mathrm{o5}}} \tag{4.12}$$

$$R_{\mathrm{n}} \cong \frac{2}{g_{\mathrm{m4}} g_{\mathrm{m6}} r_{\mathrm{o6}}} \tag{4.13}$$

Frequency characteristics of the input terminal impedances of the proposed CDBA are given in Figure 4.24. It turns out that impedances at terminal-p and terminal-n are the same and equal to 63.5 Ω for a wide frequency range.

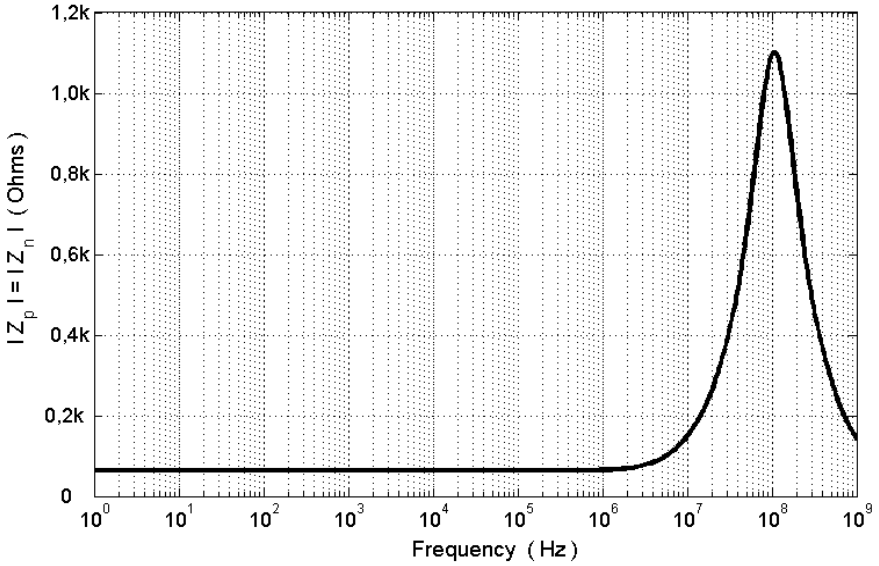

Figure 4.24. Frequency variation of terminal-p and terminal-n impedance magnitudes

Figure 4.25 shows the impedance at terminal-z which is equal to 218 kΩ at frequencies up to 1 MHz.

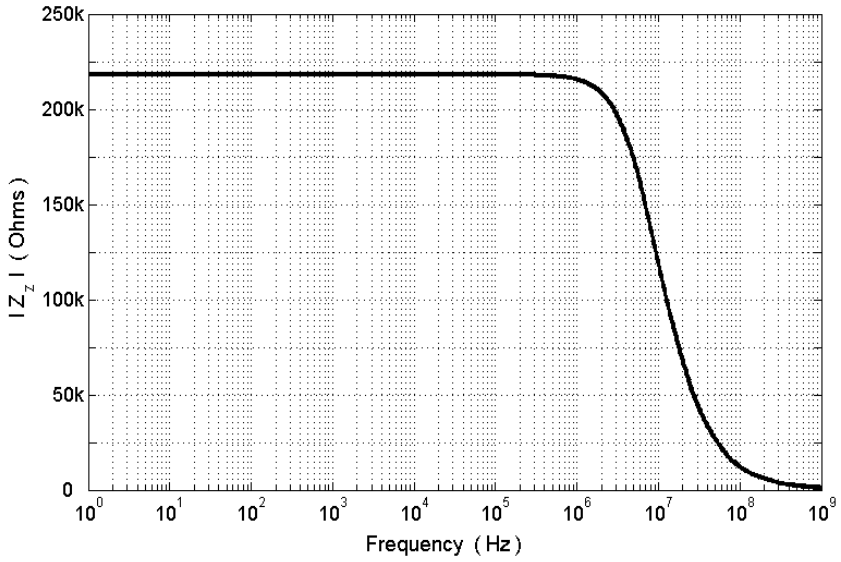

Figure 4.25. Frequency variation of terminal-z impedance magnitude

This circuit also offers a very low output impedance value. Output resistance of the proposed CDBA can be formulated as;

$$R_{\mathrm{w}} = \frac{1}{g_{\mathrm{m19}}(1+g_{\mathrm{m12}}\frac{r_{\mathrm{o}}}{2})} // \frac{1}{g_{\mathrm{m20}}(1+g_{\mathrm{m16}}\frac{r_{\mathrm{o}}}{2})} \tag{4.14}$$

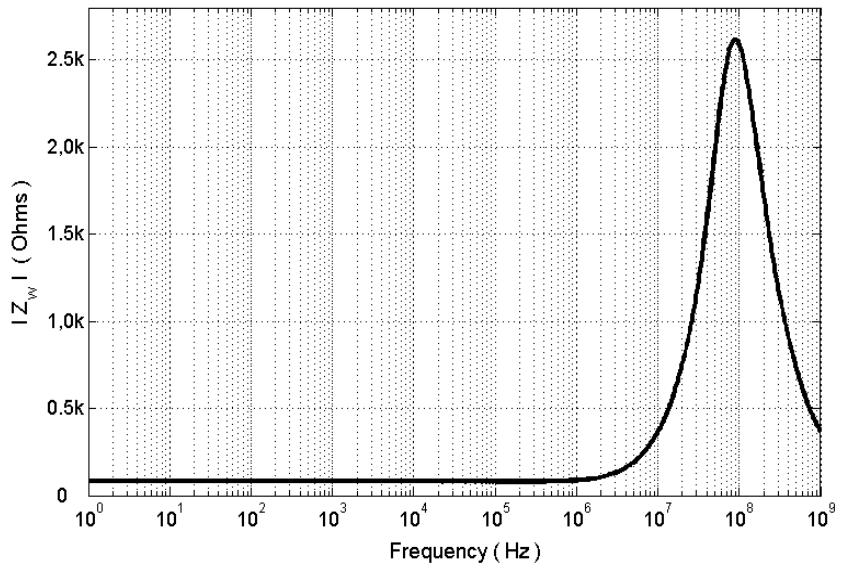

Figure 4.26. Frequency variation of terminal-w impedance magnitude

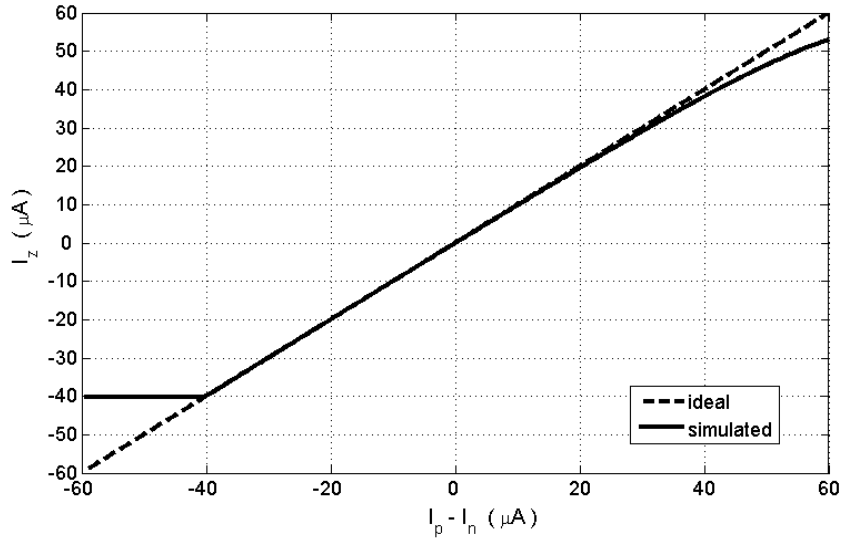

Figure 4.27. DC current transfer characteristic

Figure 4.26 depicts the frequency response of the output impedance. Figure 4.27 displays DC current transfer characteristic of the proposed CDBA. It is obvious that this CDBA has a high linearity over the entire dynamic range (I_{B1}=40 μA) and its offset current at terminal-z is 0.1 μA.

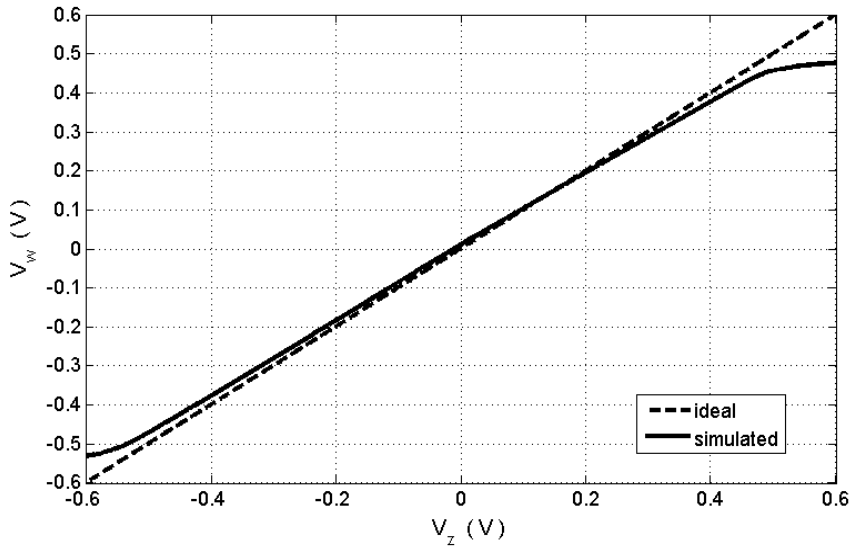

Figure 4.28. DC voltage transfer characteristic

In order to have a common-mode signal range which extends from rail to rail, an n-channel and a p-channel differential pairs are connected in parallel as shown in Figure

4.23. This circuit provides an excellent output voltage swing capability. The n-channel differential pair (M_{11}-M_{12}) is able to reach the positive supply rail, while the p-channel one (M_{15}-M_{16}) can sense common-mode voltages around the negative supply rail. DC voltage transfer characteristic of the circuit is shown in Figure 4.28.

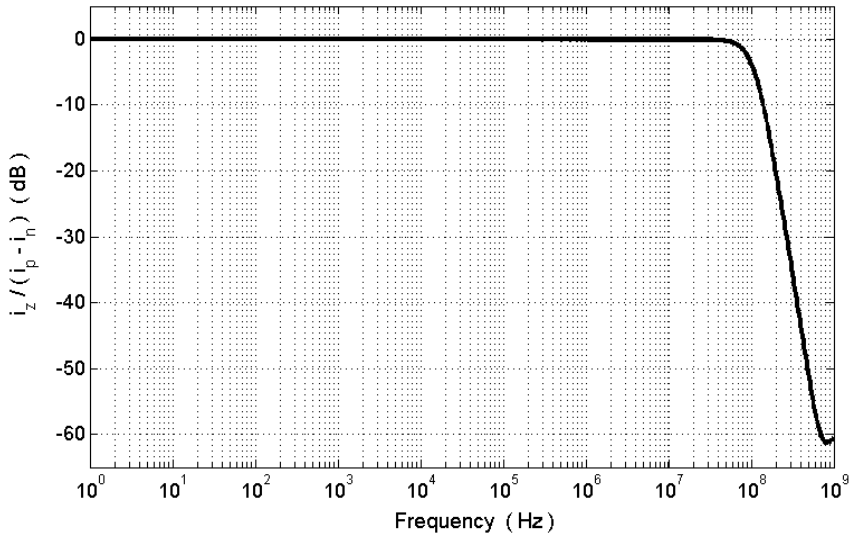

Figure 4.29. Frequency response of the current transfer ratio

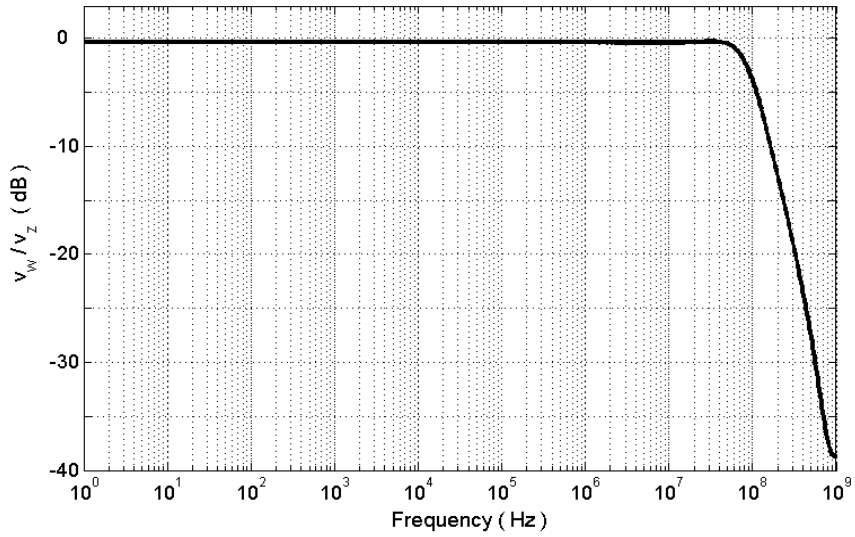

Figure 4.30. Frequency response of the voltage transfer ratio

AC transfer characteristics of the proposed CDBA are given in Figure 4.29 and Figure 4.30. Current transfer ratios (α_p, α_n) and the voltage transfer ratio (β_v) are found to

be 0.990, 0.995 and 0.963. The –3dB bandwidths of the transfer ratios are 93.5 MHz, 121 MHz and 87 MHz, respectively.

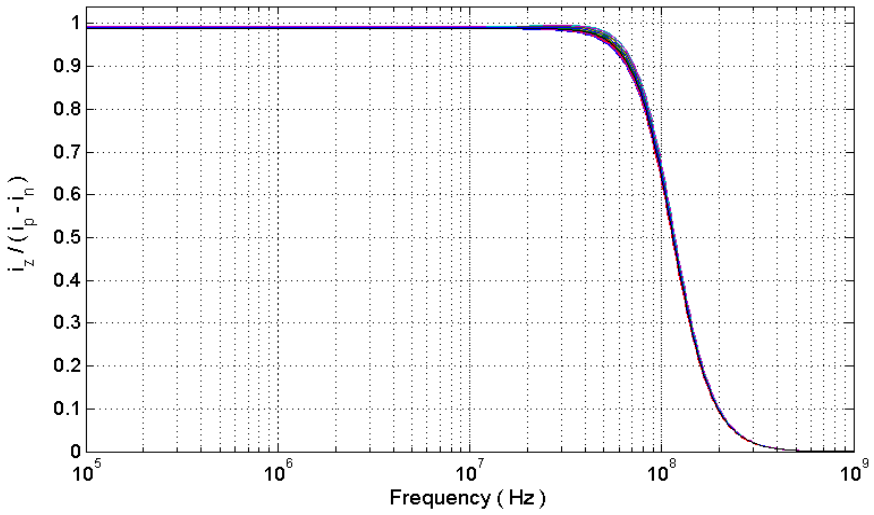

Figure 4.31. Monte-Carlo analysis of the current transfer ratio

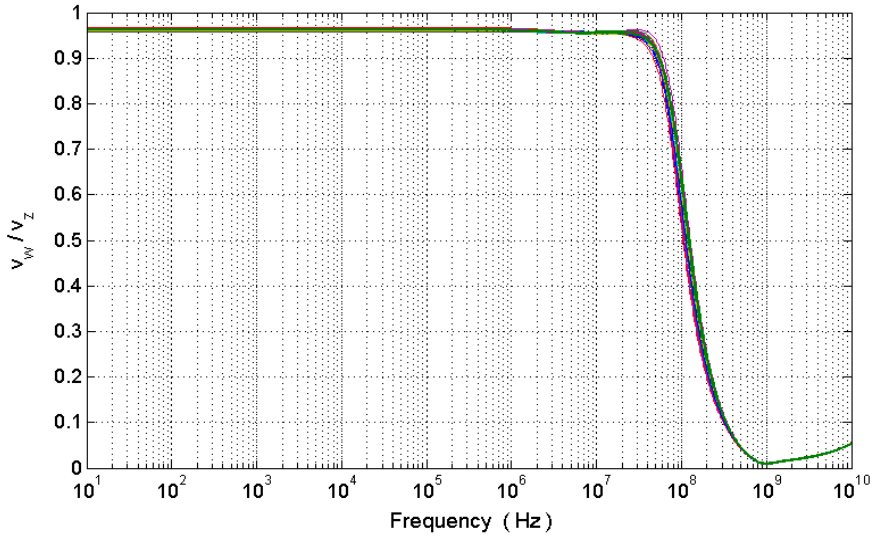

Figure 4.32. Monte-Carlo analysis of the voltage transfer ratio

To illustrate the effects of parameter variations on the proposed circuit, Monte-Carlo simulations are done. W, L and V_{T0} parameters of each transistor are varied by using values supplied by UMC. Simulation results are given in Figure 4.31 and Figure 4.32. Variations on the current and voltage transfer ratios are 0.5% and 1.15%, respectively. Summary of the CDBA performance is shown in Table 4.4.

Table 4.4. Performance of the proposed CDBA

Simulation Results	
Parameter	**Schematic**
Power supply	±0.6 V
Power dissipation	311 μW
Bias voltage, V_{B1}	+0.45 V
Bias voltage, V_{B2}	–0.2 V
Bias current, I_{B1}	40 μA
Bias current, I_{B2}	20 μA
Output voltage swing	(–0.48 V)-(+0.52 V)
Current transfer ratio, $\alpha_p = I_z / I_p$	0.990
Current transfer ratio, $\alpha_n = I_z / I_n$	0.995
Current transfer BW of α_p	93.5 MHz
Current transfer BW of α_n	121 MHz
Voltage transfer ratio, $\beta_v = V_w / V_z$	0.963
Voltage transfer BW	87 MHz
Terminal-p resistance	63.5 Ω
Terminal-n resistance	63.5 Ω
Terminal-z resistance	218 kΩ
Terminal-w resistance	80.5 Ω
Input current linear range	(–40 μA)-(+40 μA)
Offset current at terminal-z	0.1 μA

4.1.3.1. Design Example. A second-order, voltage-mode notch filter circuit shown in Figure 4.33 is chosen from the literature [95] as a design example.

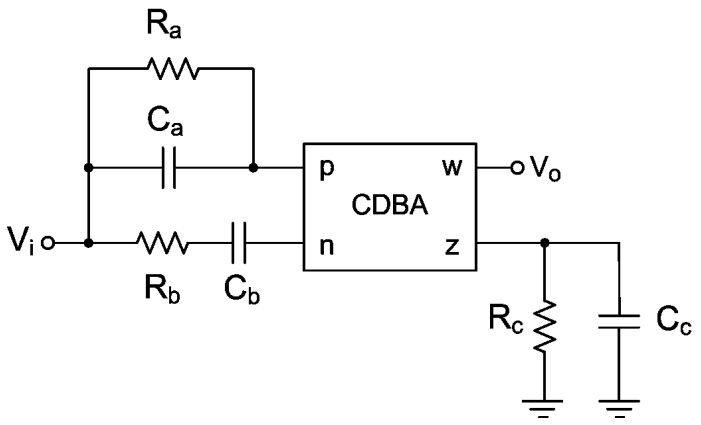

Figure 4.33. Second-order voltage-mode notch filter

Transfer function of the circuit is given as follows;

$$\frac{V_o}{V_i} = \frac{C_a}{C_c} \frac{s^2 + \dfrac{1}{R_a R_b C_a C_b}}{s^2 + \left(\dfrac{1}{R_b C_b} + \dfrac{1}{R_c C_c}\right)s + \dfrac{1}{R_b R_c C_b C_c}} \tag{4.15}$$

The angular resonant frequency (ω_o) and quality factor (Q) of the filter can be expressed in (4.16) and (4.17);

$$\omega_o = \sqrt{\frac{1}{R_b R_c C_b C_c}} \tag{4.16}$$

$$Q = \frac{\sqrt{R_b R_c C_b C_c}}{R_b C_b + R_c C_c} \tag{4.17}$$

If the external component values are chosen as R_a=8 kΩ, R_b=4 kΩ, R_c=8 kΩ, C_a=50 pF, C_b=100 pF and C_c=50 pF, then the center frequency of the circuit is found as f_o=393 kHz. Figure 4.34 and Figure 4.35 depict the gain and phase responses of the filter.

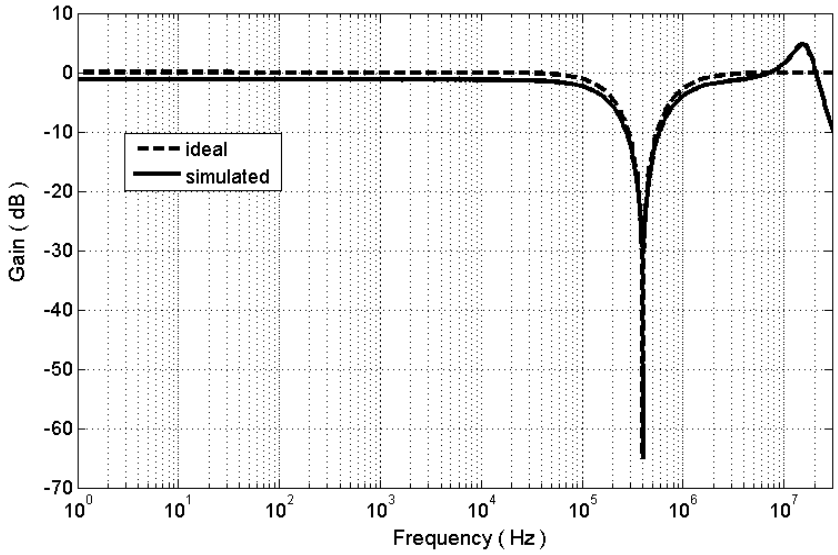

Figure 4.34. Gain response of the second-order notch filter

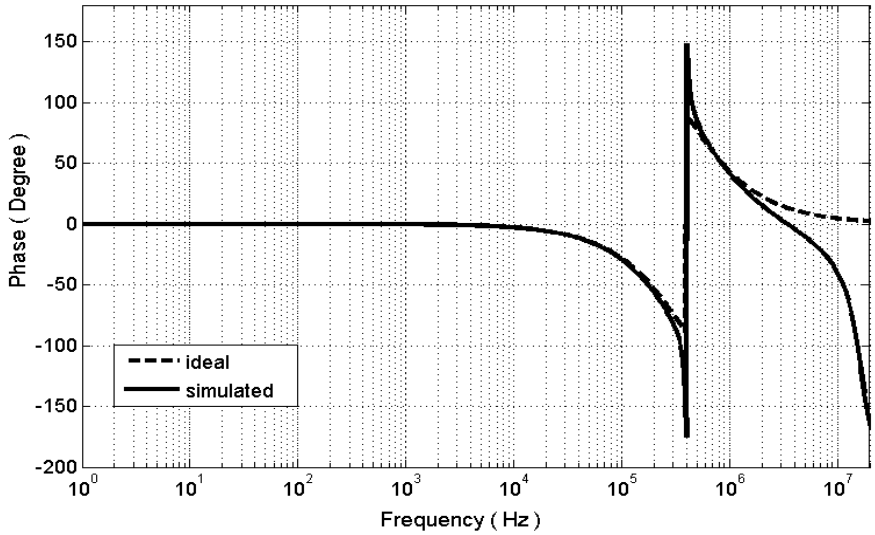

Figure 4.35. Phase response of the second-order notch filter

Finally, THD of the notch filter is simulated by applying 100 kHz sinusoidal input signal with various amplitudes to the input of the filter. Figure 4.36 shows that THD is less than 10% over the input range of ±0.4 V.

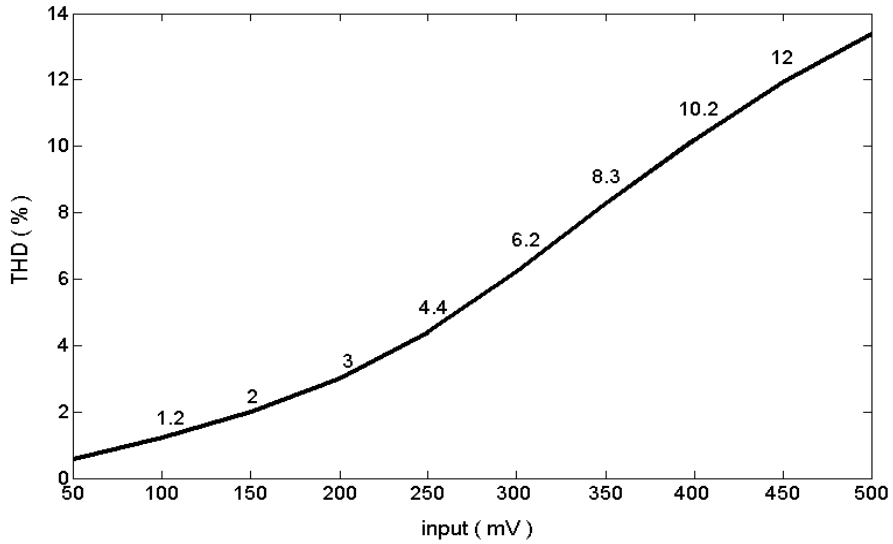

Figure 4.36. Output harmonic distortion versus input voltage of 100 kHz

4.1.4. Third Proposed Low-Voltage CDBA

A novel CMOS current differencing buffered amplifier suitable for low-voltage operation is presented. The proposed circuit operates with the power supplies of ±0.6 V and

consumes approximately 335 μW power. It also has a larger output voltage swing compared to the CDBAs proposed in the literature. 0.18 μm twin-well CMOS technology is used for the simulations. Performance of the CDBA is verified with HSPICE. Simulation results show that the proposed CDBA has terminal resistances of R_p=R_n=2.95 Ω, R_z=218 kΩ and R_w=16.3 Ω. Moreover, it provides high current and voltage transfer ratios which are α_p = 0.994, α_n = 1.01 and β_v = 0.97.

4.1.4.1. Current Differencing Circuit. The current differencing circuit is based on the flipped voltage follower current sources (FVFCS) which is shown in Figure 4.37.

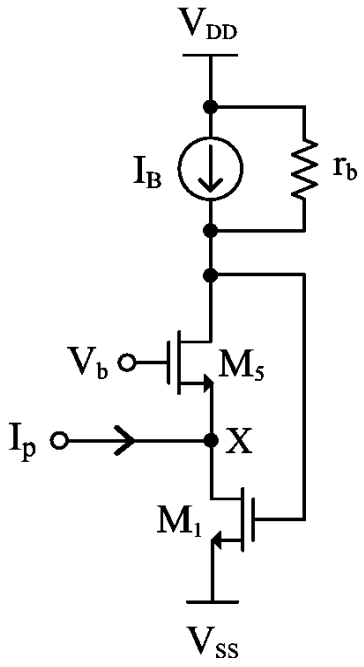

Figure 4.37. Flipped voltage follower current source (FVFCS)

There are two main benefits of using the FVFCS. The first one is that it is very useful for low-voltage operation and the minimum input voltage is given by;

$$V_{\text{in, min}} = V_{\text{DSAT (M1)}} \tag{4.18}$$

The other big advantage of the FVFCS is that it gives rise to very low resistance values at node-X. The input resistance looking at node-X can be formulated as;

$$R_x \cong \frac{\frac{1}{g_{m5}}\left(1+\frac{r_b}{r_{o5}}\right) /\!/\ r_{o1}}{g_{m1}\left(r_b /\!/ g_{m5} r_{o1} r_{o5}\right)} \tag{4.19}$$

where r_b is the output resistance of the current source, r_o is the output resistance and g_m is the transconductance of the transistors. For a simple current source ($r_b = r_{o5}$), the resistance at node-X in (4.19) is changed to;

$$R_x \cong \frac{2}{g_{m1} g_{m5} r_{o5}} \tag{4.20}$$

It is possible to make an improvement on this topology. For this purpose, we have applied a feedback circuitry to the topology by which the resistance at terminal-X has been further reduced. The resulting circuit is shown in Figure 4.38.

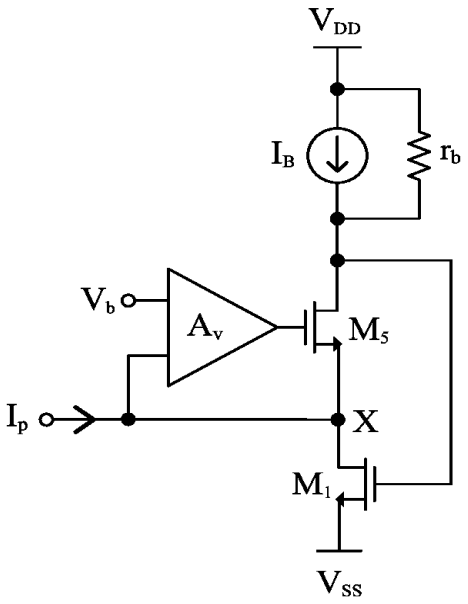

Figure 4.38. FVFCS with feedback

For the resulting circuit, the resistance at node-X in (4.20) is modified to;

$$R_{x,\,new} \cong \frac{2}{A_v g_{m1} g_{m5} r_{o5}} \tag{4.21}$$

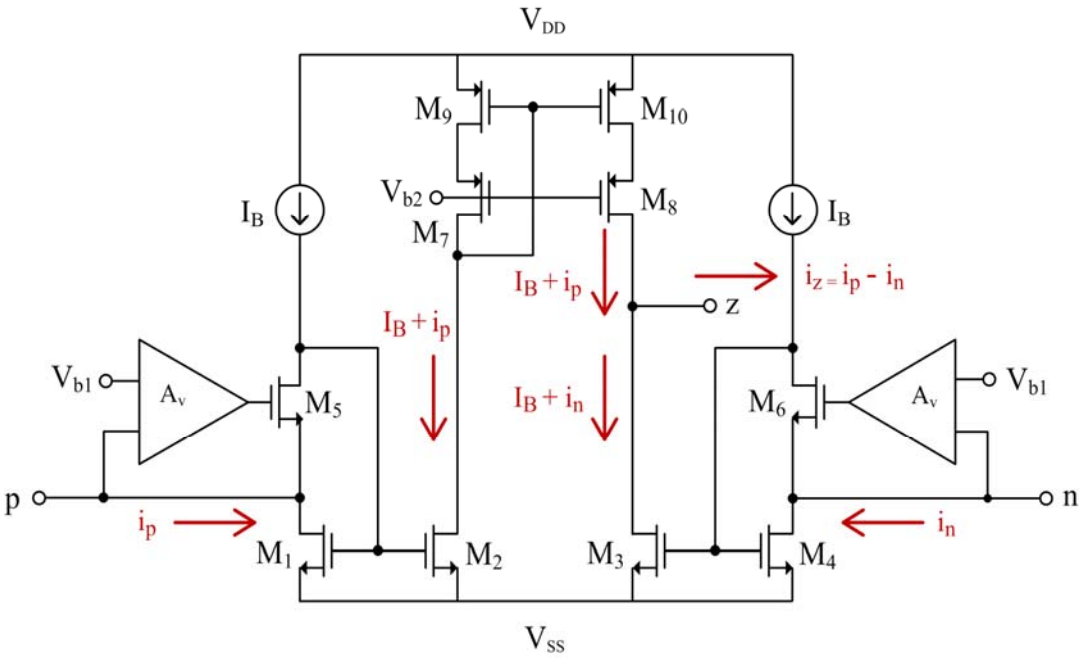

Figure 4.39. Current subtractor circuit

The current subtractor circuit shown in Figure 4.39 is formed by the transistors M_1 to M_{10}. Frequency characteristics of the input terminal impedances of the proposed CDBA are given in Figure 4.40. It turns out that impedances at terminal-p and terminal-n are the same and equal to 2.95 Ω for a wide frequency range. Terminal-z impedance is 218 kΩ at frequencies up to 1 MHz which is shown in Figure 4.41.

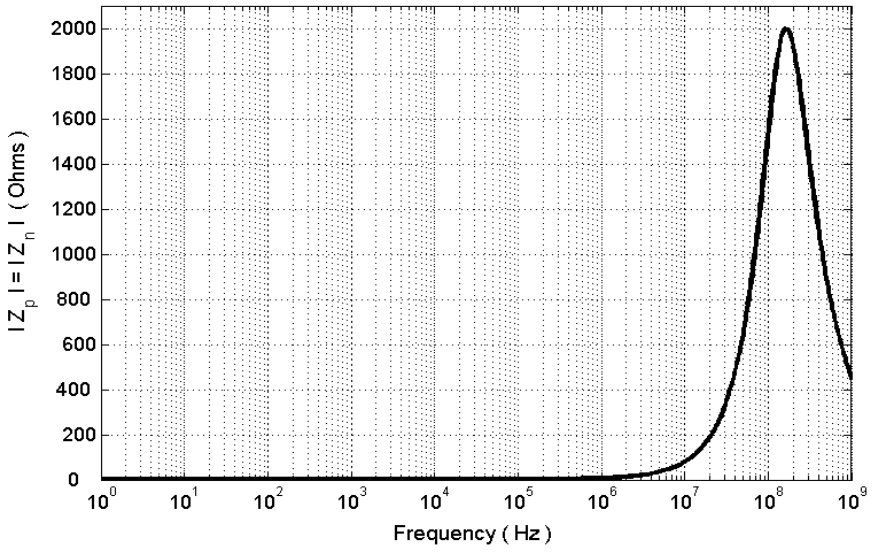

Figure 4.40. Frequency variation of terminal-p and terminal-n impedance magnitudes

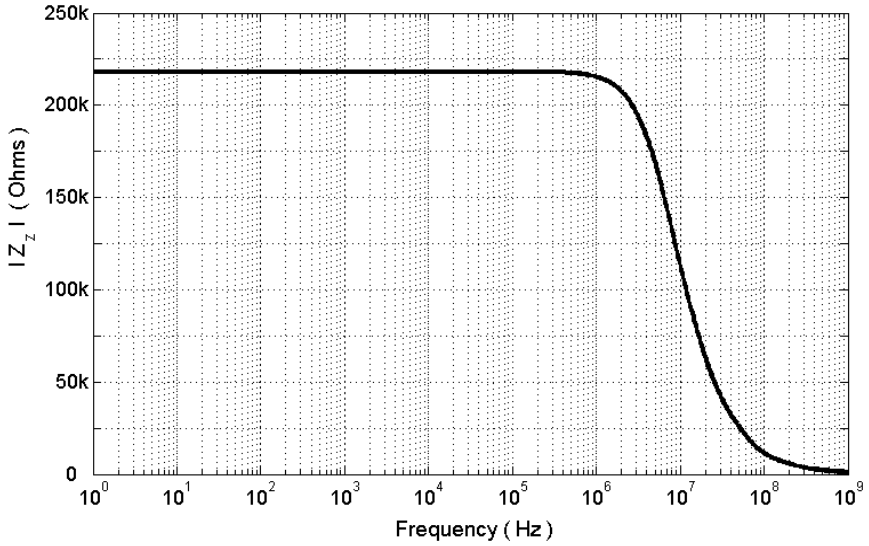

Figure 4.41. Frequency variation of terminal-z impedance magnitude

DC current transfer characteristic of the proposed CDBA is illustrated in Figure 4.42. It can be seen that this CDBA has a high linearity over the entire dynamic range (I_B=40 μA) and the offset current at terminal-z is 60 nA.

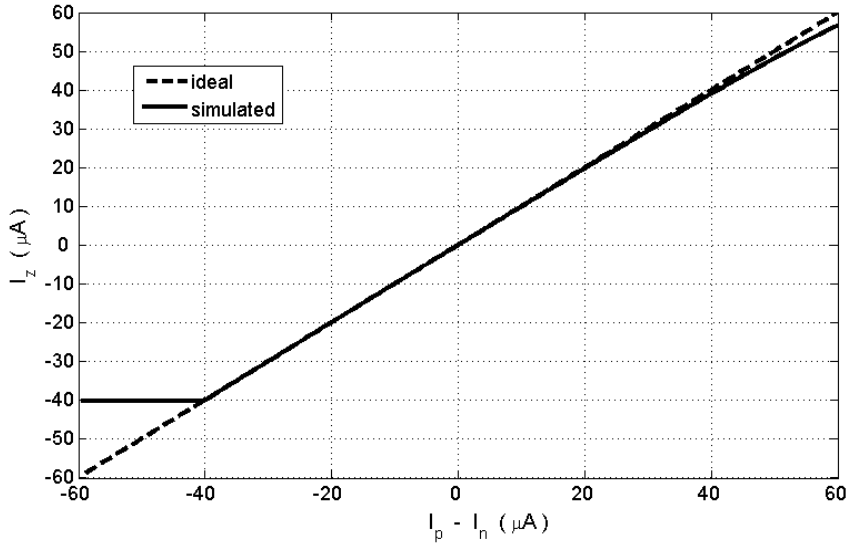

Figure 4.42. DC current transfer characteristic

4.1.4.2. Voltage Buffer. Output stage of the proposed circuit is illustrated in Figure 4.43. This circuit has an excellent output voltage swing capability which extends from rail to rail. An n-channel and a p-channel differential pairs are connected in parallel as shown in

Figure 4.43 in order to have such a large common-mode signal range. The n-channel differential pair (M_{15}-M_{16}) is able to reach the positive supply rail, while the p-channel one (M_{19}-M_{20}) can sense common-mode voltages around the negative supply rail.

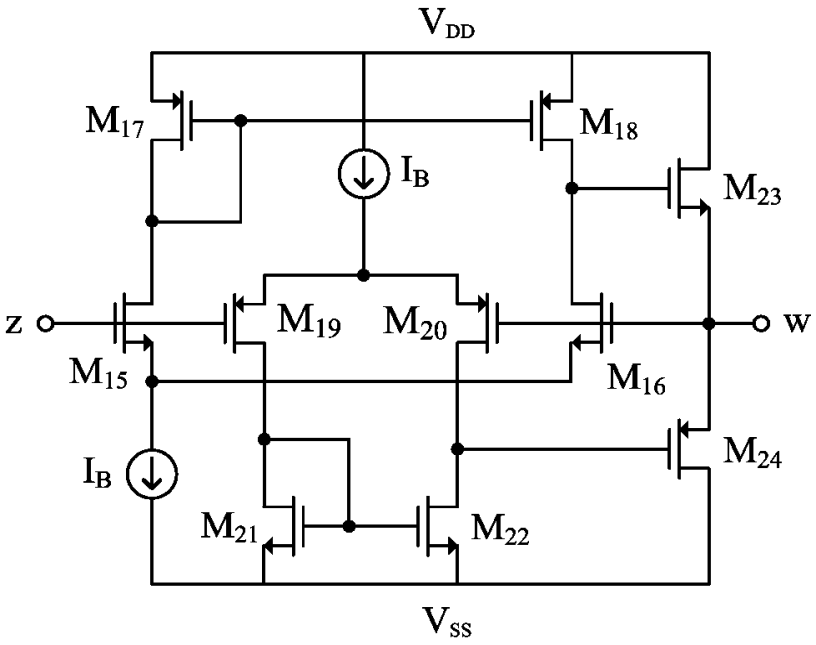

Figure 4.43. Output stage

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Figure 4.44 shows DC voltage transfer characteristic of the circuit. Maximum and minimum output voltages are +0.49 V and –0.52 V, respectively.

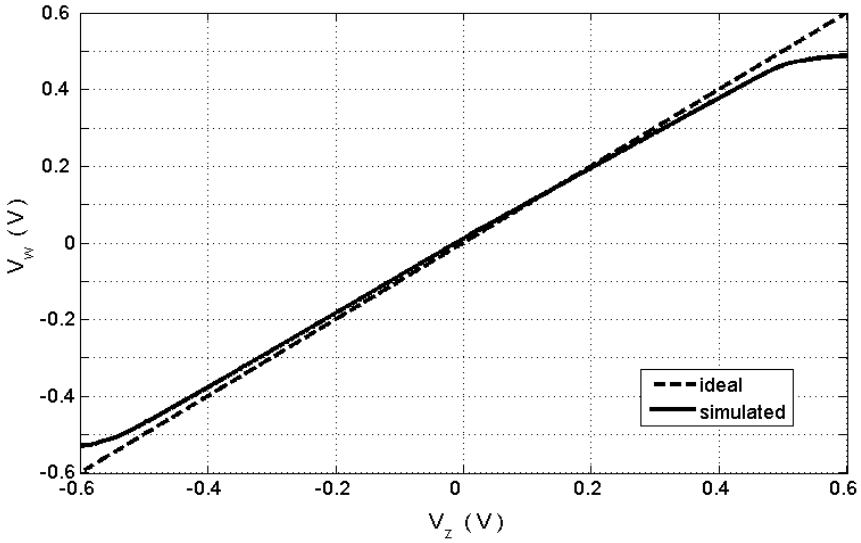

Figure 4.44. DC voltage transfer characteristic

Additionally, this output stage offers very low output resistance values which can be formulated as;

$$R_{w} = \frac{1}{g_{m23}\left(1 + g_{m16}\frac{r_o}{2}\right)} // \frac{1}{g_{m24}\left(1 + g_{m20}\frac{r_o}{2}\right)} \tag{4.22}$$

It is possible to decrease this resistance down to smaller values by using an additional transistor (M_{25}) in local feedback configuration (super-source follower) which is shown in Figure 4.45.

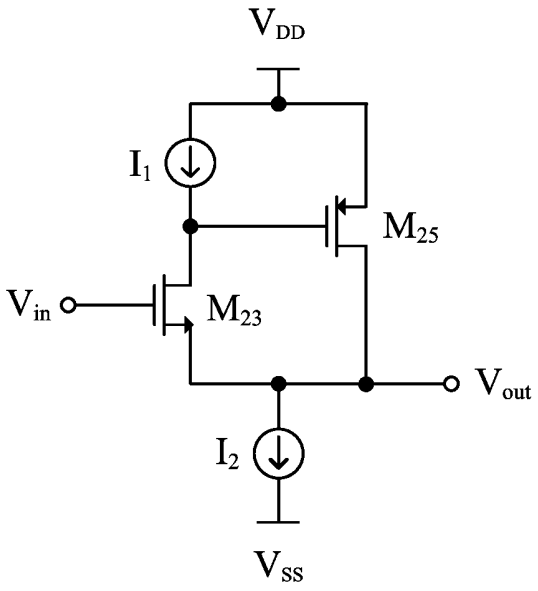

Figure 4.45. Source follower with local feedback

In this case, resistance value at the output terminal which is given in (4.22) can be rearranged as follows;

$$R_{w,new} = \frac{1}{g_{m23}g_{m25}r_o\left(1 + g_{m16}\frac{r_o}{2}\right)} // \frac{1}{g_{m24}\left(1 + g_{m20}\frac{r_o}{2}\right)} \tag{4.23}$$

Figure 4.46 represents the modified version of the output stage. Figure 4.47 shows the resistance value at terminal-w which is 6.3 Ω in the practical frequency range.

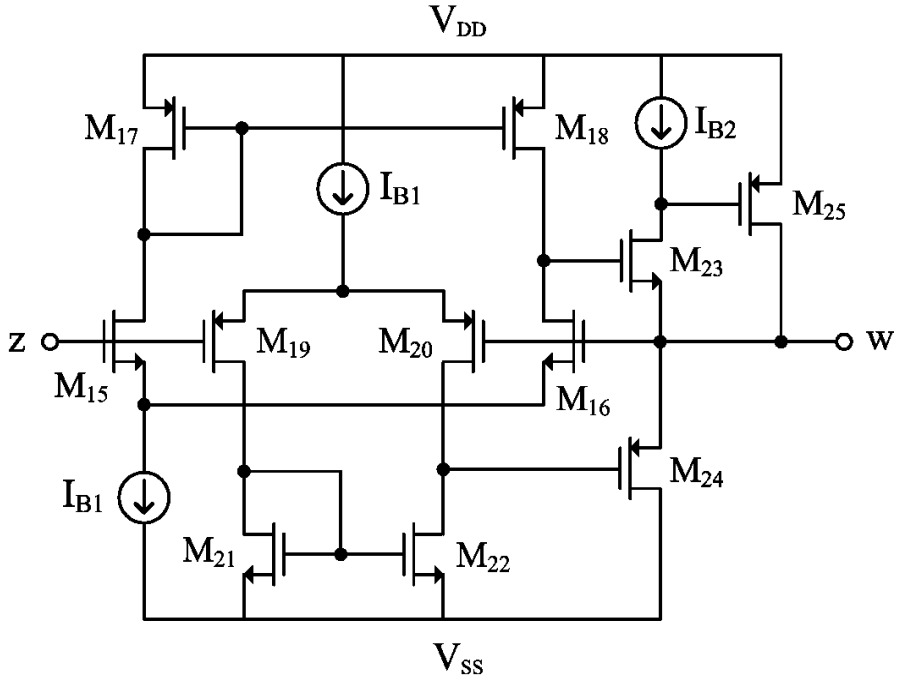

Figure 4.46. Output stage with feedback

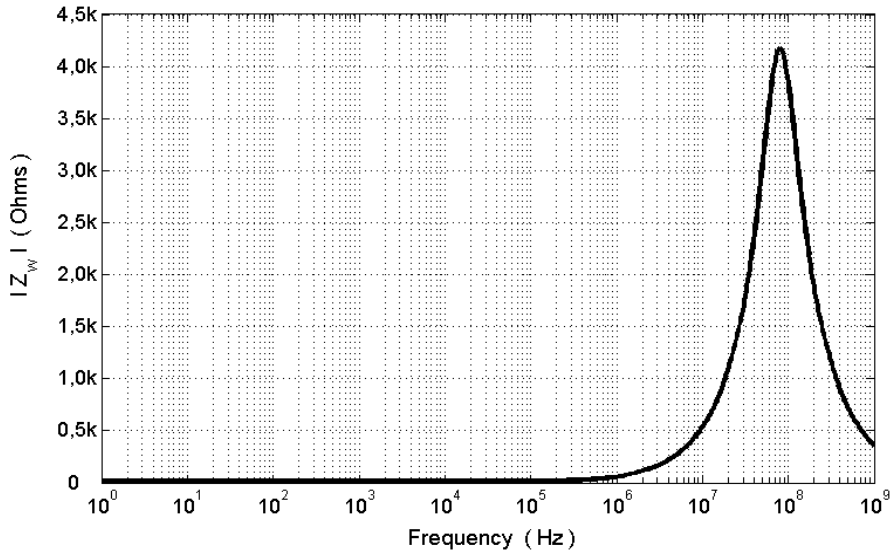

Figure 4.47. Frequency variation of terminal-w impedance magnitude

4.1.4.3. Proposed Low-Voltage Low-Power CDBA. Schematic and layout of the proposed CDBA are given in Figure 4.48 and Figure 4.49, respectively. It is based on the use of the current differencing circuit (M_1-M_{14}) and voltage buffer (M_{15}-M_{25}). Aspect ratios of the transistors are reported in Table 4.5.

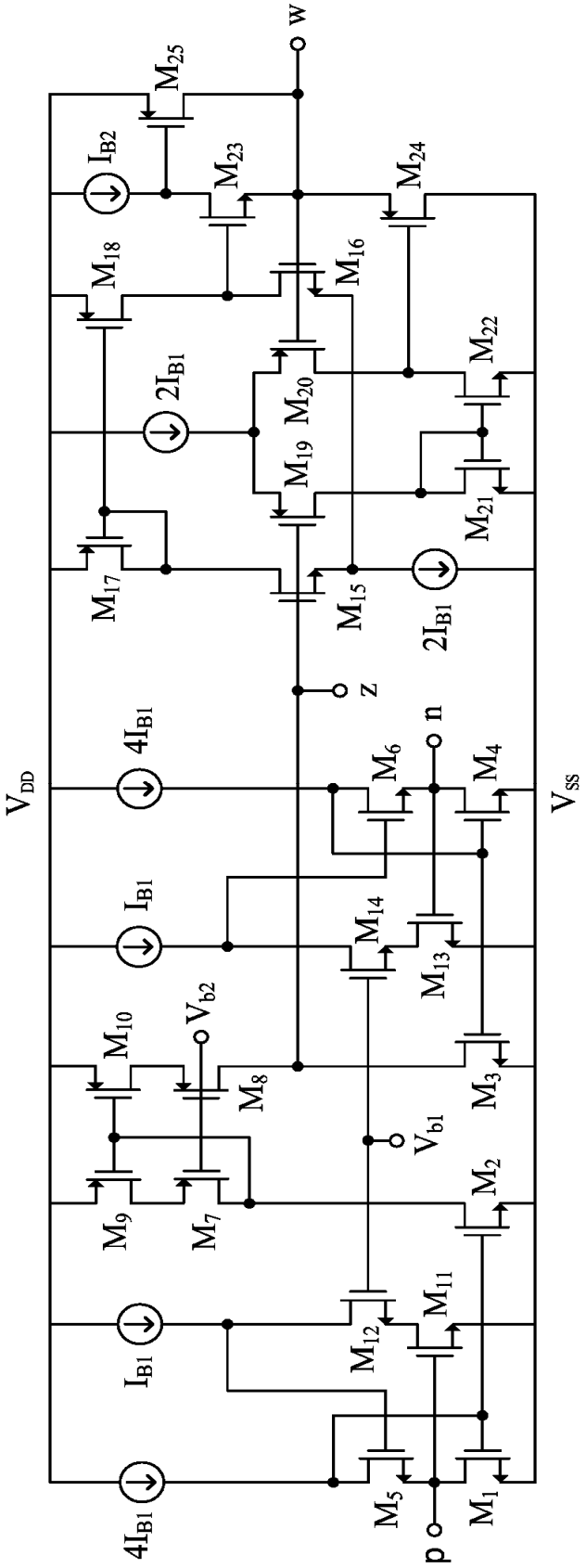

Figure 4.48. Third proposed CDBA

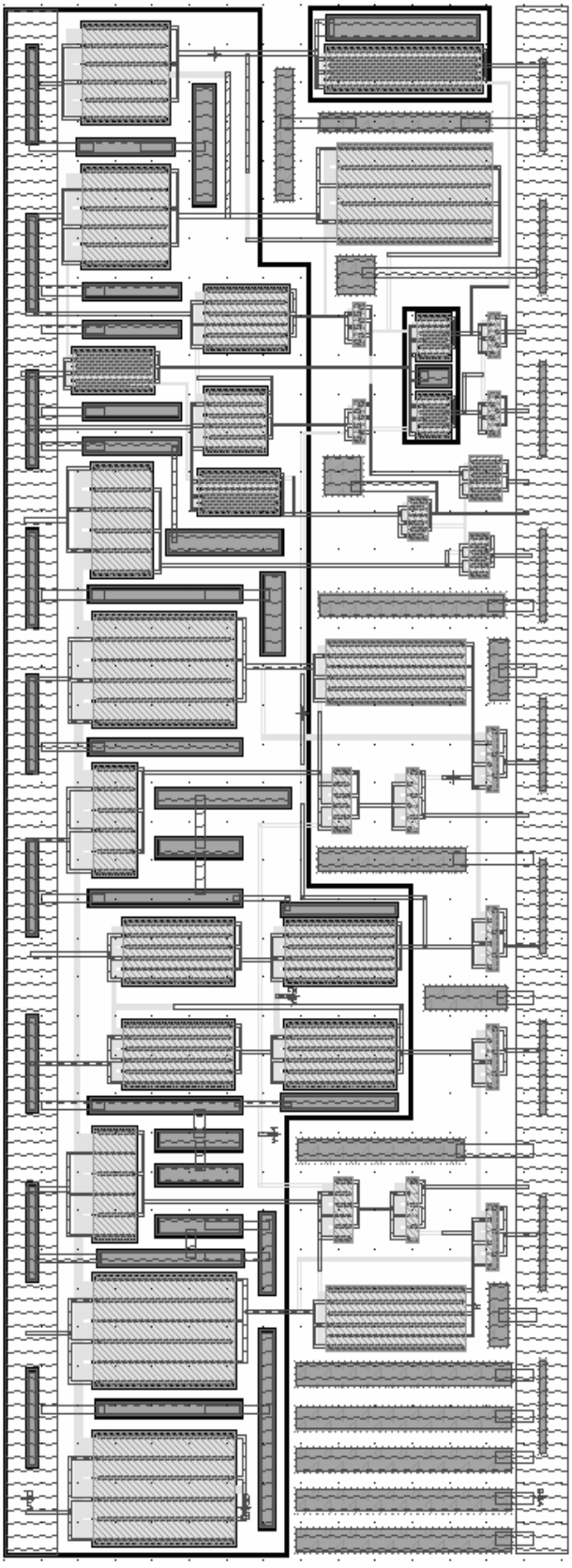

Figure 4.49. Layout of the proposed CDBA

Table 4.5. Aspect ratios

Transistor	W/L [µm/µm]
M_1, M_2, M_3, M_4	3.6/0.90
M_5, M_6	90/0.90
M_7, M_8	70/0.90
M_9, M_{10}	70/0.90
M_{11}, M_{13}	4.5/0.90
M_{12}, M_{14}	9/0.90
M_{15}, M_{16}	4.5/0.36
M_{17}	36/0.90
M_{18}	52/0.90
M_{19}, M_{20}	18/0.36
M_{21}, M_{22}	4.5/0.36
M_{23}	100/1.80
M_{24}	100/0.36
M_{25}	54/1.80

AC transfer characteristics of the proposed CDBA are given in Figure 4.50 and Figure 4.51. Current transfer ratios are $\alpha_p = 0.994$ and $\alpha_n = 1.01$. The voltage transfer ratio is found to be $\beta_v = 0.97$. The –3dB bandwidths of the current and voltage transfer ratios are 92.4 MHz, 151 MHz and 105 MHz, respectively.

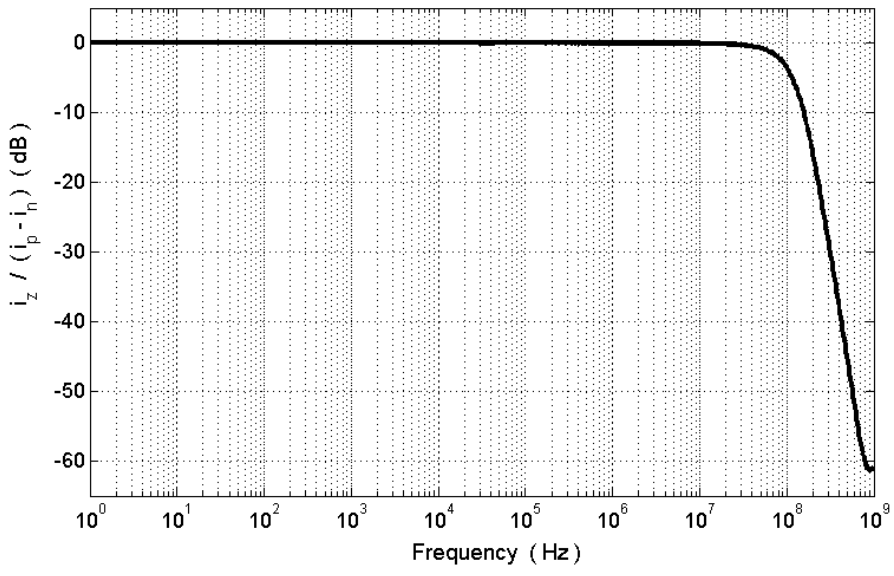

Figure 4.50. Current transfer ratio

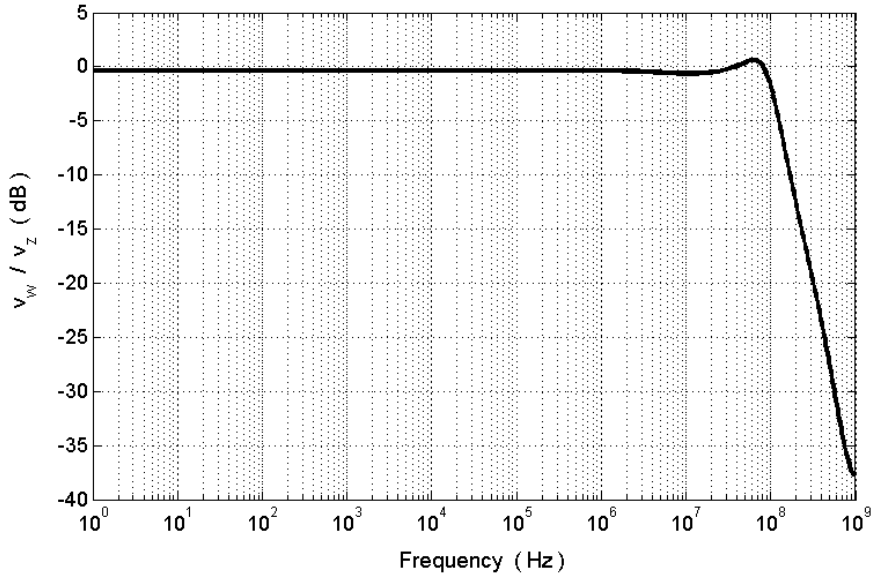

Figure 4.51. Voltage transfer ratio

To illustrate the effects of parameter variations on the proposed circuit, Monte-Carlo simulations are done. W, L and V_{T0} parameters of each transistor are varied by using values supplied by UMC. Simulation results are given in Figure 4.52 and Figure 4.53. Variations on the current and voltage transfer ratios are 0.6% and 6.5%, respectively. Summary of the simulation results for the proposed CDBA is shown in Table 4.6.

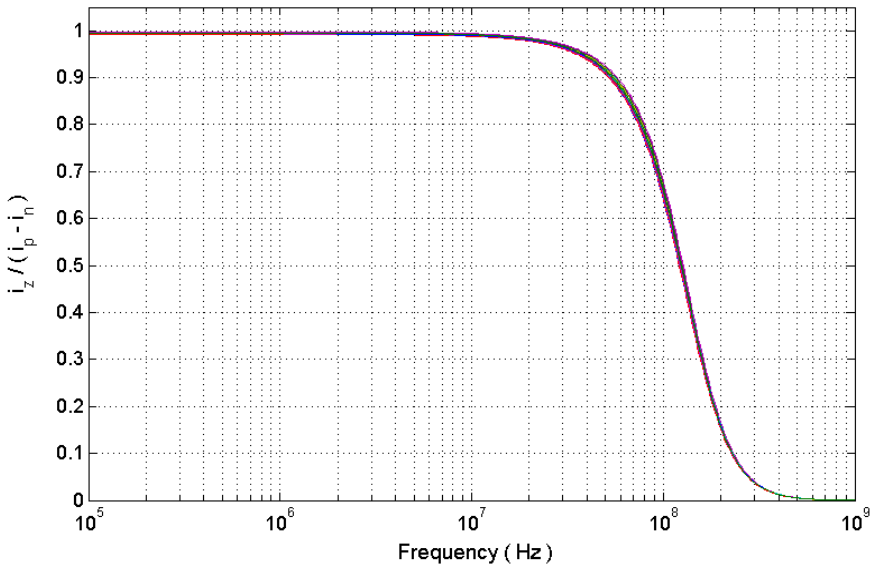

Figure 4.52. Monte-Carlo analysis of the current transfer ratio

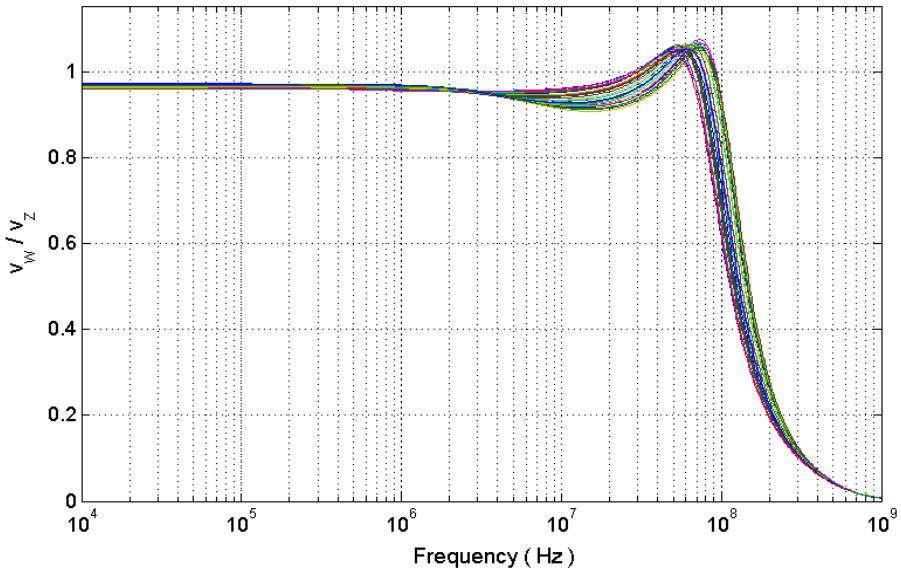

Figure 4.53. Monte-Carlo analysis of the voltage transfer ratio

Table 4.6. Performance of the proposed CDBA

Simulation Results	
Parameter	**Schematic**
Power supply	±0.6 V
Power dissipation	335 µW
Bias voltage, V_{B1}	+0.4 V
Bias voltage, V_{B2}	–0.2 V
Bias current, I_{B1}	10 µA
Bias current, I_{B2}	5 µA
Output voltage swing	(–0.52 V)-(+0.49 V)
Current transfer ratio, $\alpha_p = I_z / I_p$	0.994
Current transfer ratio, $\alpha_n = I_z / I_n$	1.01
Current transfer BW of α_p	92.4 MHz
Current transfer BW of α_n	151 MHz
Voltage transfer ratio, $\beta_v = V_w / V_z$	0.97
Voltage transfer BW	105 MHz
Terminal-p resistance	2.95 Ω
Terminal-n resistance	2.95 Ω
Terminal-z resistance	218 kΩ
Terminal-w resistance	16.3 Ω
Input current linear range	(–40 µA)-(+40 µA)
Offset current at terminal-z	60 nA

4.1.4.4. Design Example. The proposed all-pass/notch filter configuration is shown in Figure 4.54.

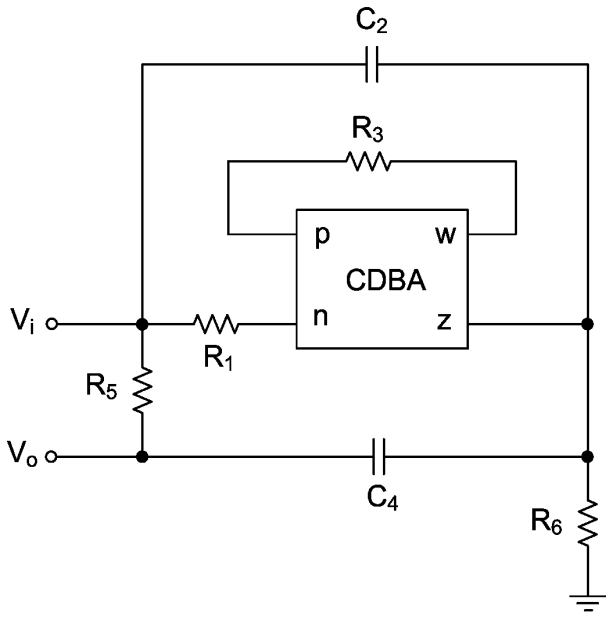

Figure 4.54. Voltage-mode second-order all-pass/notch filter

From Figure 4.54, the voltage transfer function for the proposed filter configuration can be written as;

$$\frac{V_o}{V_i} = \frac{-Y_1Y_4 + Y_2Y_4 + Y_2Y_5 - Y_3Y_5 + Y_4Y_5 + Y_5Y_6}{Y_2Y_4 - Y_3Y_4 + Y_2Y_5 - Y_3Y_5 + Y_4Y_5 + Y_4Y_6 + Y_5Y_6} \tag{4.24}$$

If components are selected as $Y_1 = G_1$, $Y_2 = sC_2$, $Y_3 = G_3$, $Y_4 = sC_4$, $Y_5 = G_5$ and $Y_6 = G_6$, the voltage transfer function becomes;

$$\frac{V_o}{V_i} = \frac{-G_3G_5 + G_5G_6 - C_4G_1s + C_2G_5s + C_4G_5s + C_2C_4s^2}{-G_3G_5 + G_5G_6 - C_4G_3s + C_2G_5s + C_4G_5s + C_4G_6s + C_2C_4s^2} \tag{4.25}$$

This transfer function allows two types of realizations for the proposed configuration by choosing the admittances appropriately. If $C_4G_1 + C_4G_3 = 2C_2G_5 + 2C_4G_5 + C_4G_6$, a second-order all-pass filter can be obtained and the voltage transfer function becomes;

$$\frac{V_o}{V_i} = \frac{G_5(G_6 - G_3) - (C_2G_5 + C_4G_5 + C_4G_6 - C_4G_3)s + C_2C_4s^2}{G_5(G_6 - G_3) + (C_2G_5 + C_4G_5 + C_4G_6 - C_4G_3)s + C_2C_4s^2} \tag{4.26}$$

From (4.26), the angular resonant frequency (ω_o) and quality factor (Q) for the filter can be expressed as;

$$\omega_o = \sqrt{\frac{G_5(G_6 - G_3)}{C_2C_4}} \tag{4.27}$$

$$Q = \frac{\sqrt{C_2C_4G_5(G_6 - G_3)}}{G_5(C_2 + C_4) + C_4(G_6 - G_3)} \tag{4.28}$$

Similarly by choosing $C_4G_1 = C_2G_5 + C_4G_5$ in (4.25), a second-order notch filter can be realized and the voltage transfer function can be written as;

$$\frac{V_o}{V_i} = \frac{G_5(G_6 - G_3) + C_2C_4s^2}{G_5(G_6 - G_3) + (C_2G_5 + C_4G_5 + C_4G_6 - C_4G_3)s + C_2C_4s^2} \tag{4.29}$$

From (4.29), the angular resonant frequency (ω_o) and quality factor (Q) for the filter can be expressed as;

$$\omega_o = \sqrt{\frac{G_5(G_6 - G_3)}{C_2C_4}} \tag{4.30}$$

$$Q = \frac{\sqrt{C_2C_4G_5(G_6 - G_3)}}{G_5(C_2 + C_4) + C_4(G_6 - G_3)} \tag{4.31}$$

For the all-pass filter, component values are chosen as R_1=R_6=1 kΩ, R_3=2 kΩ, R_5=8 kΩ and C_2=C_4=0.1 nF, which results in a center frequency of 400 kHz. Magnitude and phase responses are given in Figure 4.55 and Figure 4.56, respectively. Note that angular resonant frequency (ω_o) can be set to lower frequencies by changing the value of G_3.

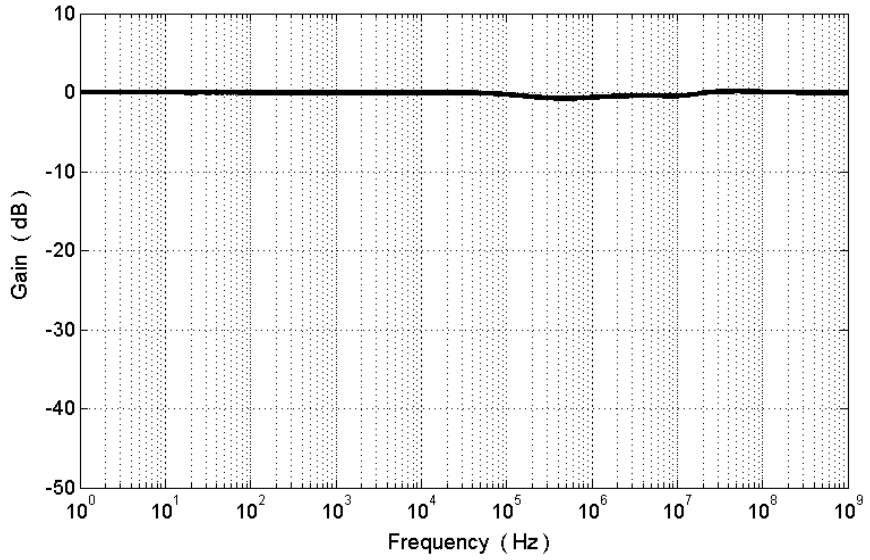

Figure 4.55. Gain response of the all-pass filter

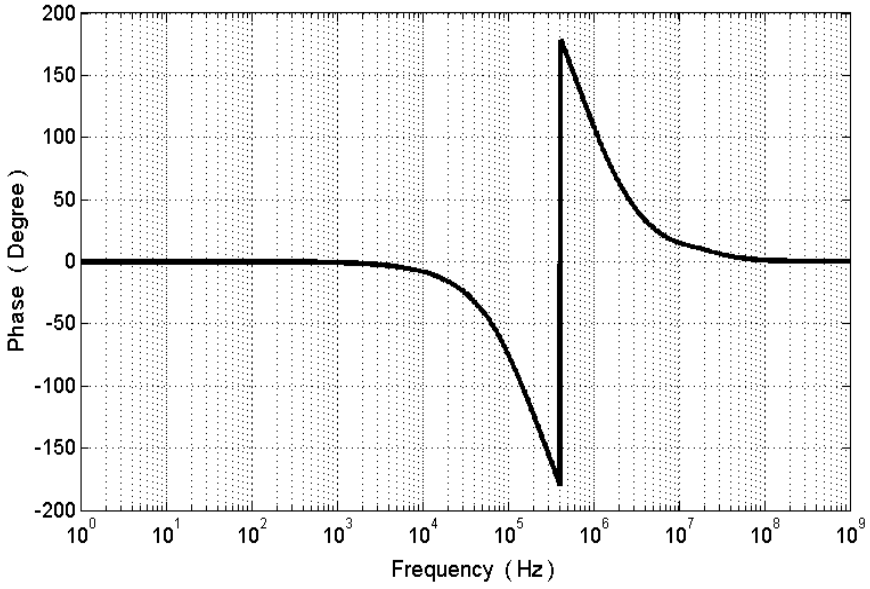

Figure 4.56. Phase response of the all-pass filter

HSPICE simulations are also performed for the notch filter. External component values are chosen as R_1=R_6=2 kΩ, R_3=R_5=4 kΩ and C_2=C_4=0.1 nF. Then the center frequency is found to be 400 kHz. Simulated magnitude response of the filter is given in Figure 4.57 and simulated phase response of the filter is given in Figure 4.58. Simulation results are in close agreement with the theoretical ones.

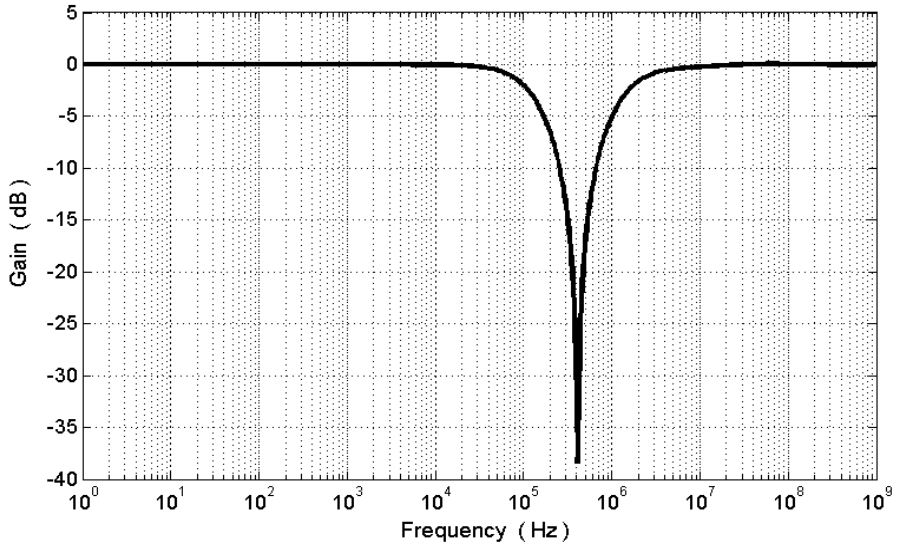

Figure 4.57. Gain response of the notch filter

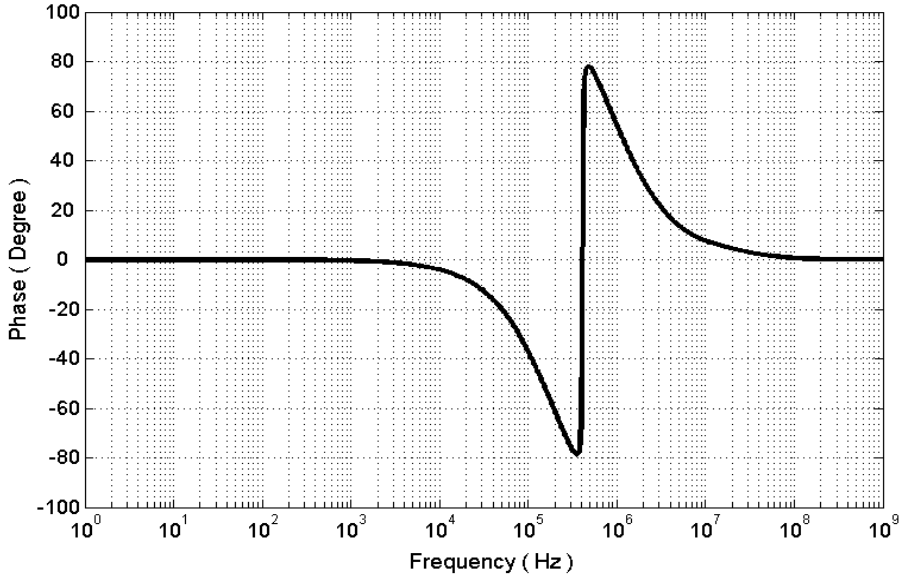

Figure 4.58. Phase response of the notch filter

4.1.5. Noise Performance of the Proposed CDBAs

Noise contributions of the proposed CDBA circuits mainly come from two sources. The first source is the current differencing circuit and the second source is the voltage buffer. Simulation results for the input-referred noise currents at terminal-p are shown in Figure 4.59. From the simulation results, the lowest input noise current is 6.2 pA/√Hz.

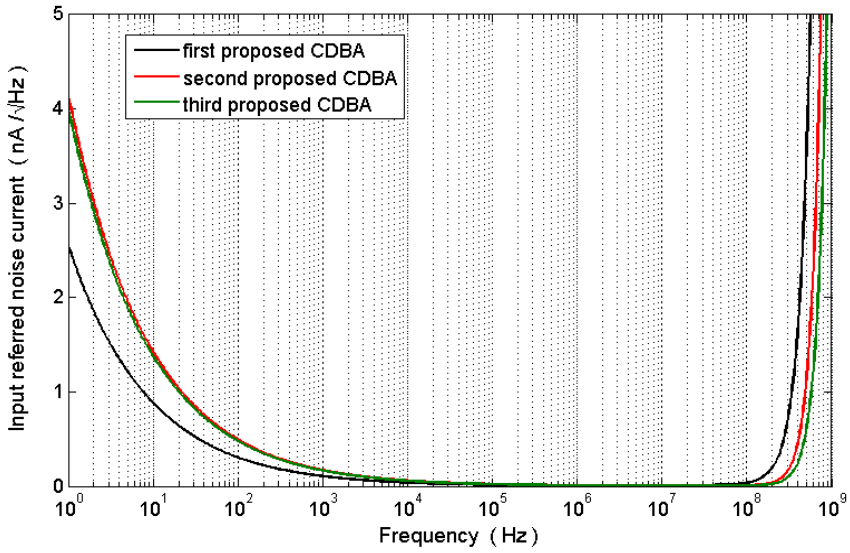

Figure 4.59. Noise currents at terminal-p

4.1.6. Summary

In this section, three CMOS current differencing buffered amplifier (CDBA) circuits suitable for low-voltage operation are proposed. UMC 0.18 µm twin-well CMOS process parameters are used for the simulations. Although the standard supply voltage is 1.8 V for the chosen technology, proposed circuits operate with the power supply of 1.2 V. From the performance comparison in Table 4.7, it can be observed that although there is approximately 35% reduction in the supply voltage, simulation results of the proposed circuits are comparable with that of the circuits reported in the literature. Proposed CDBAs except the first one that has a limited output voltage swing can swing from the positive supply rail to negative supply rail. Additionally, proposed CDBAs consume less power than their counterparts.

Simulation results show that terminal resistance values for the first two CDBAs are comparable with the CDBAs in the literature and terminal resistance values for the third proposed CDBA are better than the CDBAs in the literature. Also, proposed CDBAs provide higher current and voltage transfer ratios than their counterparts. Finally, different types of filter configurations are proposed and the usefulness of the CDBAs is illustrated on these configurations. Simulation results are in remarkable agreement with the expected ones.

Table 4.7. Comparison of CDBAs

Parameter	**[84]**	**[85]**	**First CDBA**	**Second CDBA**	**Third CDBA**
Power supply	±5 V	±1.25 V	±0.6 V	±0.6 V	±0.6 V
Power dissipation	NA	1.15 mW	565.25 µW	311 µW	335 µW
Output voltage swing	NA	NA	−0.15 V +0.1 V	−0.52 V +0.48 V	−0.52 V +0.49 V
Offset current	NA	0.49 µA	0.05 µA	0.1 µA	60 nA
Terminal-p resistance	645 Ω	14 Ω	56.4 Ω	63.5 Ω	2.95 Ω
Terminal-n resistance	645 Ω	14 Ω	56.4 Ω	63.5 Ω	2.95 Ω
Terminal-z resistance	678 MΩ	290 kΩ	157 kΩ	218 kΩ	218 kΩ
Terminal-w resistance	49 Ω	14 Ω	270 Ω	80.5 Ω	16.3 Ω
Voltage gain, $\beta_v = V_w / V_z$	0.999	0.989	0.978	0.963	0.970
Voltage transfer BW	37 MHz	507 MHz	474 MHz	87 MHz	105 MHz
Current gain, $\alpha_p = I_z / I_p$	0.996	0.991	0.981	0.990	0.994
Current transfer BW of α_p	70 MHz	580 MHz	25 MHz	93.5 MHz	92.4 MHz
Current gain, $\alpha_n = I_z / I_n$	0.996	0.996	0.991	0.995	1.01
Current transfer BW of α_n	70 MHz	643 MHz	74.8 MHz	121 MHz	151 MHz

4.2. Operational Transresistance Amplifier (OTRA)

The circuit symbol and equivalent circuit of an ideal OTRA are illustrated in Figure 4.60. The port relations of an OTRA can be characterized by the following matrix form;

$$\begin{bmatrix} V_{\mathrm{p}} \\ V_{\mathrm{n}} \\ V_{\mathrm{z}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_{\mathrm{m}} & -R_{\mathrm{m}} & 0 \end{bmatrix} \begin{bmatrix} I_{\mathrm{p}} \\ I_{\mathrm{n}} \\ I_{\mathrm{z}} \end{bmatrix} \tag{4.32}$$

Input and output terminals are characterized by low impedance. Input terminals are internally grounded leading to circuits that are insensitive to the stray capacitances. For ideal operation, the transresistance (R_m) approaches infinity forcing input currents to be equal. Thus, the OTRA must be used in a feedback configuration in a way that is similar to

the opamp. A CDBA can also be considered as an OTRA with open-circuit terminal-z. Therefore, all circuits that have been designed so far can also be used for OTRA applications.

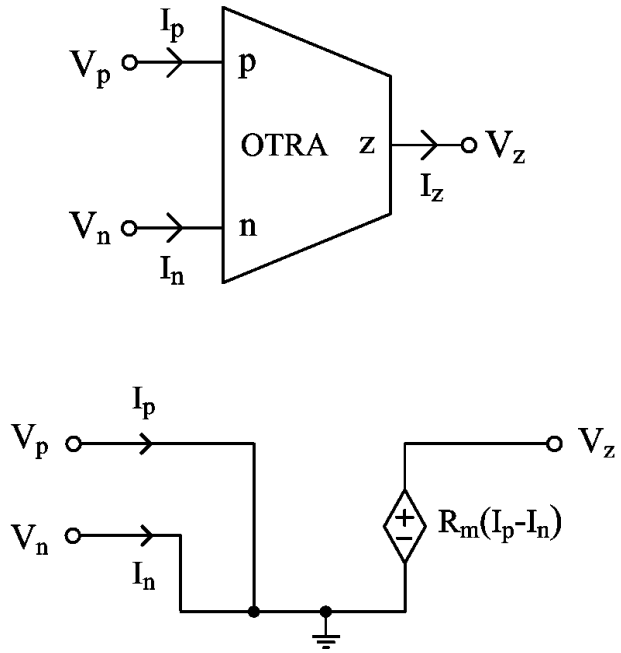

Figure 4.60. Symbol and equivalent circuit of an ideal OTRA

4.2.1. Realization of the OTRA Using AD844

To evaluate the theoretical analysis of the proposed circuit, a commercial integrated circuit (IC) namely AD844AN is adopted to implement an OTRA as shown in Figure 4.61 [96-97]. The AD844AN differs from a conventional opamp in that the voltage on the non-inverting signal input is transferred to the inverting input. Thus, an inherent virtual short exists between these two terminals without any external negative feedback path. Also, the current into the inverting terminal is equal to the current into the slewing node (T_z). Moreover, the output voltage is the same as the voltage at T_z. To simulate the virtual ground of the two input terminals of an OTRA, the non-inverting terminals of the AD844AN's should be grounded. To produce an output voltage proportional to the difference of the non-inverting and the inverting input currents, T_z node of the first AD844AN is connected to the inverting input terminal of the second IC. Then T_z node of the second IC is connected to ground through a resistance R_m.

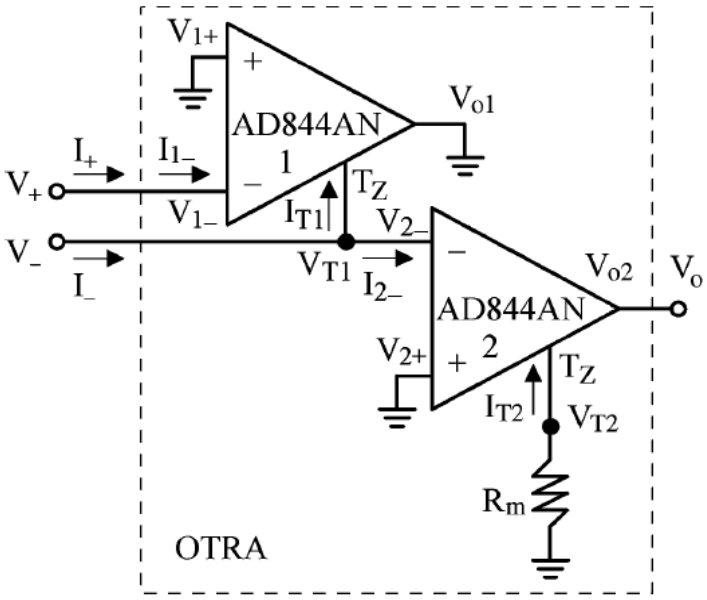

Figure 4.61. OTRA realization using AD844AN as one chip

Referring to Figure 4.61, the relationships among these variables are described in the following equations;

$$V_+ = V_{1-} = V_{1+} = 0$$

$$V_- = V_{2-} = V_{2+} = 0$$

$$V_{o1} = V_{T1} = V_{2-} = V_{2+} = 0$$

$$I_{T1} = I_{1-} = I_+$$

$$I_{T2} = I_{2-} = I_- - I_{T1} = I_- - I_+$$

$$V_o = V_{T2} = -R_m I_{T2} = R_m (I_+ - I_-) \tag{4.33}$$

Therefore, the exact terminal characteristics of the OTRA can be precisely fulfilled. From (4.33), if R_m is large enough (for example, T_z node of the second AD844AN is open-circuited), then only a little difference between I_+ and I_- is required to drive the output voltage of the OTRA to its saturation levels.

4.2.2. Non-Ideal Characteristics of CMOS OTRA

4.2.2.1. Frequency-Dependent Finite Gain. The output voltage (V_{out}) of an OTRA is given by;

$$V_{\text{out}} = R_{\text{m}}\left(I_{\text{p}} - I_{\text{n}}\right) \tag{4.34}$$

In ideal operation, it is assumed that the transresistance gain (R_m) approaches infinity. However, in reality, R_m has a finite value and it is frequency dependent. Considering a single-pole model for the transresistance gain, R_m is expressed by;

$$R_{\text{m}} = \frac{R_{\text{mo}}}{1 + \dfrac{j\omega}{\omega_{\text{o}}}} \tag{4.35}$$

4.2.2.2. Parasitic Input Resistances and Capacitances. Since the input nodes are internally grounded in an OTRA, effects of these resistances and capacitances are negligible. However, for a good model of the OTRA, these effects should be included in the model. The following circuit can be used to model an OTRA with its parasitic resistances and capacitances.

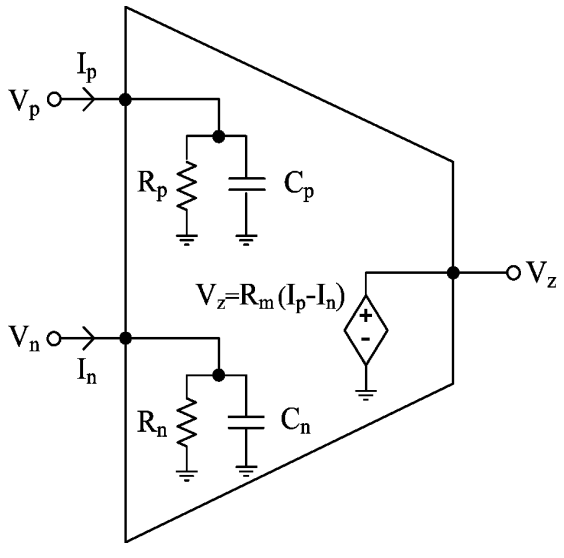

Figure 4.62. OTRA with parasitic input impedances

An OTRA with parasitics is shown in Figure 4.62. Voltages at input terminals are given as;

$$V_{\mathrm{p}} = I_{\mathrm{p}} / \left(G_{\mathrm{p}} + sC_{\mathrm{p}}\right)$$
$$V_{\mathrm{n}} = I_{\mathrm{n}} / \left(G_{\mathrm{n}} + sC_{\mathrm{n}}\right) \tag{4.36}$$

4.2.2.3. Tracking Error. The output voltage of an OTRA can be expressed as;

$$V_{\mathrm{out}} = R_{\mathrm{m}} \left(I_{\mathrm{p}} - I_{\mathrm{n}}\right) \tag{4.37}$$

Due to some non-symmetry of the input nodes at the transistor level, the gains of the input currents can be different. This will cause the voltage to depend on one of the currents more than it depends on the other. For some constants α and β, V_{out} can be expressed as;

$$V_{\mathrm{out}} = R_{\mathrm{m}} \left(\alpha I_{\mathrm{p}} - \beta I_{\mathrm{n}}\right) \tag{4.38}$$

4.2.3. Proposed CMOS OTRA

A CMOS implementation of the OTRA is shown in Figure 4.63. Transistors M_1 to M_{12} form the current differencing stage and transistors M_{13} to M_{23} realize the second stage which is a voltage buffer. The proposed circuit is supplied by ±0.6 V. The bias voltage and bias currents are chosen as V_{B1}=0.4 V, I_{B1}=10 μA and I_{B2}=4 μA. Aspect ratios of the transistors are reported in Table 4.8.

Performance of the proposed OTRA is verified with HSPICE. It consumes less power than its counterparts that have been reported in the literature. Power dissipation is 345 μW. Frequency response of the transresistance gain is shown Figure 4.64. In practical applications, the effects of the finite gain must be considered especially at high frequencies where the gain of the OTRA is reduced considerably. The cut-off frequency of the CMOS OTRA is 6.78 MHz and gain-bandwidth product (GBP) is 578 MHz. Note that GBP of a 741 opamp is only 1 MHz.

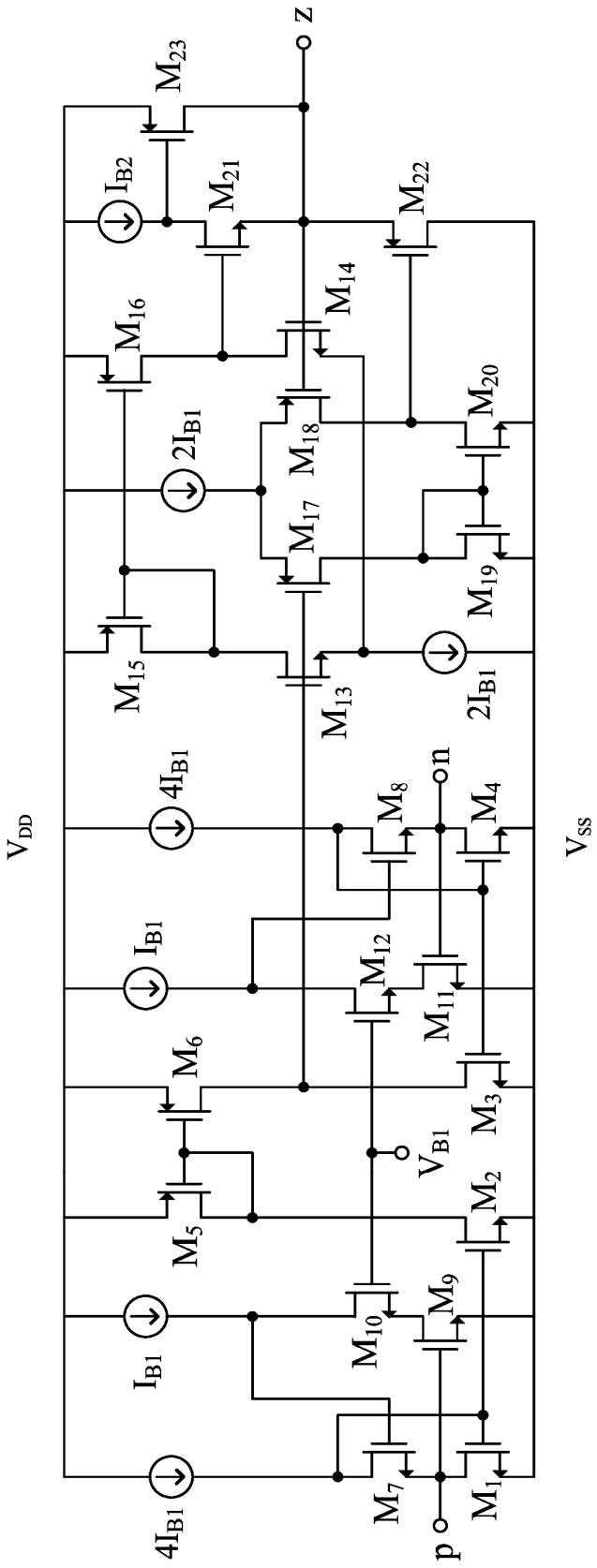

Figure 4.63. Proposed OTRA

Table 4.8. Aspect ratios

Transistor	**W/L [µm/µm]**
M_1, M_2, M_3, M_4	3.6/0.90
M_5, M_6	90/0.90
M_7, M_8	63/0.90
M_9, M_{11}	4.5/0.90
M_{10}, M_{12}	9/0.90
M_{13}, M_{14}	4.5/0.36
M_{15}	36/0.90
M_{16}	52/0.90
M_{17}, M_{18}	27/0.36
M_{19}, M_{20}	6.3/0.36
M_{21}	90/1.80
M_{22}	90/0.36
M_{23}	54/1.80

The proposed OTRA is capable of working efficiently even at much higher frequencies. The gain of the designed OTRA at 100 MHz is around 75 dB which is more than a gain of 5000.

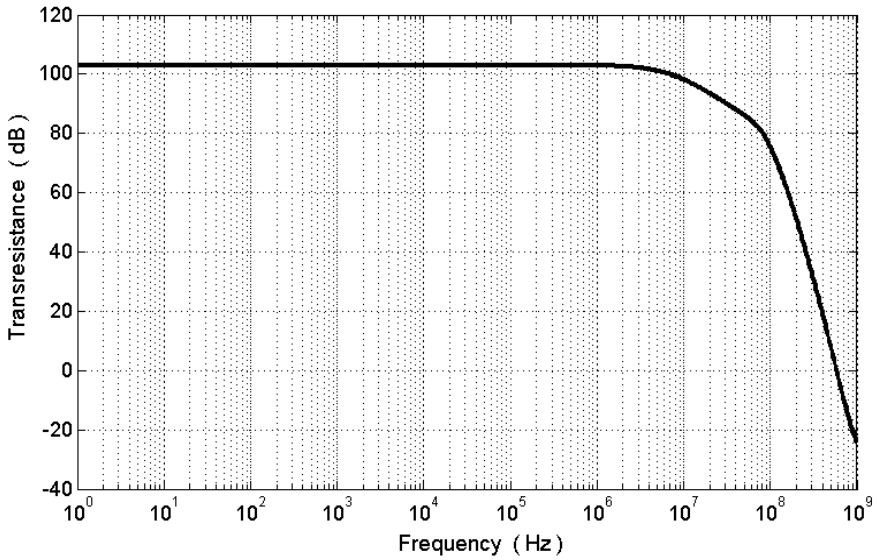

Figure 4.64. Open-loop transresistance gain

The typical DC simulation result is shown in Figure 4.65. Maximum and minimum output voltages are +0.49 V and –0.52 V, respectively.

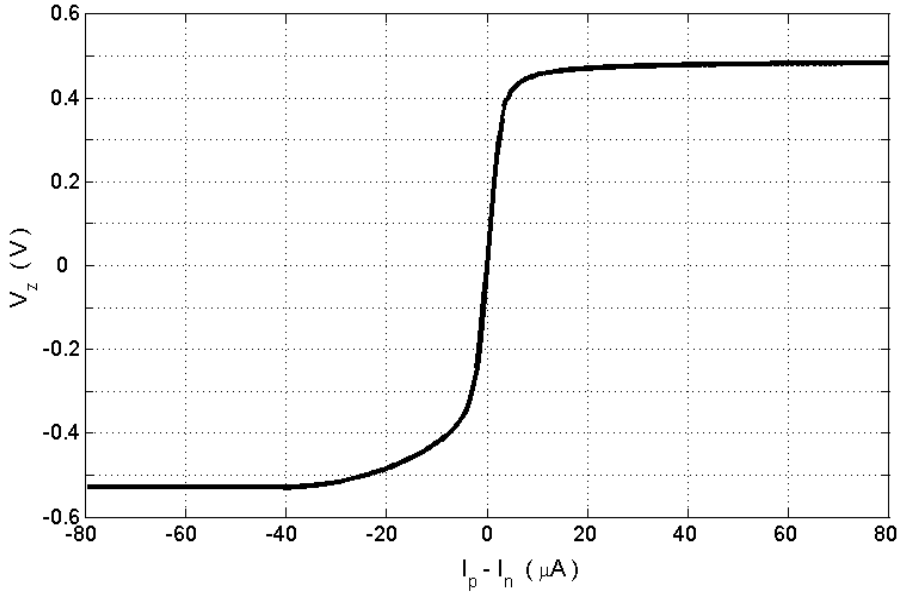

Figure 4.65. Typical DC simulation result of the OTRA

The current differencing circuit is formed by the transistors M_1 to M_{12}. It is based on the flipped voltage follower current sources (FVFCS). With a feedback circuitry to the topology, resistances at terminal-p and terminal-n have been further reduced. For this circuit, resistances at the input terminals can be formulated as follows;

$$R_{\mathrm{p}} \cong \frac{2}{A_{\mathrm{v}} g_{\mathrm{m1}} g_{\mathrm{m7}} r_{\mathrm{o7}}} \tag{4.39}$$

$$R_{\mathrm{n}} \cong \frac{2}{A_{\mathrm{v}} g_{\mathrm{m4}} g_{\mathrm{m8}} r_{\mathrm{o8}}} \tag{4.40}$$

Frequency response of the input terminal impedances is given in Figure 4.66. It turns out that impedances at terminal-p and terminal-n are the same and equal to 2.95 Ω at frequencies up to 1 MHz. In addition to that, the proposed OTRA offers very low output resistance which can be written as;

$$R_{\mathrm{z}} = \frac{1}{g_{\mathrm{m21}} g_{\mathrm{m23}} r_{\mathrm{o}} \left(1 + g_{\mathrm{m14}} \frac{r_{\mathrm{o}}}{2}\right)} // \frac{1}{g_{\mathrm{m22}} \left(1 + g_{\mathrm{m18}} \frac{r_{\mathrm{o}}}{2}\right)} \tag{4.41}$$

Figure 4.67 shows the output impedance variation of the proposed OTRA. Terminal-z impedance is equal to 14.8 Ω at frequencies up to 1 MHz.

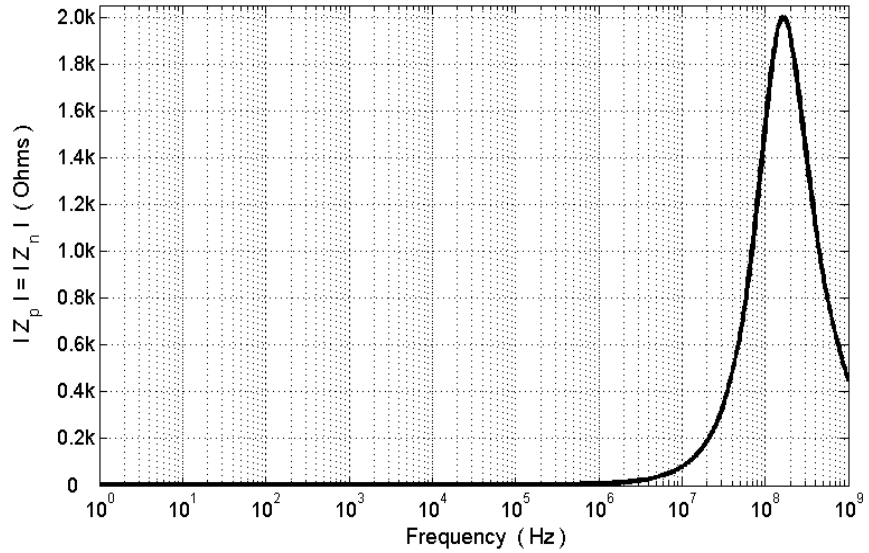

Figure 4.66. Frequency variation of terminal-p and terminal-n impedance magnitudes

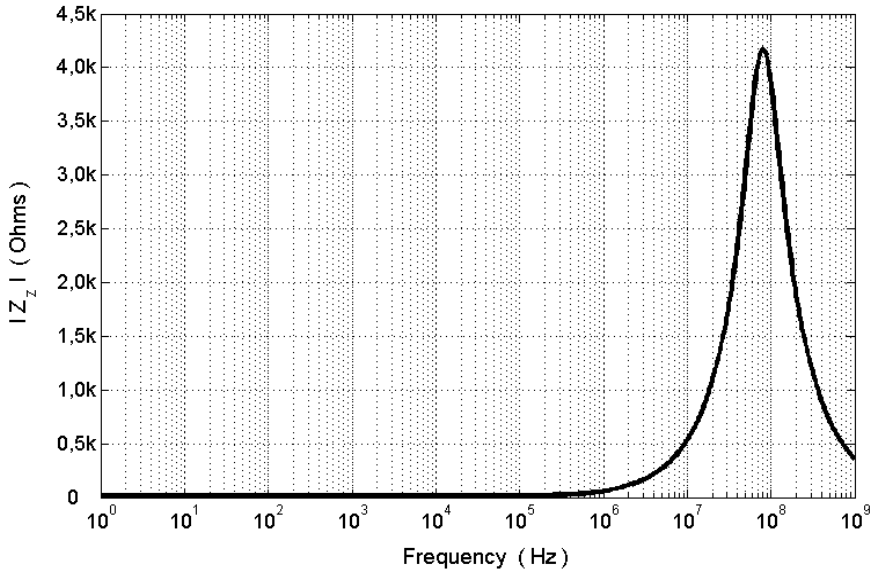

Figure 4.67. Frequency variation of terminal-z impedance magnitude

Summary of the OTRA performance is shown in Table 4.9 from which it can be observed that supply voltages are chosen as ±0.6 V. This OTRA has low power consumption and it provides high output voltage swing values.

Table 4.9. Performance of the proposed OTRA

Simulation Results	
Power supply	±0.6 V
Bias voltage, V_{B1}	0.4 V
Bias current, I_{B1}	10 μA
Bias current, I_{B2}	4 μA
Power dissipation	345 μW
Maximum output voltage	+0.49 V
Minimum output voltage	−0.52 V
Terminal-p resistance	2.95 Ω
Terminal-n resistance	2.95 Ω
Terminal-z resistance	14.8 Ω
Transresistance gain	103 dB
Cut-off frequency	6.78 MHz
Unity-gain bandwidth	578 MHz
Offset current at terminal-z	0.06 μA

4.2.4. Design Example

As a design example, a multi-function filter configuration shown in Figure 4.68 is proposed. Voltage transfer functions can be obtained as follows;

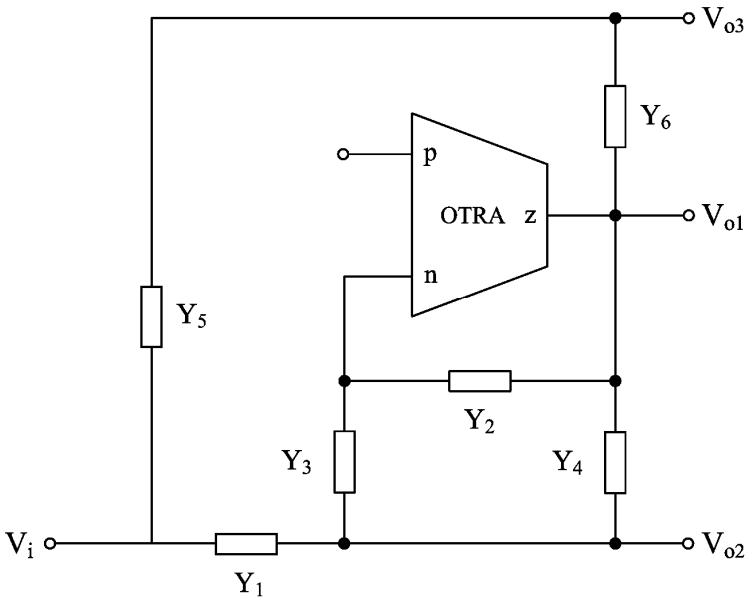

Figure 4.68. Multi-function filter configuration

$$\frac{V_{o1}}{V_i} = -\frac{Y_1 Y_3}{Y_1 Y_2 + Y_2 Y_3 + Y_2 Y_4 + Y_3 Y_4} \tag{4.42}$$

$$\frac{V_{o2}}{V_i} = \frac{Y_1 Y_2}{Y_1 Y_2 + Y_2 Y_3 + Y_2 Y_4 + Y_3 Y_4} \tag{4.43}$$

$$\frac{V_{o3}}{V_i} = \frac{Y_1 Y_2 Y_5 + Y_2 Y_3 Y_5 + Y_2 Y_4 Y_5 + Y_3 Y_4 Y_5 - Y_1 Y_3 Y_6}{(Y_1 Y_2 + Y_2 Y_3 + Y_2 Y_4 + Y_3 Y_4)(Y_5 + Y_6)} \tag{4.44}$$

These transfer functions allow us to realize two kinds of filters for the proposed configuration by choosing the admittances appropriately.

4.2.4.1. Realization-I. For $Y_1 = sC_1$, $Y_2 = sC_2$, $Y_3 = G_1$, $Y_4 = G_2$ and $Y_5 = Y_6 = G_3$, the resulting circuit is shown in Figure 4.69. This configuration provides high-pass, band-pass and notch filter responses.

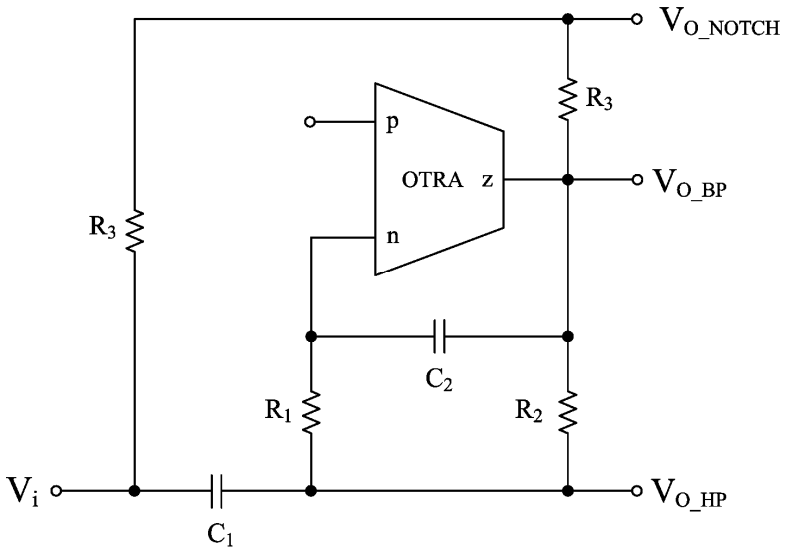

Figure 4.69. Realization-I

Transfer functions for the Realization-I are obtained as follows;

$$\frac{V_{o1}}{V_i} = \frac{V_{O\_BP}}{V_i} = -\frac{C_1 G_1 s}{G_1 G_2 + (C_2 G_1 + C_2 G_2)s + C_1 C_2 s^2} \tag{4.45}$$

$$\frac{V_{o2}}{V_i} = \frac{V_{O\_HP}}{V_i} = \frac{C_1 C_2 s^2}{G_1 G_2 + (C_2 G_1 + C_2 G_2)s + C_1 C_2 s^2} \tag{4.46}$$

$$\frac{V_{o3}}{V_i} = \frac{V_{O\_NOTCH}}{V_i} = \frac{1}{2}\frac{G_1 G_2 + (C_2 G_1 + C_2 G_2 - C_1 G_1)s + C_1 C_2 s^2}{G_1 G_2 + (C_2 G_1 + C_2 G_2)s + C_1 C_2 s^2} \tag{4.47}$$

The angular resonant frequency (ω_o) and quality factor (Q) for the three responses can be expressed as;

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \tag{4.48}$$

$$Q = \sqrt{\frac{C_1}{C_2}}\frac{\sqrt{G_1 G_2}}{(G_1 + G_2)} \tag{4.49}$$

Sensitivity of Q to the four passive elements is given as follows;

$$S_{C_1}^{Q} = -S_{C_2}^{Q} = 0.5$$

$$S_{G_1}^{Q} = -S_{G_2}^{Q} = -0.5\frac{G_1 - G_2}{G_1 + G_2} \tag{4.50}$$

Sensitivity of ω_o to the four passive elements is given as follows;

$$S_{G_1}^{\omega_o} = S_{G_2}^{\omega_o} = 0.5$$

$$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -0.5 \tag{4.51}$$

Frequency response of the proposed multi-function filter is shown in Figure 4.70. Passive elements are chosen as R_1=R_2=1 kΩ, R_3=R_4=10 kΩ, C_1=0.2 nF and C_2=0.1 nF, which results in a cut-off (center) frequency of 1.12 MHz.

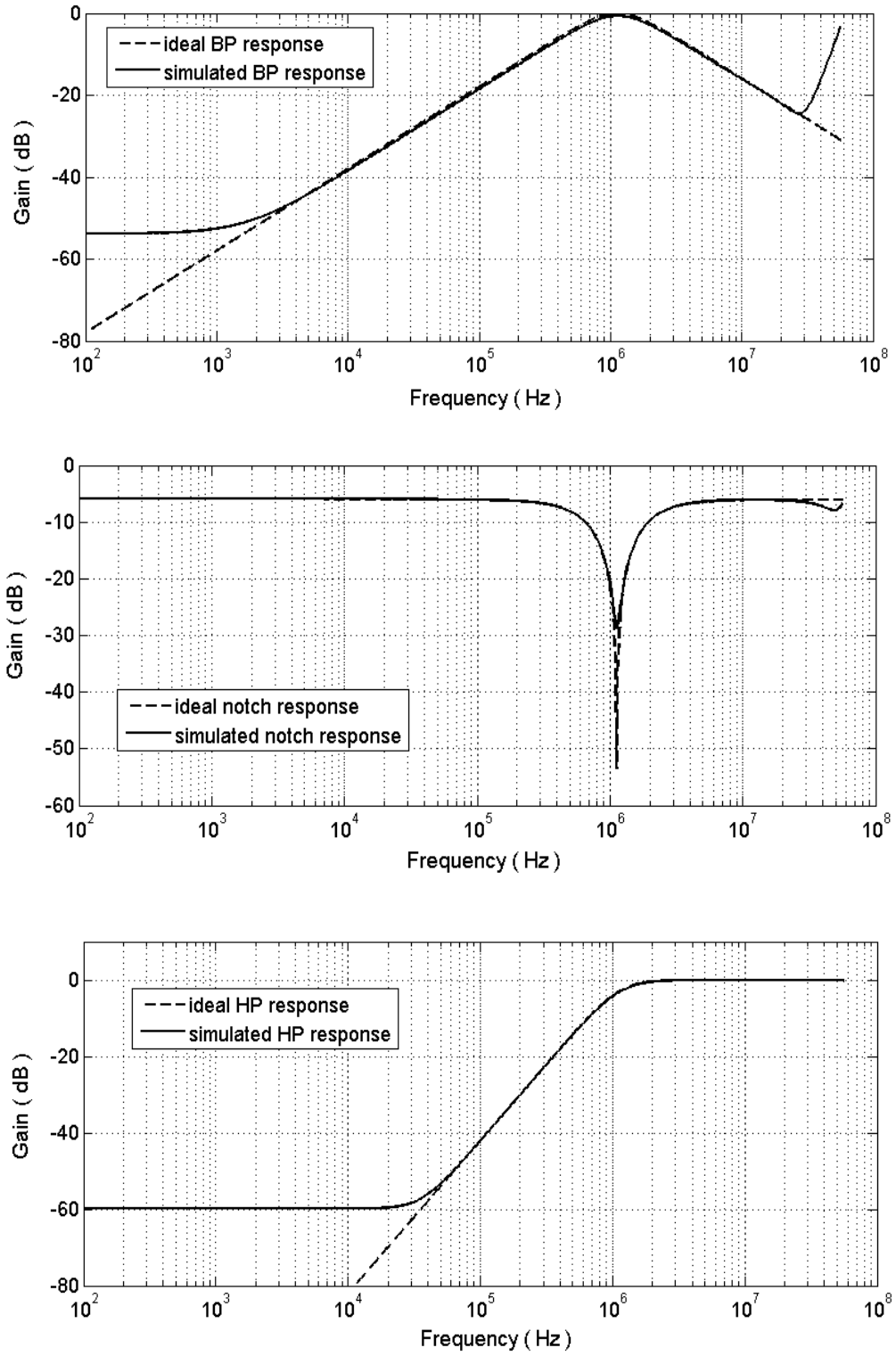

Figure 4.70. Frequency response of the proposed multi-function filter

4.2.4.2. Realization-II. For $Y_1 = G_1$, $Y_2 = G_2$, $Y_3 = sC_1$, $Y_4 = sC_2$ and $Y_5 = Y_6 = G_3$, the circuit shown in Figure 4.71 provides low-pass, band-pass and notch filter responses.

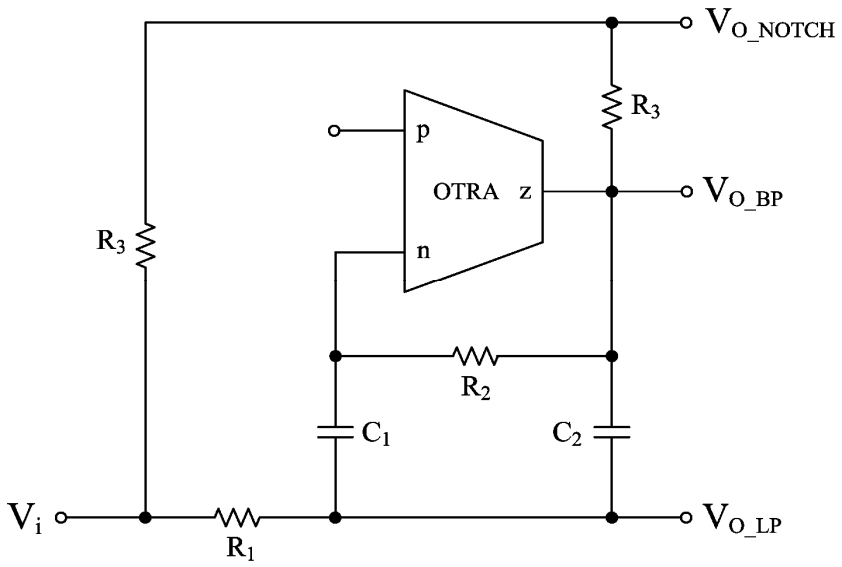

Figure 4.71. Realization-II

Transfer functions for the Realization-II are given by;

$$\frac{V_{o1}}{V_i} = \frac{V_{O\_BP}}{V_i} = -\frac{C_1 G_1 s}{G_1 G_2 + (C_1 G_2 + C_2 G_2)s + C_1 C_2 s^2} \tag{4.52}$$

$$\frac{V_{o2}}{V_i} = \frac{V_{O\_LP}}{V_i} = \frac{G_1 G_2}{G_1 G_2 + (C_1 G_2 + C_2 G_2)s + C_1 C_2 s^2} \tag{4.53}$$

$$\frac{V_{o3}}{V_i} = \frac{V_{O\_NOTCH}}{V_i} = \frac{1}{2}\frac{G_1 G_2 + (C_1 G_2 + C_2 G_2 - C_1 G_1)s + C_1 C_2 s^2}{G_1 G_2 + (C_1 G_2 + C_2 G_2)s + C_1 C_2 s^2} \tag{4.54}$$

The angular resonant frequency (ω_o) and quality factor (Q) for three filters can be expressed as;

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \tag{4.55}$$

$$Q = \sqrt{\frac{G_1}{G_2}}\frac{\sqrt{C_1 C_2}}{(C_1 + C_2)} \tag{4.56}$$

Frequency response of the proposed multi-function filter is illustrated in Figure 4.72. If component values are chosen as R_1=1 kΩ, R_2=2 kΩ, R_3= R_4=10 kΩ and C_1=C_2=0.1 nF, then the cut-off (center) frequency is found as 1.12 MHz.

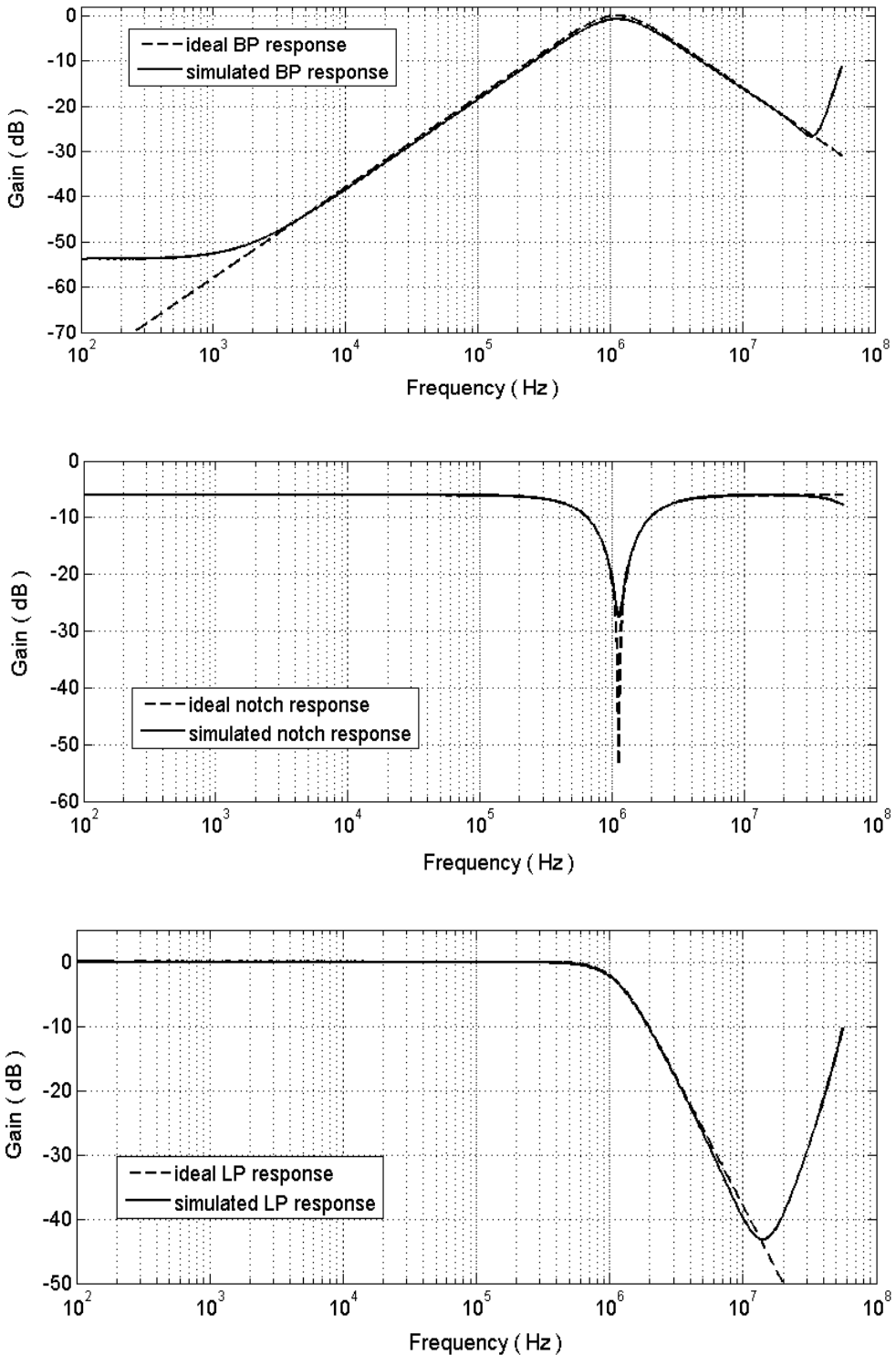

Figure 4.72. Frequency response of the proposed multi-function filter

Sensitivity of Q to the four passive elements is given as follows;

$$S_{G_1}^{Q} = -S_{G_2}^{Q} = 0.5$$

$$S_{C_1}^{Q} = -S_{C_2}^{Q} = -0.5\frac{C_1 - C_2}{C_1 + C_2} \tag{4.57}$$

Sensitivity of ω_o to the four passive elements is given as follows;

$$S_{G_1}^{\omega_o} = S_{G_2}^{\omega_o} = 0.5$$

$$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -0.5 \tag{4.58}$$

It is known that integration in frequency domain is simply multiplication of a function by s^{-1}. We also know that the three basic frequency responses namely band-pass, low-pass and high-pass filters differ only by their numerators. The numerator of the high-pass response is "as^2", that of the band-pass response is "bs" and the numerator of the low-pass response is "c". From these, we can see that the band-pass response is actually the integral of the high-pass response and the low-pass response is the integral of the band-pass response. Therefore, if we connect an integrator to the V_{O_BP} node of the circuit in Figure 4.69, we will obtain a low-pass filter response which is shown in Figure 4.73. Transfer function for the low-pass filter can be expressed as;

$$\frac{V_{O\_LP}}{V_i} = \frac{G_1 G_4 C_1}{C_3\left(G_1 G_2 + C_2 G_1 s + C_2 G_2 s + C_1 C_2 s^2\right)} \tag{4.59}$$

It is also known that differentiation in the frequency domain is simply multiplication by s. It is obvious that the band-pass response is actually the derivative of the low-pass response and the high-pass response is the derivative of the band-pass response. Therefore, with a differentiator connected to the V_{O_BP} node of the circuit in Figure 4.71, we will obtain a high-pass filter response. Figure 4.74 depicts the resulting circuit. Transfer function for the high-pass filter is given by;

$$\frac{V_{O\_HP}}{V_i} = \frac{C_1 C_3 G_1 s^2}{G_4\left(G_1 G_2 + C_1 G_2 s + C_2 G_2 s + C_1 C_2 s^2\right)} \tag{4.60}$$

Specifications of the proposed filter configuration including the matching condition, gain, cut-off frequency and quality factor are given in Table 4.10.

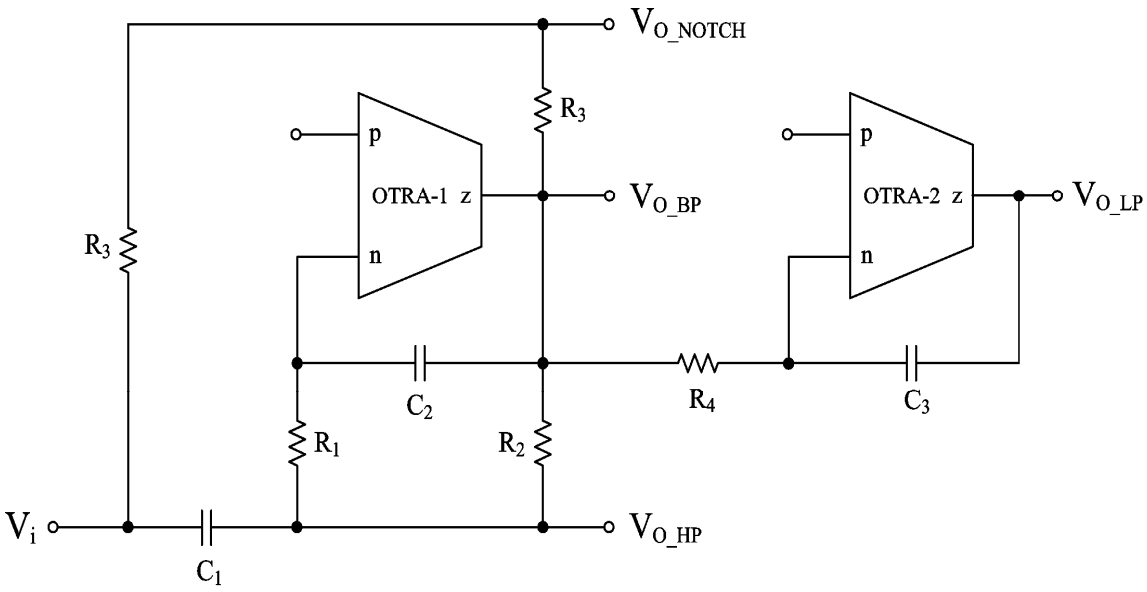

Figure 4.73. Realization-I with a low-pass filter response

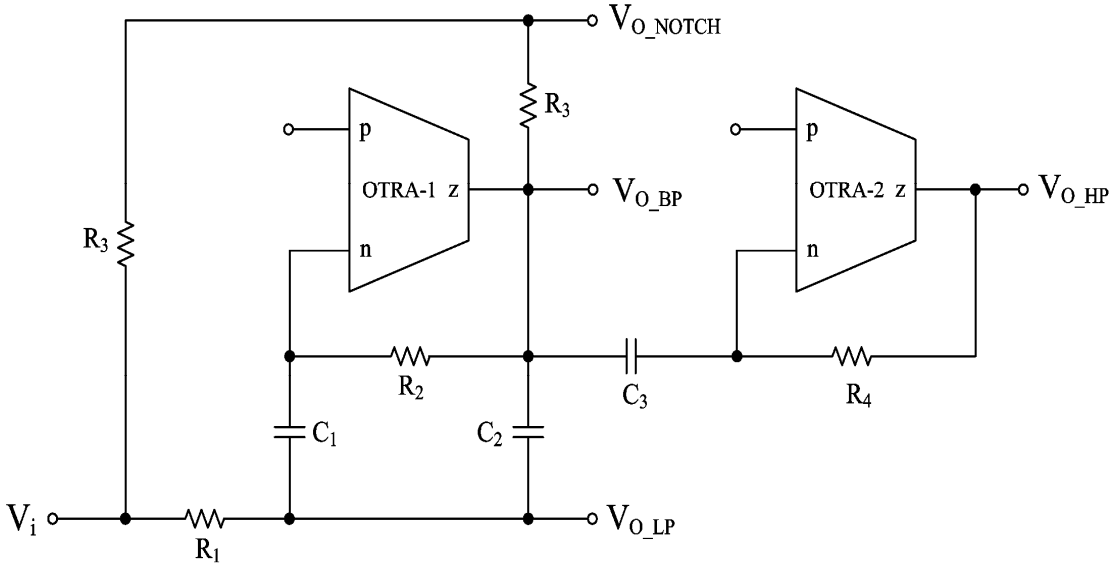

Figure 4.74. Realization-II with a high-pass filter response

Table 4.10. Specifications of the proposed filter configuration

Realization	Matching condition	Filter type	Gain	Cut-off frequency	Quality factor
I	$C_1=2C_2$, $G_1=G_2$,	Band-pass	1	$\frac{G_1}{\sqrt{2}C_2}$	$\frac{\sqrt{2}}{2}$
		High-pass	1	$\frac{G_1}{\sqrt{2}C_2}$	$\frac{\sqrt{2}}{2}$
		Notch	$\frac{1}{2}$	$\frac{G_1}{\sqrt{2}C_2}$	$\frac{\sqrt{2}}{2}$
II	$G_1=2G_2$, $C_1=C_2$,	Band-pass	1	$\frac{G_1}{\sqrt{2}C_1}$	$\frac{\sqrt{2}}{2}$
		Low-pass	1	$\frac{G_1}{\sqrt{2}C_1}$	$\frac{\sqrt{2}}{2}$
		Notch	$\frac{1}{2}$	$\frac{G_1}{\sqrt{2}C_1}$	$\frac{\sqrt{2}}{2}$

4.2.5. Noise Performance of the Proposed OTRA

Noise contributions of the proposed OTRA mainly come from two sources. The first source is the current subtractor circuit and the second source is the voltage buffer. Simulation results for the input-referred noise currents at input terminals are shown in Figure 4.75. From the simulation results in Figure 4.75, the lowest input noise current is 6.2 pA/√Hz.

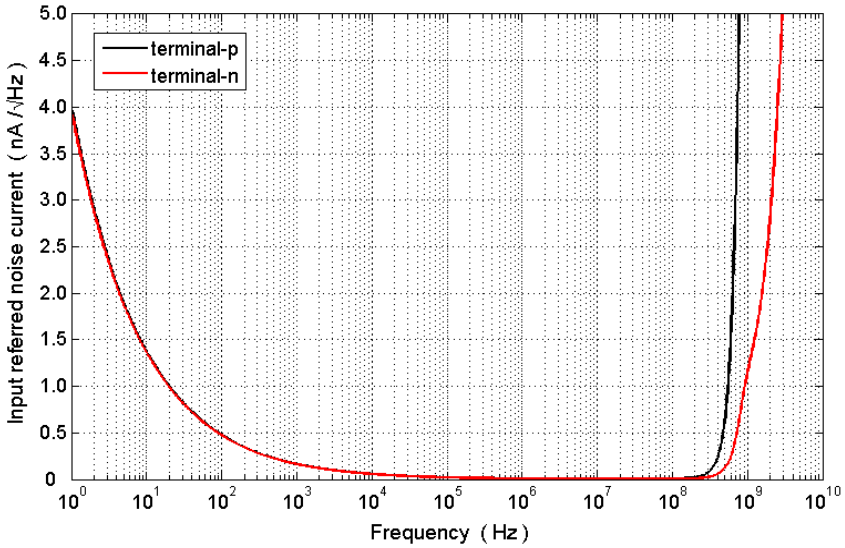

Figure 4.75. Noise currents at input terminals

4.2.6. Summary

In this section, a new low-voltage, low-power and high-swing CMOS operational transresistance amplifier (OTRA) circuit is proposed. From the performance comparison in Table 4.11, it is clear that the proposed OTRA can swing from the positive supply rail to the negative one. Also, it has the lowest power consumption which is 345 μW. Finally, as an application example, a multi-function filter configuration is proposed and the usefulness of the proposed OTRA is illustrated on this configuration.

Table 4.11. Comparison of OTRAs

Parameter	**[77]**	**[80]**	**[81]**	**Proposed OTRA**
Type	Single-ended	Single-ended	Differential	Single-ended
Power supply	±1.5 V	±1.5 V	±0.6 V	±0.6 V
Power dissipation	900 μW	600 μW	11.88 mW	345 μW
Output voltage swing	NA	NA	Rail to rail	(–0.52 V)-(+0.48 V)
Terminal-p resistance	15.5 Ω	4.2 Ω	51.8 Ω	2.95 Ω
Terminal-n resistance	15.5 Ω	4.2 Ω	51.8 Ω	2.95 Ω
Terminal-z resistance	NA	NA	1.45 Ω	14.8 Ω
Transresistance gain	80 dB	162 dB	91,74 dB	103 dB

4.3. Current Differencing Transconductance Amplifier (CDTA)

Recently, a new active element named current differencing transconductance amplifier (CDTA) has been proposed [87] and some applications have also been presented. A CDTA element with two current inputs and two current outputs enables an easy implementation of multiple-input current integrators. It also exhibits the ability of tuning by the help of the transconductance parameter. All these advantages together with the advantages of current-mode operation make the CDTA a promising building block of current-mode filters. The defining equations of the CDTA are given in (4.61). The general structure of the CDTA is given in Figure 4.76.

$$\begin{bmatrix} V_{\mathrm{p}} \\ V_{\mathrm{n}} \\ I_{\mathrm{z}} \\ I_{\mathrm{x+}} \\ I_{\mathrm{x-}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & k_1 g_{\mathrm{m}} & 0 & 0 \\ 0 & 0 & k_2 g_{\mathrm{m}} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{\mathrm{p}} \\ I_{\mathrm{n}} \\ V_{\mathrm{z}} \\ V_{\mathrm{x+}} \\ V_{\mathrm{x-}} \end{bmatrix} \tag{4.61}$$

where,

$k_1 = k_2 = 1$ for the CDTA++

$k_1 = 1$ and $k_2 = -1$ for the CDTA +– and

$k_1 = k_2 = -1$ for the CDTA––

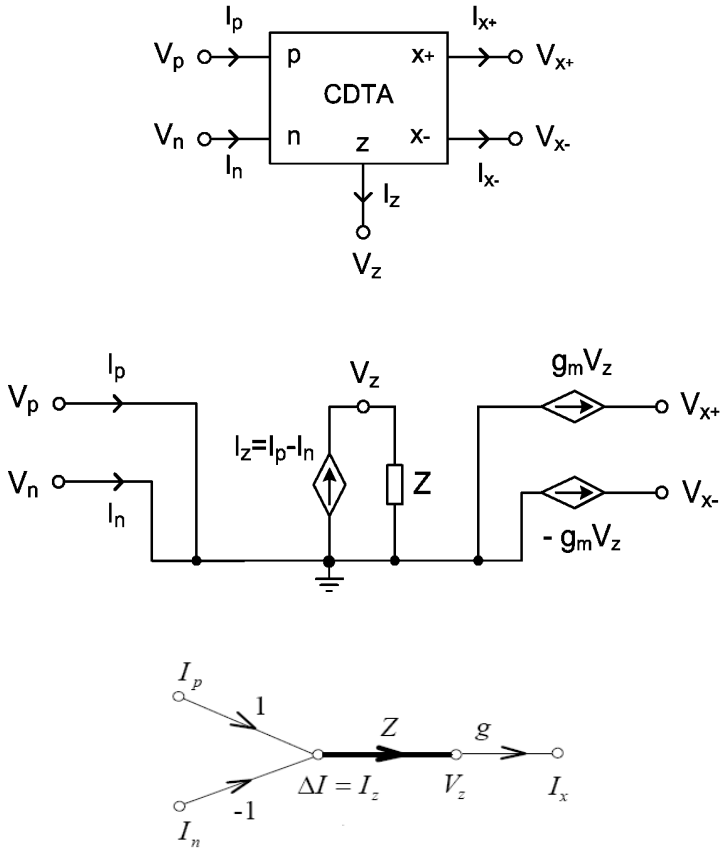

Figure 4.76. Block diagram, equivalent circuit and "IVI" flow graph of the CDTA+–

The CDTA+– element shown in Figure 4.76 has a pair of low-impedance current inputs (p and n) and an auxiliary terminal-z whose outgoing current is the difference of input currents. Here output terminal currents are equal in magnitude, but they flow in opposite directions and the product of the transconductance (g_m) and voltage at terminal-z

gives their magnitudes. Therefore, this active element can be characterized by the following equations;

$$V_p = V_n = 0,\ I_z = I_p - I_n,\ I_{x+} = g_m V_z,\ I_{x-} = -g_m V_z \tag{4.62}$$

where $V_z = I_z Z_z$ and Z_z is the external impedance connected to terminal-z of the CDTA+–. The main advantage of the CDTA is the transconductance parameter which provides electronic tunability in filter applications. A second benefit is the availability of two current outputs which enable the current to be used in feedback loops.

A CDTA+– can be thought of as a combination of a current differencing unit followed by a dual-output operational transconductance amplifier (DO-OTA). Ideally, the OTA is assumed as an ideal voltage-controlled current source and can be described by $I_x=g_m(V_+–V_-)$ where I_x is the output current and V_+ and V_- denote the non-inverting and the inverting input voltage of the OTA, respectively. Note that g_m is a function of the bias current. When this element is used in the CDTA+–, one of its input terminals is grounded (e.g., $V_- = 0$ V). With dual-output availability, $I_{x+} = –I_{x-}$ condition is assumed. The part of the CDTA+– that takes the difference current of the input terminals is the same as the input part of the current differencing buffered amplifier (CDBA). Instead of using a voltage buffer which is the case in the CDBA, a DO-OTA is employed in terminal-z. Realization of the CDTA+– with commercially available ICs is given in Figure 4.77.

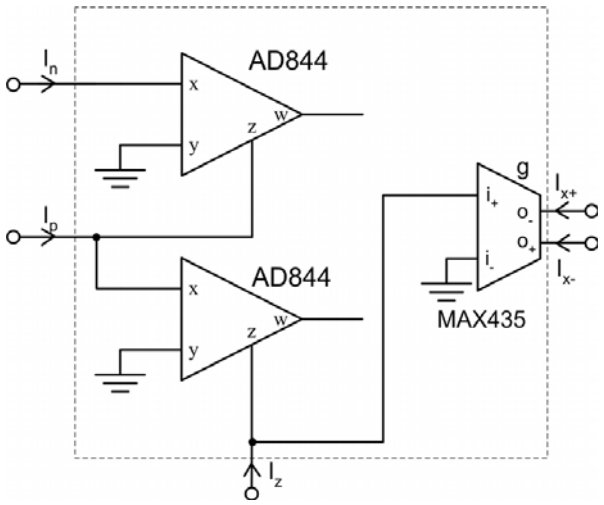

Figure 4.77. CDTA+– implementation with CDBAs and an OTA

4.3.1. CMOS Realization of the CDTA+–

A novel CMOS current differencing transconductance amplifier (CDTA+–) which is suitable for low-voltage operation is presented in this section. The proposed circuit given in Figure 4.78 operates with the power supplies of ±0.6 V and consumes approximately 320 µW power. UMC 0.18 µm CMOS technology is used for the simulations. Performance of the CDTA+– is verified with HSPICE. Simulation results show that the proposed CDTA+– has the terminal resistances of R_p=R_n=2.95 Ω, R_z=218 kΩ and R_x=523 kΩ. Aspect ratios of the transistors are reported in Table 4.12.

Table 4.12. Aspect ratios

Transistor	W/L [µm/µm]
M_1, M_2, M_3, M_4	3.6/0.90
M_5, M_6	90/0.90
M_7, M_8, M_9, M_{10}	70/0.90
M_{11}, M_{13}	4.5/0.90
M_{12}, M_{14}	9/0.90
M_{15}, M_{17}, M_{19}, M_{21}	16.2/0.72
M_{16}, M_{18}, M_{20}, M_{22}	3.6/2.1

The current subtractor circuit is formed by the transistors M_1 to M_{14}. Input terminal impedances can be calculated with the following formulas;

$$R_{\mathrm{p}} \cong \frac{2}{A_{\mathrm{v}} g_{\mathrm{m1}} g_{\mathrm{m5}} r_{\mathrm{o5}}} \tag{4.63}$$

$$R_{\mathrm{n}} \cong \frac{2}{A_{\mathrm{v}} g_{\mathrm{m4}} g_{\mathrm{m6}} r_{\mathrm{o6}}} \tag{4.64}$$

Figure 4.79 shows input terminal impedance magnitudes of the proposed CDTA+–. Impedances at terminal-p and terminal-n are equal to 2.95 Ω for a wide frequency range. Figure 4.80 and Figure 4.81 illustrate terminal-z and terminal-x+ impedance magnitudes which are 218 kΩ and 523 kΩ, respectively.

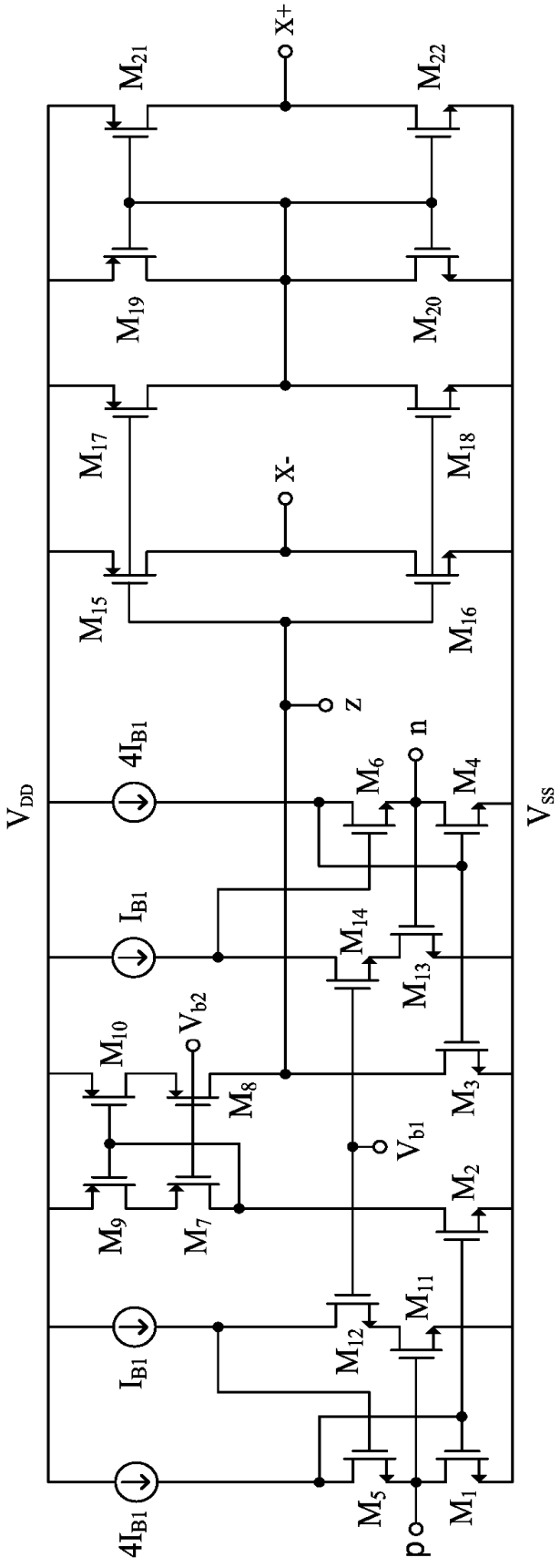

Figure 4.78. Proposed CDTA+–

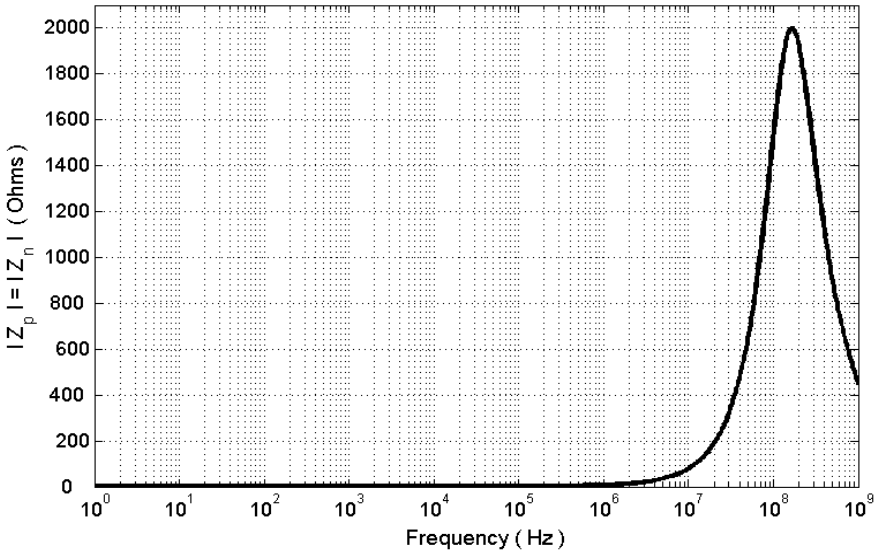

Figure 4.79. Frequency variation of terminal-p and terminal-n impedance magnitudes

The output stage of the CDTA+– consists of inverters that are used for analog signal processing. The negative output is taken at the output of the first inverter and using another inverter signal is mirrored at the input of the third inverter which is connected in a unity gain topology. The last one inverts the negative signal and produces the positive output current [98].

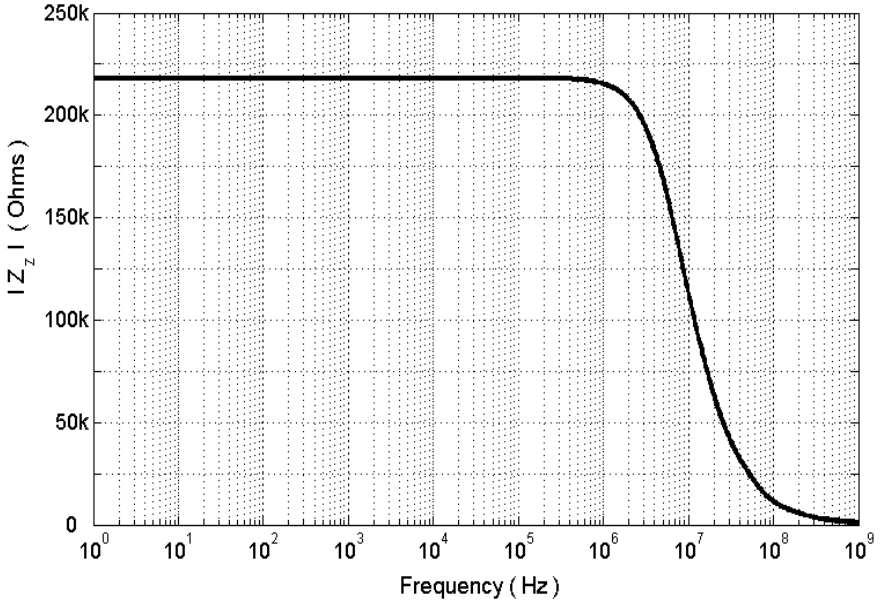

Figure 4.80. Frequency variation of terminal-z impedance magnitude

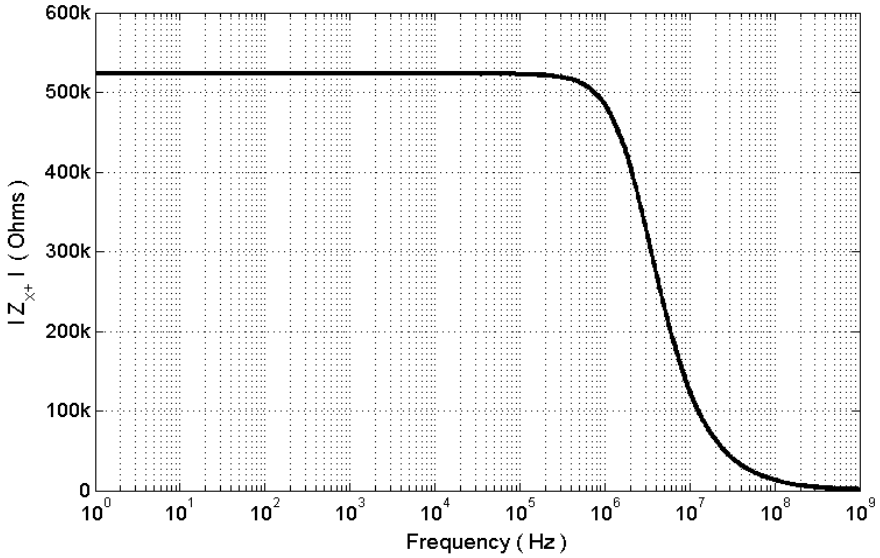

Figure 4.81. Frequency variation of terminal-x+ impedance magnitude

Figure 4.82 displays the DC current transfer characteristic of the proposed CDTA+–. It can easily be seen that this CDTA+– is linear for the current values (I_p–I_n) between –40 μA and +60 μA. Also, the offset current at terminal-z is 0.06 μA.

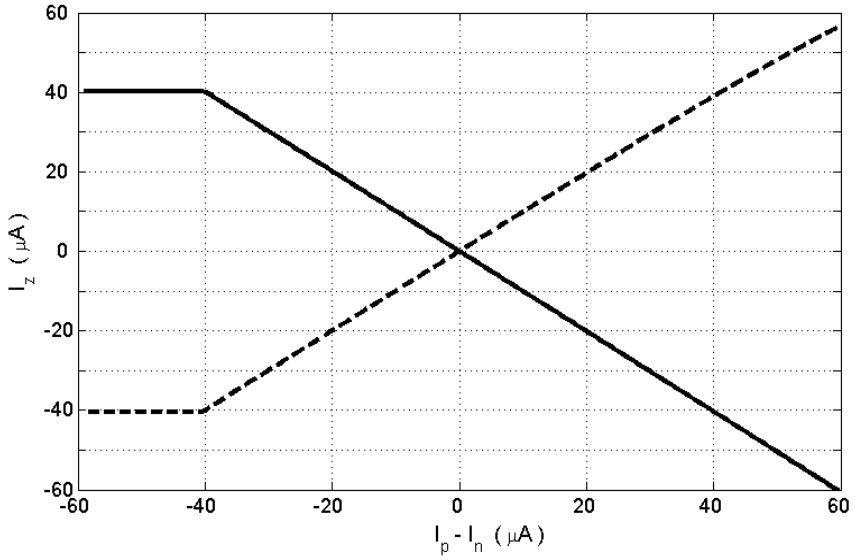

Figure 4.82. DC current transfer characteristic

The –3dB cut-off frequencies of the current transfer ratios are shown in Figure 4.83. Cut-off frequencies of i_z/i_p and i_z/i_n are located at 93 MHz and 152 MHz, respectively.

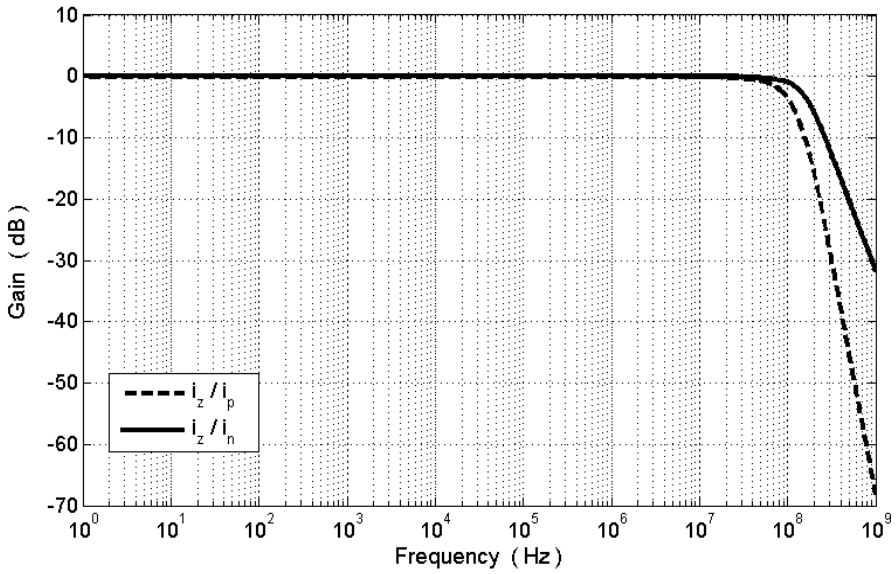

Figure 4.83. Frequency response of the current transfer ratios

Transconductance is a very important feature of the CDTA+– because it directly affects circuit equations. Transconductances of both positive and negative outputs are given in Figure 4.84. Thanks to the simple topology of the output transconductors, transconductance of the CDTA+– has large bandwidth which makes it suitable for high frequency operation.

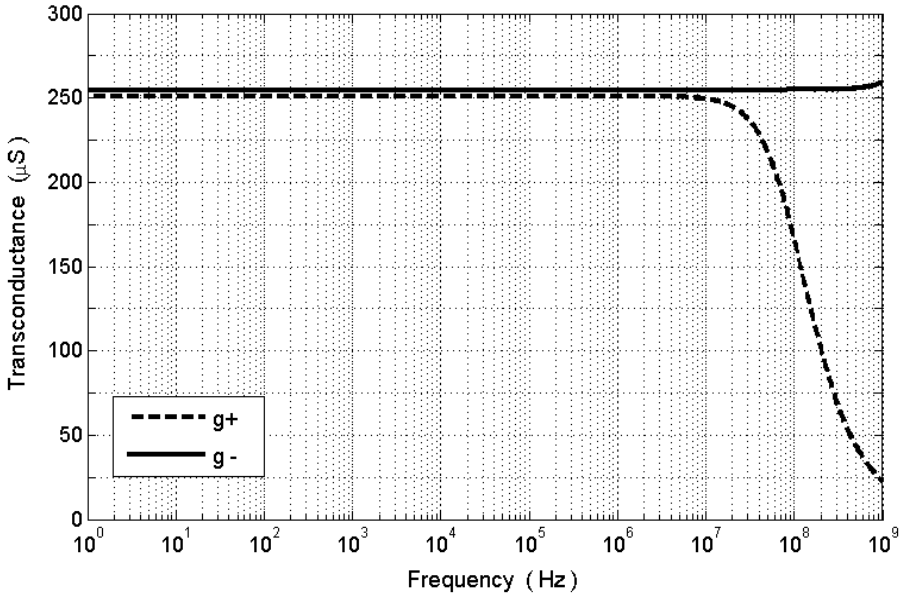

Figure 4.84. Transconductances of the CDTA+–

To illustrate the effects of parameter variations on the proposed circuit, Monte-Carlo simulations are performed. W, L and V_{T0} parameters of each transistor are varied by using values supplied by UMC. Simulation results are given in Figure 4.85 and Figure 4.86. Variations on the negative and positive transconductances are 5.4% and 5.5%, respectively. In Table 4.13, summary of HSPICE simulation results is shown in a tabular format.

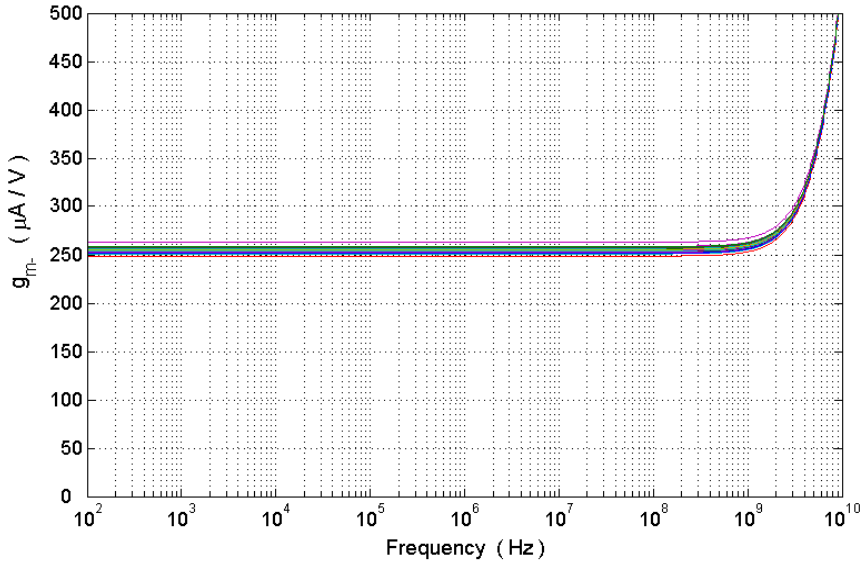

Figure 4.85. Monte-Carlo analysis of the negative transconductance

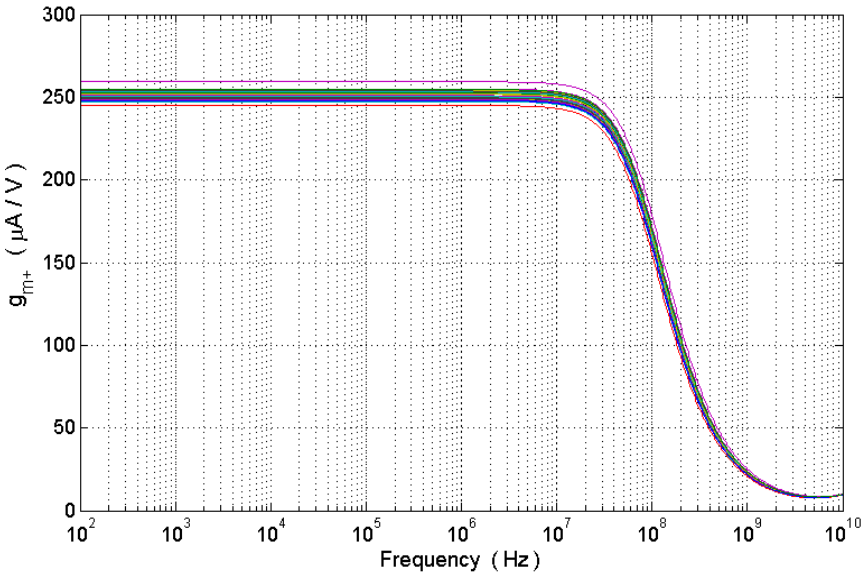

Figure 4.86. Monte-Carlo analysis of the positive transconductance

Table 4.13. Performance of the proposed CDTA+–

Simulation Results	
Power supply	±0.6 V
Bias voltage, V_{B1}	+0.4 V
Bias voltage, V_{B2}	–0.2 V
Bias current, I_{B1}	10 µA
Power dissipation	320 µW
Current transfer BW of I_z / I_p	93 MHz
Current transfer BW of I_z / I_n	152 MHz
Terminal-p and n resistances	2.95 Ω
Terminal-z resistance	218 kΩ
Terminal-x resistance	523 kΩ
Transconductance	251 µA/V
Input current linear range	(–40 µA)-(+40 µA)
Offset current at terminal-z	0.06 µA

4.3.1.1. Design Example. All-pass filters have application areas from delay equalization in anti-aliasing filters to quadrature oscillators. In this section, a first-order all-pass filter employing a single CDTA+– element is chosen from the literature [89]. The general all-pass filter configuration is shown in Figure 4.87.

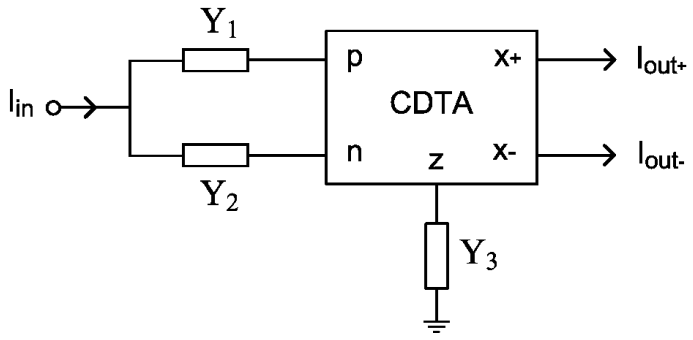

Figure 4.87. General all-pass filter configuration

Transfer function of the chosen configuration can be written as follows;

$$\frac{I_{\text{out}-}}{I_{\text{in}}} \cong \left(\frac{g_{\text{m}}}{Y_3}\right)\left(\frac{Y_2 - Y_1}{Y_1 + Y_2}\right) \tag{4.65}$$

where g_m is the transconductance parameter of the CDTA+– element. Choosing $Y_1=sC_1$, $Y_2=G_2$ and $Y_3=G_3$, the transfer function in (4.65) becomes a first-order all-pass response where g_m / Y_3 is the DC gain and it can be adjusted to 1 for the all-pass topology.

$$\frac{I_{\text{out}-}}{I_{\text{in}}} \cong \frac{1 - sC_1R_2}{1 + sC_1R_2} \tag{4.66}$$

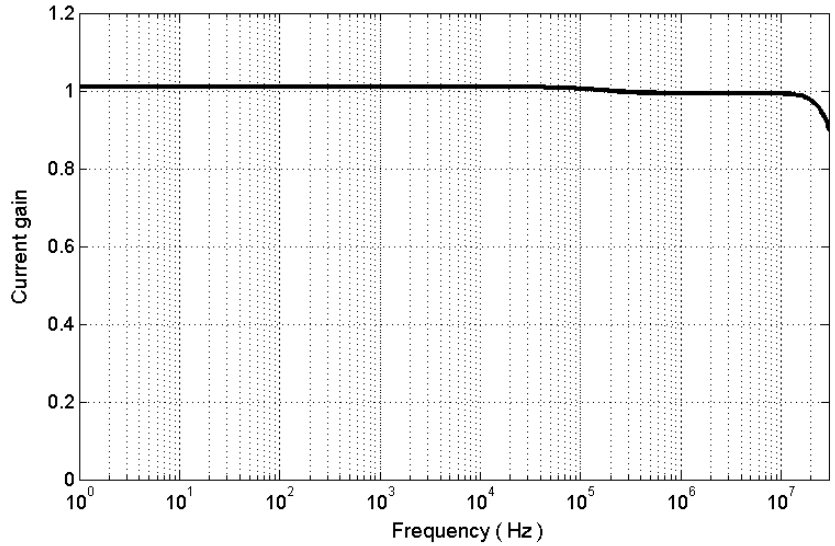

Figure 4.88. All-pass filter magnitude response

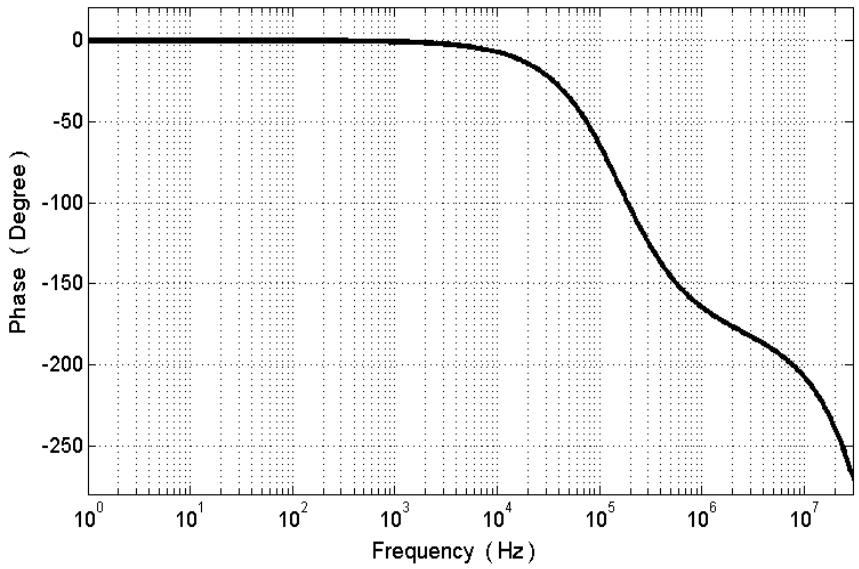

Figure 4.89. All-pass filter phase response

This first-order all-pass filter topology is also able to give an inverted output and requires only three passive elements, which is an improvement over its voltage-mode OTRA counterpart [99]. Simulation results of the all-pass filter employing the proposed low-voltage CDTA+– are shown in Figure 4.88 and Figure 4.89 where passive components are chosen as R_1=1 kΩ, R_3=4.2 kΩ and C_2=1 nF.

4.3.2. CMOS Realization of the CDTA++

A novel CMOS current differencing transconductance amplifier (CDTA++) suitable for low-voltage and low-power applications is presented in this section. The proposed circuit shown in Figure 4.90 operates with the power supplies of ±0.6 V. Power dissipation of the circuit is 272 μW. Simulation results show that the proposed CDTA++ has the terminal resistances of R_p=R_n=4.2 Ω, R_z=219 kΩ and R_x=162 kΩ. Aspect ratios of the transistors are reported in Table 4.14.

Table 4.14. Aspect ratios

Transistor	W/L [μm/μm]
M_1, M_2	3.6/0.90
M_3, M_4	3.6/0.90
M_5, M_6	90/0.90
M_7, M_8	70/0.90
M_9, M_{10}	70/0.90
M_{11}, M_{13}	4.5/0.90
M_{12}, M_{14}	9/0.90
M_{15}, M_{16}	3.6/2.1
M_{17}, M_{18}	9/0.36
M_{19}, M_{20}	3.6/2.1
M_{21}, M_{22}	9/0.36

Figures 4.91 to 4.93 show terminal impedances of the CDTA++. Impedances at terminal-p and terminal-n are equal to 4.2 Ω for a wide frequency range. Terminal-z and terminal-x impedances are 219 kΩ and 162 kΩ, respectively.

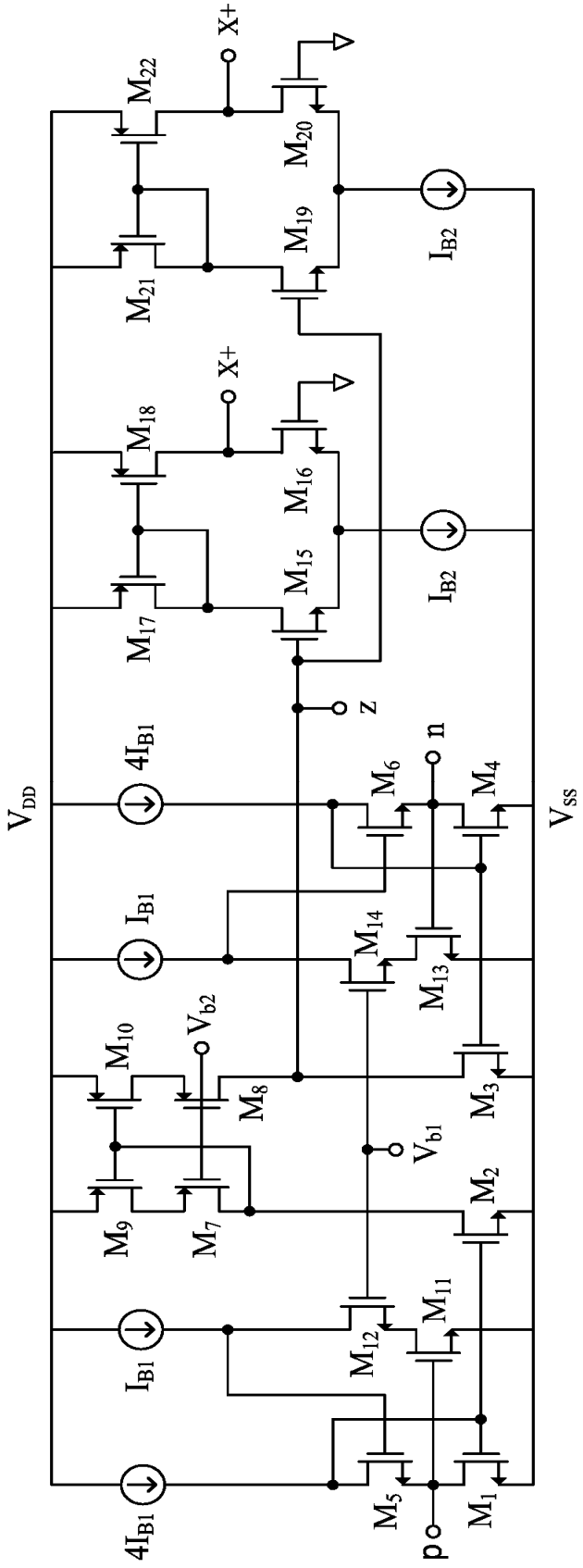

Figure 4.90. Proposed CDTA++

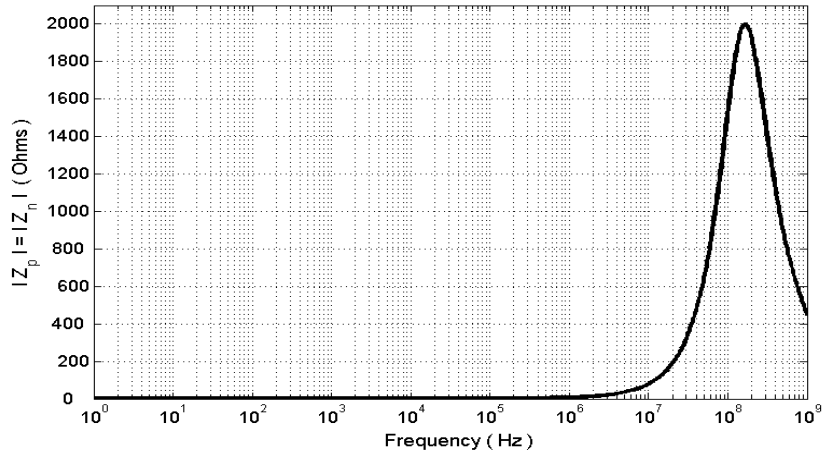

Figure 4.91. Frequency variation of terminal-p and terminal-n impedance magnitudes

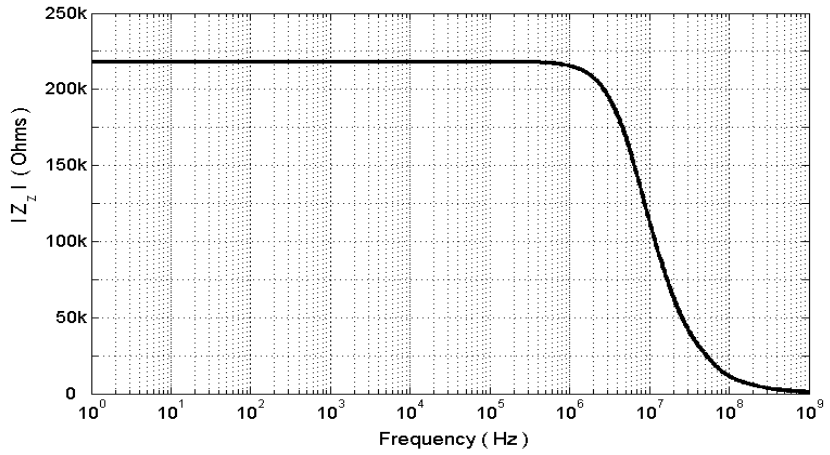

Figure 4.92. Frequency variation of terminal-z impedance magnitude

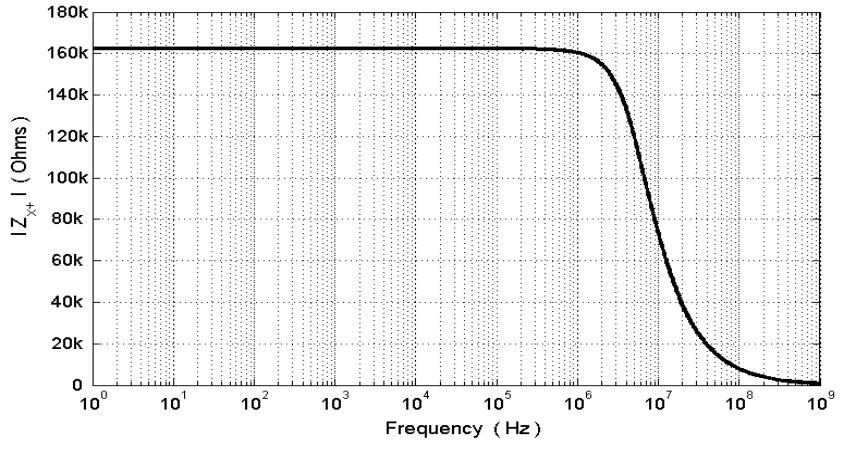

Figure 4.93. Frequency variation of terminal-x+ impedance magnitude

Figure 4.94 shows the transconductance of the proposed CDTA++ which is 40 µS at frequencies up to 50 MHz. Monte-Carlo analysis of the transconductance is illustrated in Figure 4.95. Variation on the transconductance is about 4%. In Table 4.15, summary of the simulation results is shown in a tabular format.

Table 4.15. Performance of the proposed CDTA++

Simulation Results	
Power supply	±0.6 V
Bias voltage, V_{B1}	+0.4 V
Bias voltage, V_{B2}	−0.2 V
Bias current, I_{B1}	10 µA
Power dissipation	272 µW
Current transfer BW of I_z / I_p	93 MHz
Current transfer BW of I_z / I_n	152 MHz
Terminal-p and n resistances	4.2 Ω
Terminal-z resistance	219 kΩ
Terminal-x resistance	162 kΩ
Transconductance	40 µA/V
Input current linear range	(−40 µA)-(+40 µA)
Offset current at terminal-z	0.06 µA

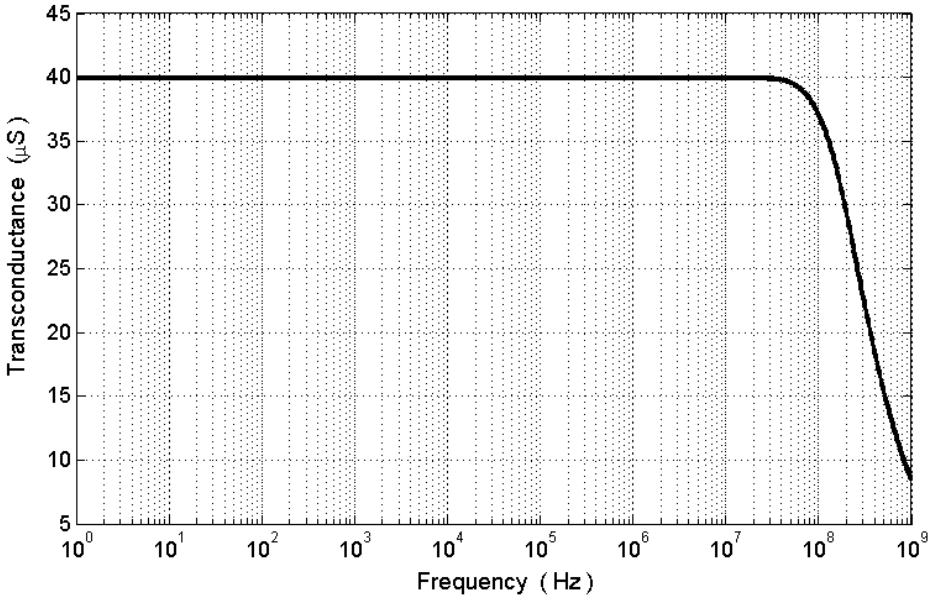

Figure 4.94. Transconductance of the CDTA++

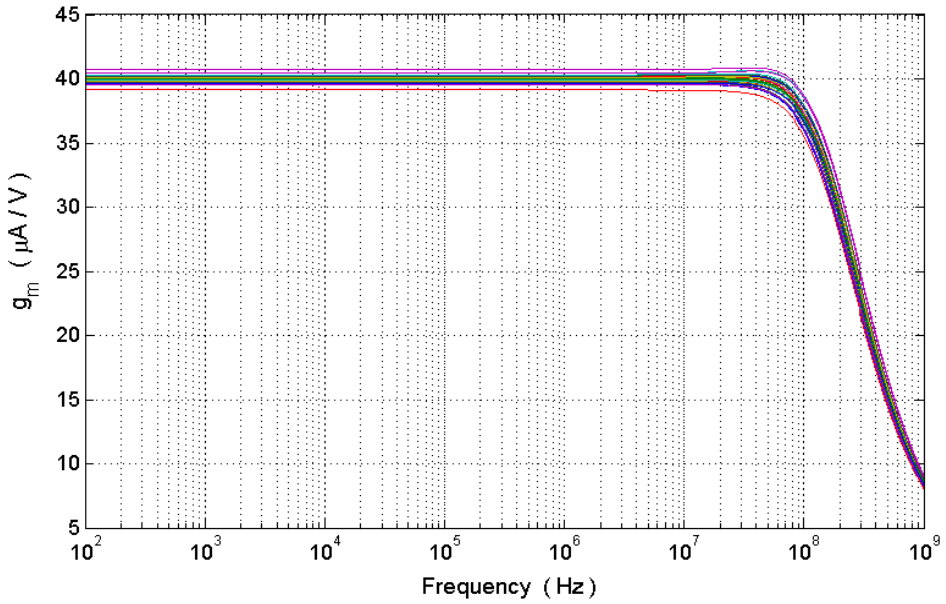

Figure 4.95. Monte-Carlo analysis of the transconductance

4.3.2.1. Design Example. The familiar Tow-Thomas biquad [87] is shown in Figure 4.96. Its simulation by means of two CDTAs is shown in Figure 4.97. OPA1 along with R_1, R_2 and C_1 forms an inverting lossy integrator. In the current-mode, it is implemented by one CDTA++ and R_2, C_1 and by the input current that drives terminal-n. The conductances of resistors R_1 and R_3 are replaced by the transconductance (g_1) of the first CDTA++.

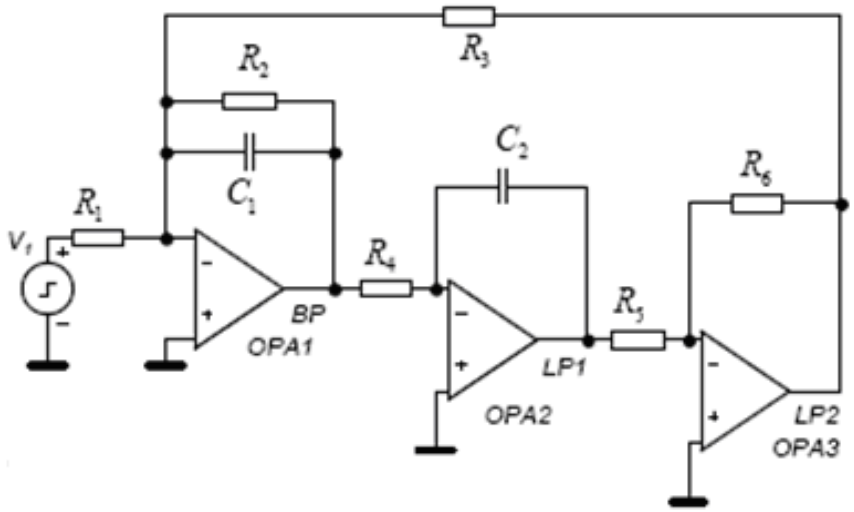

Figure 4.96. Second-order Tow-Thomas filter

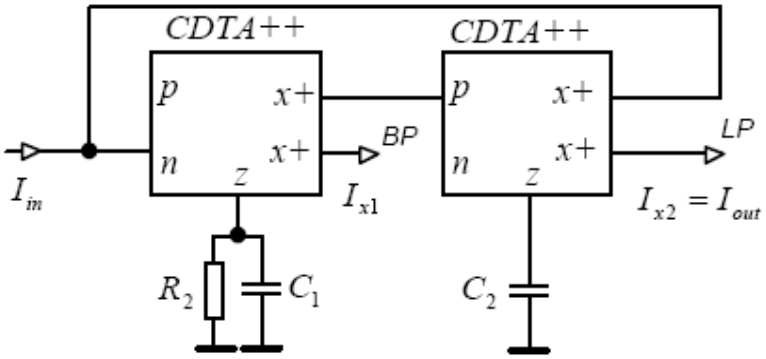

Figure 4.97. Implementation by two CDTAs

The following integrator and inverting amplifier with OPA2 and OPA3 are implemented by a single CDTA++ and by a capacitor C_2. Evaluating the reduced "IVI" graph in Figure 4.98 yields the transfer functions of BP (current I_{x1}) and LP (current I_{x2}) filters.

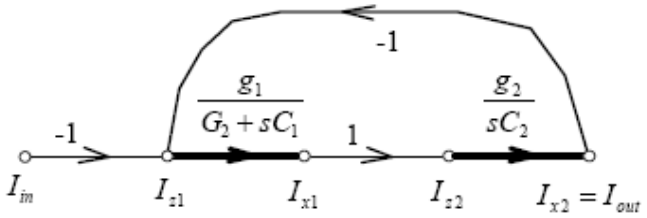

Figure 4.98. Reduced "IVI" flow graph

The non-inverting variant can be obtained by applying the input current to terminal-p instead of terminal-n. The angular resonant frequency (ω_o) and the quality factor (Q) are;

$$\omega_o = \sqrt{\frac{g_1 g_2}{C_1 C_2}} \tag{4.67}$$

$$Q = \sqrt{\frac{C_1}{C_2}} R_2 \sqrt{g_1 g_2} \tag{4.68}$$

Simulation results of the Tow-Thomas biquad filter configuration employing the proposed low-voltage CDTA++ are shown in Figure 4.99 where passive components are chosen as R_2=30 kΩ, C_1=0.01 nF and C_2=0.01 nF.

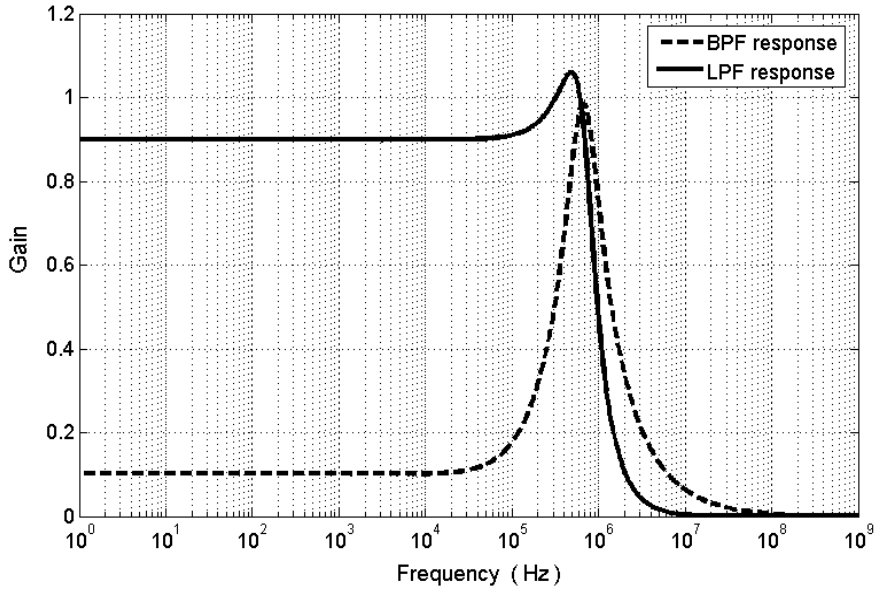

Figure 4.99. Frequency response of the biquad filter

4.3.3. Noise Performance of the Proposed CDTAs

Noise contributions of the proposed CDTA circuits come from the current subtractor circuit and transconductor stages. For two CDTA circuits, input-referred noise currents at terminal-p are shown in Figure 4.100 and Figure 4.101.

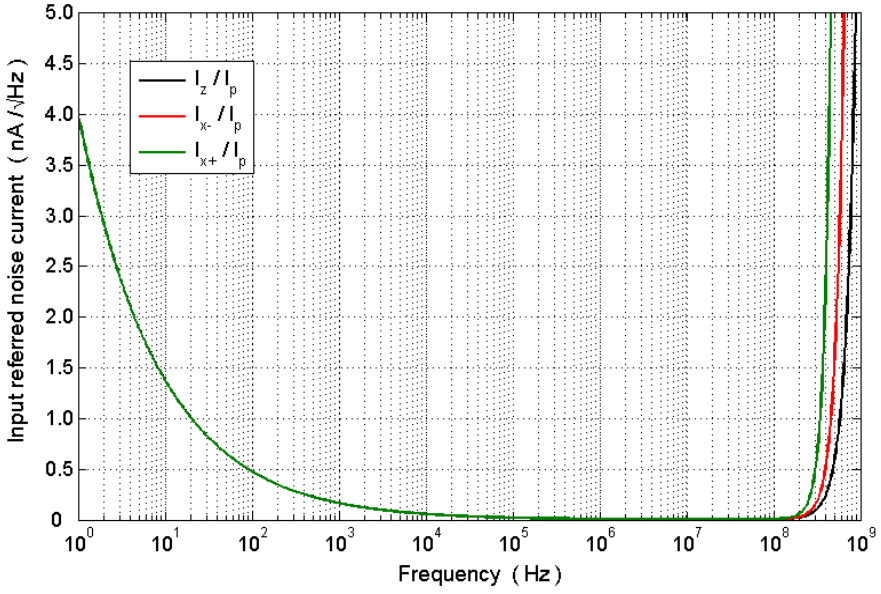

Figure 4.100. Noise currents at terminal-p for the CDTA+–

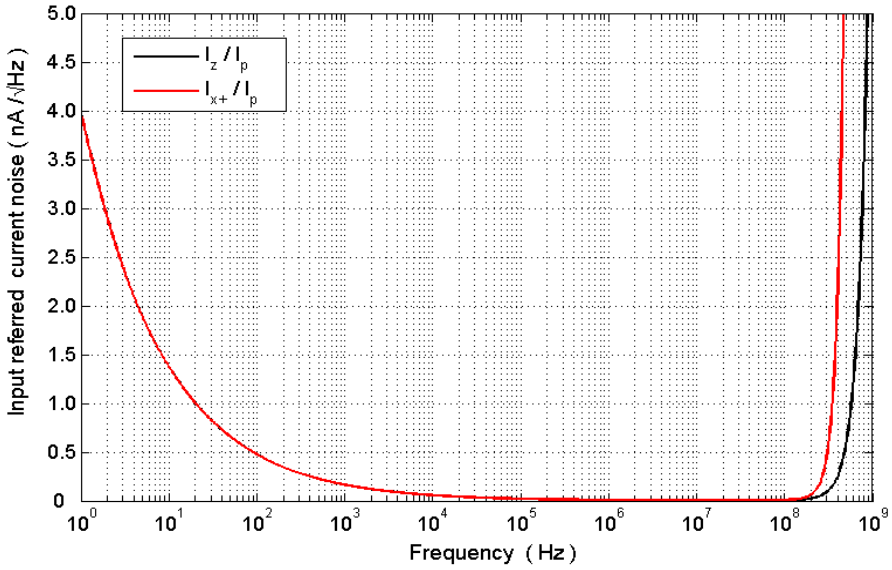

Figure 4.101. Noise currents at terminal-p for the CDTA++

4.3.4. Summary

In this section, different types of CMOS current differencing transconductance amplifier (CDTA) circuits are proposed.

Table 4.16. Comparison of CDTAs

Parameter	**[100]**	**[89]**	**First Proposed**	**Second Proposed**
Type	Single-ended	CDTA+–	CDTA+–	CDTA++
Power supply	±1.5 V	±0.75 V	±0.6 V	±0.6 V
Power dissipation	1.23 mW	370 µW	320 µW	272 µW
Bandwidth of I_z / I_p	65 MHz	87 MHz	93 MHz	93 MHz
Bandwidth of I_z / I_n	49 MHz	20 MHz	152 MHz	152 MHz
Terminal-p resistance	10 kΩ	25 Ω	2.95 Ω	4.2 Ω
Terminal-n resistance	10 kΩ	25 Ω	2.95 Ω	4.2 Ω
Terminal-z resistance	73.53 kΩ	NA	218 kΩ	219 kΩ
Terminal-x resistance	76.67 kΩ	NA	523 kΩ	162 kΩ
Transconductance (g_m)	5 ns-51 mS	210 µS	251 µS	40 µS
Input current linear range	(–60 µA) (+60 µA)	(–54 µA) (+54 µA)	(–40 µA) (+40 µA)	(–40 µA) (+40 µA)
Offset current at terminal-z	NA	0.4 µA	0.06 µA	0.06 µA

Table 4.16 summarizes specifications of the proposed circuits. They consume less power than their counterparts. Power dissipation values are 320 μW for the CDTA+– and 272 μW for the CDTA++. Simulation results show that terminal resistances of the proposed circuits are better than that of their counterparts. In addition, they have higher bandwidths compared to the circuits in the literature.

5. DESIGN OF LOW-POWER CHEBYSHEV-TYPE LOW-PASS FILTERS FOR BLUETOOTH APPLICATIONS

To demonstrate performance of the proposed active elements, Chebyshev-type low-pass filters (LPF) suitable for Bluetooth applications are presented in this section. Then performance of the LPFs is compared with that of the LPFs proposed in the literature.

5.1. Bluetooth

Bluetooth is a short-range wireless data communication standard. It provides a communication medium for electronic devices without the need for connection cables in short-range. Figure 5.1 depicts typical members of a piconet which is a collection of devices connected via Bluetooth technology.

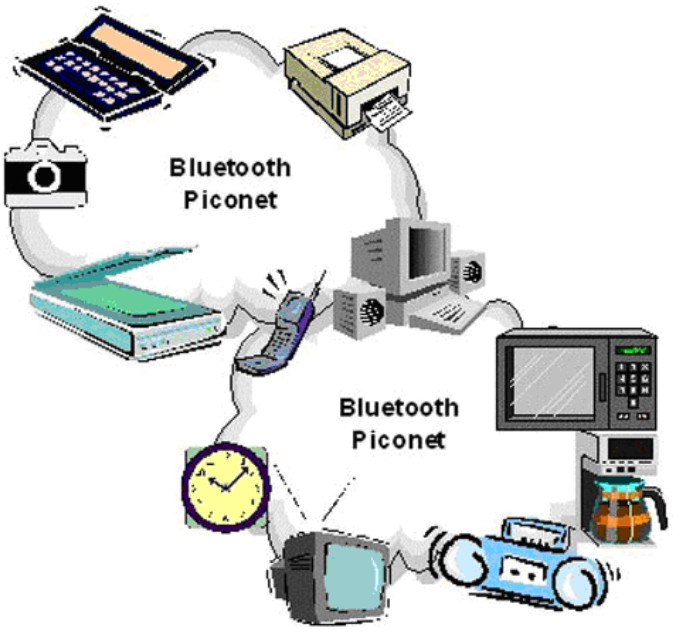

Figure 5.1. Members of a piconet

Bluetooth operates in the 2.4 GHz Industrial Scientific Medicine (ISM) band and it has a range of 10-100 m (0-20 dBm). Bluetooth uses Frequency Hopping Spread Spectrum (FHSS) which divides the frequency band into 79 hop channels starting from 2.402 GHz to

2.480 GHz as shown in Figure 5.2. The whole frequency band is 79 MHz and channel spacing is 1 MHz. One channel is divided into 625 intervals in time-domain.

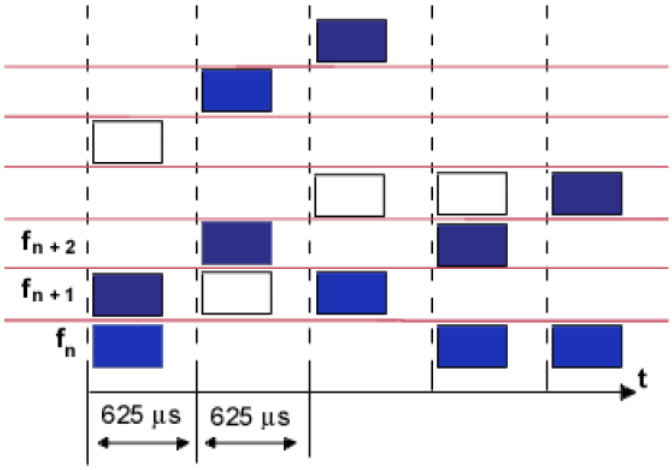

Figure 5.2. Frequency hopping

Bluetooth is used in mobile phones, all wireless connections of PCs, digital cameras, computer mouses and most wireless toys.

5.2. Application Example

Table 5.1 summarizes the main specifications of a baseband LPF for different standards [101]. It is clear from the table that a LPF for Bluetooth requires a cut-off frequency of 1 MHz and minimum attenuation of 30 dB at 1.5 MHz.

Table 5.1. Input specifications for a baseband LPF for a multi-standard zero-IF receiver

Standard	**BW_{tot}**	**Min. Attenuation**	**$v_{n,in}$**	**IIP3**
Bluetooth	1 MHz	30 dB @ 1.5 MHz	96-183 μV_{rms}	17.3 dBm
UMTS TDD	1.28 MHz	63 dB @ 3.84 MHz	52-104 μV_{rms}	18.4 dBm
UMTS FDD	3.84 MHz	58 dB @ 11.92 MHz	51-106 μV_{rms}	20.42 dBm
DVB-H	7.6 MHz	49.8 dB @ 19.8 MHz	62-127 μV_{rms}	17.9 dBm
WLAN 802.11a	16.66 MHz	49.8 dB @ 48.6 MHz	53-105 μV_{rms}	21.5 dBm
WLAN 802.11n	33.2 MHz	49.8 dB @ 96.6 MHz	75-149 μV_{rms}	21.5 dBm

Filters can be designed using Butterworth, Chebyshev and Bessel approximation methods. Here we prefer Chebyshev approximation method due to its specifications which are suitable for Bluetooth applications. Chebshev filters have a steeper roll-off compared to the other approximation methods, while they have more ripple in the passband. From the filter responses shown in Figure 5.3, it can be observed that Chebysev filters have the steepest roll-off, but more ripple in the passband.

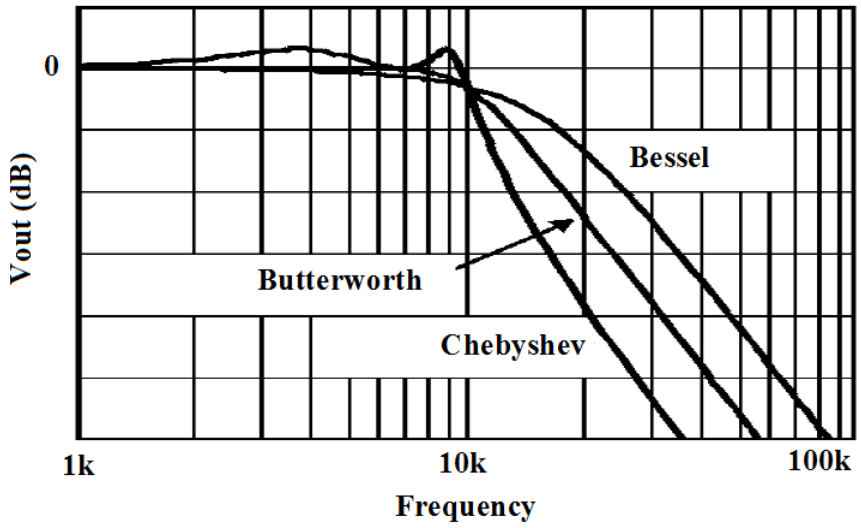

Figure 5.3. Filter approximation methods

A third-order and a fifth-order Chebyshev LPFs are designed by using the RLC-type LPF prototype shown in Figure 5.4.

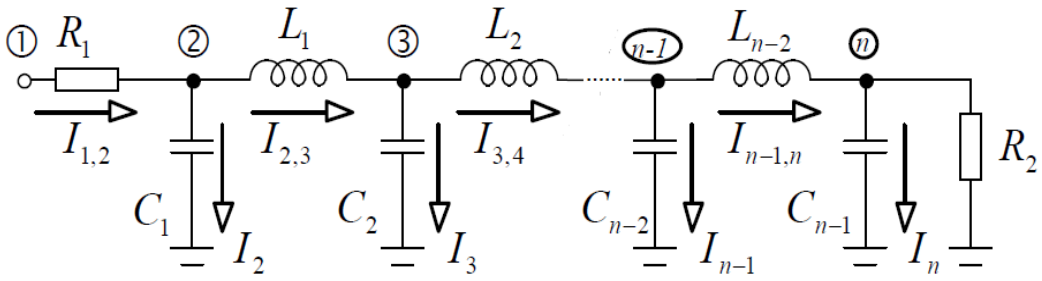

Figure 5.4. Low-pass ladder filter prototype

By using the corresponding signal-flow graph (SFG) shown in Figure 5.5, a CDBA-based LPF can be realized. From the SFG, following equations can be drawn;

$$I_{1,2} = G_1(V_1 - V_2) \qquad V_2 = \frac{1}{sC_1}(I_{1,2} - grI_{2,3})$$

$$rI_{2,3} = \frac{1}{sL_1/r^2}(gV_2 - gV_3) \qquad V_3 = \frac{1}{sC_2}(grI_{2,3} - grI_{3,4})$$

$$\vdots \qquad \vdots$$

$$rI_{n-1,n} = \frac{1}{sL_{n-2}/r^2}(gV_{n-1} - gV_n) \qquad V_n = \frac{1}{sC_{n-1}}(grI_{n-1,n} - G_2V_n) \qquad (5.1)$$

where r and g=1/r denote auxiliary resistances and conductances.

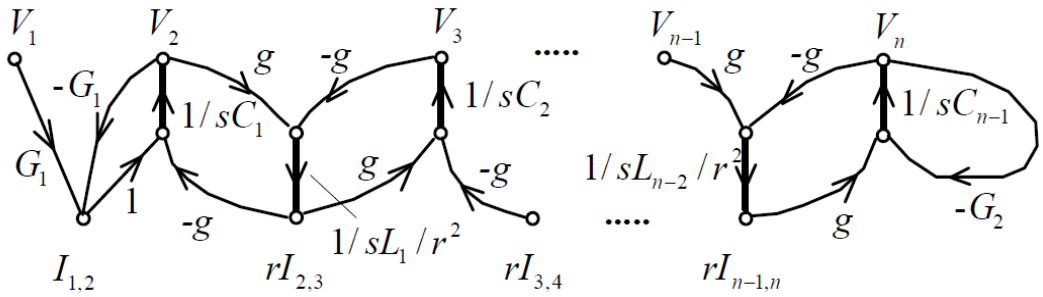

Figure 5.5. Signal-flow graph of the low-pass ladder filter

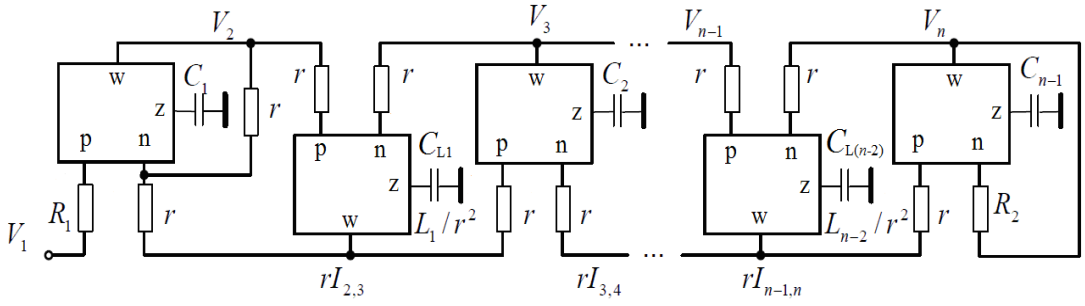

Figure 5.6. CDBA-based active filter implementation

The resulting CDBA-based filter topology is depicted in Figure 5.6. Passive component values are chosen as R_1=R_2= r =10 kΩ, C_1=C_2=53.296 pF and C_{L1}=11.327 pF

for the third-order filter and $R_1=R_2=$ r =10 kΩ, $C_1=C_3=55.413$ pF, $C_2=72.226$ pF and $C_{L1}=C_{L2}=12.124$ pF for the fifth-order filter. The cut-off frequency for both filters is 1 MHz. Simulated magnitude responses of the third-order and fifth-order filters are given in Figure 5.7.

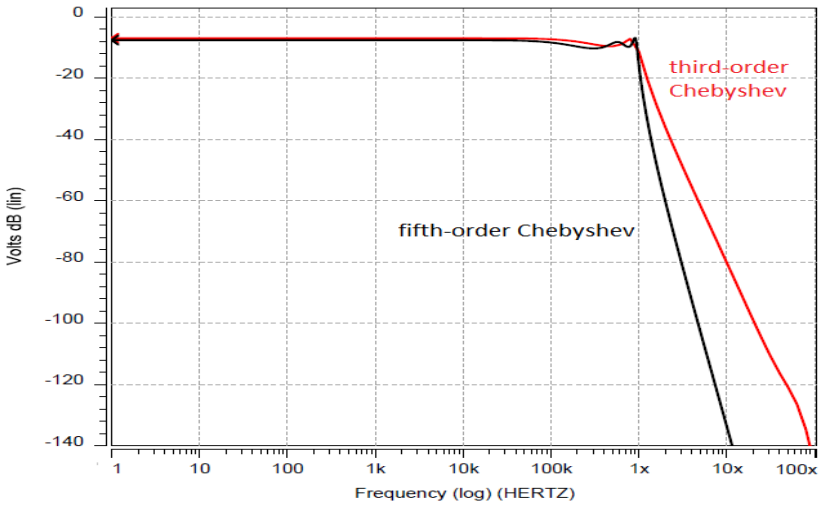

Figure 5.7. Simulated magnitude responses of the filters

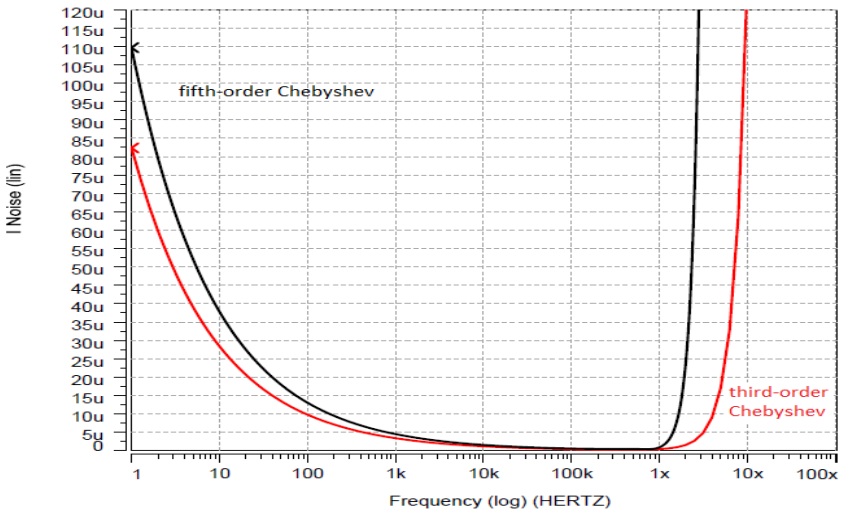

Figure 5.8. Input-referred noise voltages

Simulation results for the filters and a performance comparison are given in Table 5.2. Both filters are designed for a cut-off frequency of 1 MHz and 3 dB ripple in the passband. Power consumption is 1 mW for the third-order filter, while it is 1.65 mW for the fifth-order filter. Input-referred noise (IRN) voltages of the third-order and fifth-order

filters are depicted in Figure 5.8. Noise floors for the third-order and fifth-order filters are 295 $nV_{rms}/\sqrt{Hz}$ and 470 $nV_{rms}/\sqrt{Hz}$, respectively.

Table 5.2. Comparison of LPFs for Bluetooth applications

Parameter	**Proposed LPFs**		**[102]**	**[103]**	**[104]**
Type	Chebyshev	Chebyshev	Elliptic	NA	Butterworth
Technology	0.18 µm CMOS	0.18 µm CMOS	0.35 µm CMOS	0.13 µm CMOS	0.35 µm CMOS
Technique	CDBA-RC	CDBA-RC	G_m-C	G_m-RC	CFA-RC
Order	3	5	3	4	4
Passband ripple	3 dB	3 dB	0.3 dB	—	—
Power supply	1.2 V	1.2 V	3 V	2.5 V	2.5 V
Power dissipation	1 mW	1.65 mW	6.2 mW	NA	1.88 mW
Bandwidth	1 MHz	1 MHz	1 MHz	1 MHz	600 kHz
IRN	295 $nV_{rms}/\sqrt{Hz}$	470 $nV_{rms}/\sqrt{Hz}$	NA	5 $nV_{rms}/\sqrt{Hz}$	175 $nV_{rms}/\sqrt{Hz}$

6. CONCLUSION

Low-voltage and low-power analog and digital circuits are needed to realize battery-optimized, reliable and low-cost electronic devices for many applications. Example applications include remote environmental monitoring, medical diagnostics, tire pressure monitoring and consumer products. The continued downscaling of the CMOS process to deep-submicron dimensions has enabled the building of a system on a chip. However, this downscaling also requires similar shrinking of the supply voltage to insure device reliability. The International Technology Roadmap for Semiconductors predicts a maximum supply voltage equal to only 0.9 V in 2013 for state-of-the-art CMOS digital technology. This aggressive supply scaling requires low-voltage operation for the on-chip interface circuitry (analog-to-digital and digital-to-analog data converters) as well. Low-power circuits that operate at low supply voltages also simplify the power management and distribution strategy, extend the operating life and reduce the size, weight and cost of batteries.

This work is focused on the issues associated with the novel design techniques of current-mode circuits for the applications which require low-power consumption. Firstly, different types of analog building blocks which are useful for low-voltage and low-power operation are proposed, designed and simulated. Then these building blocks are used to implement current-mode active elements such as current differencing buffered amplifiers (CDBA), operational transresistance amplifiers (OTRA) and current differencing transconductance amplifiers (CDTA).

Finally, Chebyshev-tpye low-pass filters for Bluetooth applications are realized by using the proposed CMOS CDBA active element in order to demonstrate the efficiency and usefulness of the proposed active elements. HSPICE tool along with UMC 0.18 μm twin-well CMOS technology parameters is used in this work for schematic capture, simulation and measuring the noise performance. The proposed circuits are translated to their corresponding layouts using Cadence tools. The simulation results are in agreement with the theory.

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