# SECOND ORDER SIGMA DELTA MODULATOR ARCHITECTURE WITH LOW VOLTAGE SWING AT THE OUTPUT OF THE FIRST INTEGRATOR

By

Necmettin Levent Çakır

B.S. Electronics Engineering, İstanbul Technical University, 2007

Submitted to the Institute for Graduate Studies in
Science and Engineering in partial fulfillment of
the requirements for the degree of
Master of Science

Graduate Program in Electronics Engineering
Boğaziçi University
2010

# ACKNOWLEDMENTS

I would like to express my gratitude to Professor Günhan Dündar for his guidance and helpful supervising during the preparation of my thesis.

Then, I would like to thank my research partner and friend Feyyaz Melih Akçakaya for his contributions to my thesis and for his friendship.

I am very grateful to all members of BETA for their friendship and suggestions during my thesis.

I sincerely thank my family for their endless support and courage during all my life time. Also, I am very grateful to them for their understanding in all my life time.

Last but not the least, I would like to express my special thanks to TUBITAK for financial support during my graduate degree.

# ABSTRACT

## SECOND ORDER SIGMA DELTA MODULATOR ARCHITECTURE WITH LOW VOLTAGE SWING AT THE OUTPUT OF THE FIRST INTEGRATOR

The technological improvements in digital Very Large Scale Integration (VLSI) circuits increase the need of analog digital converter with high performance and lower power consumption. Primarily, the oversampling techniques such as sigma delta modulation should be chosen instead of Nyquist rate analog digital converters to satisfy this need. Because sigma delta modulation combines oversampling, quantization noise shaping and digital filtering in order to achieve high performance. Also, the output swing and the speed performance of the op-amps which are utilized in the modulators should be optimized for low voltage and high speed applications.

In this thesis, first of all, basic concepts of oversampling analog digital converter are explained and similar works which had been done before are examined. After that, a new low power second order sigma delta modulator in Mentor Graphics environment is proposed. To reduce the voltage swing at the output of first integrator as much as possible is the purpose of the research. Moreover, the proposed sigma delta modulator is compared to similar work in this area and it is shown that it has the lowest voltage swing at the first integrator output. As a result of the reduction of the voltage swing, op-amps with less power consumption or an inverter as an op-amp can be used instead of ideal op-amps in the project; and, this will provide less power consumption in the whole circuit. All sigma delta modulator architectures are designed with using ideal op-amp, real op-amp, differential amplifier and an inverter respectively in order to find the architecture that consumes the minimum power.

# ÖZET

## BİRİNCİ İNTEGRATÖR ÇIKIŞINDA DÜŞÜK GERİLİM SALINIMLI İKİNCİ DERECE SİGMA DELTA KİPLEYİCİ YAPISI

Sayısal Çok Büyük Ölçekli Birleşen (ÇBÖB) devrelerdeki teknolojik ilerlemeler, yüksek performanslı ve daha düşük güç harcayan analog sayısal çeviricilere olan ihtiyacı artırmaktadır. Bu ihtiyacı karşılamak için öncelikle, Nyquist oranlı analog sayısal çeviriler yerine sigma delta kiplemesi gibi fazla örnekleme (oversampling) teknikleri seçilmelidir. Çünkü sigma delta kipleme, yüksek performansa ulaşmak için fazla örneklemeyi, niceleme gürültü şekillendirmeyi ve sayısal süzgeçlemeyi bir araya getirir. Ayrıca düşük gerilimli ve yüksek hızlı uygulamalar için, kipleyicilerde yararlanılan işlemsel kuvvetlendiricilerin çıkış salınımları ve hız performansları en uygun hale getirilmelidir.

Bu tezde ilk olarak, fazla örneklemeli analog sayısal çevirilerin ana kavramları açıklanmış ve daha önce yapılan benzer çalışmalar incelenmiştir. Bundan sonra, Mentor Graphics ortamında yapılan yeni bir düşük güçlü ikinci derece sigma delta kipleyici önerilmiştir. Araştırmanın amacı birinci integratör çıkışındaki gerilim salınımını olabildiği kadar düşürmektir. Ayrıca, önerilen sigma delta kipleyici bu alandaki benzer çalışmalarla karşılaştırılmış ve birinci integratör çıkışında en düşük gerilim salınımına sahip olduğu gösterilmiştir. Gerilim salınımının azalmasının sonucu olarak, daha düşük güç tüketimli işlemsel kuvvetlendiriciler veya işlemsel kuvvetlendirici olarak bir çevirici, projedeki ideal işlemsel kuvvetlendiricilerin yerine kullanılabilirler. Bu, tüm devrede daha az güç kullanılmasını sağlayacaktır. En az güç harcayan yapıyı bulmak için, tüm sigma delta kipleyici yapıları sırasıyla ideal işlemsel kuvvetlendirci, gerçek işlemsel kuvvetlendirici, diferensiyel yükseltici ve çevirici kullanılarak tasarlanmıştır.

# TABLE OF CONTESTS

# LIST OF FIGURES

# LIST OF TABLES

# LIST OF SYMBOLS / ABBREVIATIONS

| | |
|---|---|
| $C_0$ | Feedback capacitor |
| $f_N$ | Nyquist frequency |
| $f_s$ | Sampling frequency |
| $F_s$ | Input sampling rate |
| $k$ | Thresholds that ADC uses |
| $M$ | Quantization interval |
| $N(f)$ | Power spectral of the noise |
| $P_{noise}$ | Power of the noise |
| $P_{sign}$ | Power of the signal |
| $R$ | Oversampling ratio |
| $T$ | Integrator time constant |
| $v_{FS}$ | Voltage range of quantizer |
| $V_{in}$ | Input voltage |
| $V_{out}$ | Output voltage |
| | |
| $\sigma_e^2$ | Quantization power |
| $\Delta$ | Quantization step |
| $\Phi_1$ | Clock phase1 |
| $\Phi_2$ | Clock phase2 |
| | |
| AD | Analog-to-digital |
| ADC | Analog-to-digital converter |
| BW | Bandwidth |
| DA | Digital-to-analog |
| DAC | Digital-to-analog converter |
| DNL | Differential non-linearity |
| DR | Dynamic range |

| | |
|---|---|
| DSP | Digital signal processor |
| ENOB | Effective number of bits |
| ERBW | Effective resolution bandwidth |
| ESD | Electrostatic discharge |
| FoM | Figure of merit |
| GBW | Gain bandwidth |
| HD | Harmonic distortion |
| IC | Integrated circuit |
| IMD | Intermodulation distortion |
| IMD2 | Two tone intermodulation distortion |
| INL | Integral non-linearity |
| MTPR | Multi-tone power ratio |
| NPR | Noise power ratio |
| NTF | Noise transfer function |
| Op-amp | Operational amplifier |
| OSR | Oversampling ratio |
| PSD | Power spectral density |
| SAR | Successive approximation register |
| SC | Switched-capacitor |
| SD | Sigma delta |
| SFDR | Spurious free dynamic range |
| SINAD or SNDR | Signal-to-noise and distortion ratio |
| SNR | Signal-to-noise ratio |
| STF | Signal transfer function |
| TSD | Total spurious distortion |
| V (INN) | Input voltage |
| V (INTOUTN) | Voltage of first integrator output of SD modulator (optimum gain) |
| V (INTOUTN1) | Voltage of first integrator output of SD modulator (feed-forward) |
| V (INTOUTN2) | Voltage of first integrator output of SD modulator (proposed) |
| V (OUTN) | Voltage of second integrator output of SD modulator (optimum gain) |
| V (OUTN1) | Voltage of second integrator output of SD modulator (feed-forward) |
| V (OUTN2) | Voltage of second integrator output of SD modulator (proposed) |
| V (YN) | Output voltage of SD ADC (optimum gain) |

| | |
|---|---|
| V (YN1) | Output voltage of SD ADC (feed-forward) |
| V (YN2) | Output voltage of SD ADC (proposed) |
| VLSI | Very large scale integration |

# 1. INTRODUCTION

## 1.1. Background Information and Aim of the Thesis

Even though real world signals are analog, it is often desirable to convert them into the digital domain using an analog-to-digital converter (ADC). Designers apply this conversion because digital signals are much more efficient than analog signals in the way of transmission and storage. Intricate processing of the signal may also involve analog-to-digital (AD) conversion, because this processing is only possible in the digital domain using either conventional digital computers or special purpose digital signal processors (DSPs). Signal processing in the digital domain is also extremely useful in some areas such as biomedical applications. It provides the needed accuracy for tasks such as ultrasound imaging [1].

AD conversion techniques can be categorized into two groups according to the sampling rate criteria. These are Nyquist-rate (conventional) converters and oversampling converters. Nyquist converters, such as a successive approximation register (SAR) and double integration, sample analog signals which have maximum frequencies slightly less than the Nyquist frequency, $f_N = f_s / 2$, where $f_s$ is the sampling frequency. At the same time, oversampling converters fulfill the sampling process at a much higher rate, $f_N \ll F_s$, where $F_s$ means the input sampling rate [2].

Due to the technological improvements in digital VLSI circuits, the need of low cost high resolution AD and DA converters have significantly increased. Also some new problems have appeared for the analog interfaces in embedded systems because the AD conversion and the digital signal processing are on the same chip. The use of Nyquist rate AD converters in such systems limits the resolution because most of the injected noise from the digital part is aliased into the baseband. Moreover, their system integration is complex because effective anti-alias filters, high performance sample and hold circuits and jitterfree timing are needed [3].

Using oversampling technique can solve many of the problems mentioned above. Sigma delta (SD) modulation is one of the most important oversampling techniques in the literature and has become more popular because it combines oversampling, quantization noise shaping and digital filtering in order to achieve high performance with reduced analog circuit complexity [3].

Furthermore, there are many other advantages of using SD modulators when designing an AD converter. The resolution of the AD converter can be increased by using SD modulation. One significant advantage of SD modulation is that analog signals are converted using only 1-bit quantization and analog signal processing circuits which have an accuracy that is usually much less than the resolution of the overall converter [1]. This enables an excellent linearity to the converter. In addition, the sharp analog anti-aliasing filter can be replaced by a simple analog filter and a digital anti-aliasing filter. This is an also important advantage because a precision filter which is implemented in the digital domain does not have need of adjustments. Moreover, an analog filter typically requires many circuit components which are difficult to implement in an integrated circuit. Another important advantage of the method is that the dither signal that is commonly added to the input of an AD converter to decorrelate successive quantization errors can be high-passed filter. Thus, little dither signal power lies in the signal band. Furthermore, the noise coupling from the digital part is small because most of the noise is digitally filtered in the decimation filter. A final advantage of oversampling AD converters is the elimination of the need for a sample and hold amplifier preceding the AD converter. Designing sample-and hold amplifiers with an accuracy greater than 13 or 14 bits is problematic because of the dielectric absorption in capacitors; therefore, their elimination is also critical for high-resolution of AD converters [3, 4].

A SD modulator contains an analog filter and a quantizer enclosed in a feedback loop. Together with the filter, the feedback loop performs to decrease the quantization noise at low frequencies while emphasizing the high-frequency noise. The high-frequency quantization noise can be removed without affecting the signal band through a digital low-pass filter which works on the output of the SD modulator because the signal is sampled at a frequency which is much greater than the Nyquist rate [5].

The simplest modulator is a first-order loop wherein the filter contains a single integrator. However, the quantization noise from first-order modulators is highly correlated and the oversampling ratio needed to achieve higher resolution is prohibitively large. Higher order SD modulators which contain more than one integrator in the forward path, offer an increased resolution. Nevertheless, modulators with more than two integrators suffer from potential instability because of the accumulation of large signals in the integrators. In order to achieve performance that is comparable to the performance of higher order modulators and deal with the stability problem, several first-order modulators can be cascaded. Second-order SD modulators are thus especially attractive for high-resolution AD conversion. The efficiency of second-order SD modulator architectures has already been illustrated in a variety of applications. Digital speech processing systems and voice-band telecommunication codecs with AD converters based on second-order SD modulation have been reported and the extension of the performance achievable with such architecture to the levels required for digital audio and higher signal bandwidths has been demonstrated [5].

Low power consumption is not always a result of low supply voltages. Although there is reduction in supply voltages, the additional signal processing can be needed to maintain the same or maybe an even better dynamic range and this additional signal processing can cause additional power consumption. A low supply voltage always supposes that all circuit techniques are also performed to decrease the power consumption. Furthermore, most low-power SD converters use switched-capacitor filters for the noise shaping. However, switches may become a problem for such low supply voltages. Rather than use switches, op-amps can be switched themselves. Nowadays, many very-low voltage SD converters use this technique [6, 7].

Moreover, for low voltage and high speed applications, designers must optimize the output swing and the speed performance of the op-amp which are utilized in the modulators. When the integrator output goes beyond the dynamic range of the op-amp, the signal is clipped to a saturation level and it results in a loss of feedback control. This occurs because the inverting period of the op-amp is no longer tightened to the non-inverting period, and is free to go up or down causing an incomplete transfer of the input signal. In order to avoid clipping, it is necessary to ensure a properly large dynamic range

of the op-amps which are used in the integrators. Moreover, first integrator is the most critical for the dynamic range because its saturation error is not shaped by any transfer function. On the other hand, the saturation of the second integrator and the saturation of the quantizer are limits to the modulator performances. It is therefore necessary to estimate the expected voltage swings carefully and to keep them within limits which are not large enough to cause saturation, but, at the same time, are not so low to become comparable with the electronic noise [6].

As obvious from the above discussion, in order to optimize the dynamic range of the op-amps and decrease the voltage swing of the output of the first integrator, some extra techniques need to be used in SD AD modulators. Scaling technique and using feed-forward path are explained as solutions to these problems in [6].

This thesis proposes a new low power second order SD modulator in Mentor Graphics environment. The aim of the design of this SD modulator is to reduce the voltage swing at the output of first integrator as much as possible. To achieve this, a new integrator is designed by using the switched-capacitor building blocks and an ideal op-amp. Compared to similar work in this area such as the second order SD modulator which has optimum gains in its integrators owing to scaling technique [6] and the second-order SD modulator which has a feed-forward path in order to reduce the voltage swing [6], it is desired that the proposed SD modulator has the lowest voltage swing at the first integrator output. Resulting from the reduction of the voltage swing, op-amps with less power consumption or an inverter as an op-amp can be used instead of ideal opamps in the project; and therefore, this will provide less power consumption in the whole circuit. All SD modulator architectures are designed with using ideal op-amp, real op-amp, differential amplifier and an inverter respectively in order to find the architecture that consumes the minimum power.

### 1.2. Outline of the Thesis

The next chapter focuses on basic concepts of oversampling sigma delta modulators such as quantization noise, oversampling and some performance measures. Properties of SD modulation and noise shaping are described; and first-order and second-order SD

modulators are explained. It finishes with architecture of a second-order SD modulator which is given in [6] with optimum gains.

In Chapter 3, the arctitectural design of the SD modulators which are used in the project, op-amp swing reduction and switched-capacitor building blocks are discussed. Finally, proposed architectural design of low power second-order SD modulator is introduced.

In Chapter 4, circuit implementations of three second order SD modulators are described in detail. All circuits have been revised for an ideal op-amp, a new designed op-amp, a differential amplifier and an inverter. The analysis results for all circuits are given.

Finally, Chapter 5 concludes the thesis.

# 2. OVERSAMPLING SIGMA DELTA MODULATORS

This chapter focuses on basic concepts of oversampling sigma delta modulators such as quantization noise, oversampling and some performance measures, and properties of first-order and second-order sigma delta modulators. It finishes with architecture of a second-order sigma delta modulator which is given in [6] with optimum gains.

The block diagram of an oversampling SD AD converter is given in Figure 2.1.

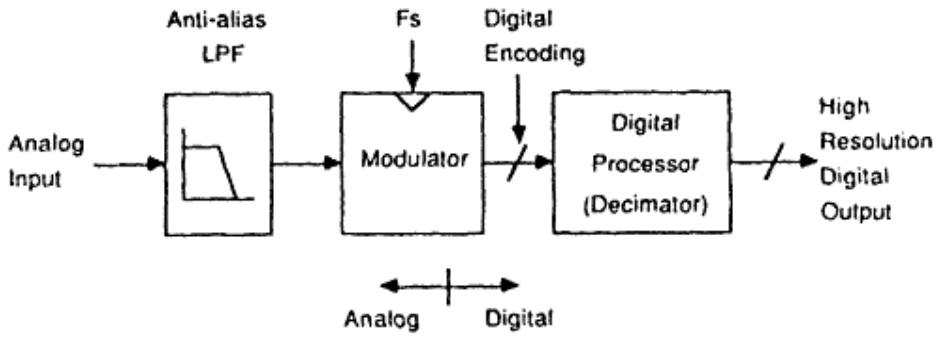


Figure 2.1. Block diagram of an oversampling ADC system [8]

A Sigma-Delta converter contains a feedback loop with a filter and a quantizer, which achieves the AD Conversion. The feedback loop is closed over a DAC. A anti-aliasing filter (prefilter filter) is required to ensure the incoming bandwidth is limited and remove frequencies above half the sampling rate. A decimator filter (post filter ) is applied to lower the sampling frequency to what satisfies Nyquist [7].

## 2.1. Basic Concepts

### 2.1.1. Quantization Noise

The quantization process which is involved in analog to digital conversion is a non-linear operation and introduces errors to the conversion. The quantization error is defined as the difference between the output and the input of the quantizer. So, it can be written

that the output is the sum of the input and the quantizer error. Compared to full-amplitude signal, the quantization error is quite small in amplitude. Nevertheless, when the input signal gets smaller, the quantization error becomes a larger part of the full signal. In addition, the quantization error is not an independent signal, it is strongly dependent on the input. Also it contains many different frequencies, and this is why the quantization error is called noise. This noise determines Signal-to-Noise ratio (SNR) and resolution of the converter [7, 9].

Because of its intense non-linearity, the analysis of the quantizer is very difficult. In order to make this analysis more easier, the quantizer is often linearized by using an input-independent additive white noise model [9].

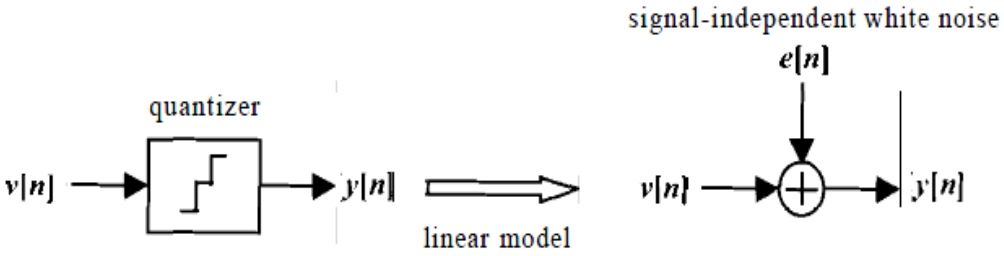


Figure 2.2. Quantizer and its linear model [9]

According to Figure 2.2, the quantizer can be represented by a function as,

$$y[n] = v[n] + e[n] \tag{2.1}$$

where $y$ is the output and $v$ is the input of the quantizer; and $e$ is the quantiziation error. If the range of the quantizer is $v_{FS} = v_{\max} - v_{\min}$ and the number of the quantization intervals is $M$, the amplitude of each quantization interval or quantization step is

$$\Delta = \frac{v_{FS}}{M} \tag{2.2}$$

As the mid point of the $n-th$ interval $v_{m,n} = (n + 1/2)\Delta$ represents all the interval amplitudes, the output of the quantizer can be rewritten as,

$$y[n] = v[n] + e[n] = (n + 1/2)\Delta \;; \quad n\Delta < v[n] < (n+1)\Delta \tag{2.3}$$

In this linear model, the quantization error is added to input to obtain the quantized output. The added term is a random quantity which is distributed in equal ratio in the interval ( $-\Delta/2$ to $\Delta/2$). In this case its mean value is zero and its power is the variance $\sigma_e^2$ given by

$$\sigma_e^2 = \int_{-\Delta/2}^{\Delta/2} e^2 f_e(e) de = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.4}$$

If the values of $e[n]$ are assumed uncorrelated and identically distributed, the quantization noise is white and its power is spread in equal ratio over the entire frequency range $[-f_s/2, f_s/2]$ . Thus, the power spectral density (PSD) of the noise can be expressed as following [10],

$$N(f) = \frac{\Delta^2}{12 f_s} \tag{2.5}$$

### 2.1.2. Oversampling

The high resolution can not be completely satisfied by the Nyquist-rate (conventional) ADCs. To increase the sampling rate many times higher than sampling rate of the Nyquist-rate ADCs is the one way of improving the resolution. This requires the various components of the ADC to function at a much higher frequency. The minimum sampling frequency according to Nyquist, is twice the maximum frequency of the input signal. Sampling at a higher rate $f_s$ which is higher than the Nyquist rate $f_N$, is called

oversampling and the ratio of this sampling frequency to the minimum Nyquist sampling frequency is called the oversampling ratio (OSR) and defined as [10]

$$R = \frac{f_s}{f_N} \tag{2.6}$$

The result of the oversampling technique is described in the Figure 2.3. It can be seen that the images of the signal band are not so close to one another. Therefore, the specifications of the anti-aliasing filter can be relaxed. Moreover, the benefits of oversampling is more than an economical anti-aliasing filter. The decimation process can be used to provide increased resolution [1, 10].

On the other hand, the oversampling is only convenient in the analog world. In the digital world, oversampling is not a appropriate characteristic because transmitting digital data and storing are effective when the lowest sampling rate which is coherent with the signal band is used. Furthermore, using large oversampling means wasting power because the power that is consumed by digital circuits is proportional to the clock frequency. As a result of this, the sampling rate of digital oversampled signals is normally reduced by the use of a convenient decimation filter [6].

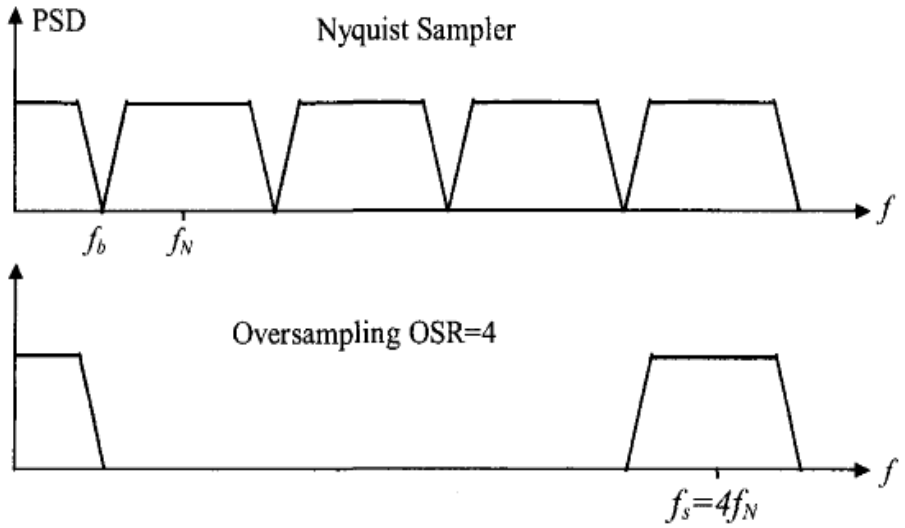


Figure 2.3. Oversampling process [10]

### 2.1.3. Performance Measures

There are many specifications that describe the performance of data converters. The specifications are divided into the following classes:

- General features: Type of analog signals, resolution, dynamic range, absolute maximum ratings, ESD (Electrostatic Discharge) notice, pin function descriptions and pin configuration, warm-up time, drift.
- Static specifications: Analog resolution, analog input range, offset, zero scale offset, common mode error, full-scale error, bipolar zero offset, gain error, differential non-linearity error (DNL), monotonicity, hysteresis, missing code, integral non-linearity (INL), power dissipation, temperature ranges, thermal resistance, lead temperature.
- Dynamic specifications: Analog input bandwidth, input impedance, load regulation or output impedance, settling time, cross-talk, aperture uncertainty (clock jitter), digital to analog glitch impulse, glitch power, equivalent input referred noise, signal to noise ratio (SNR), signal to noise and distortion ratio (SINAD or SNDR), Dynamic range, effective number of bits (ENOB), harmonic distortion (HD), total spurious distortion (TSD), spirious free dynamic range (SFDR), intermodulation disortion (IMD), two tone intermodulation distortion (IMD2), multi-tone power ratio (MTPR), noise-power ratio (NPR), effective resolution bandwidth (ERBW), figure of merit (FoM).
- Digital and switching specifications: Logic levels, encode or clock rate, clock timing, clock source, sleep mode [6].

Some of the most important specifications can be summarized as follows, other issues are discussed in more detail in [6].

2.1.3.1. Signal-to-Noise-Ratio (SNR). It is the ratio between the power of the signal and the total noise produced by quantization and the noise of the circuit. It is defined as

$$SNR|_{DB} = 10 \bullet \log \frac{P_{sign}}{P_{noise}} \tag{2.7}$$

where $P_{sign}$ and $P_{noise}$ are the power of the signal and the power of the noise in the band of interest respectively [1]. Also, for a sine wave input signal with full scale amplitude variation $2A = (2^B - 1)\Delta$, its power is $A^2/2$ and the SNR is expressed as following [10]:

$$SNR = 10 \bullet \log\left(\frac{A^2/2}{\Delta^2/2}\right) \cong 10 \bullet \log\left(\frac{3 \bullet 2^{2B}}{2}\right) = (6.02 \bullet B + 1.76)dB \qquad (2.8)$$

2.1.3.2. Signal-to-Noise-and-Distortion-Ratio(SINAD). It is similar in definition to the SNR except that non linear distortion terms, which are generated by the input sine wave, are also accounted for. The SINAD is the ratio between the root-mean-square of the signal and the root-sum-square of the harmonic components plus noise [6].

2.1.3.3.Effective-Number-of-Bits (ENOB). It measures the distortion ratio and the signal-to-noise using bits [6]. SINAD and ENOB are linked by

$$ENOB = \frac{SINAD_{DB} - 1.76}{6.02} \qquad (2.9)$$

2.1.3.4.Dynamic Range(DR). It is the value of the input signal at which the SNR is 0dB. The parameter is beneficial for some kinds of data converters which do not obtain maximum SNR at 0 $dB_{FS}$ input. This typically happens in sigma-delta converters [6].

2.1.3.5.Spurious Free Dynamic Range. It is the ratio of the root-mean square signal amplitude to the root-mean-square value of the highest spurious spectral component in the first Nyquist zone. The *SFDR* provides information similar to the total harmonic distortion but focuses on the worst tone. The *SFDR* depends on the input amplitude. With large input signals the highest tone is given by one of the harmonics of the signal. The importance of SFDR depends on the application. In some applications, a good SFDR is more important than a good DR. For example, it might be important to keep the amplitude of spurious tones low in radio systems. Because nonlinearities may cause them to intermodulate and corrupt the desired signal, while the total amount of inband noise may not matter so much [11].

## 2.2. Sigma Delta Modulators

### 2.2.1. Sigma Delta Modulation and Noise Shaping

The two main types of oversampling modulators are the delta modulator and the sigma delta modulator. Figure 2.4 shows the block diagram of a basic delta modulator.

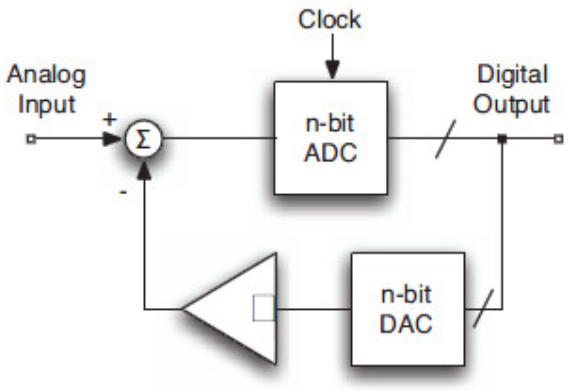


Figure 2.4. Block diagram of a delta modulator [6]

In delta modulation, a ADC quantize the difference between the signal and its estimation. At the same time, a DAC transforms the digital output into analog in the feedback loop and the integration of this signal is the estimation of the input. This kind of modulator is difficult to be analyzed and has some disadvantages. To overcome these problems, an integrator can be used in front of the delta modulator and it results in encoding the integral of the input signal. Then, the resulting modulator is called Sigma-Delta modulator and the block diagram of this kind of modulator is given in Figure 2.5. The difference between the sigma delta and the delta modulator is that the integrator operates on the error difference and not on the estimation of the signal. Therefore, the modulator response changes from high pass to low pass [6, 10].

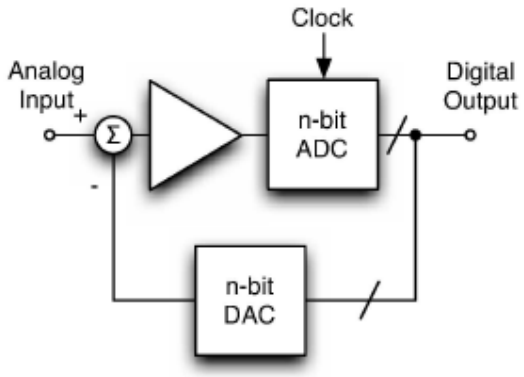


Figure 2.5. Block diagram of a sigma-delta modulator [6]

The important property of SD modulation is the spectral shaping of the noise. It increases the benefits of oversampling on ADCs. In general, if the loop filter has a high gain in the signal band, the inband quantization noise is strongly attenuated and the process is called noise shaping [6].

The system given in the Figure 2.5 can be represented in z-domain by

$$Y(z) = X(z)\frac{H(z)}{H(z)+1} + E(z)\frac{1}{H(z)+1} \tag{2.10}$$

where $Y(z)$, $X(z)$, $E(z)$ and $H(z)$ are the z-transforms of the output, input, quantization noise and transfer function of the integrator respectively. The above equation shows that signal and quantization noise pass through two different transfer functions

$$Y(z) = X(z)STF(z) + E(z)NTF(z) \tag{2.11}$$

named signal transfer function (STF) and noise transfer function (NTF). $STF(z)$ and $NTF(z)$ are mathematically defined as

$$STF(z) = \left.\frac{Y(z)}{X(z)}\right|_{E(z)=0} \text{ and } NTF(z) = \left.\frac{Y(z)}{E(z)}\right|_{X(z)=0} \tag{2.12}$$

When the integrator in Figure 2.5 is defined as

$$H(z) = \frac{1}{1 - z^{-1}} \tag{2.13}$$

(2.10) can be simplified to

$$Y(z) = X(z) + E(z)(1 - z^{-1}) \tag{2.14}$$

The output is the sum of the input signal and the quantization noise which is shaped by a first order differentiation. The filtering function $\left(1 - z^{-1}\right)$ is the noise transfer function (NTF). NTF is a high pass filter with a zero at dc. The squared magnitude of the NTF as a function of frequency is given in Figure 2.6 [12].

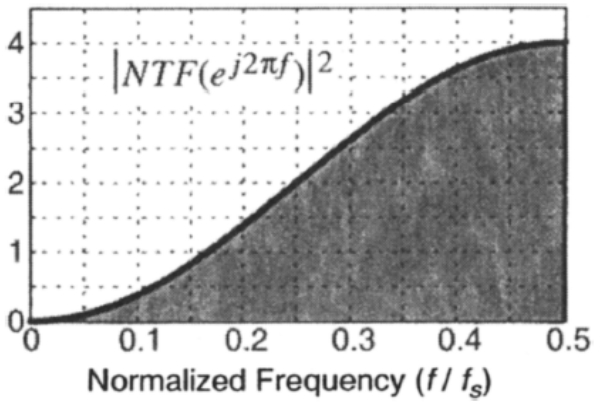


Figure 2.6. Noise shaping function for a SD modulator [12]

### 2.2.2. First Order Sigma Delta Modulators

The simplest analog SD modulator which is given in the Figure 2.7, is a first-order loop containing an integrator, a 1-bit ADC and a 1-bit DAC. This block diagram integrates the difference between the analog input and the output of the DAC to generate sampled-data input of the ADC. Moreover, this modulator uses oversampling to spread the quantization noise over the [0, $f_s$ / 2] frequency band, as well as noise shaping in order to push most of the inband noise out of this band to higher frequencies [10, 12].

Figure 2.7 also shows the block diagram of the first-order SD modulator which uses the transfer function

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.15}$$

for analog to digital integration.

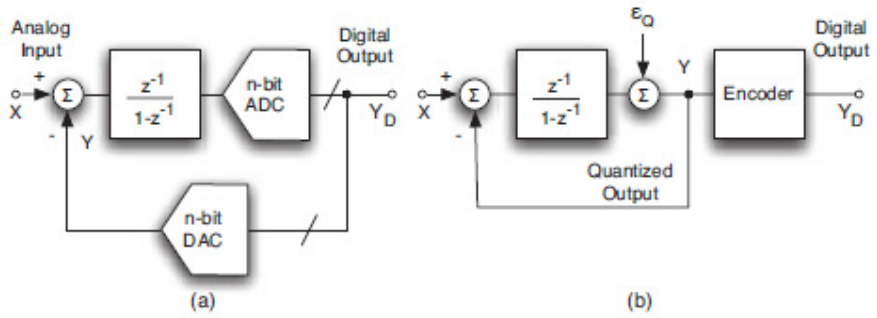


Figure 2.7. (a)Block diagram of the first order SD modulator (b) its linear model [6]

By analysis of the linear system in Figure 2.7 (b), it can be obtained the following;

$$Y(z) = \{X(z) - Y(z)\}\frac{z^{-1}}{1 - z^{-1}} + E(z) \tag{2.16}$$

simplifying to

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1}) \tag{2.17}$$

According to (2.17), the signal is delayed by one clock period and the noise is passed through $(1 - z^{-1})$. This shows that the signal and the quantization noise are processed differently by the modulator. Using (2.12), the STF and the NTF are found as following:

$$STF(z) = z^{-1} \qquad NTF(z) = 1 - z^{-1} \tag{2.18}$$

It can be seen from (2.18) that the STF(z) does not change the signal. It is just delayed by one clock period, whereas the NTF(z) high-passes the quantization noise.

Furthermore, the maximum SNR of the first order SD modulator is given by

$$SNR = \frac{12}{8} k^2 \frac{3}{\pi^2} OSR^3 \tag{2.19}$$

where $k$ is the number of thresholds that ADC uses (Detailed analysis of the PSD, in-band noise power and SNR are found in [6], [12] and [10]). So for the first-order SD modulator, the noise is attenuated by the third power of the oversampling ratio.

Consequently, some remarks help us to understand important characteristics of the SD modulators. The first remark is that the output of an integrator is limited if its input is zero. Therefore, the subtraction between input and the output of DAC must have zero average. The second remark is that the quantization noise is zero at dc. Also a first order modulator reduces the global noise performance, but thanks to the noise shaping, it pushes a major part of the power to high frequencies. The last remark is about the linearity and noise specifications of the ADC and the DAC. The digital signal that is generated by the ADC are relaxed by the feedback loop. The ADC error must be referred to the input of the integrator and then referred to the input of the modulator. The result of these two operations leads to a division of the error by the transfer function of the integrator. The error is greatly attenuated in the signal band because the integrator has a very large gain at low frequency. The same benefit does not apply to the DAC because its error affects directly at the input of the modulator together with the input [6].

### 2.2.3. Second Order Sigma Delta Modulators

Although the first order SD modulators have advantages on simplicity, robustness and stability, its overall performance in terms of resolution is inadequate for most applications. This section focuses on the second-order SD modulators.

A second-order SD modulator which is given in the Figure 2.8 (b) is formed by using two integrators around the loop. It is necessary to remove one of the two integrators by using one of the two options represented by the dotted line of Figure 2.8 (a), because the usage of two integrators in a feedback loop can cause instability.

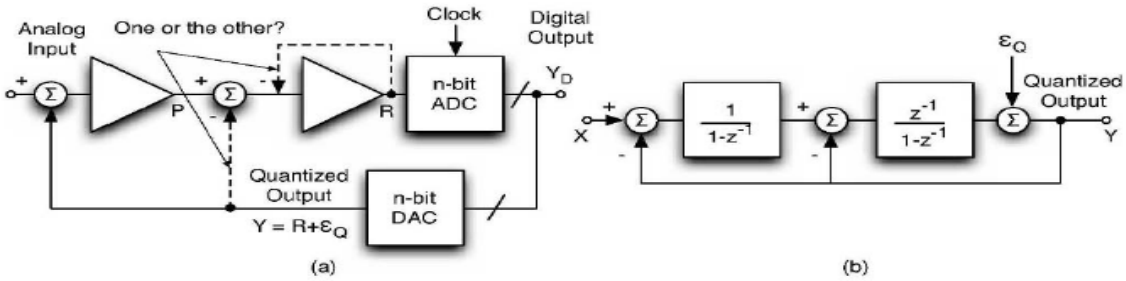


Figure 2.8 (a) Conceptual second order SD Modulator (b) block diagram of a second order SD modulator [6]

By analysis of the linear system in Figure 2.7 (b), it can be obtained the following;

$$\{[X(z)-Y(z)]\frac{1}{1-z^{-1}}-Y(z)\}\frac{z^{-1}}{1-z^{-1}}+E(z)=Y(z) \tag{2.20}$$

simplifying to

$$Y(z)=X(z)z^{-1}+E(z)(1-z^{-1})^2 \tag{2.21}$$

According to (2.12) and (2.21), the STF, $z^{-1}$, is just delay and the NTF is $(1-z^{-1})^2$, the square of the result achieved by a first-order SD modulator. As a result of this, increased attenuation of quantization noise at low frequencies is expected.

Moreover, SNR of the second order SD modulator is given by

$$SNR=\frac{12}{8}k^2\frac{5}{\pi^4}OSR^5 \tag{2.22}$$

where $k$ is the number of thresholds that ADC use (Detailed analysis of the PSD, in-band noise power, NTF, SNR are found in [6], [10] and [12]). So for the second-order SD modulator, the noise is attenuated by the fifth power of the oversampling ratio.

In addition to this, Figure 2.9 compares the NTF magnitude of first-order and second-order SD modulator where MOD1 is first-order SD modulator and MOD 2 is second-order SD modulator. At low frequencies, the NTF of MOD1 displays a 20 dB/decade slope, while the NTF of MOD2 has a 40 dB/decade slope. The increased attenuation at frequencies close to dc is desirable because it reduces the amount of quantization noise within the signal band. Unfortunately, the NTF of the second-order SD modulator is greater than first order SD modulator's NTF at high frequency region. As a result of this, the total power of the quantization noise at the output of MOD2 is more than that of MOD1 [12].

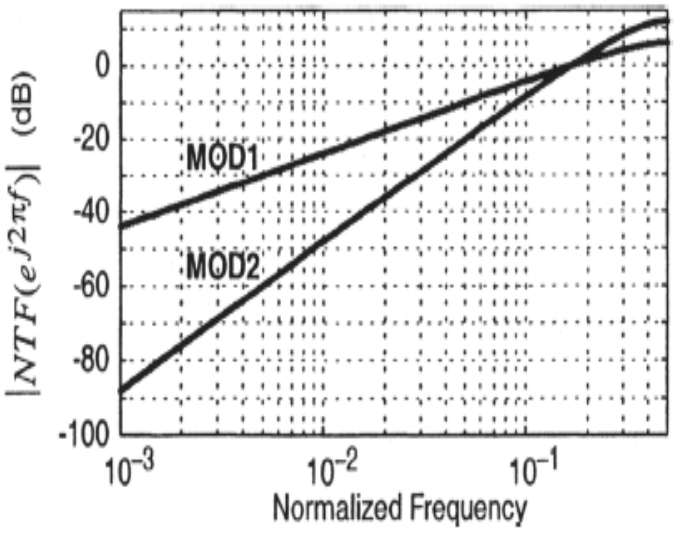


Figure 2.9 NTFs of the first and second order SD modulators [12]

Moreover, Figure 2.10 (a) shows a possible realization of sampled-data second-order SD modulator with two delayed integrators. A and B are the gains for the first and second integrator respectively. In addition to the benefit of an extra clock period which is available for the feedback loop implementation, the use of proper gains carries out appropriate signal and noise transfer functions. Also, it provides a scaling of the first integrator. Scaling by suitable attenuation at the input of the integrator is compensated by

an inverse amplification at the input of the next stage. Since the attenuation and the amplification neutralize each other, the response of the filter is unchanged but the output of the op-amp is optimized.

The equation describing the circuit is

$$\left[(X-Y)\frac{Az^{-1}}{1-z^{-1}}-Y\right]\frac{Bz^{-1}}{1-z^{-1}}+E=Y \tag{2.23}$$

giving rise to

$$Y=\frac{XABz^{-2}+E(1-z^{-1})^2}{1-(2-B)z^{-1}+(1-B+AB)z^{-2}} \tag{2.24}$$

The signal gain is 1 if AB=1; also, B=2 cancels the $z^{-1}$ and $z^{-2}$ terms of the decimator. Therefore, using A=1/2 and B=2 results in

$$Y=Xz^{-2}+E(1-z^{-1})^2 \tag{2.25}$$

which is the optimum choice and leads to the same transfer functions as the already studied second order modulator in Figure 2.8 (b). There is only one difference of an extra delay in the input transfer function. Because the gain of the first integrator is $1/2$, its output swing is reduced accordingly. The gain by 2 of the second integrator compensates for the first integrator attenuation. Detailed analyses about the second-order SD modulator given in Figure 2.10 (b) will be discussed in Chapter 4.

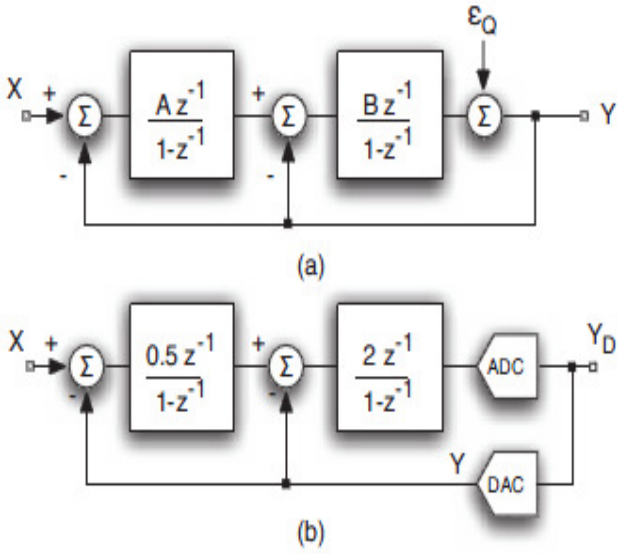


Figure 2.10 (a) Block diagram of a second order SD modulator with delayed integrators (b) optimum gains [6]

# 3. ARCHITECTURAL DESIGN

This chapter focuses on the arctitectural design of SD modulators which are used in the project. It starts with basic information about switched-capacitor building blocks that are necessary for the circuit design of blocks which take place in the block diagram of the SD modulators. Then, it goes on with properties of op-amp swing reduction and the architectural design of a second-order SD modulator given in [6] for low swing in the output of the first integrator. Finally, it finishes with the proposed architectural design of low power second-order SD modulator.

## 3.1. Swiched-capacitor building blocks

The switched capacitor (SC) technique is the basis for the circuit implementations of sampled-data SD modulators. As required by modulator architecture, it is possible to design integrators with delay or without delay by using SC blocks. Moreover, the subtraction of signals can be obtained with SC structures. SC building blocks are often classified into two categories: passive and active. A passive SC building block is defined as a network which is composed of switches and capacitors only, whereas its active counterpart is not only built from switches and capacitor. It is also built from active devices such as op-amps. Also, a MOS switch is an active device and it is composed of one or more transistors. In analog integrated circuits (ICs), the op-amp is usually regarded as the dividing line between passive and active integrated implementations [6, 13].

The circuit in Figure 3.1 is called the parasitic-sensitive paralel SC integrator. All parasitic capacitances can be ignored to simplify the analysis. Also, charge conservation is used in order to find the transfer characteristic of the integrator. Once $\Phi_1$ is off, the charge on the feedback capacitor $C_0$ will remain the same till $\Phi_1$ is on again. In other words, the charge on $C_0$ at the instant $nT$ (by the end of $\Phi_1$) is equal to that at the instant $(nT - T/2)$ (by the end of previous $\Phi_2$), so the following equation can be written [13]:

$$C_0 V_{out}(nT) = C_0 V_{out}(nT - T/2) \tag{3.1}$$

Similarly, at time $(nT-T)$, $C$ is charged to $CV_{in}(nT-T)$. Next, $\Phi_1$ is off and $\Phi_2$ is on; this charge $CV_{in}(nT-T)$ is thus sent to $C_0$ and combined with the existing charge across $C_0$, which is given by $C_0V_{out}(nT-T)$. The outcome is the charge. The polarity of $CV_{in}(nT-T)$ is opposite to $C_0V_{out}(nT-T)$. According to charge behaviour of the integrator from $(n-1)T$ till $(n-1/2)T$, the following charge equation can be obtained [13]:

$$C_oV_{out}(nT-T)-CV_{in}(nT-T)=C_0V_{out}(nT-T/2) \tag{3.2}$$

When these two equations are combined and the z-transform is applied to both side of the resulting equation, the following equation can be got [13]

$$C_oV_{out}(z)=C_0V_{out}(z)z^{-1}-CV_{in}(z)z^{-1} \tag{3.3}$$

Then, the transfer function of the integrator in Figure 3.1 can be found by using the equation:

$$H(z)=\frac{V_{out}(z)}{V_{in}(z)}=-\frac{C}{C_0}\frac{1}{z-1}=-\frac{C}{C_0}\frac{z^{-1}}{1-z^{-1}} \tag{3.4}$$

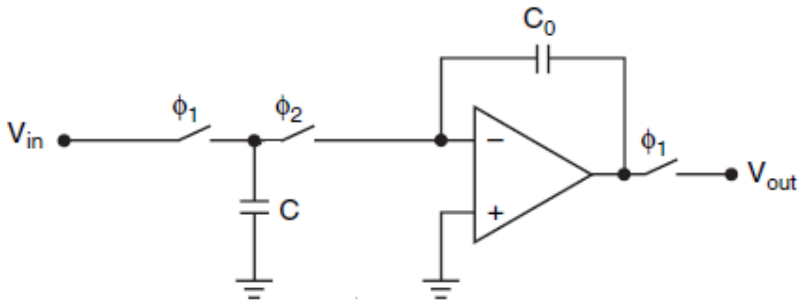


Figure 3.1. Parasitic-sensitive paralel SC integrator [13]

Transfer functions of parasitic-sensitive SC integrators are affected by parasitic capacitances. So, parasitic-insensitive SC integrators which are given in Figure 3.2 are used in this project instead of parasitic-sensitive SC integrators.

The transfer function of the integrator in Figure 3.2 (a) can be found by analysing the charge behaviour of the integrator as done for the integrator in Figure 3.1 and comparing these two SC integrators. The polarity of the net charge transferred from $V_{in}$ to $V_{out}$ is the key difference between these two integrators. During $\Phi_1$ is on, in Figure 3.1 the input $V_{in}$ is charged onto the top plate of $C$, while in Figure 3.2 (a) the input is charged onto the bottom plate of $C$. As a result of this, the transfer function of the integrator in Figure 3.2 (a) has a sign opposite to the transfer function of the integrator in Figure 3.1 because the polarity of the transfer function is determined by the that of the net charge. Then, the transfer function of the integrator in Figure 3.2 (a) is given as following [13]:

$$H(z) = \frac{V_{out}}{V_{in}} = \frac{C}{C_0} \frac{z^{-1}}{1 - z^{-1}} \tag{3.5}$$

Moreover, the transfer functions of the other integrators given in Figure3.2 (b), (c) and (d) can also be found by using charge conservation and these functions are given as following, respectively [13]:

$$H = \frac{V_{out}}{V_{in}} = -\frac{C}{C_0} \frac{z^{-1}}{1 - z^{-1}} \tag{3.6}$$

$$H = \frac{V_{out}}{V_{in}} = \frac{C}{C_0} \frac{1}{1 - z^{-1}} \tag{3.7}$$

$$H = \frac{V_{out}}{V_{in}} = -\frac{C}{C_0} \frac{1}{1 - z^{-1}} \tag{3.8}$$

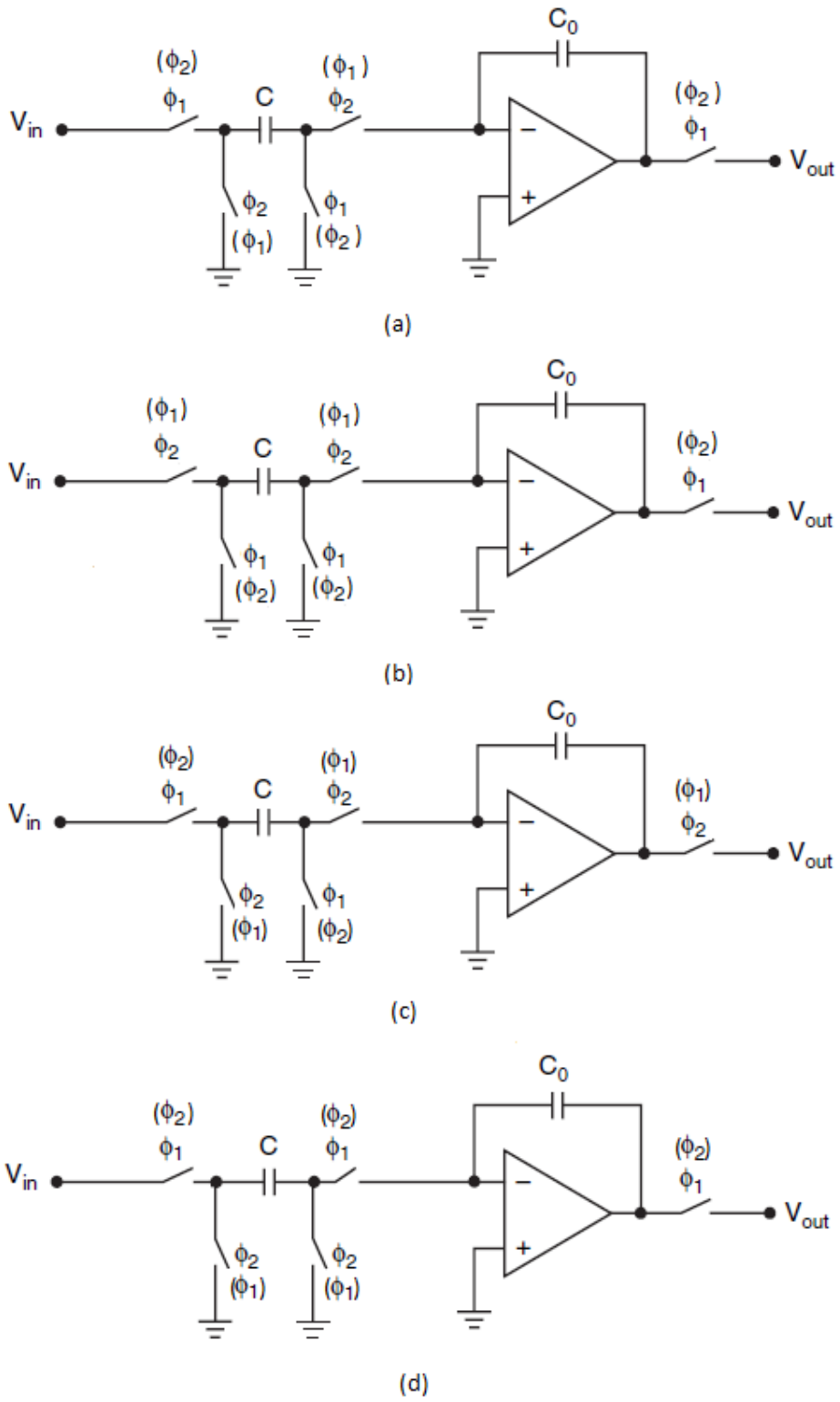


Figure 3.2. Parasitic insensitive SC integrators [6, 13]

### 3.2. Op-amp Swing Reduction

For low voltage and high speed applications, designers must optimize the output swing and the speed performance of the op-amp utilized in the modulators. In addition to this, using a suitable dynamic range in the op-amps is necessary for protecting the SNR and avoiding harmonic distortion. The most critical is the first integrator because its saturation error is not shaped by any transfer function. On the other hand, the saturation of the second integrator and the saturation of the quantizer are also limits to the modulator performances. It is therefore necessary to estimate the expected voltage swings carefully and to keep them within limits which are not large enough to cause saturation, but, at the same time, are not so low to become comparable with the electronic noise [6].

The first op-amp swing can be reduced by using a feed-forward path which compensates for the feedback signal contribution. The architecture with the feed-forward path in [6] is given in Figure 3.3.

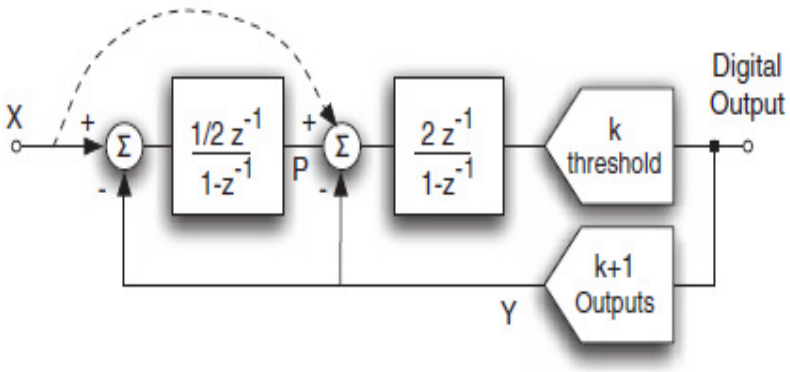


Figure 3.3. Block diagram of a second order modulator with the feed-forward path [6]

Before we examine the second-order modulator with the feed-forward path, it is more clear if we find the output of the first integrator in Figure 2.10 (b). This output, $P$, can be found as following:

$$P = (X - Y)\frac{1/2z^{-1}}{1-z^{-1}} \tag{3.9}$$

Using (2.25), (3.9) results in

$$\begin{aligned} P(z) &= \left[ X(z) - X(z)z^{-2} - E(z)(1-z^{-1})^2 \right] \frac{1/2z^{-1}}{1-z^{-1}} \\ &= X(z)\frac{z^{-1}(1+z^{-1})}{2} + E(z)\frac{z^{-1}(1-z^{-1})}{2} \end{aligned} \tag{3.10}$$

If (3.10) is examined, it can be seen that the first term dominates the equation. The second term which is equal to the quantization error is attenuated by 2 and passes through a first order high pass transfer function.

By analysis of the architecture with the feed-forward path in Figure 3.3, the following can be obtained:

$$\left\{ \left[ X(z) - Y(z) \right] \frac{1/2z^{-1}}{1-z^{-1}} - Y(z) + X(z) \right\} \frac{2z^{-1}}{1-z^{-1}} + E(z) = Y(z) \tag{3.11}$$

using (3.11), the output , $Y(z)$, is

$$Y(z) = X(z)\left[ z^{-2} + 2z^{-1}(1-z^{-1}) \right] + E(z)(1-z^{-1})^2 \tag{3.12}$$

Then, by using (3.12), the output of the first integrator $P(z)$ in Figure 3.3 can be found as

$$\begin{aligned} P(z) &= \left[ X(z) - Y(z) \right] \frac{1/2z^{-1}}{1-z^{-1}} \\ &= \left\{ X(z) - X(z)\left[ z^{-2} + 2z^{-1}\left(1-z^{-1}\right) \right] - E(z)(1-z^{-1})^2 \right\} \frac{1/2z^{-1}}{1-z^{-1}} \\ &= X(z)\frac{z^{-1}(1-z^{-1})}{2} + E(z)\frac{z^{-1}(1-z^{-1})}{2} \end{aligned} \tag{3.13}$$

If this equation is compared with (3.10), a major reduction of $X(z)$ contribution can be seen easily. According to (3.13), $X$ passes through a high pass $\left(1-z^{-1}\right)$ filter which

causes a large attenuation. (Circuit implementation and analysis results will be discussed in Chapter 4 in great detail.)

The reduction of the swing in the second integrator is not as important as for the first one. The dynamic range of the second op-amp can be scaled down by increasing the feedback capacitor in the integrator. The reference voltage of the quantizer must be reduced accordingly. On the other hand, having a signal at the op-amp output with small amplitude and noise-like can be beneficial for harmonic distortion [14].

The benefit of the feed-forward path in reducing the op-amp swing can be explained by an opinion. If the input of the second block is, on average, zero, its output is limited because the second block is an integrator. In turn, as the input of the second integrator is made by three terms, $-Y, P$ and $X$, it must be verified that $-Y+P+X \simeq 0$. Recall now that the output follows the input with a difference that is in the order of the quantization error. Accordingly, the condition $P \simeq Y-X$ indicates that $P$ is also in the order of the quantization error, and has a fairly small amplitude for quantization [6].

### 3.3.Proposed Architecture for Low Power Second Order SD Modulator

In previous section, we discussed how output swing reduction and dynamic range affect the power consumption and performance of SD AD Converters. In [6], by using feed-forward path, a term which is proportional to $\left(1-z^{-1}\right)$ times of input signal is found in the output of the first integrator. When this value is compared with the amplitude of the output of the first integrator in the second order SD modulator with optimum gains in Figure 2.10 (b), it is seen that the swing of the first integrator decreases with an additional branch. Taking this fact into consideration, we aimed to construct a new second-order SD modulator which has a lower value than a term that is multiplied by $\left(1-z^{-1}\right)$ at the output of the first integrator. In order to achieve this aim, we decide to obtain $\left(1-2z^{-1}+z^{-2}\right)$ times of input signal at the output of the first integrator and $z^{-2}$ times of input signal at the output of the second integrator. The desired architecture of SD modulator is given in Figure 3.4.

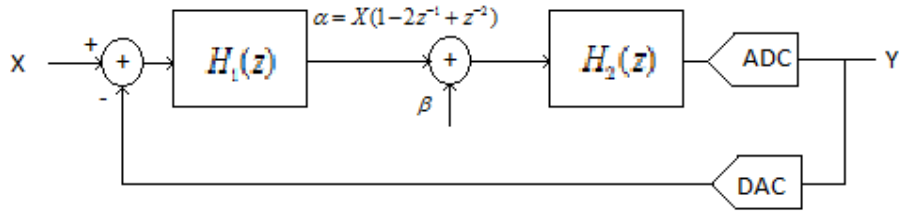


Figure 3.4. Sketch of the proposed second order SD modulator

According to the Figure 3.4, the output of the second integrator is $Y$ and the output of the SD ADC is $Y+E$ because of the quantization. If we ignore quantization noise for the calculation of the input of the first integrator, we can get the following:

$$X(z)-Y(z)=X(z)-X(z)z^{-2}=X(z)(1-z^{-2}) \tag{3.14}$$

Then, the transfer function of the first integrator can be found by using (3.14) and output of the first integrator, as a result, we can obtain the equation:

$$H_1(z)=\frac{X(z)\left(1-2z^{-1}+z^{-2}\right)}{X(z)-Y(z)}=\frac{X(z)\left(1-2z^{-1}+z^{-2}\right)}{X(z)\left(1-z^{-2}\right)}=\frac{1-z^{-1}}{1+z^{-1}} \tag{3.15}$$

Circuit implementation of the first integrator using switched capacitors will be explained in Chapter 4 in detail.

Furthermore, by inspection of the circuit we can get the following equation in order to find the tranfer function of the second integrator.

$$H_2(z)=\frac{Y(z)}{\alpha+\beta}=\frac{X(z)z^{-2}}{\left(1-2z^{-1}+z^{-2}+\beta\right)}=\frac{K_1+K_2z^{-1}}{1-z^{-1}} \tag{3.16}$$

where $K_1$ and $K_2$ are coefficients for the second integrator. Then (3.16) can be enlarged to

$$z^{-2}-z^{-3}=K_1-2K_1z^{-1}+K_1z^{-2}+K_2z^{-1}-2K_2z^{-2}+K_2z^{-3}+\frac{\beta}{X(z)}\left(K_1+K_2z^{-1}\right) \tag{3.17}$$

If we choose $K_1 = 0$ and $\beta = X(z) - Y(z) = X(z)\left(1 - z^{-2}\right)$, (3.17) can be simplified to

$$z^{-2} - z^{-3} = \left(K_2 z^{-1} - 2K_2 z^{-2} + K_2 z^{-3}\right) - \left(K_2 z^{-1} - K_2 z^{-3}\right) = \left(-2K_2 z^{-2} + 2K_2 z^{-3}\right) \quad (3.18)$$

So, we can get $K_2 = -0.5$ from (3.18). As a result of this analysis, the transfer function of the second integrator is found as:

$$H_2(z) = \frac{Y(z)}{\alpha + \beta} = \frac{X(z) z^{-2}}{X(z)\left(1 - 2z^{-1} + z^{-2}\right) - X(z)\left(1 - z^{-2}\right)} = -\frac{0.5 z^{-1}}{1 - z^{-1}} \quad (3.19)$$

By moving the minus signal to earlier steps in Figure 3.4, the transfer function of the second integrator is rescued from that signal. This helps us for easier circuit design. Circuit implementation of the second integrator using switched capacitors will be explained in Chapter 4 in detail.

After the transfer functions of the first and the second integrators, the feedback path and the feed-forward path are found, the architecture of the proposed second-order SD modulator forms as following:

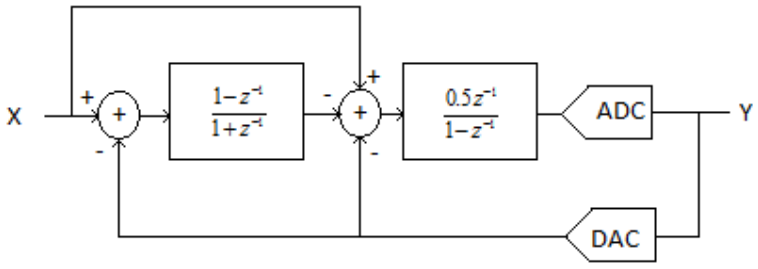


Figure 3.5. Block diagram of the proposed SD modulator

By analysis of the proposed architecture in Figure 3.5, it can be obtained the following:

$$\left\{X(z) - \left[X(z) - Y(z)\right]\frac{1 - z^{-1}}{1 + z^{-1}} - Y(z)\right\}\frac{0.5 z^{-1}}{1 - z^{-1}} + E(z) = Y(z) \quad (3.20)$$

simplifying to

$$X(z)z^{-2} + E(z)z^{-2} = Y(z) \tag{3.21}$$

Then, by using (3.21), the output of the first integrator $P(z)$ in Figure 3.5 can be found as

$$\begin{aligned} P(z) &= \left[X(z) - Y(z)\right]\frac{1-z^{-1}}{1+z^{-1}} \\ &= \left\{X(z) - \left[X(z)z^{-2} + E(z)\left(1-z^{-2}\right)\right]\right\}\frac{1-z^{-1}}{1+z^{-1}} \\ &= X(z)\left(1-2z^{-1}+z^{-2}\right) + E(z)\left(1-2z^{-1}+z^{-2}\right) \end{aligned} \tag{3.22}$$

If this equation is compared with (3.10) and (3.13), it can be seen that (3.22) has the lowest $X(z)$ contribution.

# 4. CIRCUIT DESIGN AND ANALYSIS RESULTS

This chapter focuses on circuit implementations of three second order SD modulators that are mentioned in previous chapters and their comparison using analysis results. In switched capacitor building blocks, firstly, a single transistor is used as a switch. Then, transmission gates are used for all switches for better results. In addition to this, analysis have been revised for an ideal op-amp, a new designed op-amp, a differential amplifier and an inverter. As a result, it can be seen that the proposed second order SD modulator has less voltage swing at the output of the first integrator. Therefore, op-amps with less power comsumption and an inverter as an op-amp can be used in this design.

In all circuit design, the sampling frequency is 2,5 MHz and OSR is equal to 64.

## 4.1.Circuit Implementations with an Differential Ideal-opamp and a Transmission Gate as a Switch

Firstly, block diagrams that are given in Figure 2.10 (b), Figure 3.3 and Figure 3.5, are built respectively by using a single transistor as a switch. After these circuit implementations are justified, transmission gates are used as switches instead of transistors because transmission gates have better performance than transistors as a switch. Also differential ideal op-amps are used in this part of the study.

### 4.1.1. Second Order SD Modulator with Optimum Gains

The block diagram of the second-order SD modulator with optimum gains is given in the Figure 2.10 (b). Taking this block diagram as a reference, the circuit is implemented by using ideal op-amps and switched capacitor blocks given in Figure 3.2. The circuit implementation of second-order SD modulator with optimum gains is given below:

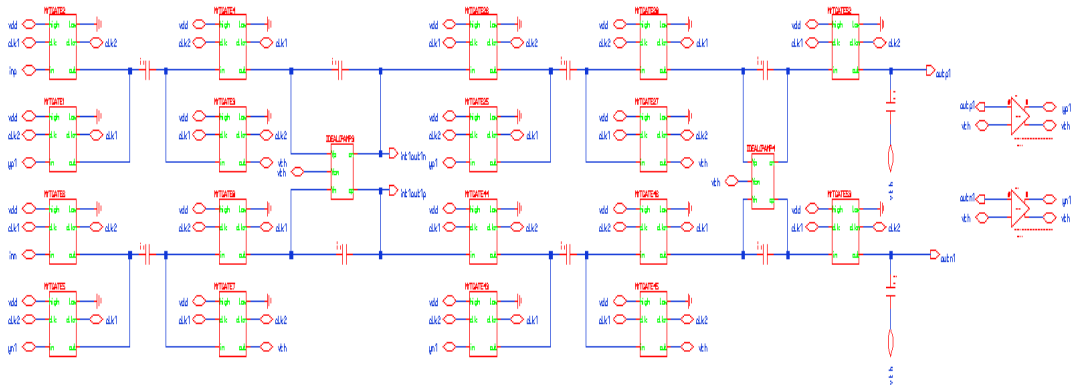

Figure 4.1. Circuit implementation of second order SD modulator with optimum gains by using ideal op-amps

Then, the circuit is simulated to see how the second order SD modulator with optimum gains works. The simulations result are given in Figure 4.2 where V(INN) is the input signal of the circuit and; V(YN1) is output of the SD AD converter. Also, V(INTOUTN1) is the first integrator output and V(OUTN1) is the second integrator output.

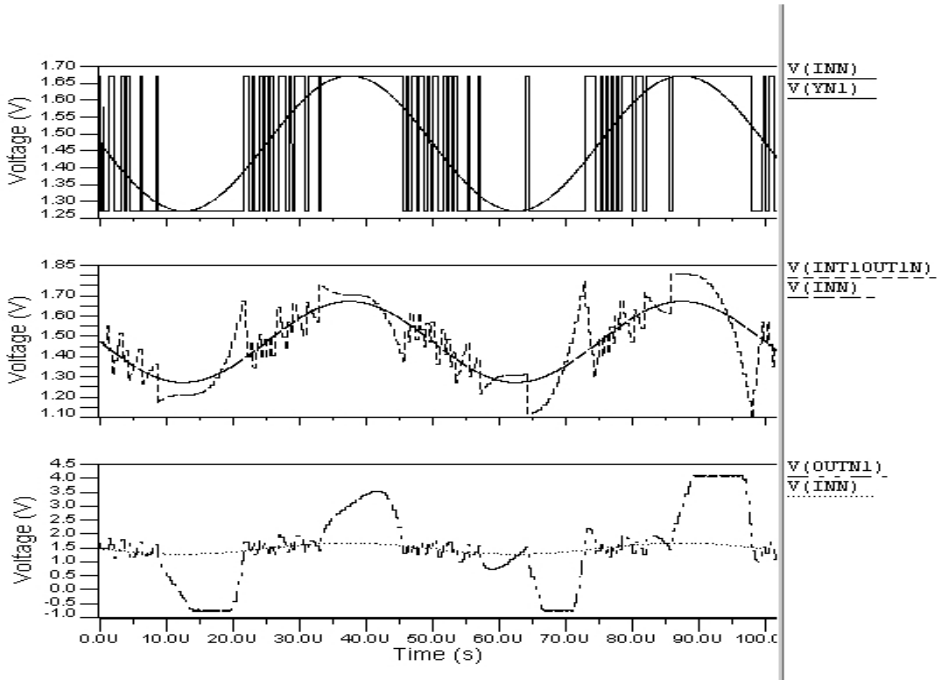


Figure 4.2.Simulation results of second order SD modulator with optimum gains by using ideal op-amps

According to Figure 4.2, output of the circuit is 1 when the input has maximum value. On the other hand, output is 0 when the input has minimum value. Also, the output is changeable in intermediate values. These are the expected results from SD AD converter.

### 4.1.2.Second Order SD Modulator with Feed-forward Path

As it is mentioned before, using feedforward path in the design of SD modulators is a very effective way of reducing the voltage swing of the first integrator. The circuit implementation of the architecture given in Figure 3.3 is carried out as below with the help of using SC building blocks in Figure 3.2 and ideal op-amps:

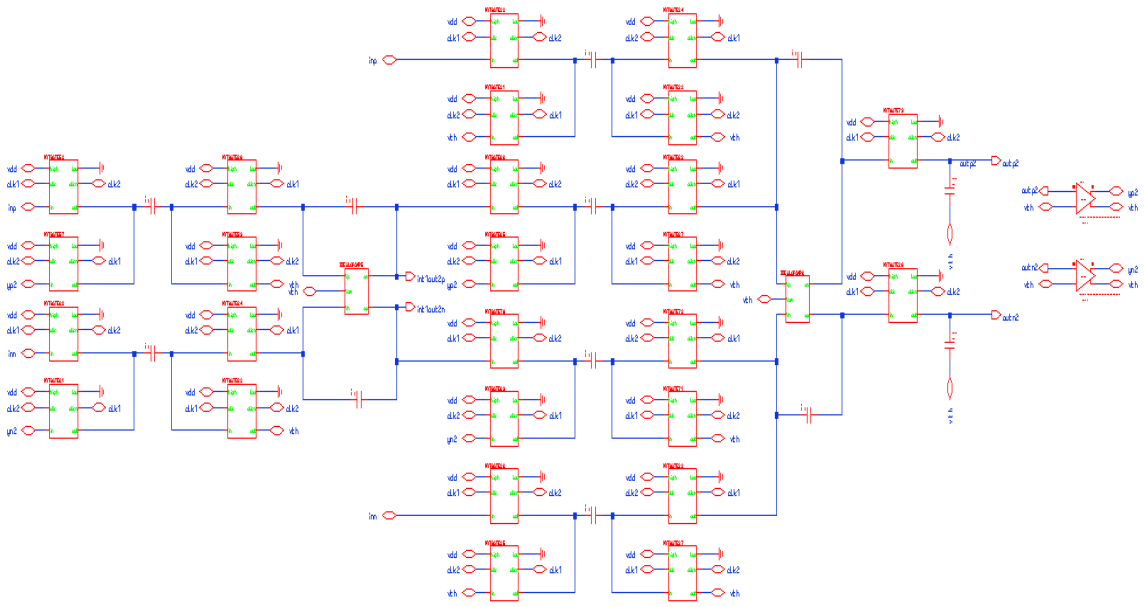

Figure 4.3. Circuit implementation of second order SD modulator with feed-forward path by using ideal op-amps

Then, the circuit is simulated in order to see the relationship between the inputs and the outputs of the circuit. The simulation results are given in Figure 4.4 where V(INN) is the input signal of the circuit and; V(YN2) is the output of the SD AD converter. Moreover, first and second integrator outputs can be seen from Figure 4.4. V(INT1OUT2N) is the output of the first integrator while V(OUTN2) is the output of the second integrator.

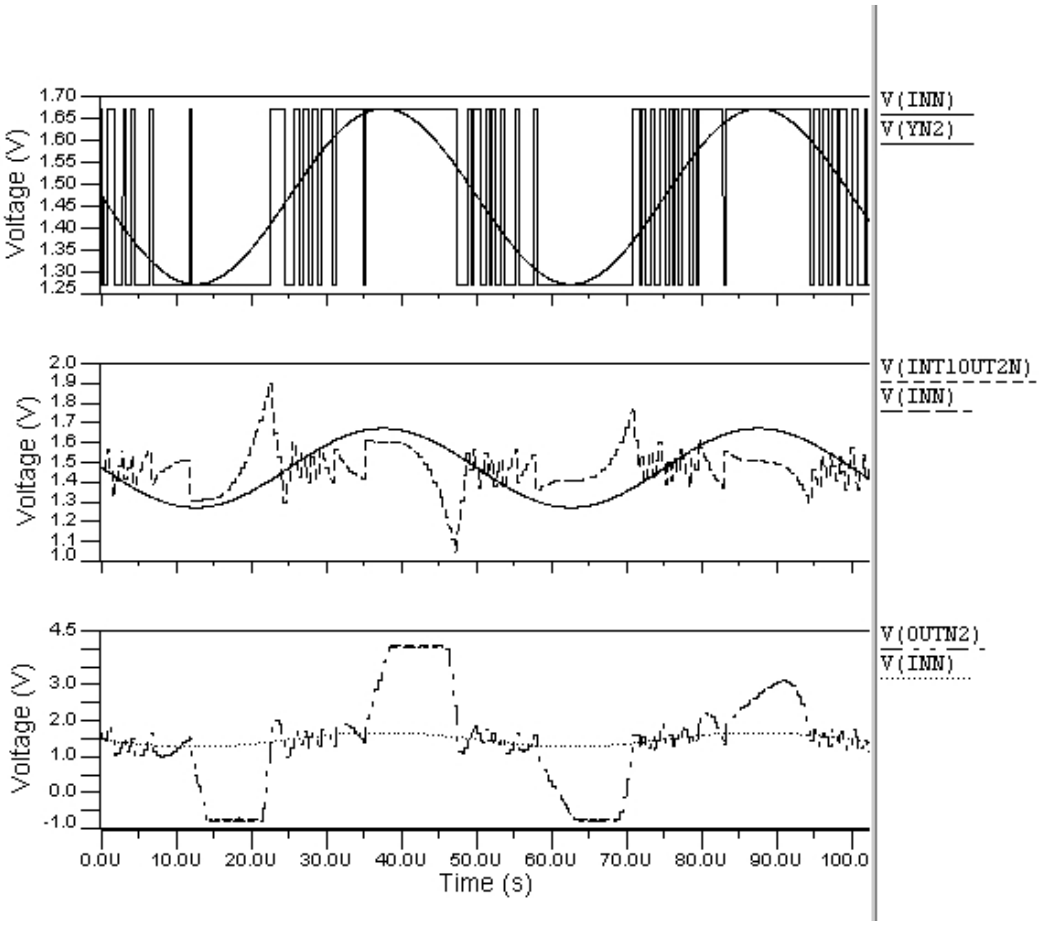


Figure 4.4. Simulation results of second order SD modulator with feed-forward path by using ideal op-amps

It can be seen from Figure 4.4 that the SD modulator works and the voltage swing at the first integrator output is lower compared to Figure 4.2. This verifies that feed-forward path is an effective way for reducing op-amp swing.

### 4.1.3.Proposed Low Power Second Order SD Modulator

The architecture of the proposed second order SD modulator is given in Figure 3.5. If the block diagram is examined, it is seen that transfer functions of the integrators in Figure 3.5 are different from transfer functions of the SC building blocks given in Figure 3.2. The calculations that are used for finding the transfer functions of the first and the second integrator, the feedback path and the feed-forward path in Figure 3.5 were given in previous chapter.

Before entire circuit implementation of the architecture is explained, the implementation of this different integrator should be provided. The transfer function of the first integrator in Figure 3.5 is

$$H_1(z) = \frac{1 - z^{-1}}{1 + z^{-1}} \tag{4.1}$$

To generate this transfer function, the following equation can use used:

$$Y = X \frac{K_1 + K_2 z^{-1}}{1 - z^{-1}} + Y \frac{K_3 + K_4 z^{-1}}{1 - z^{-1}} \tag{4.2}$$

where $Y$ is the output and $X$ is the input of the integrator; and $K_1$, $K_2$, $K_3$ and $K_4$ are coefficients for the integrator. (4.2) causes

$$\begin{aligned} Y(1 - z^{-1}) &= X(K_1 + K_2 z^{-1}) + Y(K_3 + K_4 z^{-1}) \\ Y(1 - K_3 - K_4 z^{-1} - z^{-1}) &= X(K_1 + K_2 z^{-1}) \\ \frac{Y}{X} &= \frac{(K_1 + K_2 z^{-1})}{(1 - K_3 - K_4 z^{-1} - z^{-1})} = \frac{1 - z^{-1}}{1 + z^{-1}} \end{aligned} \tag{4.3}$$

According to (4.3), coefficients, $K_1$, $K_2$, $K_3$ and $K_4$ can be chosen as 1, -1, 0 and -2 respectively. Instead of using $K_1$, $K_2$ and switches, a single capacitor can be used in the design of the first integrator because a single capacitor can be identified as $(1 - z^{-1})$. Figure 4.5 shows the circuit implementation of the first integrator with single transistors as switches.

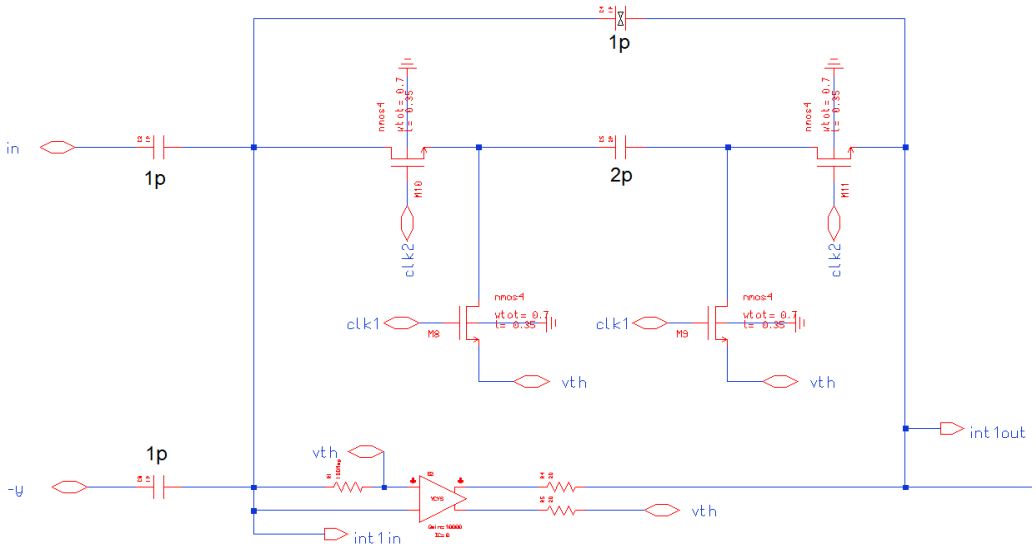


Figure 4.5. Design of the first integrator of the proposed SD modulator

Then, using the transfer function that was found in the previous chapter, the second integrator is implemented with single transistors as swiches and SC building block given in Figure 3.2 (a). Figure 4.6 shows the implementation of the second integrator.

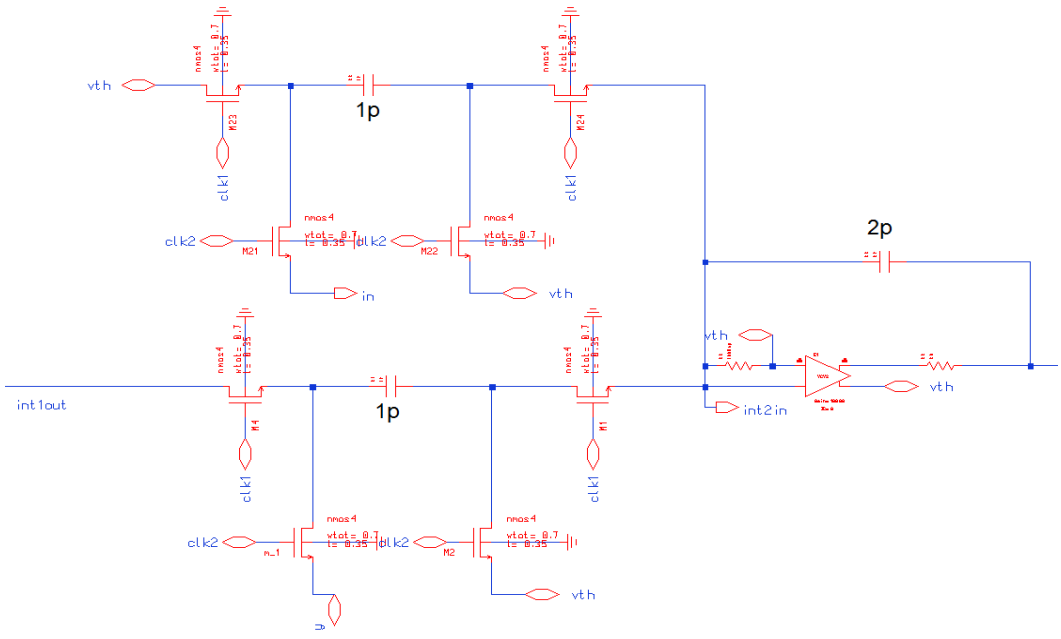


Figure 4.6. Design of the second order of the proposed SD modulator

Now, the architecture which is given in Figure 3.5 can be carried out with differential ideal op-amps and transmission gates as switches. The circuit implementation is given in Figure 4.7.

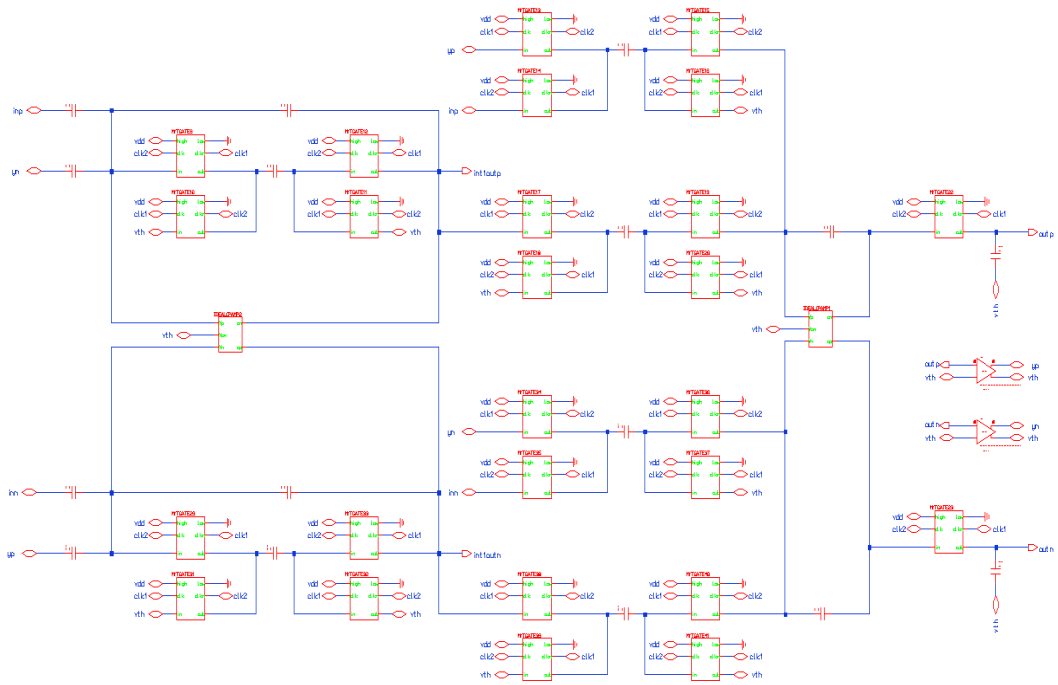

Figure 4.7. Circuit implementation of proposed SD modulator by using ideal op-amps

Furthermore, the circuit is simulated and the relationship between the inputs and the outputs are found in Figure 4.8 where V(INN) refers the input signal of the circuit and V(YN) refers the output of the SD AD converter. Also, V(INTOUTN) is the output of the first integrator and V(OUTN) is the output of the second integrator.

According to Figure 4.8, the proposed SD modulator works well as a converter and has very low voltage swing at the output of the first integrator.

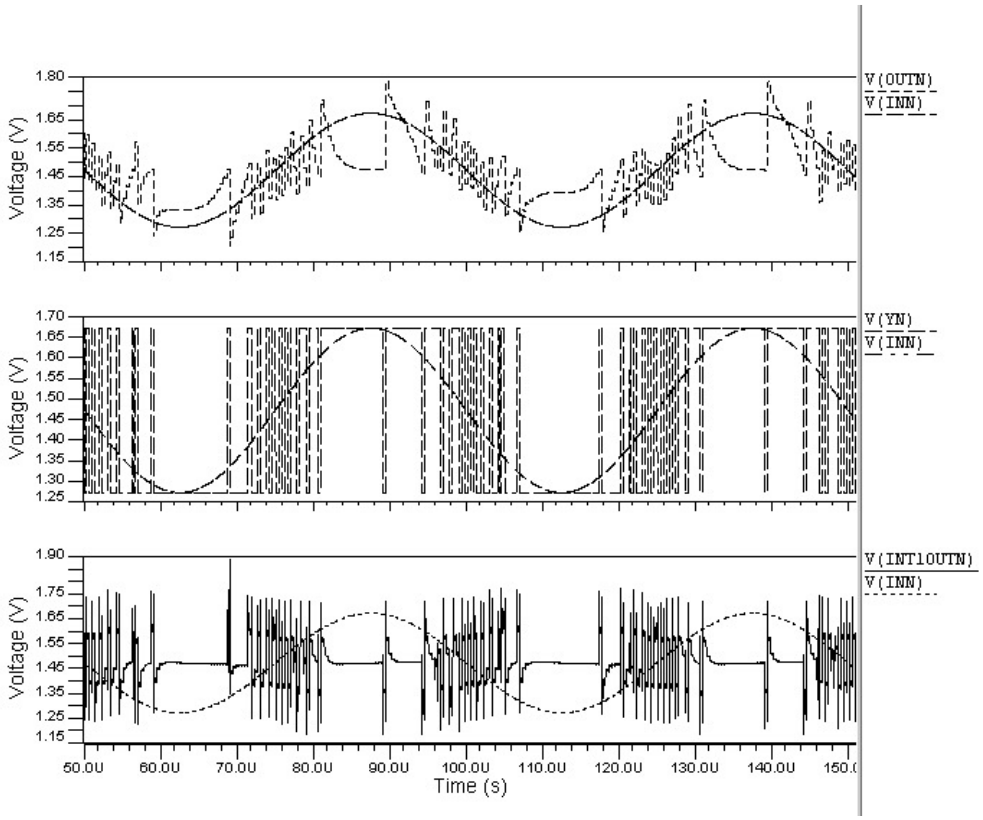


Figure 4.8. Simulation results of second order proposed SD modulator by using ideal op-amps

### 4.1.4. Analysis Results

As mentioned before, the swing at the output of the first integrator is more important than the swing at the second integrator output. So, outputs of the first integrators should be analyzed. Figure 4.9 shows the comparison of first integrators outputs of three second order SD modulators where V(INTOUT1N) and V(INTOUT1P) are first integrator outputs of Figure 2.10 (b), V(INTOUT2N) and V(INTOUT2P) are first integrator outputs of Figure 3.3 and V(INTOUTN) and V(INTOUTP) are first integrator outputs of Figure 3.5.

The outputs of the second order SD modulator with feed-forward path and proposed second order SD modulator are quite different from a sine wave. Figure 4.9 verifies the comparison of (3.10), (3.13) and (3.22). In other words, proposed architecture has the lowest voltage swing at the output of the first integrator. Moreover, to understand results of

the analysis more easily, the histograms of the first integrators which are shown in Figure 4.10 can be used. These histograms compare output voltage distributions of the first integrators of three SD modulators. Y axis shows the number of occurence of the voltage interval that is shown in X axis. According to these histograms, it can be easily seen that values are gathered at the center of the figure in the histogram for the proposed architecture. It means that output mostly takes these values and therefore, the voltage swing at the output of the first integrator of proposed architecture is the lowest one. As a result of low voltage swing, it is decided to test all circuits with a new designed op-amp instead of an ideal op-amp and examine the power consumption of circuits. Because low voltage swing at the first integrator output enables to use worse op-amps in the design. In order to achieve this, the next section will introduce a differential folded-cascode op-amp modified from the op-amp in [15] and analysis results of three SD modulators with this real op-amp.

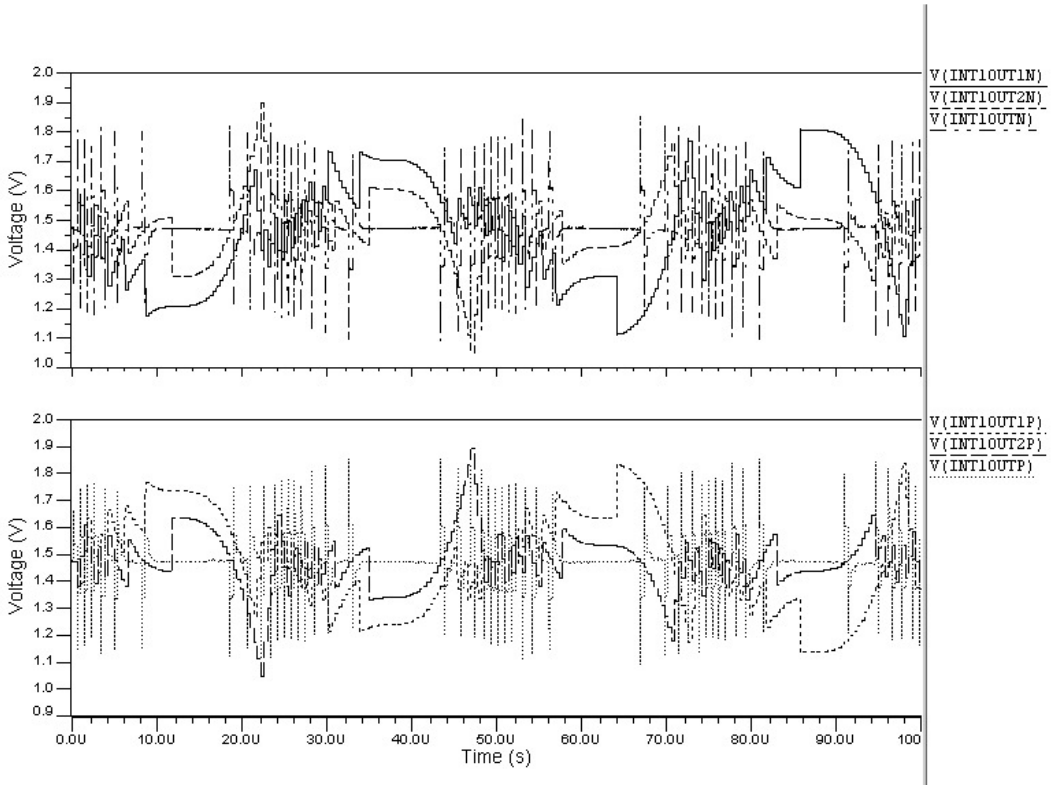


Figure 4.9. Comparison of the first integrator outputs of three SD modulator (ideal op-amps)

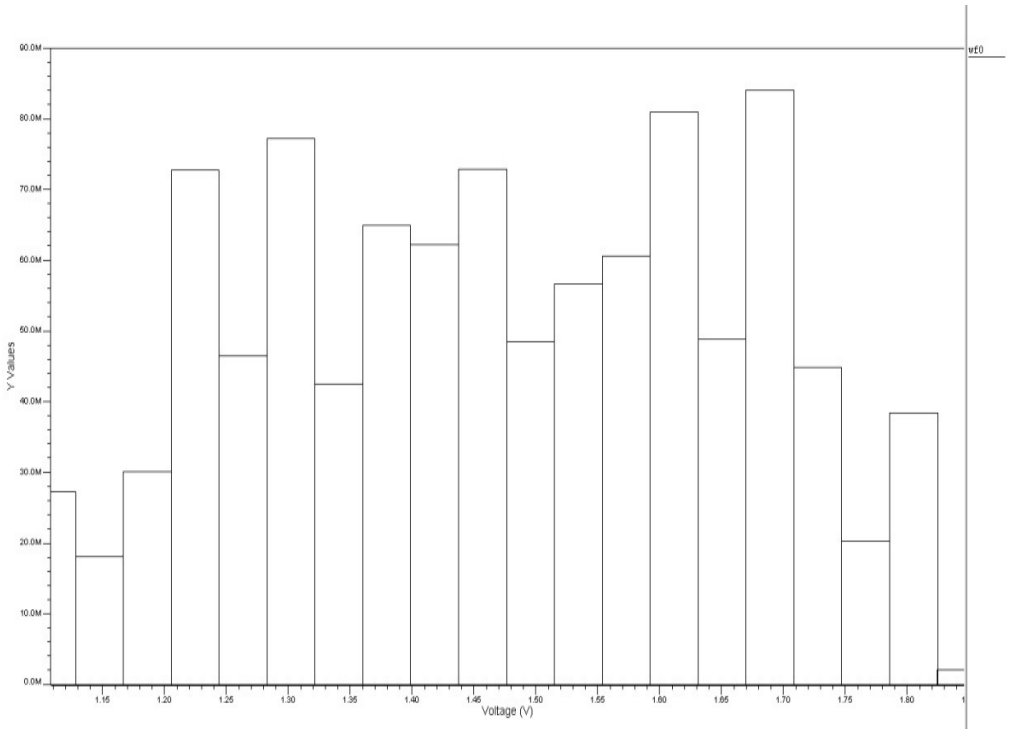


Figure 4.10. Histogram of output of the first integrator with optimum gains (ideal op-amp)

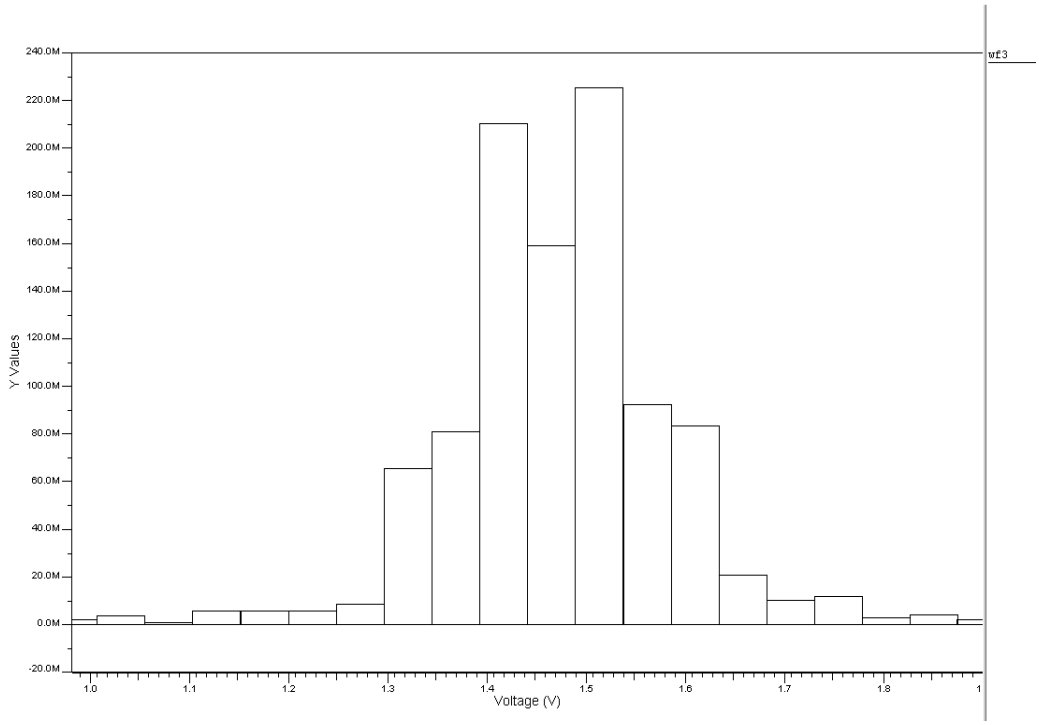


Figure 4.11. Histogram of output of the first integrator with feed-forward path (ideal op-amp)

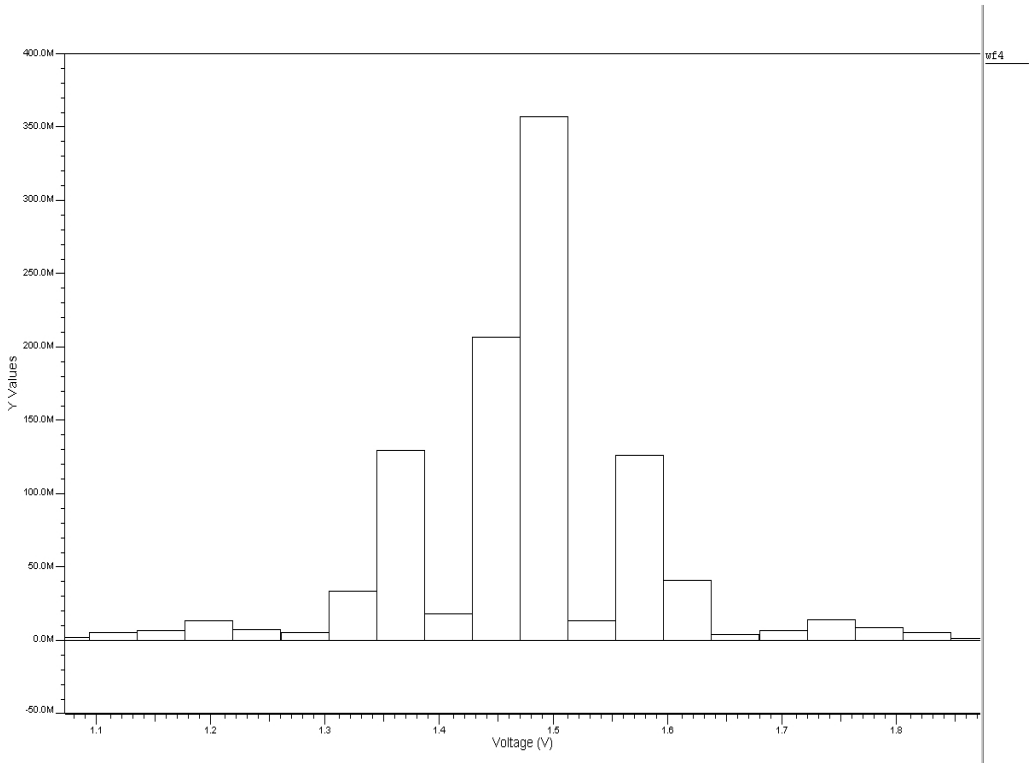


Figure 4.12. Histogram of output of the first integrator of the proposed architecture (ideal op-amp)

### 4.2. Circuit Implementations with a New Designed Differential Op-amp

A folded-cascode op-amp has been designed in order to be used instead of ideal op-amps. The specifications of this op-amp are as follows: Gain=76,5 dB, GBW= 200 MHz, BW=55 kHz. The output DC level of the op-amp is $1.472V$ and the bias voltages are $V_{nb} = 1.83V$ and $V_{pb} = 2.1V$ . Figure 4.13 shows the schema of the designed differential op-amp.

The op-amp has been designed as folded cascode to have a high gain by using only a single stage, and consequently to avoid any need for frequency compensation, which decreases the speed of the op-amp. More information about folded cascode op-amps can be found in [7].

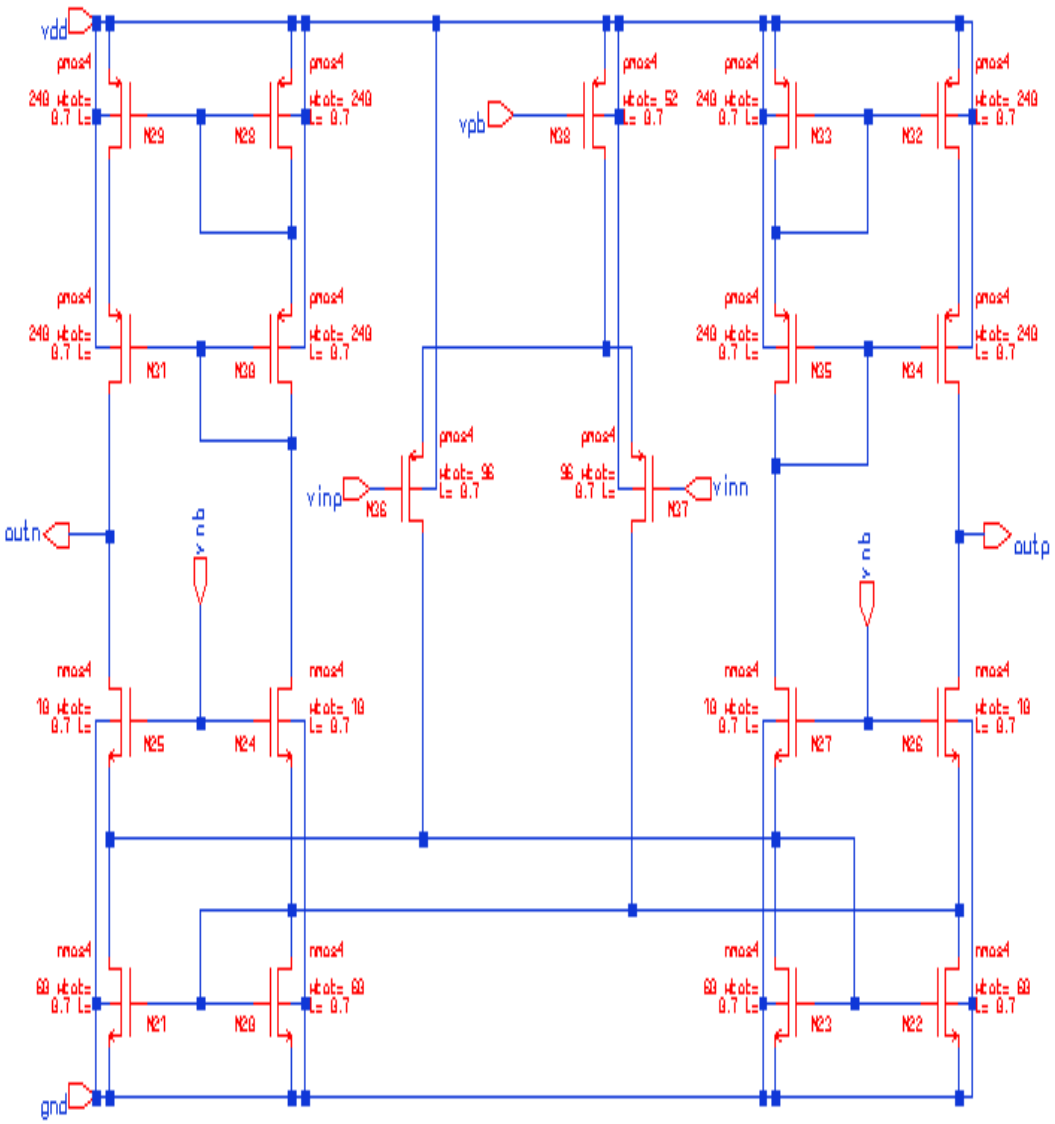


Figure 4.13. Differential folded-cascode op-amp

### 4.2.1.Second order SD modulator with optimum gain

The designed op-amp is swapped with ideal op-amps in Figure 4.1. The circuit implementation has turned out the following schematic:

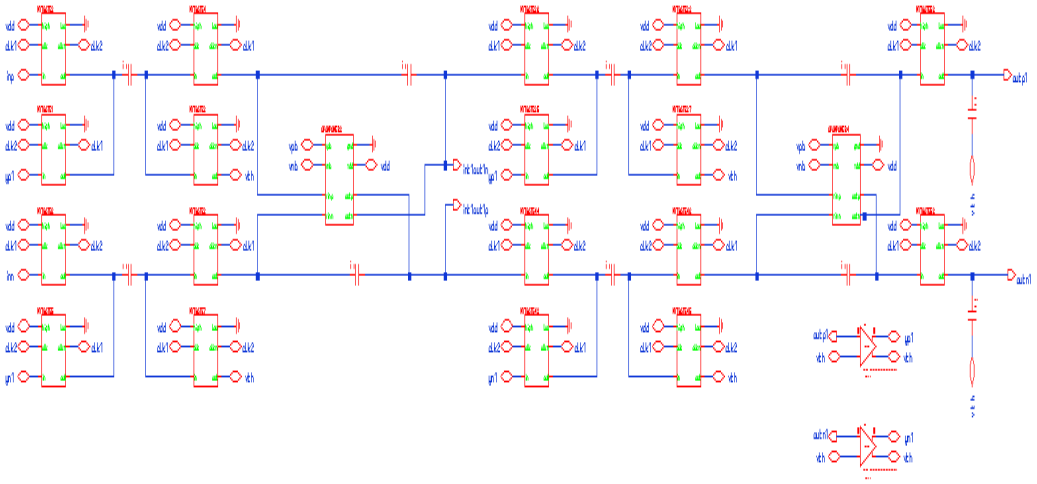

Figure 4.14. Circuit implementation of second order SD modulator with optimum gains by using real op-amps

Figure 4.15 shows the simulation result of the circuit in Figure 4.14 where V(INN) is the input signal of the circuit and V(YN1) is the output of the SD AD converter. Moreover, V(INTOUTN1) is the output of the first integrator and V(OUTN1) is the output of the second integrator.

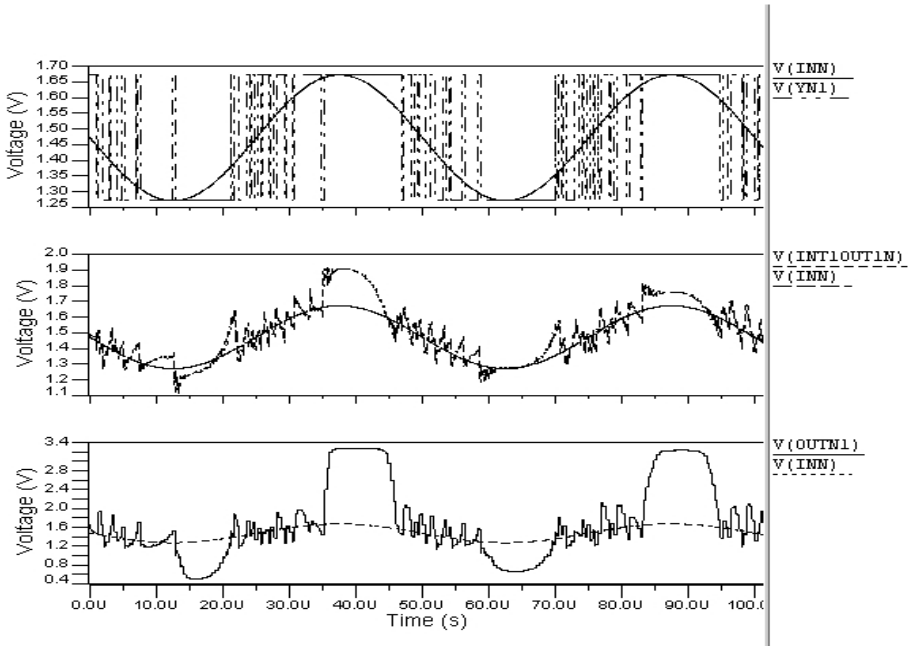


Figure 4.15. Simulation results of second order SD modulator with optimum gains by using real op-amps

According to Figure 4.15, the second order SD modulator with optimum gains still works with the designed op-amp.

### 4.2.2.Second order SD modulator with feed-forward path

The designed differential folded-cascode op-amp is used instead of ideal op-amps in Figure 4.3. Figure 4.16 shows the circuit implementation of the second-order SD modulator with feed-forward path and the new op-amp.

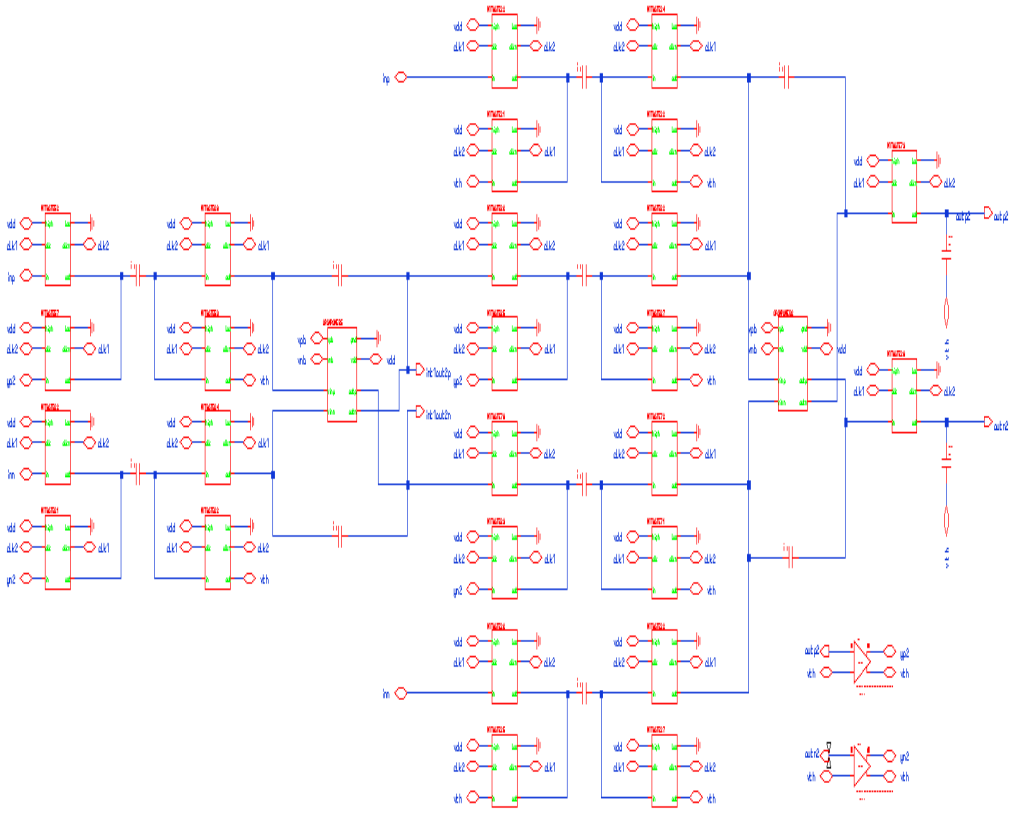

Figure 4.16. Circuit implementation of second order SD modulator with feed-forward path by using real op-amps

Figure 4.17 shows relationship between inputs and outputs of the SD AD converter which is given in Figure 4.16. V(INN) is the input signal of the circuit and V(YN2) is the output of the SD AD converter. Also, V(INTOUTN2) is the output of the first integrator and V(OUTN2) is the output of the second integrator.

It can be seen from Figure 4.17 that SD modulator with the feed-forward path still functions properly when the new op-amp is used in the design. Also its swing is lower than that of circuit in Figure 4.14.

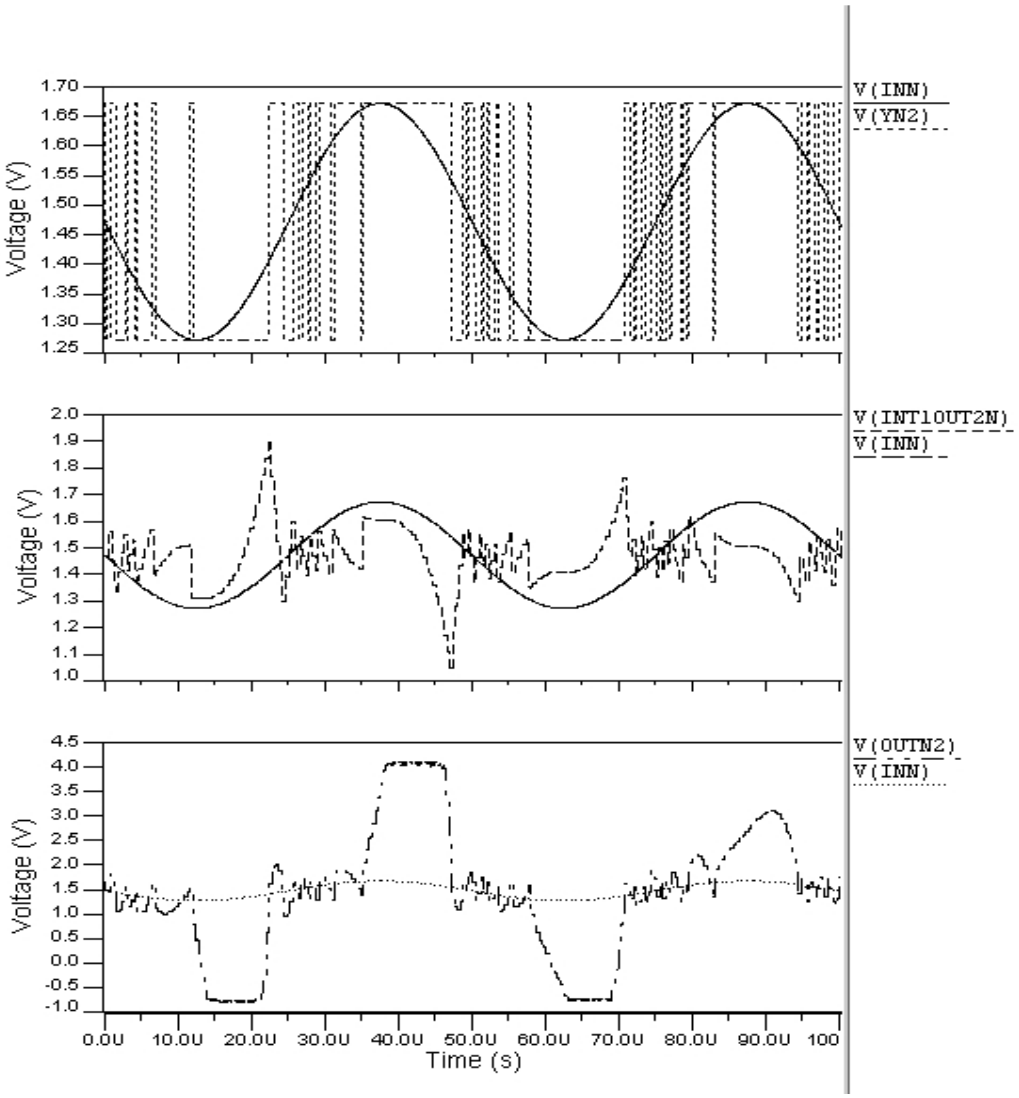


Figure 4.17. Simulation results of second order SD modulator with feed-forward path by using real op-amps

### 4.2.3.Proposed Low Power Second Order Modulator

The circuit given in Figure 4.7 is redesigned with the differential folded-cascode op-amp. The implementations is given below:

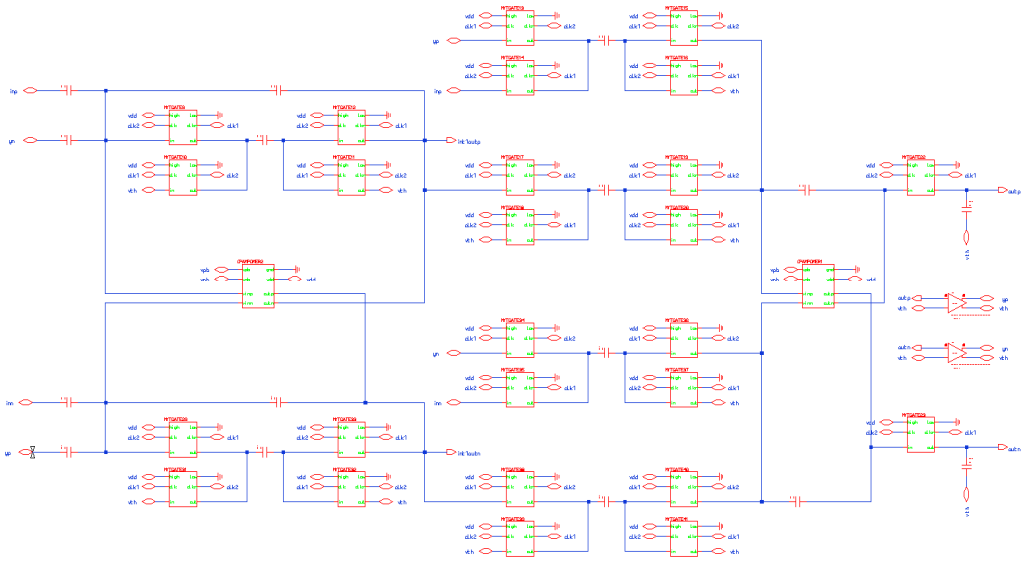

Figure 4.18. Circuit implementation of proposed SD modulator by using real op-amps

Figure 4.19 shows the simulation results of the circuit of Figure 4.18.

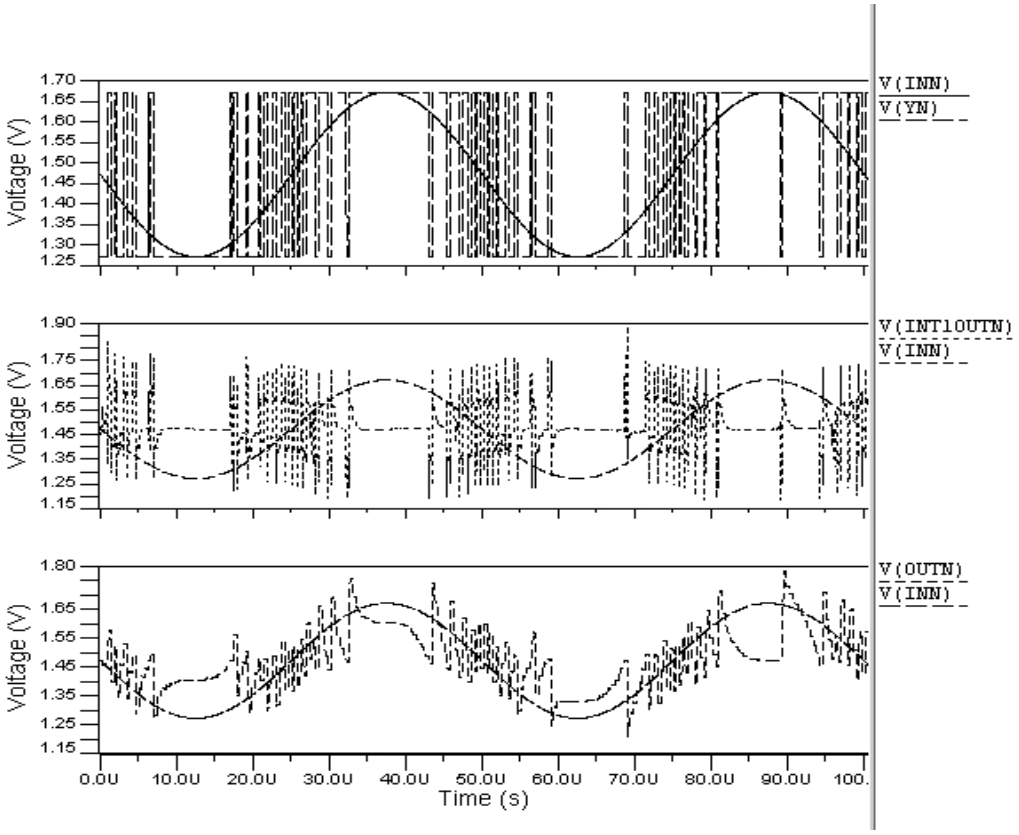


Figure 4.19. Simulation results of proposed SD modulator by using real op-amps

V(INN) is the input signal of the circuit; V(YN) is the output of the SD AD converter; V(INTOUTN) is the output of the first integrator and V(OUTN) is the output of the second integrator. The proposed SD modulator still has low voltage swing at the output of the first integrator when the new op-amp is used.

### 4.2.4.Analysis Results

Figure 4.20 shows outputs of first integrators of three second order SD modulators which are implemented with the designed op-amp. It can be seen that the first integrator output of the proposed architecture has the lowest the voltage swing. Also, histograms that are given in Figure 4.21, Figure 4.22 and Figure 4.23 support this result. Voltage values are gathered at the center and they do not change so much in Figure 4.23 that represents the output voltage of the first integrator of proposed SD modulator.

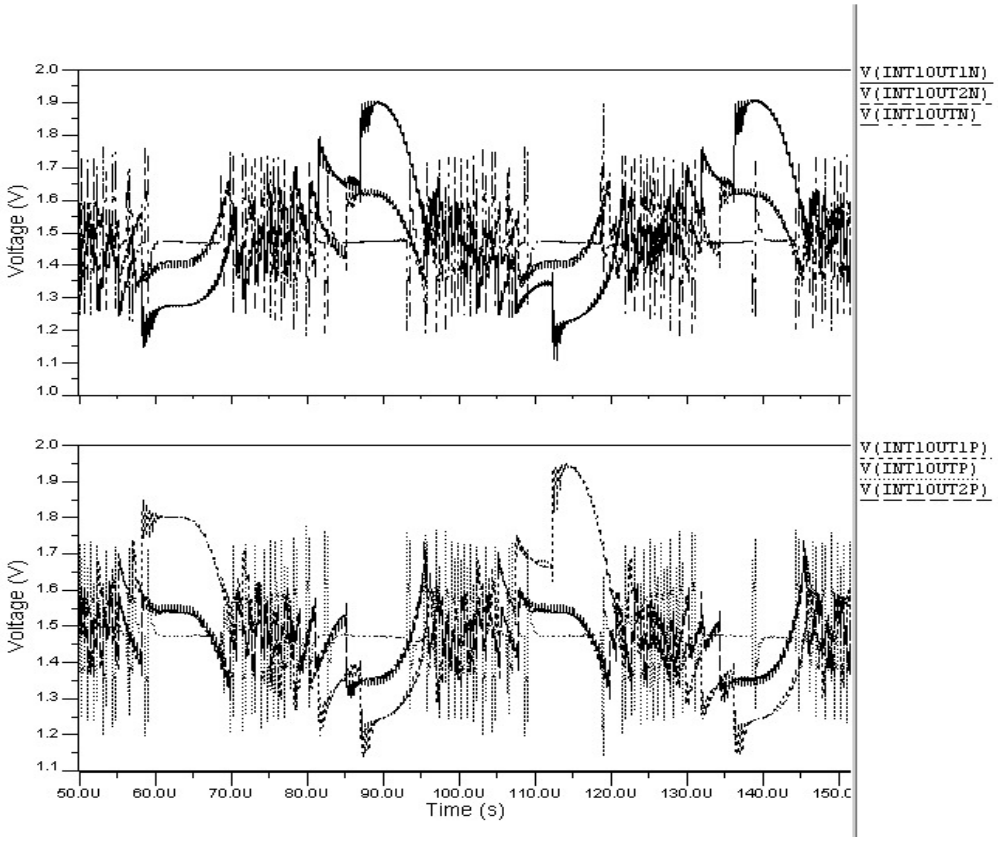


Figure 4.20. Comparison of the first integrator outputs of three SD modulator (real op-amps)

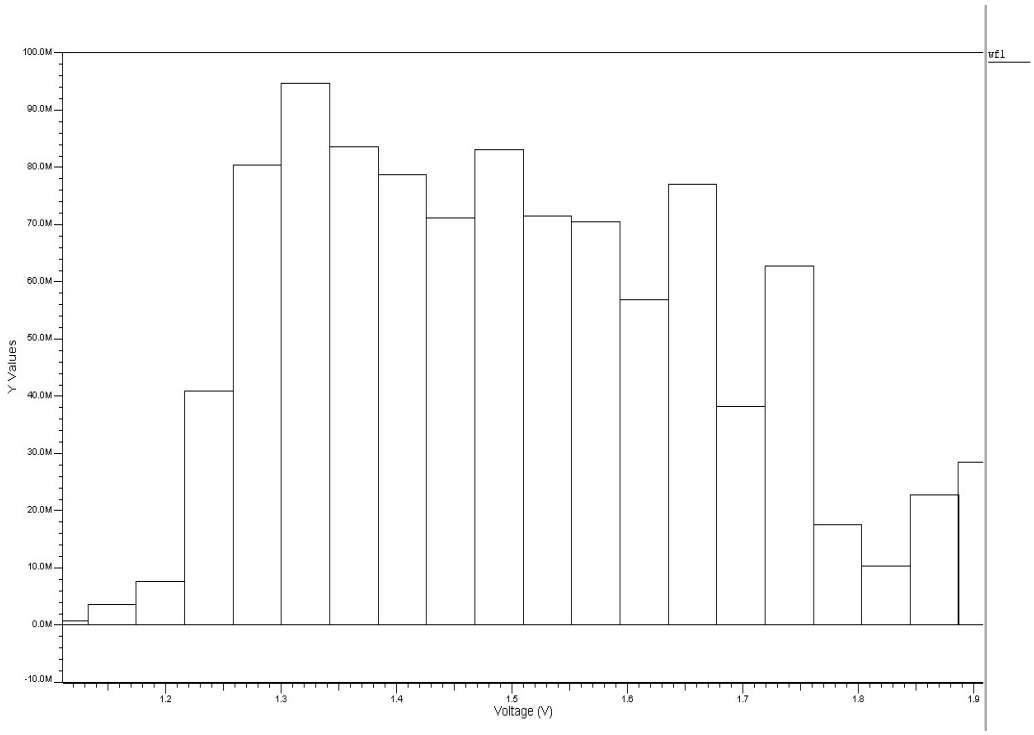


Figure 4.21. Histogram of output of the first integrator with optimum gains (real op-amp)

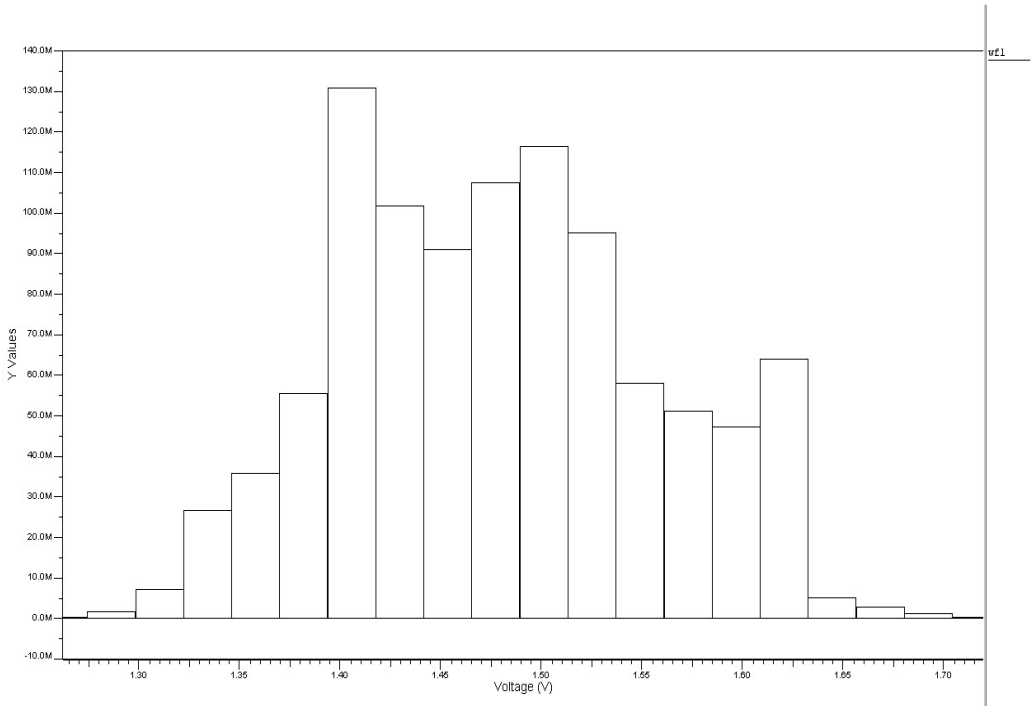


Figure 4.22. Histogram of output of the first integrator with feed-forward path (real op-amp)

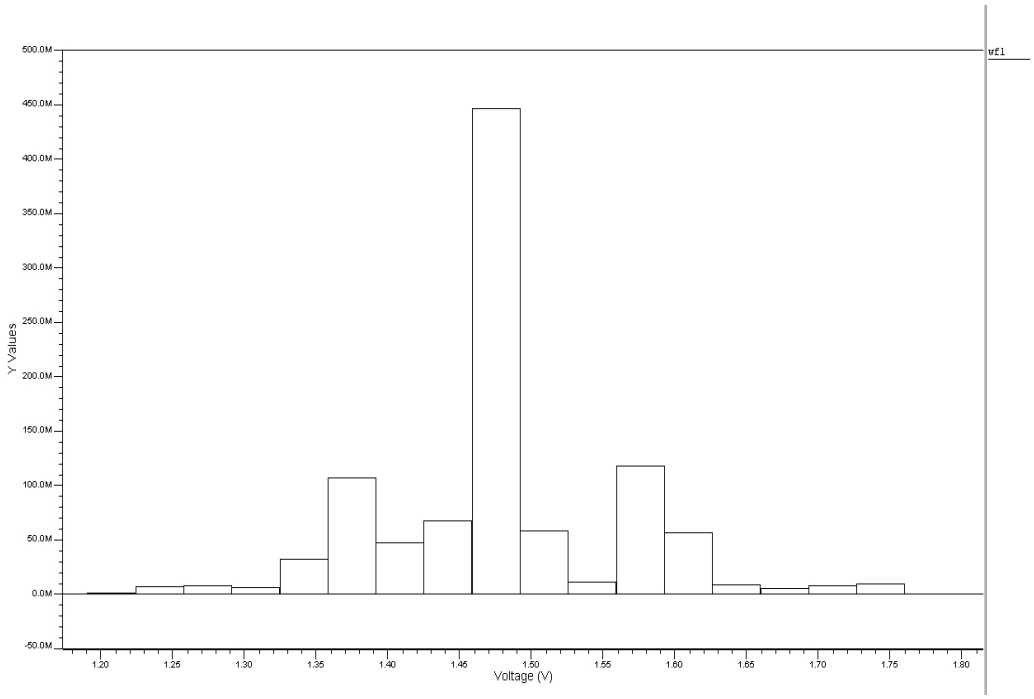


Figure 4.23. Histogram of output of the first integrator of the proposed architecture (real op-amp)

Also, the power consumption of SD modulators with optimum gains and feed-forward path; and proposed one are $5.6495mW$, $5.6107mW$, $5.6041mW$, respectively. The simulations are performed using EldoSpice in Mentor Graphics environment. According to results, the proposed SD modulator has the lowest power consumption by a small magrin.

Moreover, SNR and SNDR of SD modulators with optimum gains and feed-forward path; and proposed one are calculated. SNR calculation are done by using Delta Sigma Toolbox in MATLAB. The results are $41.29dB$, $45.79dB$ and $37.74dB$ respectively. SNDR calculation are done by using FFT analyses in HSpice. The results are $56.94dB$, $56.68dB$ and $56.69dB$.

According to the FFT analysis of the proposed modulator, it is seen that there is a problem. FFT plot does not display a 40 dB/decade slope which is expected from the analysis of second order SD modulators. This problem may occur because the proposed integrator architectures are not exact second order architectures.

After these results are obtained from circuits with real op-amps, circuits will be tested with simpler amplifiers than the op-amp in Figure 4.13, since low voltage swing at outputs of the first integrators enables to use these amplifiers. Furthermore, the power consumption of circuits may decrease with the usage of simpler amplifiers because they consume less power than the op-amp in Figure 4.13.

### 4.3.Circuit Implementations with Differential Amplifier

A simple differential amplifier is designed in order to test performance of the circuits. Figure 4.24 shows the differential amplifier. Then, this amplifier is modified in order to be used in a differential architecture. Figure 4.25 shows the modified differential amplifier. The specifications of this amplifier are as follows: Gain=37 dB, GBW= 10 MHz, BW=140 kHz. The output DC level of the op-amp is $1.5V$ and the bias voltages are $1V$ .

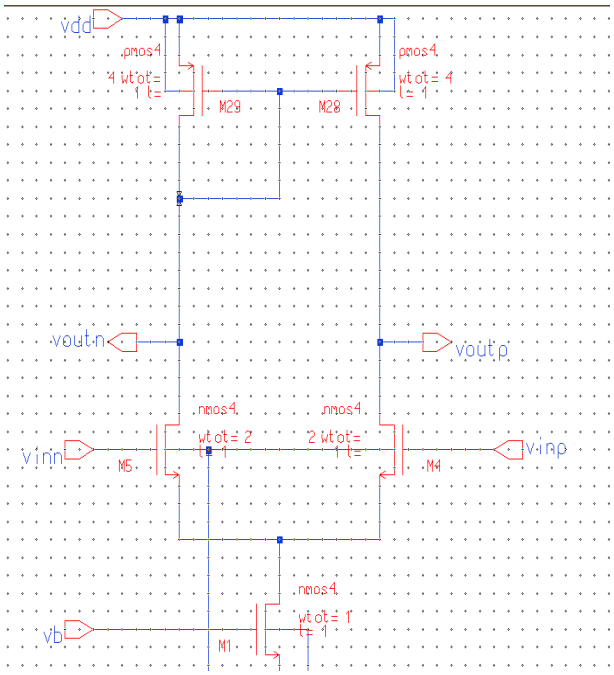


Figure 4.24. Differential amplifier

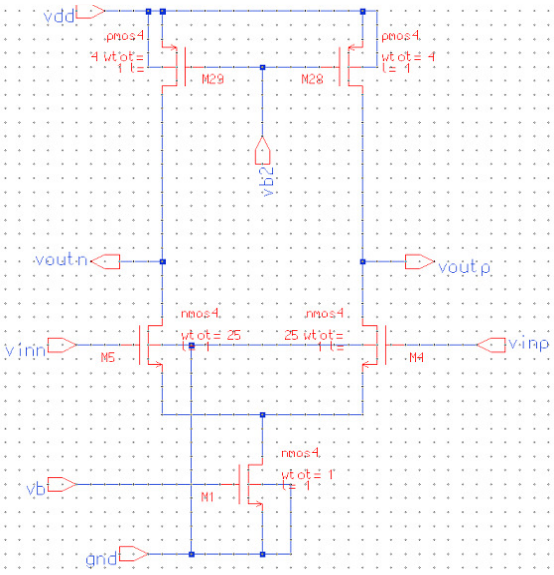


Figure 4.25. Modified Differential Amplifier

### 4.3.1.Second Order SD Modulator with Optimum Gains

The designed differential amplifier is replaced with real op-amps. Figure 4.26 shows the circuit implementation of SD modulator with differential amplifier.

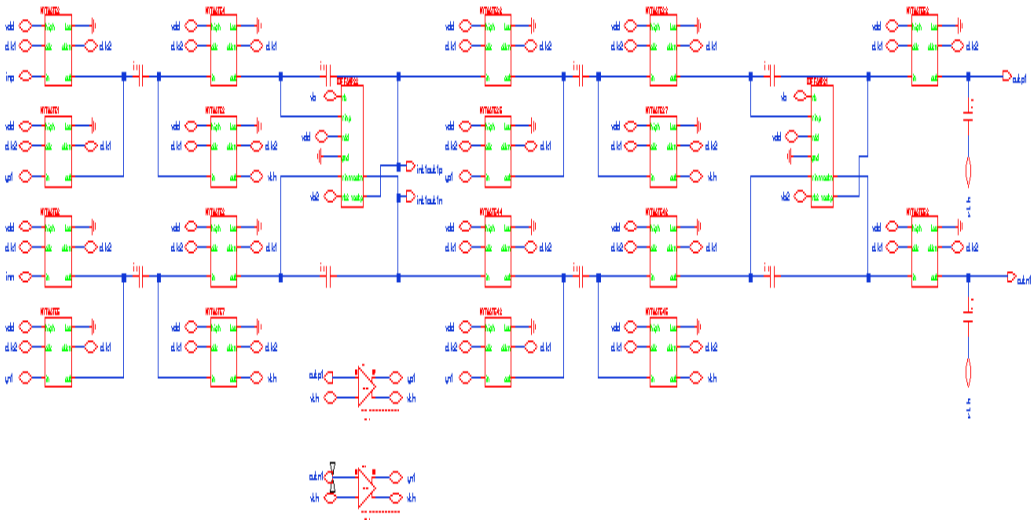

Figure 4.26. Circuit implementation of second order SD modulator with optimum gains by using differential amplifiers

Then the circuit is simulated and the relationship between inputs and outputs are given in Figure 4.27.

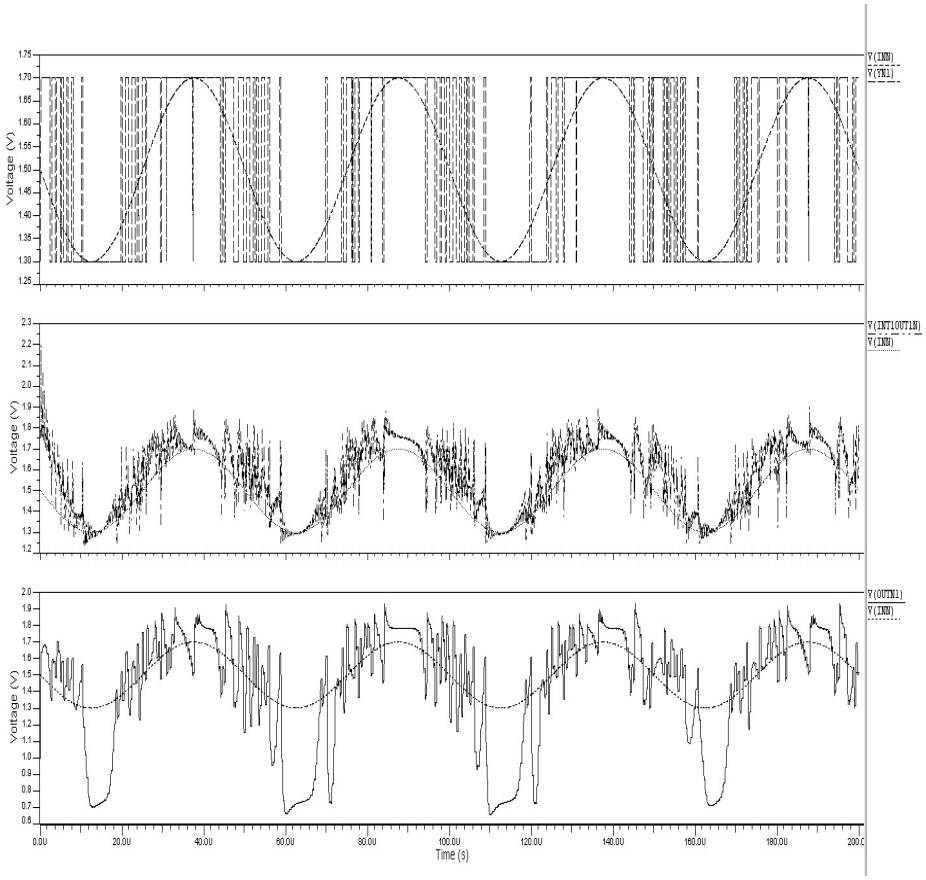


Figure 4.27.Simulation results of second order SD modulator with optimum gains by using differential amplifiers

V(INN) is the input signal of the circuit; V(YN1) is the output of the SD AD converter; V(INTOUTN1) is the output of the first integrator and V(OUTN1) is the output of the second integrator. According to the results, second order SD modulator with optimum gains stil works properly as a ADC.

### 4.3.2. Second Order SD Modulator with Feed-forward Path

The designed differential amplifier is swapped with real op-amps in Figure 4.16. The circuit implementation has turned out the following schematic:

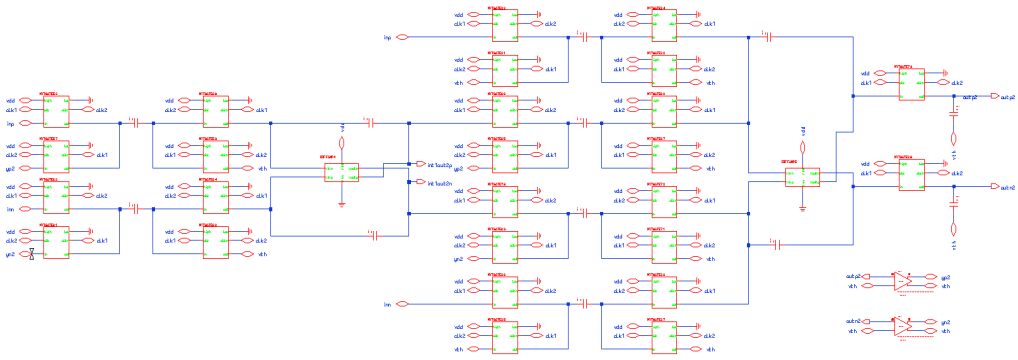

Figure 4.28. Circuit implementation of second order SD modulator with feed-forward path by using differential amplifiers

Figure 4.29 shows the simulation result of the circuit in Figure 4.28. V(INN) is the input signal of the circuit and V(YN2) is the output of the SD AD converter. Also, V(INTOUTN2) is the output of the first integrator and V(OUTN2) is the output of the second integrator.

According to Figure 4.29, although SD modulator functions smoothly, the voltage swing of the first integrator output changes obviously.

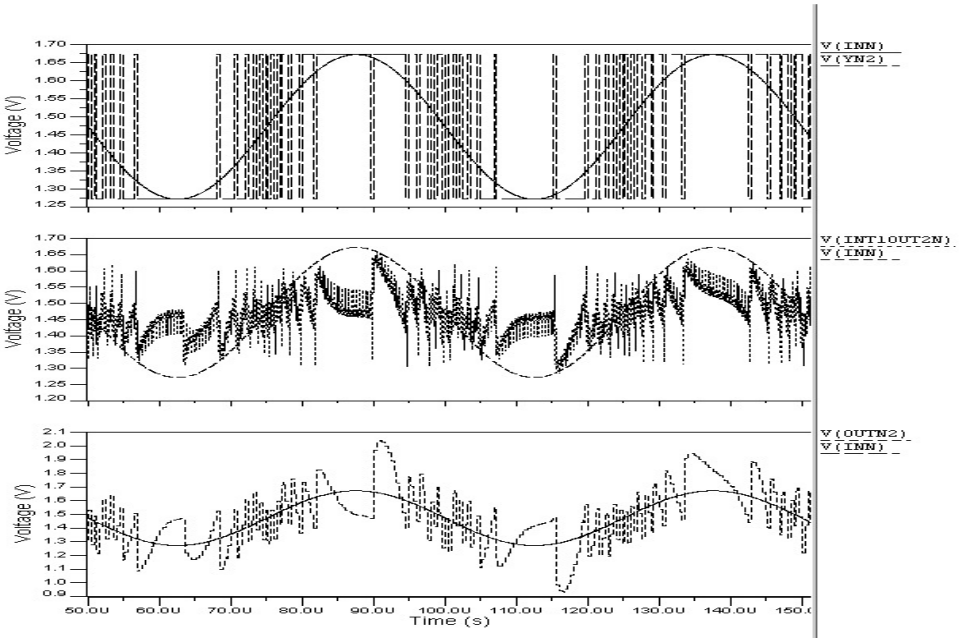


Figure 4.29. Simulation results of second order SD modulator with feed-forward path by using differential amplifiers

### 4.3.3. Proposed Low Power Second Order SD Modulator

The designed differential amplifier is used instead of real op-amps in Figure 4.18. Figure 4.30 shows the circuit implementation of the proposed low power second-order SD modulator with differenatial amplifiers.

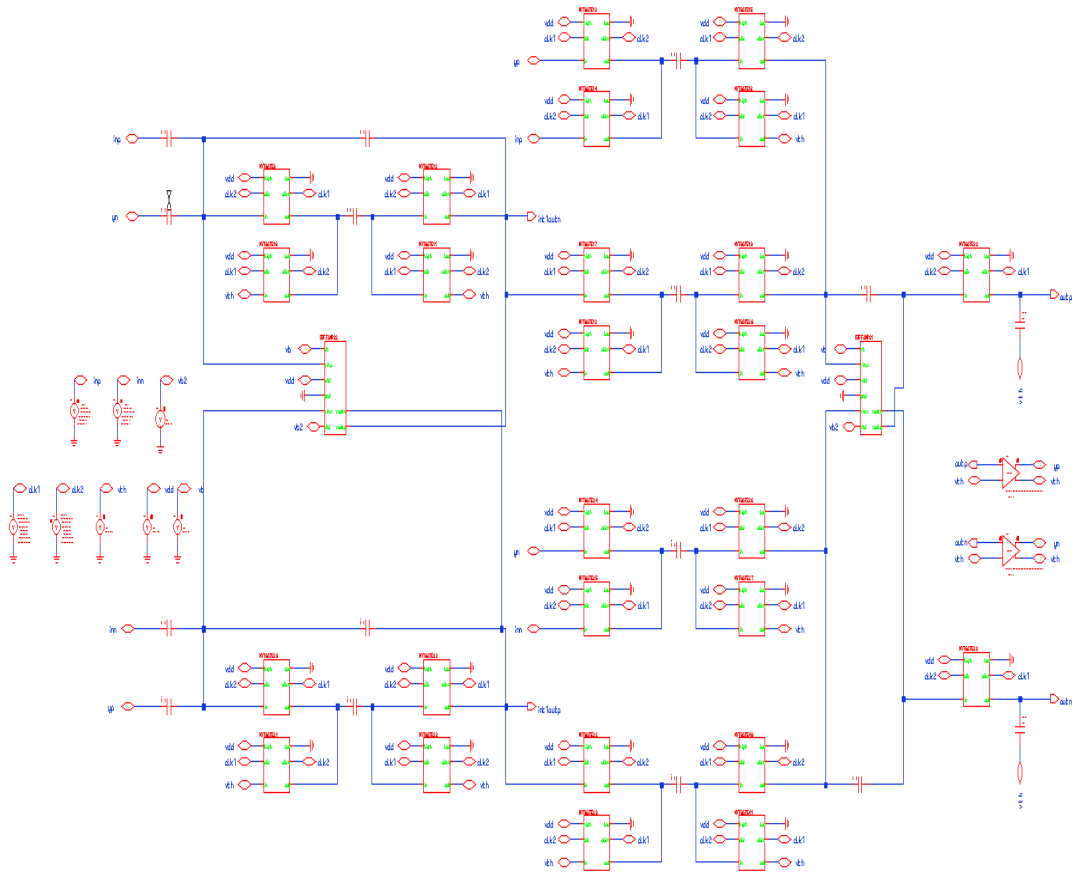

Figure 4.30. Circuit implementation of proposed SD modulator by using differential amplifiers

Figure 4.31 shows relationship between inputs and outputs of the SD AD converter which is given in Figure 4.30. V(INN) is the input signal of the circuit and V(YN) is the output of the SD AD converter. Furthermore, V(INTOUTN) is the output of the first integrator and V(OUTN) is the output of the second integrator. The proposed SD modulator functions properly with differential amplifier as an ADC. Also, the voltage swing at the output of the first integrator is low.

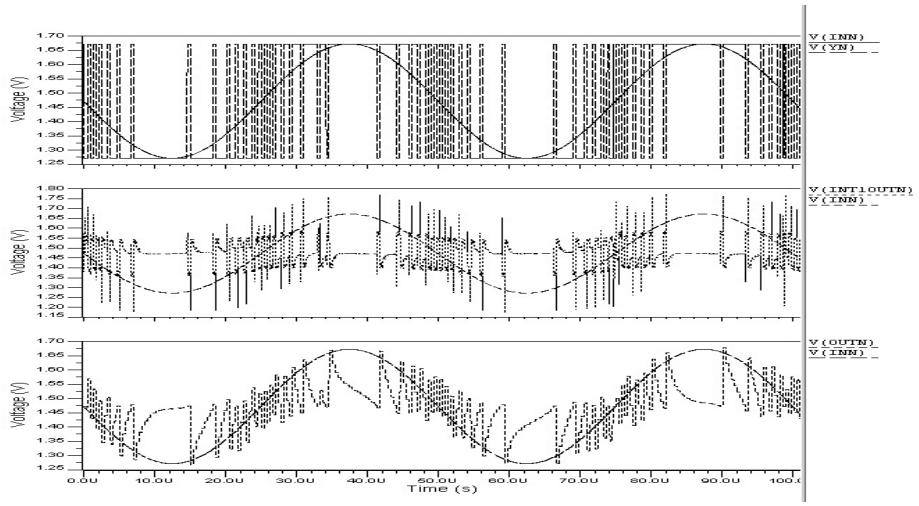


Figure 4.31. Simulation results of proposed SD modulator by using differential amplifier

### 4.3.4.Analysis Results

Figure 4.32 shows the comparison of the outputs of first integrators of three second order SD modulators which are implemented with differential amplifiers. According to Figure 4.32, it can be said that proposed SD modulator has the lowest voltage swing at the first integrator output. Also, histograms of first integrator outputs prove this statement. Figure 4.33, Figure 4.34 and Figure 4.35 show histograms for three SD modulators.

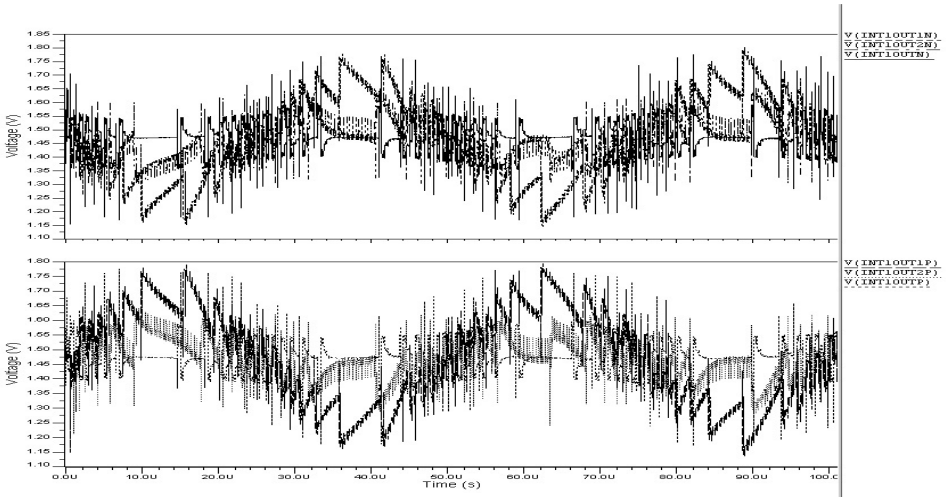


Figure 4.32. Comparison of the first integrator outputs of three SD modulators (differential amplifier)

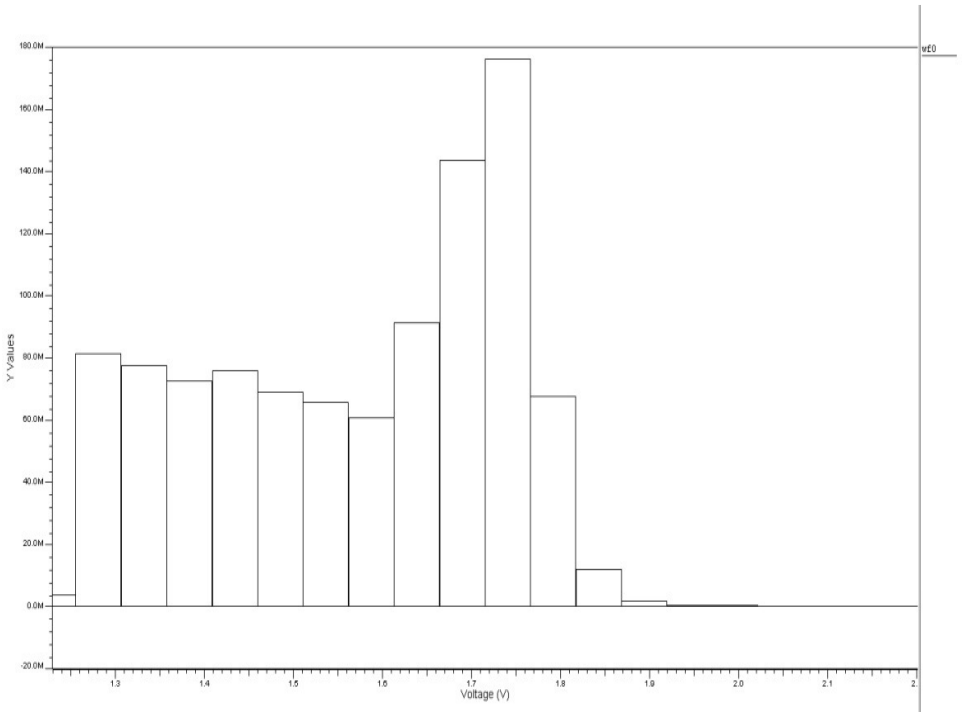


Figure 4.33. Histogram of output of the first integrator with optimum gains (differential amplifier)

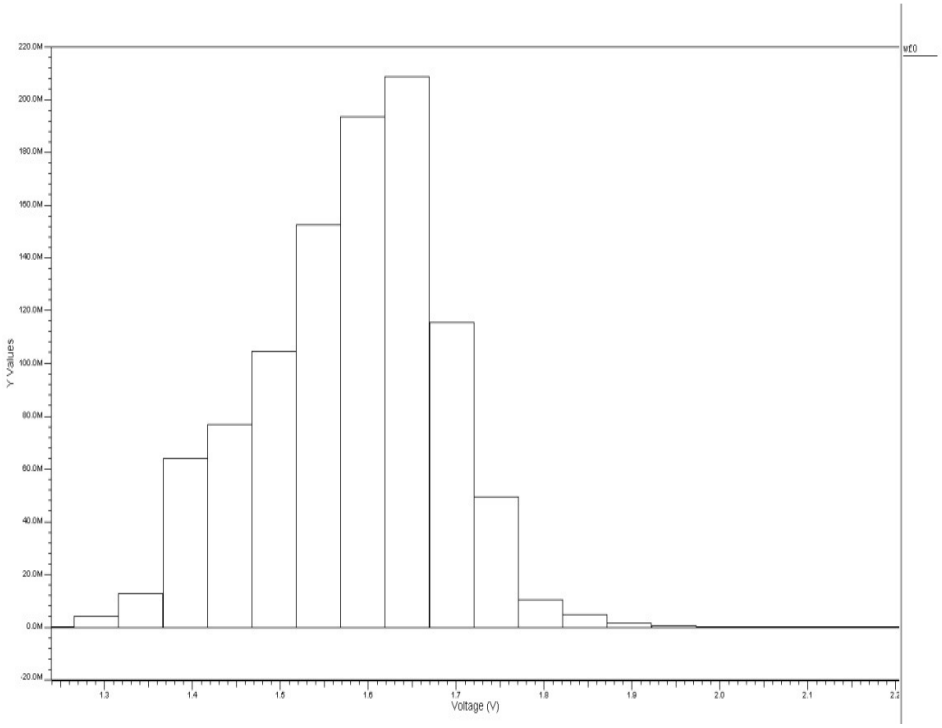


Figure 4.34. Histogram of output of the first integrator with feed-forward path (differential amplifier)

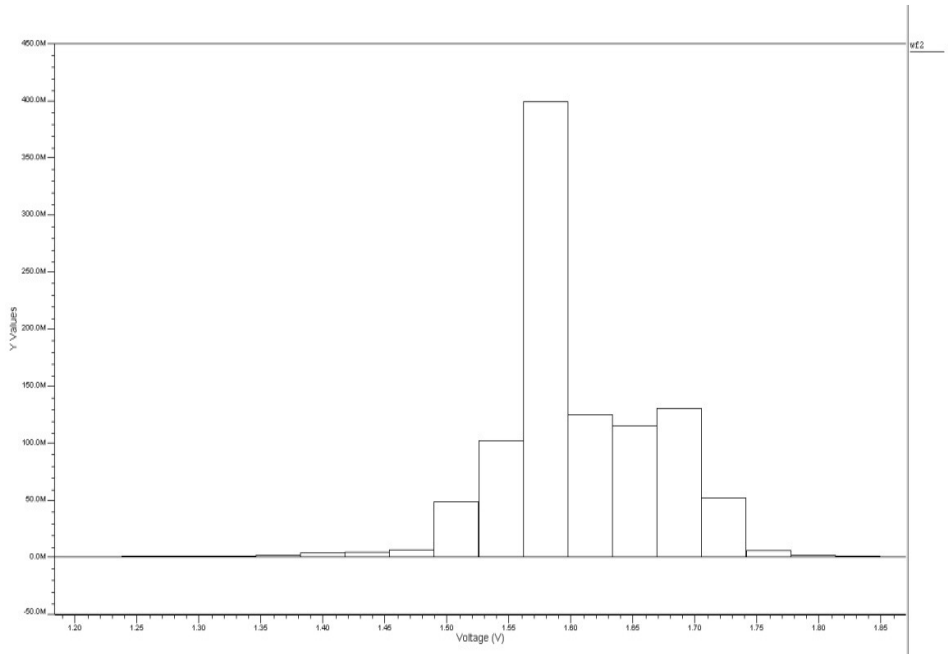


Figure 4.35. Histogram of output of the first integrator of the proposed architecture (differential amplifier)

According to Figure 4.33, Figure 4.34 and Figure 4.35, the voltage swing at the first integrator of proposed SD modulator is at the lowest level. The output voltages do not change as much as second order SD modulators with optimum gains and with feed-forward path do.

Also, the power consumption of SD modulators with optimum gains and feed-forward path; and proposed one are $54.6259uW$, $51.5253uW$, $50.2392W$, respectively. The simulations are performed using EldoSpice in Mentor Graphics environment. According to results, the proposed SD modulator has the lowest power consumption by a small margin.

Moreover, SNR and SNDR of SD modulators with optimum gains and feed-forward path; and proposed one are calculated. SNR calculation are done by using Delta Sigma Toolbox in MATLAB. The results are $32.89dB$, $37.71dB$ and $34.18dB$ respectively. SNDR calculation are done by using FFT analyses in HSpice. The results are $48.38dB$, $56.88dB$ and $50.88dB$. The results are lower compared to SNR and SNDR of

SD modulators with real op-amps because the differential amplifier has worse performance than the real op-amp.

After that, circuits are tested with inverters as op-amps to try to reduce power consumption as much as possible.

## 4.4.Circuit Implementations with an Inverter

Finally, an inverter is designed in order to test performance of the circuit. Although an inverter has a very low gain, at the same time it consumes very low power. So, if circuits run smoothly as a SD AD converter with inverters, the power consumption of the circuits will be in the lowest level of all.

The specifications of the inverter are as follows: $\left(W/L\right)_n = 16/0.35$, $\left(W/L\right)_p = 16/0.35$, Gain= 13 dB, GBW= 8.8 MHz, $V_{DD} = 1.3V$.

### 4.4.1.Second Order SD Modulator with Optimum Gain

The designed inverter is swapped with differential amplifiers in Figure 4.26. The circuit implementation has turned out the following schematic:

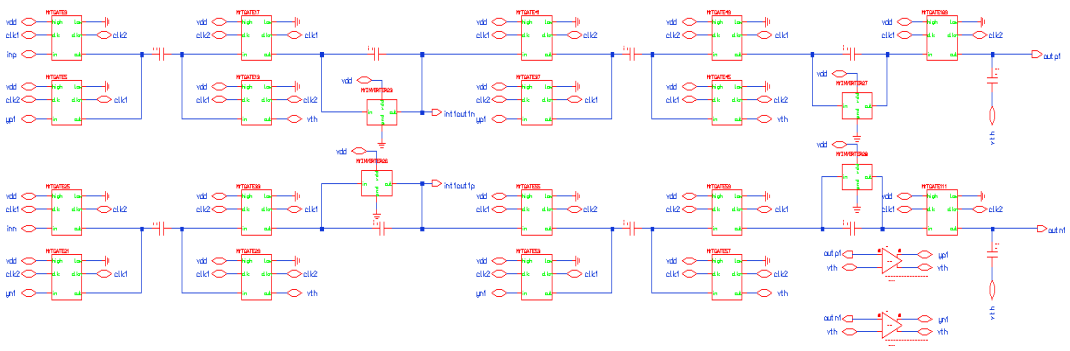

Figure 4.36. Circuit implementation of second order SD modulator with optimum gains by using inverters

Figure 4.37 shows the simulation result of the circuit of Figure 4.36.

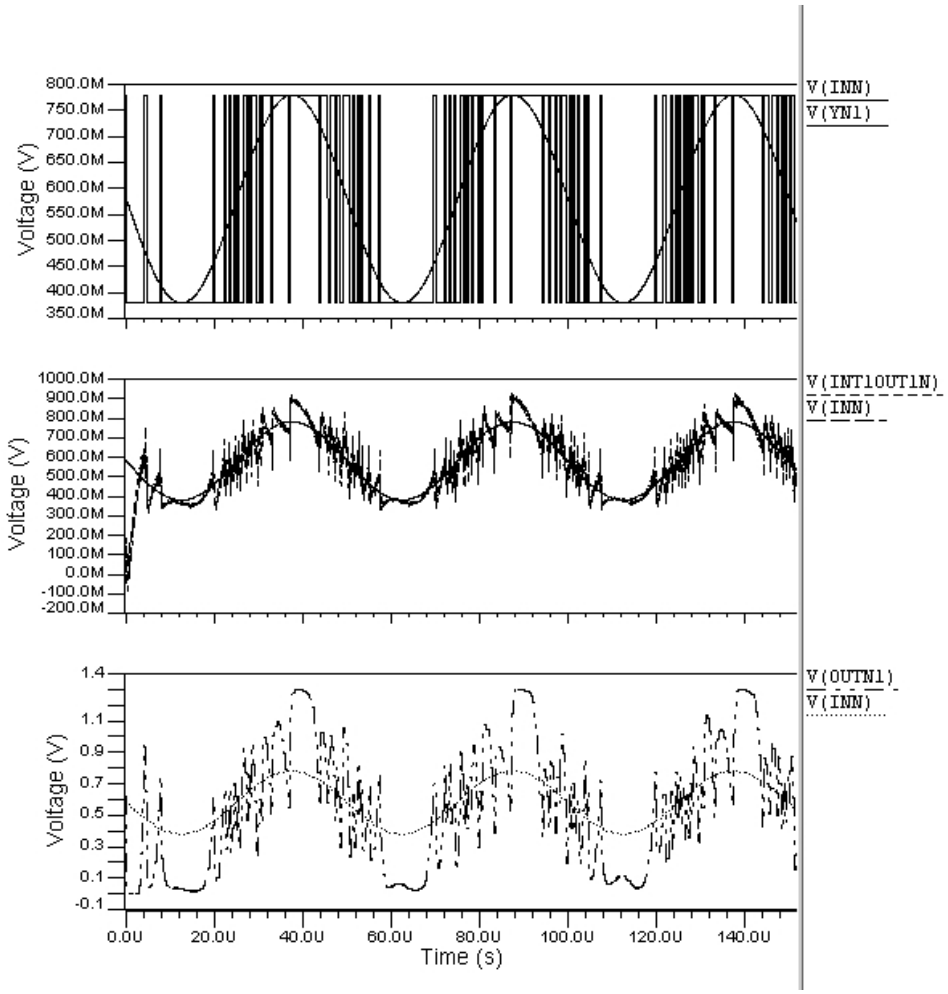


Figure 4.37. Simulation results of second order SD modulator with optimum gains by using inverters

It can be seen from Figure 4.37 that the second order SD modulator with optimum gain functions properly when inverters are used as op-amps.

### 4.4.2.Second Order SD Modulator with Feed-forward Path

The designed inverter is replaced with differential amplifiers. Figure 4.38 shows the circuit implementation of SD modulator with inverters.

Figure 4.39 shows relationship between inputs and outputs of the SD AD converter which is given in Figure 4.38. V(INN) is the input signal of the circuit and V(YN2) is the

output of the SD AD converter. Also, V(INTOUTN2) is the output of the first integrator and V(OUTN2) is the output of the second integrator.

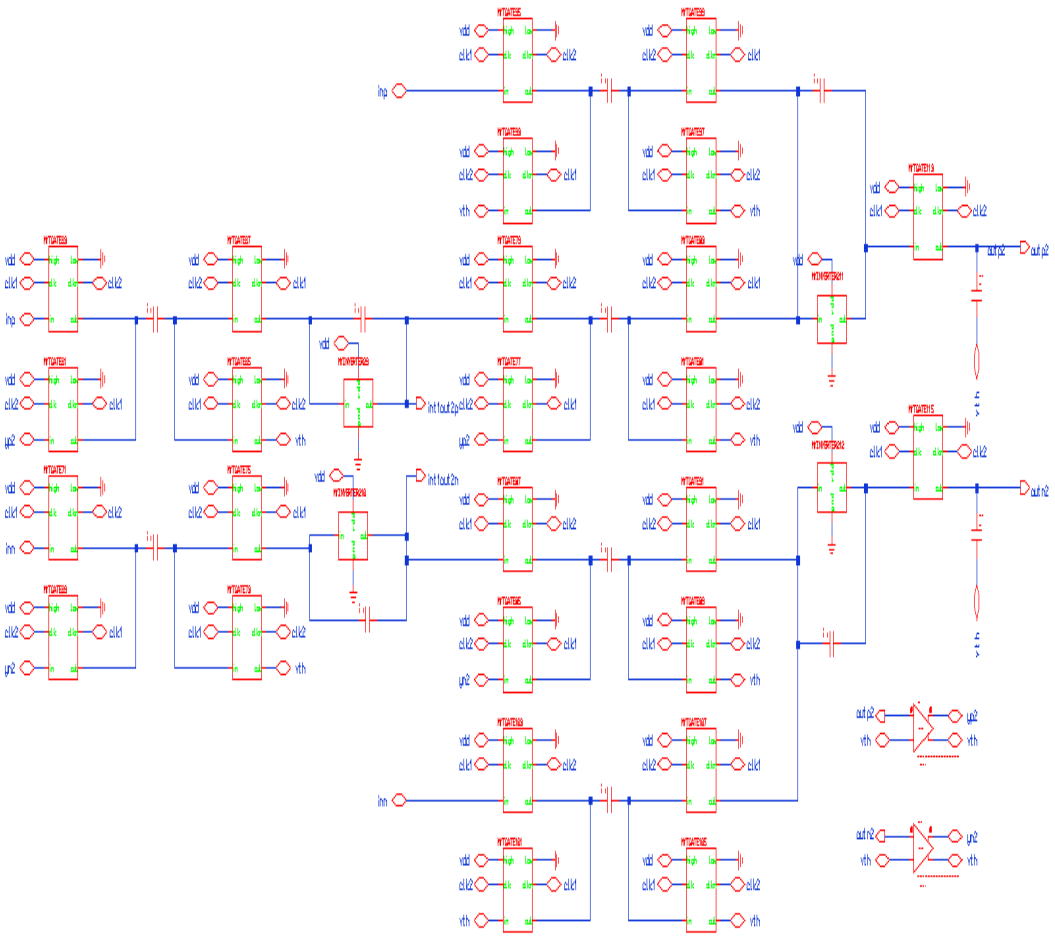

Figure 4.38. Circuit implementation of second order SD modulator with feed-forward path by using inverters

According to Figure 4.39, it can be said that the voltage swing of SD modulator with feed-forward path is lower than that of SD modulator with optimum gains when inverters are used as op-amps.

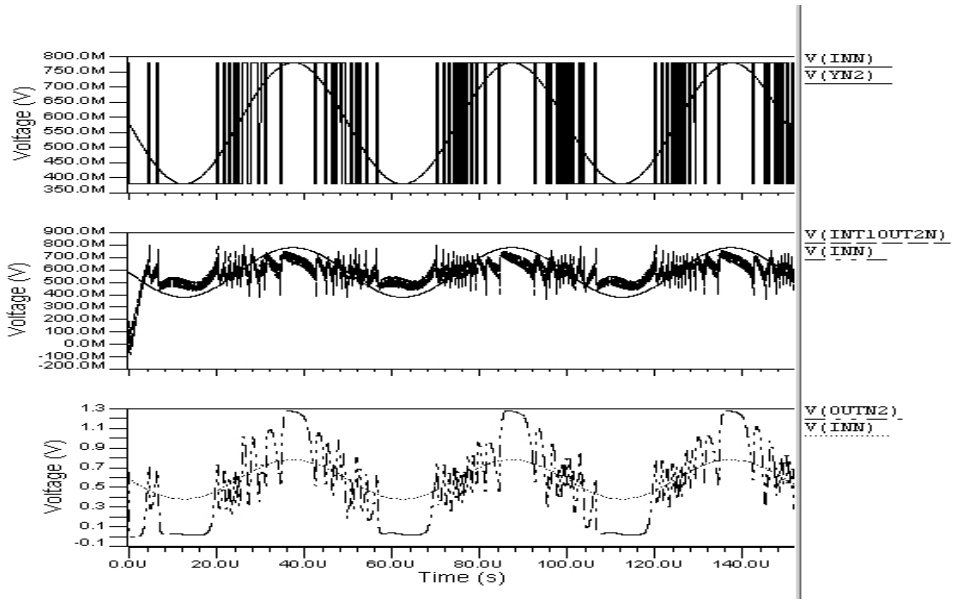


Figure 4.39. Simulation results of second order SD modulator with feed-forward path by using inverters

### 4.4.3.Proposed Low Power Second Order SD Modulator

The circuit given in Figure 4.30 is redesigned with the inverters. The implementation of the circuit is given below:

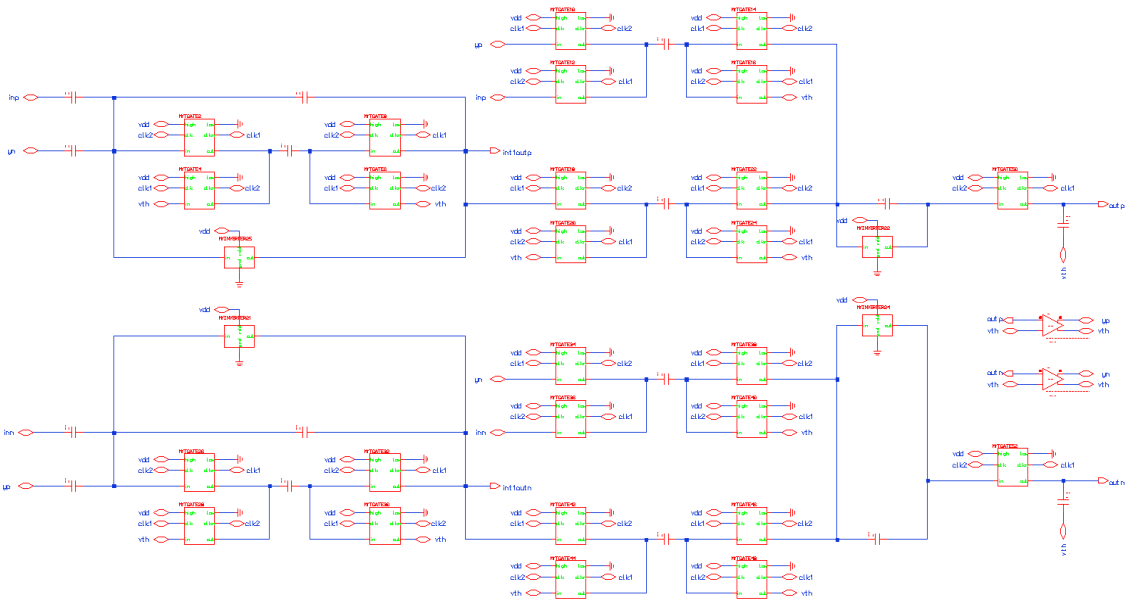

Figure 4.40. Circuit implementation of proposed SD modulators by using inverters

Then the circuit is simulated and the relationships between inputs and outputs are given in Figure 4.41. V(INN) is the input signal of the circuit; V(YN) is the output of the SD AD converter. Also, V(INTOUTN) and V(OUTN) refer the output of the first and second integrator respectively.

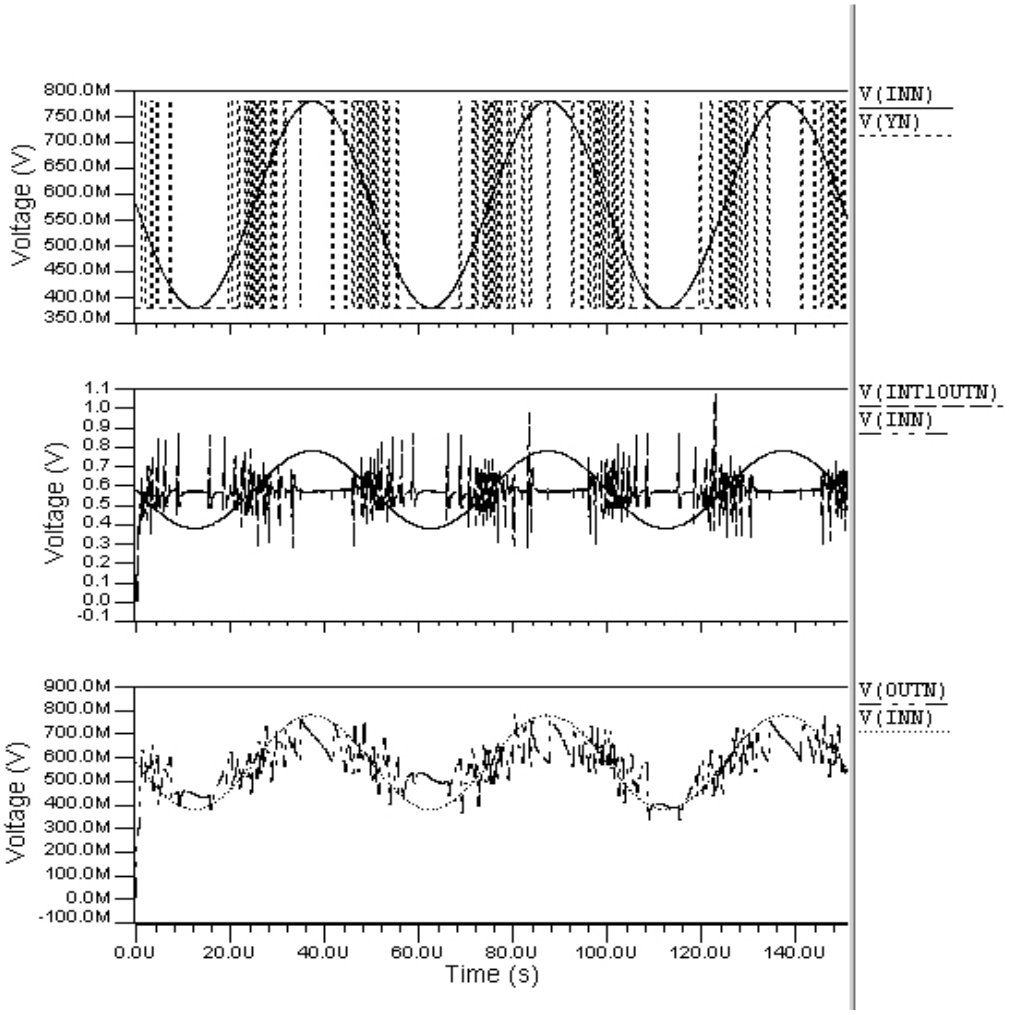


Figure 4.41. Simulation results of proposed SD modulator by using inverters

### 4.4.4.Analysis Results

Figure 4.42 shows outputs of the first integrators of three second order SD modulators which are implemented with designed op-amp. It can be seen that the first integrator output of the proposed architecture has the lowest the voltage swing. In addition to this, histograms that are given in Figure 4.43, Figure 4.44 and Figure 4.45 verify this

idea. Figure 4.45 shows that the voltage swing at the output of the first integrator is at the lowest level.

Also, the power consumption of SD modulators with optimum gains and feed-forward path; and proposed one are $19.3027uW$, $12.0759uW$, $11.9068uW$, respectively. The simulations are performed using EldoSpice in Mentor Graphics environment. According to results, the proposed SD modulator has the lowest power consumption.

Moreover, SNR and SNDR of SD modulators with optimum gains and feed-forward path; and proposed one are calculated. SNR calculation are done by using Delta Sigma Toolbox in MATLAB. The results are $58.35dB$, $62.47dB$ and $55.67dB$ respectively. SNDR calculation are done by using FFT analyses in HSpice. The results are $58.93dB$, $59.98dB$ and $58.71dB$.

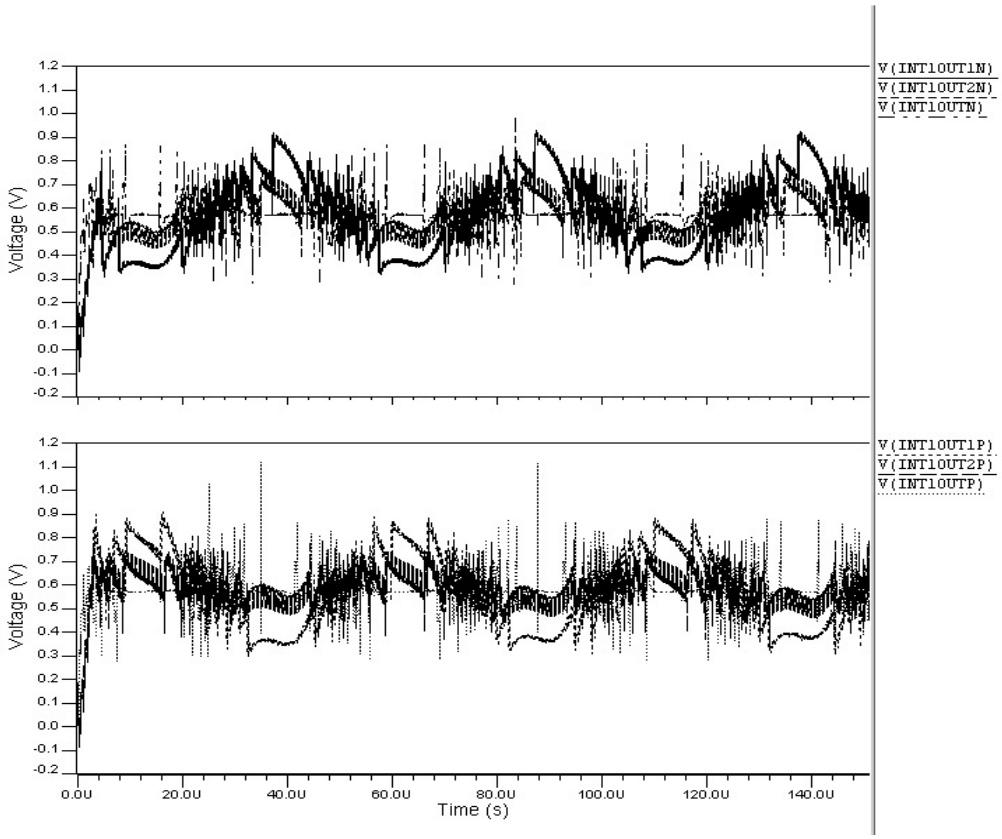


Figure 4.42. Comparison of the first integrator outputs of three SD modulators (inverter)

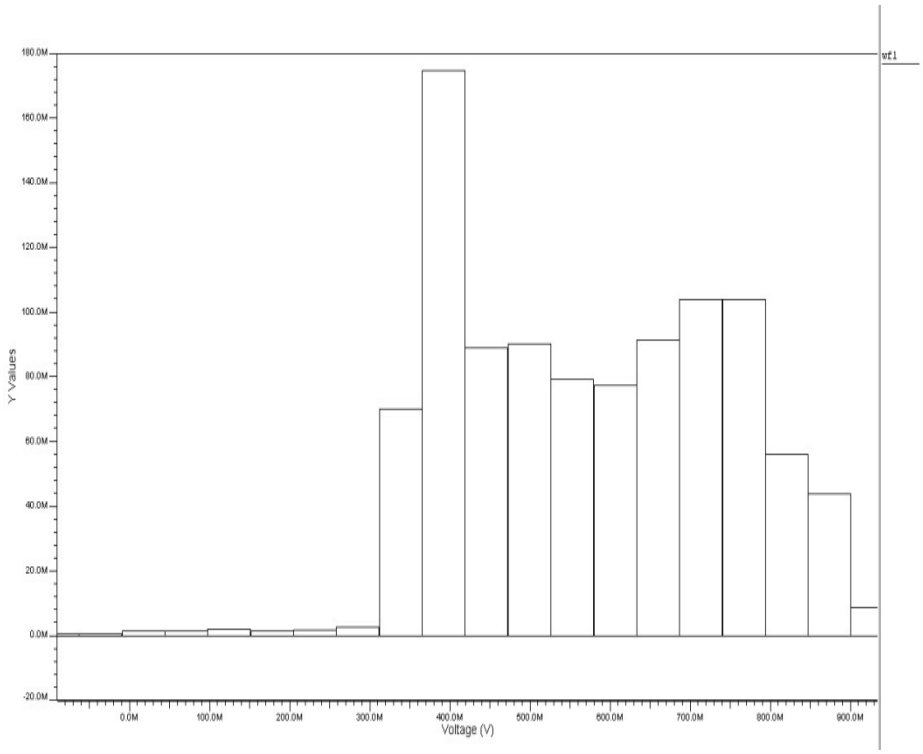


Figure 4.43. Histogram of output of the first integrator with optimum gains (inverter)

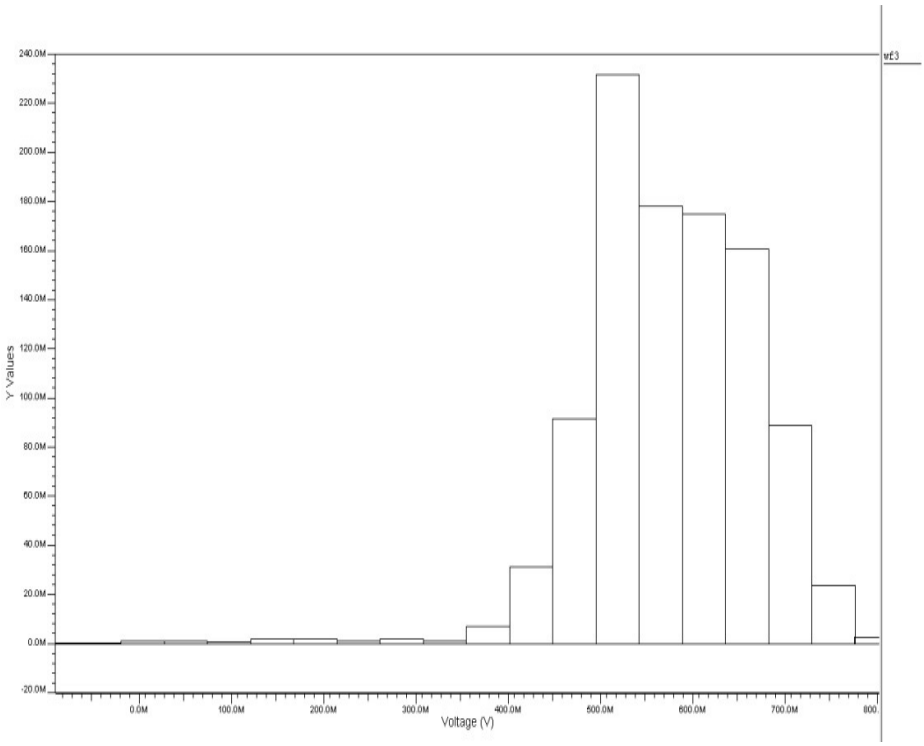


Figure 4.44. Histogram of output of the first integrator with feed-forward path (inverter)

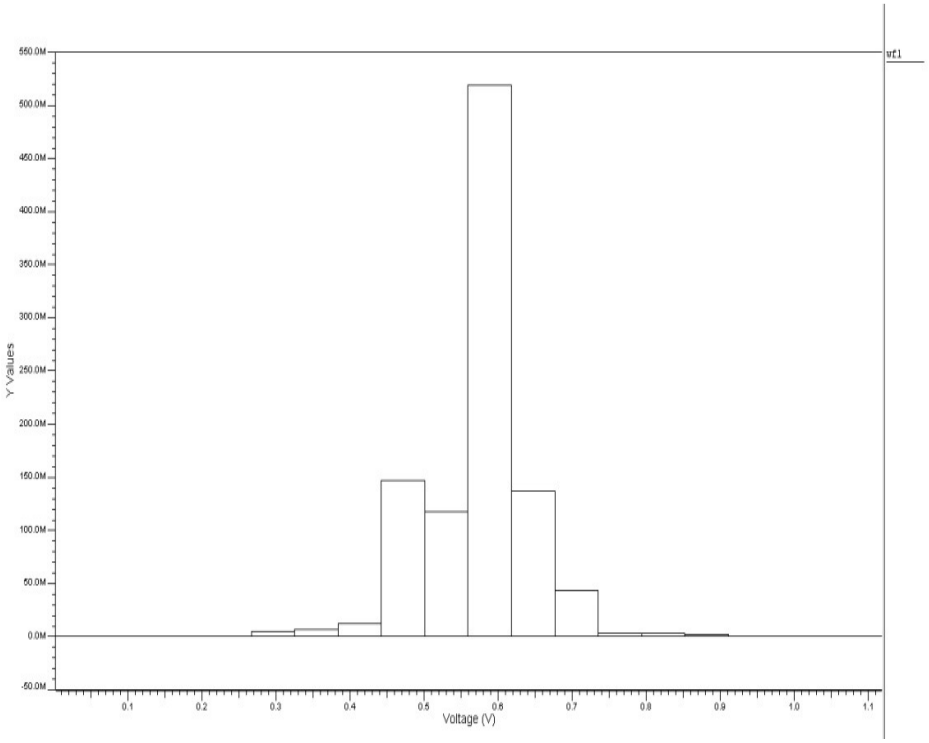


Figure 4.45. Histogram of output of the first integrator of the proposed architecture (inverter)

# 5.CONCLUSIONS AND FUTURE WORKS

SD modulators have become a usual technique for AD conversion because they have reduced circuit complexity and there is no need for a sample and hold amplifier. Also SD modulators combine oversampling, quantization noise shaping and digital filtering; and therefore, they are very suitable in high performance and low power applications. Moreover, designers should optimize the output swing and the speed performance of op-amps which are utilized in the modulators for high performance and low power consumption. The first integrator is the most critical because the power of the first integrator is the major consumption to the overall power dissipation in SD modulator. For that reason, a substantial amount of power can be saved by a suitable circuit design.

In this thesis, a new SD modulator structure is proposed in order to reduce the power consumption of the circuit and compared with similar works in this area. Since the most critical is the first integrator, the aim of the study is to find a suitable first integrator architecture to reduce the voltage swing at its output. The simulations performed during this project show that the proposed SD modulator has the lowest voltage swing at the output of the first integrator, compared to second order SD modulator with optimum gains and second order SD modulator with feed-forward path.

Moreover, low voltage swing at the output of the first integrator enables to use different kind of components as an op-amp in the circuit. Thus, also, affects the power consumption of the whole circuit. For that reason, an ideal op-amp, a real op-amp, a differential amplifier and an inverter are used in the design of three SD modulators respectively. As a result of simulations done for power consumption, it is seen that when a component that consumes less power is used for the first integrator block, the power dissipation of the whole circuit decrease too. Also, proposed SD modulator and second order SD modulator with feed-forward path consume less power compared to second order SD modulator with optimum gains.

Futhermore, effective number of bits are found using (2.9) and figure of merit is calculated by using following formula:

$$FoM = \frac{Power}{2^{ENOB} \cdot 2 \cdot BW} \tag{5.1}$$

Table 5.1 shows all these results perfectly.

Table 5.1. Results for all SD modulators in this study

| | | Power | SNR(dB) | SNDR(dB) | ENOB | FoM |
|---|---|---|---|---|---|---|
| Optimum gains | Real op-amps | 5.6495mW | 41.29 | 56.94 | 9 | 2.7585 x$10^{-10}$ |
| | Differential amplifier | 54.6259uW | 32.89 | 48.38 | 7 | 0.1067 x$10^{-10}$ |
| | Inverter | 19.3027uW | 58.35 | 58.93 | 9 | 9.4251 x$10^{-13}$ |
| Feed-forward path | Real op-amps | 5.6107mW | 45.79 | 56.68 | 9 | 2.7396 x$10^{-10}$ |
| | Differential amplifier | 51.5253uW | 37.71 | 56.88 | 9 | 2.5158 x$10^{-12}$ |
| | Inverter | 12.0759uW | 62.47 | 59.98 | 9 | 5.896x $10^{-13}$ |
| Proposed | Real op-amps | 5.6041mW | 37.37 | 56.69 | 9 | 2.7363 x$10^{-10}$ |
| | Differential amplifier | 50.2392uW | 34.18 | 50.88 | 8 | 4.9061 x$10^{-12}$ |
| | Inverter | 11.9068uW | 55.67 | 58.71 | 9 | 5.8139 x$10^{-13}$ |

According to results in Table 5.1, the proposed architecture has better results than architectures with optimum gains and feed-forward path for a specific component. In addition to this, the proposed architecture with an inverter is the best choice of all.

On the other hand, although proposed SD modulator has the lowest voltage swing and power consumption, it has some problems. According to the FFT analysis, the proposed SD modulator do not behave like a second order filter. 40 dB/decade slope is not measured in the SNR grahps. In other words, although the proposed SD modulator seems to be a second order modulator as an architecture, it does not function like a second order modulator. So, the second order SD modulator architecture that has $\left(1-2z^{-1}+z^{-2}\right)$ times of input signal in the output of the first integrator and $z^{-2}$ times of input signal in the output of the second integrator can not be designed exactly.

Also, some other architectures can be designed as future works for same aim that is, low voltage swings at the output of the first integrator and low power consumption. These designs are given below.

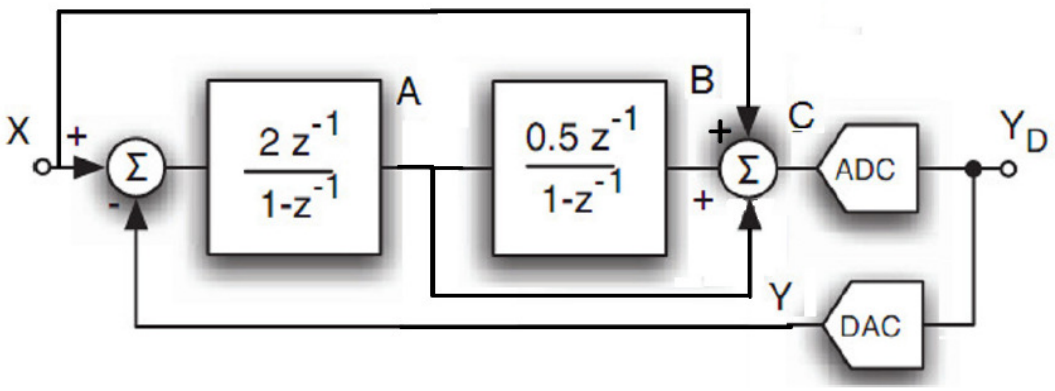


Figure 5.1. Alternative second order SD modulator (1)

By analysis of the linear system in Figure 5.1, followings can be obtained;

$$A=(X-Y)\frac{2z^{-1}}{1-z^{-1}} \tag{5.1}$$

$$B=(X-Y)\frac{z^{-2}}{(1-z^{-1})^2} \tag{5.2}$$

$$C = (X-Y)\frac{2z^{-1}}{1-z^{-1}} + (X-Y)\frac{z^{-2}}{(1-z^{-1})^2} + X = (X-Y)\frac{2z^{-1}-2z^{-1}+z^{-2}}{(1-z^{-1})^2} + X \quad (5.3)$$

$$Y = (X-Y)\frac{2z^{-1}-z^{-2}}{(1-z^{-1})^2} + X + E = X - E(1-z^{-1})^2 \quad (5.4)$$

where A is the output of the first integrator, B is the output of the second integrator, C is the output of the quantizer and Y is the output of the modulator. Then, by using above equations, A and B can be enlarged to followings;

$$A = \left[E(1-z^{-1})^2\right]\frac{2z^{-1}}{1-z^{-1}} = E2z^{-1}(1-z^{-1}) \quad (5.5)$$

$$B = E(1-z^{-1})^2\frac{z^{-2}}{(1-z^{-1})^2} = Ez^{-2} \quad (5.6)$$

As a result of these equations, it can be seen that the output of the first integrator (A) has lower X(z) contribution compared to (3.10) and (3.13).

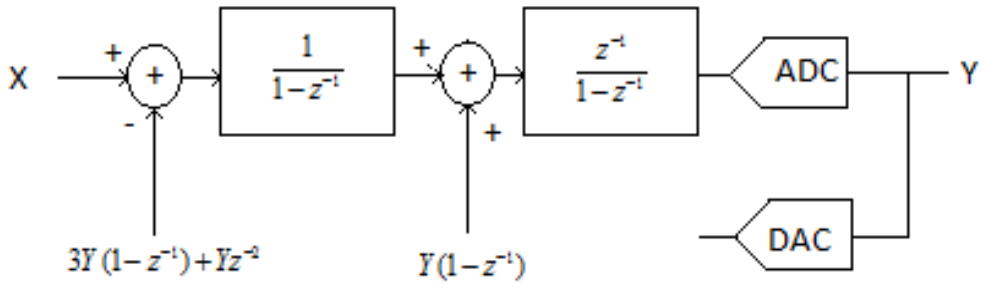


Figure 5.2. Alternative second order SD modulator (2)

By analysis of the linear system in Figure 5.2, the output of the first integrator and the output of the circuit are found as following;

$$P = X(1-2z^{-1}+z^{-2}) \quad (5.7)$$

$$Y = Xz^{-1} + E(1-z^{-1})^2 \qquad (5.8)$$

If (5.7) is compared with (3.10) and (3.13), it can be seen that (5.7) has the lowest $X(z)$ contribution.

Finally, all things considered, it can be said that the approach of reducing voltage swing of the first integrator in this study for less power consumption, is very effective way. But, $(1-2z^{-1}+z^{-2})$ times of input signal in the output of the first integrator and $z^{-2}$ times of input signal in the output of the second integrator are not suitable values to design a low-power second order SD modulator.

# REFERENCES


1. Aziz, P. M., Sorensen, H. V. and van der Spiegel, J., "An Overview of Sigma-Delta Converters: How a 1-bit ADC achieves more than 16-bit resolution", *IEEE Signal Processing Magazine,* volume 13, issue 1, pp 61-84, September 1996.

2. Park, S., *Motorola Digital Signal Processors: Principles of Sigma-Delta Modulation for Analog-to-Digital Converters.*

3. Karema, T., Ritoniemi, T. and Tenhunen H., *An Oversampled Sigma-Delta A/D Converter Circuit Using Two-Stage Fourth Order Modulator*, Tampere University of Technology, P.O.Box: 527, SF-33101 Tampere, Finland.

4. Carley, L. R., "An Oversampling Analog-to-Digital Converter Topology for High-Resolution Signal Acquisition Systems", *IEEE Transactions on Circuits and Systems,* Vol. CAS-34, No.1, pp. 184-191, January 1987.

5. Boser, B. E. and Wooley, B., A., "The Design of Sigma-Delta Modulation Analog- to-Digital Converters", *IEEE Journal Of Solid-State Circuits,* Vol. 23, No. 6, pp. 293-303, December 1988.

6. Maloberti, F., *Data Converters,* Springer, Dordrecht, 2007.

7. Sansen, W. M. C., *Analog Design Essentials,* Springer, Dordrecht, 2006.

8. Kirk, C., H. Chaq, S. Nadeem, W. L. Lee and C. G. Sodini, "A Higher Order Topology fot Interpolation Modulators for Oversampling A/D Converters", *IEEE Transactions on Circuits and Systems,* Vol. 37, No. 3, pp. 196-205, March 1990.

9. Kozak, M. and Kale, İ., *Oversampled Delta-Sigma Modulators: Analysis, Applications and Novel Topologies,* Kluwer Academic Publishers, Boston, 2003.

10. Bourdopoulos, G. I., A. Pnevmatikakis, V. Anastassopoulos and T. L. Deliyannis, *Delta-Sigma Modulators: Modelling, Design and Applications,* Imperial College Press, London, 2003.

11. Cherry, J. A., Snelgrove, W. M., *Continuous-Time Delta-Sigma Modulators For High-Speed A/D Conversion: Theory, Practice and Fundemental Performance Limits,* Kluver Academic Publishers, New York, 2002.

12. Schreier, R. and G. C. Temes, *Understanding Delta-Sigma Data Converters,* IEEE Press, New Jersey, 2005.

13. Liu, M., *Demystifying Switched-Capacitor Circuits,* Elsevier, Oxford, 2006.

14. Kwon, S. and F. Maloberti, "Op-amp Swing Reduction in Sigma-Delta Modulators", *IEEE ISCAS,* pp. 525-528, 2004.

15. Yetik, Ö., *An Automatic Architecture Generator for Sigma-Delta Modulators Considering Component Non-Idealities,* M.S. Thesis, Boğaziçi University, 2005.

16. Norsworty, S. R., R. Schreier and G. C. Temes (Editors), *Delta-Sigma Data Converters: Theory, Design and Simulation,* IEEE Press, New York, 1997.

17. Razavi, B., *Principles of Data Conversion System Design,* IEEE Press, New York, 1995.

18. Razavi, B., *Design of Analog CMOS Integrated Circuits,* McGraw-Hill, New York, 2001.

19. Boser, B. E., K. Karmann, H. Martin and B. A. Wooley, "Simulating and Testing Oversampled Analog-to-Digital Convertera", *IEEE Transactions on Computer- Aided Design,* Vol. 7, No. 6, pp. 168-173, June 1988.

20. Murmann, B. and B. E. Boser, ”A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification”, *IEEE Journal of Solid-State Circuits,* Vol. 38, No.12, pp.2040-2050, December 2003.

21. Roh, H., H. Lee, Y. Choi and J. Roh, ” A 0.8-V 816-nW Delta-Sigma Modulator for Low-Power Biomedical Applications”, *Analog Integr. Circ. Sig. Process,* Springer, 2010.

22. Candy, J. C. and G. C. Temes, *Oversampling Delta-Sigma Data Converters: Theory, Design and Simulation,* IEEE Press, New York, 1992.

23. Gray, R. M., ”Oversampled Sigma-Delta Modulation, *IEEE Transactions on Communications,* Vol. COM-35, No. 5, pp. 73-80, May 1987.

24. Norsworthy, S. R., I. G. Post and H. S. Fetterman, “A 14-bit 80-kHz Sigma-Delta A/D Converter: Modeling, Design, and Performance Evaluation”, *IEEE Journal of Solid-State Circuits,* Vol. 24, No. 2, pp. 342-352, April 1989.