SYSTEM LEVEL DESIGN OF PHASE LOCKED LOOPS

by

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ABSTRACT

SYSTEM LEVEL DESIGN OF PHASE LOCKED LOOPS

Phase Locked Loops (PLLs) are extensively used in microprocessors and digital signal processors for clock generation and as frequency synthesizers in RF communication systems for clock extraction and generation of a low phase noise local oscillator signal from on-chip voltage controlled oscillator (VCO). In the design of PLLs, the designer typically have to optimize a large set of parameters, including the performance of the building blocks, in order to achieve the desired system specifications. In view of the inherent non-linearity of the PLL and continuously varying operation frequency of the building blocks, this optimization process has to be carried out at the system level. Transistor level simulation of PLLs is only possible for final validation or for the extraction of the electrical parameters of the basic blocks. In this thesis, the analytical expressions for the system specifications of simple loop PLL architecture are derived and tested with VHDL-AMS simulations to develop an approach allowing the systematic design of PLLs. This approach allows the designer to maintain a grasp of the fundamentals using the coarse models at the early stage of the design and eventually to gain insight on the lower order effects by gradually increasing the level of detail as the design develops. The problem of noise analysis of PLLs is addressed in the presence of circuit white noise sources yielding the spectrum of the PLL output. Behavioral modeling of phase noise and jitter in PLLs with VHDL-AMS is implemented, and the correlation between the developed models and analytical noise analysis expressions is shown.

ÖZET

SİSTEM DÜZEYİNDE EVRE KENETLEME DÖNGÜSÜ TASARIMI

Evre kenetleme döngüleri (EKD), yaygın olarak, mikroişlemcilerde ve sayısal sinyal işlemcilerinde saat eşzamanlaması üretimi, RF haberleşme sistemlerinde ise yonga üstü gerilim denetimli salıngaçtan düşük evre gürültülü yerel salıngaç sinyali üretimi ve saat eşzamanlaması cıkartımı için sıklık birleştiricisi olarak kullanılır. EKD tasarımlarında, tasarımcı tipik olarak istenilen sistem belirtimlerine ulaşmak icin geniş bir değiştirge takımını yapı bloklarının performanslarıyla beraber en iyi hale getirmek zorundadır. EKD'nin içşel dogrusal olmayan görünümünde ve yapı bloklarının sürekli değişen işlem sıklıklarında, bu en iyileştirme süreci sistem seviyesinde tamamlanmalıdır. EKD'lerin transistör seviyesinde benzetimleri ise nihai doğrulamada veya temel blokların elektriksel değiştirgelerinin üretimi için mümkündür. Bu tezde, basit döngü EKD mimarisinin sistem belirtimleri için cözümsel ifadeler türetilmiş ve VHDL-AMS benzetimleri ile EKD'lerin sistematik tasarımına izin veren bir yaklaşımla test edilmiştir. Bu yaklaşım, tasarımcıya kaba modeller kullanarak tasarımın erken evrelerinde temel bilgileri kavramayı sürdürmesine ve tasarım geliştikçe, aşamalı olarak ayrıntı seviyesini arttırarak, sonunda düşük düzeyli etkiler üzerine bir anlayış edinmesine izin verir. Gürültü analizi problemi EKD çıkışının izgesini veren beyaz gürültü kaynaklarının mevcudiyetinde belirtilmiştir. EKD'lerde evre gürültüsü ve seğirmenin davranışsal modellemesi VHDL-AMS ile gerçekleştirilmiş ve geliştirilen modellerle çözümsel gürültü ifadeleri arasındaki ilinti gösterilmiştir.

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LIST OF SYMBOLS/ABBREVIATIONS

A_0	Maximum perturbation
G_{LPF}	Loop filter linear voltage transfer function
I_p	Charge pump current
I_{p_eff}	Effective charge pump current
J_n	Random signal
ΔI_P	Charge pump current mismatch
K	Loop gain
K_{PD}	Phase detector gain
K_{VCO}	Voltage controlled oscillator gain
Ron_tgate	Transmission gate on resistance
$Rout\_pmos$	Current mirror output impedance
T_0	Ideal output period
T_n	n^{th} period of output
$\overline{T}$	Mean period
ΔT_n	Timing jitter
ΔT_c	Cycle jitter
ϕ_{in}	Input phase
ϕ_{out}	Output phase
ϕ_e	Phase error
ϕ_{VCO}	Voltage controlled oscillator phase noise
τ_{dec}	Decay time constant
ω_{LPF}	Loop filter cut-off frequency
ω_n	Natural frequency
ζ	Damping factor

CPPLL	Charge Pump Phase Locked Loop
CPU	Central Processing Unit
DSB	Double Side Band
IC	Integrated Circuit
LPF	Low Pass Filter
NMOS	N-Channel Metal Oxide Semiconductor
PD	Phase Detector
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
PMOS	P-Channel Metal Oxide Semiconductor
PSD	Power Spectral Density
RMS	Root Mean Square
SSB	Single Side Band
VCO	Voltage Controlled Oscillator
VHDL-AMS	Very High Speed Integrated Circuit Hardware Description Language - Analog and Mixed Signal

1. INTRODUCTION

PLLs find wide application in areas such as communications, wireless systems, digital circuits, and disk drive electronics. While the concept of phase locking has been in use for more than half a century, monolithic implementation of PLLs has become possible only in the last twenty years and popular in the last ten years. Two factors account for this trend: the demand for higher performance and lower cost in electronic systems, and the advance of integrated circuit (IC) technologies in terms of speed and complexity [1].

In the design of PLLs, we typically have to optimize a large set of parameters, including the performance of the building blocks, in order to achieve the desired system specifications. In view of the inherent non-linearity of the PLL and continuously varying operation frequency of the building blocks, this optimization process has to be carried out at the system level. Transistor level simulation of PLLs is only possible for final validation or for the extraction of the electrical parameters of the basic blocks.

In studying PLLs, the designer encounters two difficulties. First the basic PLL is deceptively simple, often tempting the designer to ignore the crucial details that determine the performance in a realistic environment. Second, the design of the PLL can not be easily described using a straight “top-down” or “bottom-up” approach, because each level of abstraction entails issues related to other levels as well.

In this thesis, the analytical expressions for the system specifications of simple loop PLL architecture are derived and tested with Very High Speed Integrated Circuit Hardware Description Language - Analog and Mixed Signal (VHDL-AMS) [2] simulations. The problem of noise analysis of PLLs is addressed in the presence of circuit white noise sources yielding the spectrum of the PLL output. In Chapter 2, simple loop PLL architecture is described with the goal of developing an intuitive understanding of the underlying principles and the important issues for more advanced topics in the following chapters. In Chapter 3, noise analysis of PLLs are discussed with a more theoretical aspect, and analytical noise analysis expressions are derived concerning the secondary effects in a

PLL mainly focusing on Charge Pump PLL architecture. In Chapter 4, the difficult issue of PLL modeling and simulation is addressed. Behavioral modeling of phase noise and jitter in PLLs with VHDL-AMS is implemented, and the correlation between the developed models and analytical noise expressions is shown.

2. SIMPLE LOOP PLL

In this chapter the principles of phase locked system design is described. Following a brief review of basic concepts, we analyze the static and dynamic behavior of phase locked loops. Next we extend the analysis to include the secondary effects and non-idealities.

2.1. Basic Topology

Phase Locked Loops (PLLs) are extensively used in microprocessors and digital signal processors for clock generation and as frequency synthesizers in RF communication systems for clock extraction and generation of a low phase noise local oscillator signal from on-chip voltage controlled oscillator (VCO), which might have a higher open loop noise performance. The basic block diagram of a PLL is shown in Figure 2.1. The phase of a local VCO signal is compared with the phase of a (hopefully) low noise reference signal and the difference of the two phases is low pass filtered and applied to the controlling node of the VCO. If the input signal is within the VCO tuning range, the VCO output is also "locked" to the same frequency as the input signal and the phase difference between the two signals is very small. In RF communication systems, frequency synthesizer noise directly degrades the overall noise performance of the system. Similarly, timing jitter in PLLs of high performance processors degrades the timing margins of the overall design. Hence, the accurate prediction of PLL noise performance is critical for the design of these systems.

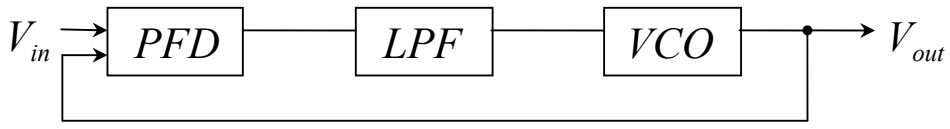

Figure 2.1. PLL block diagram

In a PLL, a VCO is present in the feedback loop and the difference in the phase of the reference and the VCO signal is filtered and used as the control signal of the VCO.

Therefore, one of the noise sources of the VCO is the difference of the phase noise of the reference signal and the VCO output along with the noise in the loop filter (LPF), phase detector (PD), and frequency dividers.

2.2. Loop Dynamics in Locked State

Figure 2.2 shows the linear model of the PLL in lock along with the transfer function of each block. The model provides the overall transfer function for the phase, $\phi_{out}(s)/\phi_{in}(s)$; hence, the PD is represented by a subtractor. The LPF is assumed to have a linear voltage transfer function $G_{LPF}(s)$.

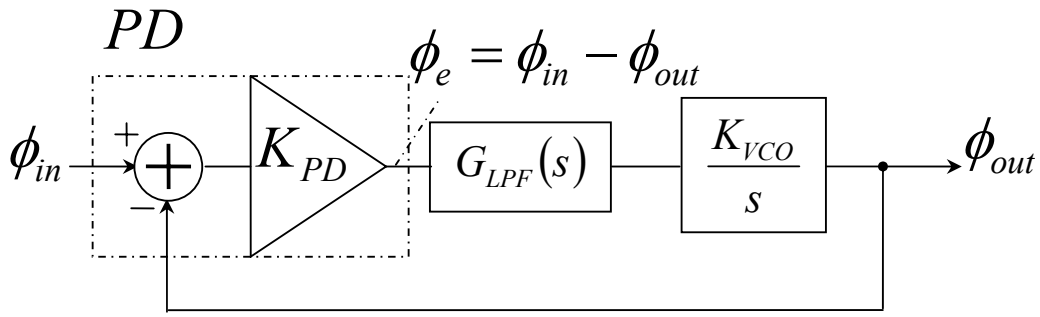

Figure 2.2. Linear model of a PLL

The open loop transfer function is therefore equal to

$$H_o(s) = K_{PD} G_{LPF}(s) \frac{K_{VCO}}{s} \tag{2.1}$$

yielding the following close loop transfer function:

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_{PD} K_{VCO} G_{LPF}(s)}{s + K_{PD} K_{VCO} G_{LPF}(s)} \tag{2.2}$$

In its simplest form, a low pass filter is implemented as in Figure 2.3, with

$$G_{LPF}(s) = \frac{1}{1 + \frac{s}{\omega_{LPF}}} \tag{2.3}$$

where $\omega_{LPF} = \frac{1}{RC}$. Equation (2.2) then reduces to

$$H(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} \tag{2.4}$$

indicating that the system is of second order, with one pole contributed by the VCO and another by the LPF. The quantity $K = K_{PD}K_{VCO}$ is called the *loop gain* of the system and expressed in rad/s.

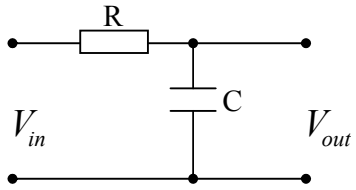

Figure 2.3. Simple low pass filter

In order to understand the dynamic behavior of the PLL, we convert the denominator of Equation (2.4) to the familiar form used in control theory: $s^2 + 2\zeta\omega_n s + \omega_n^2$ where ζ is the damping factor and ω_n is the natural frequency of the system. Thus,

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.5}$$

where

$$\omega_n = \sqrt{\omega_{LPF} K} \tag{2.6}$$

and

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K}} \tag{2.7}$$

The -3 dB bandwidth of the system is equal to:

$$\omega_{3dB} = \omega_n \left(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\right)^{1/2} \tag{2.8}$$

For $\zeta < 1$, the step response is,

$$y(t) = \left[1 + \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin\left(\omega_n \sqrt{1-\zeta^2}\, t - \psi\right)\right] u(t) \tag{2.9}$$

where $\psi = \sin^{-1}\sqrt{1-\zeta^2}$. Thus, the decay time constant is

$$\tau_{dec} = \frac{1}{\zeta\omega_n} = \frac{2}{\omega_{LPF}} \tag{2.10}$$

The phase error transfer function, defined as $H_e(s) = \frac{\phi_e(s)}{\phi_{in}(s)}$ in Figure 2.2:

$$H_e(s) = 1 - H(s) = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.11}$$

Suppose the input excess frequency is equal to $\Delta\omega u(t)$, where $u(t)$ is the unit step function. The output excess frequency then exhibits the typical step response of a second

order system, eventually settling to $\Delta\omega$ rad/s higher than its initial value. The output excess *phase*, on the other hand, is given by

$$\phi_{out}(s) = H(s)\phi_{in}(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}\frac{\Delta\omega}{s^2} \tag{2.12}$$

which is the response of a second order system to a *ramp* input. More importantly, the phase error is

$$\phi_e(s) = H_e(s)\phi_{in}(s) = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}\frac{\Delta\omega}{s^2} \tag{2.13}$$

whose final value is given by

$$\phi_e(t=\infty) = \lim_{s\to 0} s\phi_e(s) = \Delta\omega\frac{2\zeta}{\omega_n} = \frac{\Delta\omega}{K} \tag{2.14}$$

Therefore, static changes in the input frequency are suppressed by a factor K when they manifest themselves in the static phase error.

An important drawback of the PLL considered thus far is the direct relationship between ζ, ω_{LPF}, and K given by Equation (2.7). For example, if the loop gain is increased to reduce the static phase error, then the settling behavior degrades. In order to allow independent choice of K and ω_{LPF}, a zero can be added to the LPF as shown in Figure 2.4, modifying its transfer function to the following:

$$G_{LPF} = \frac{R_2 Cs + 1}{(R_1 + R_2)Cs + 1} \tag{2.15}$$

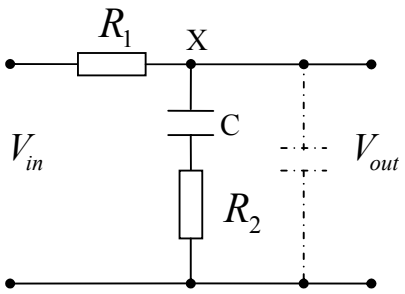

Figure 2.4. Low pass filter with a zero

Thus, the PLL transfer function is

$$H(s)=\frac{K\left(\frac{s}{\omega_z}+1\right)}{\frac{s^2}{\omega_p}+\left(\frac{K}{\omega_z}+1\right)s+K}=\frac{K\omega_p\left(\frac{s}{\omega_z}+1\right)}{s^2+\omega_p\left(\frac{K}{\omega_z}+1\right)s+K\omega_p} \tag{2.16}$$

Where $\omega_z=\frac{1}{R_2C}$ and $\omega_p=\frac{1}{[(R_1+R_2)C]}$. The damping factor is then equal to:

$$\zeta=\frac{1}{2}\sqrt{\frac{\omega_p}{K}}\left(\frac{K}{\omega_z}+1\right) \tag{2.17}$$

The -3 dB bandwidth of the system is equal to:

$$\omega_{3dB}=\frac{\omega_n}{2\pi}\left(a+\sqrt{a^2+1}\right)^{1/2} \tag{2.18}$$

where $a=2\zeta^2+1-\frac{\omega_n}{K}\left(4\zeta-\frac{\omega_n}{K}\right), \omega_n=\sqrt{K\omega_p}$.

The LPF attenuation of high-frequency signals is only $R_2/(R_1+R_2)$, usually a troublesome drawback. To alleviate this effect, a second capacitor can be connected from

node X in Figure 2.4 to ground so as to provide another pole beyond the zero(with some penalty in settling time).

The phase error transfer function is

$$H_e(s) = 1 - H(s) = \frac{s^2 + \omega_p s}{s^2 + \omega_p\left(\frac{K}{\omega_z} + 1\right)s + K\omega_p} \tag{2.19}$$

and the phase error for the input excess frequency of $\Delta\omega u(t)$, where $u(t)$ is the unit step function, is

$$\phi_e(s) = H_e(s)\phi_{in}(s) = \frac{s^2 + \omega_p s}{s^2 + \omega_p\left(\frac{K}{\omega_z} + 1\right)s + K\omega_p}\frac{\Delta\omega}{s^2} \tag{2.20}$$

whose final value is given by

$$\phi_e(t=\infty) = \lim_{s\to 0} s\phi_e(s) = \Delta\omega\frac{\omega_p}{K\omega_p} = \frac{\Delta\omega}{K} \tag{2.21}$$

2.3. Charge Pump Phase Locked Loops

Charge pump PLLs (CPPLLs) incorporate a PFD (or PD) and a charge pump (Figure 2.5) instead of the combinational PD and the LPF in the generic architecture of Figure 2.2. The combination of the PFD and a charge pump offers two important advantages: 1) the capture range is only limited by the VCO output frequency range; 2) the static phase error is zero if mismatches and offsets are negligible.

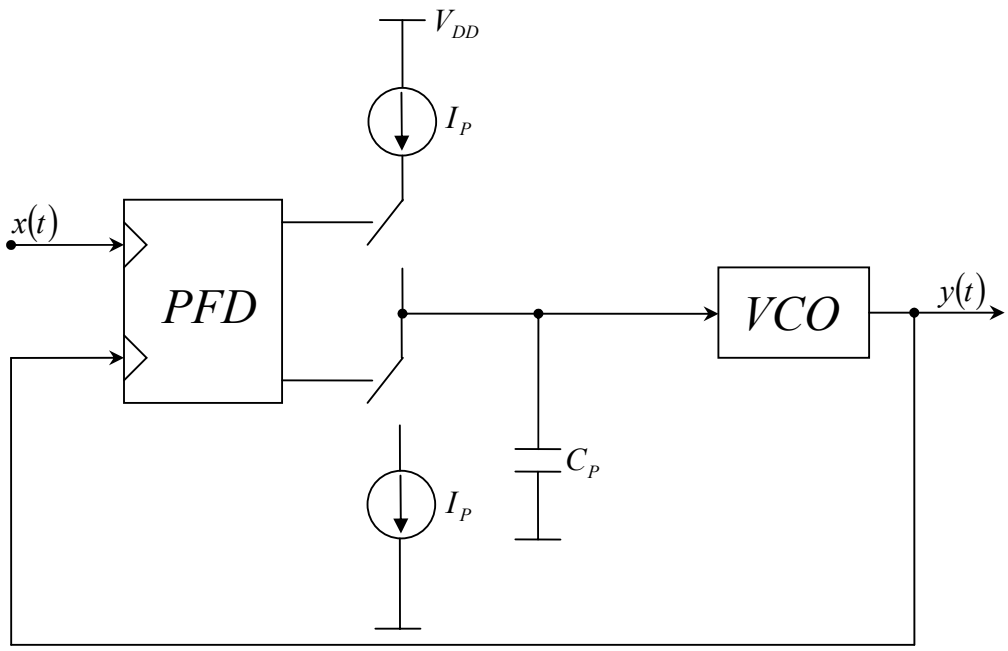

Figure 2.5. Charge pump PLL

Charge pumps provide an infinite gain for a *static* phase difference at the input of the PFD. From another point of view, the response of a PFD/charge pump to a phase step is a linear ramp, indicating that the transfer function of the circuit contains a pole at *the origin*. With another such pole contributed by the VCO, a charge pump PLL cannot remain stable. In fact, representing the transfer function of the PFD/charge pump with K_{PFD}/s, we note that the closed loop transfer function of the PLL is

$$H(s) = \frac{\dfrac{K_{PFD}}{s}\dfrac{K_{VCO}}{s}}{1+\dfrac{K_{PFD}}{s}\dfrac{K_{VCO}}{s}} = \frac{K_{PFD}K_{VCO}}{s^2 + K_{PFD}K_{VCO}} \tag{2.22}$$

revealing two imaginary poles at $\omega = \pm j\sqrt{K_{PFD}K_{VCO}}$. To avoid instability, a zero must be added to the open loop transfer function. This is in contrast to the case of a simple low pass filter, where the loop is, in principle, stable even with no zero. The stabilizing zero in a CPPLL can be realized by placing a resistor in series with the charge pump capacitor (Figure 2.6).

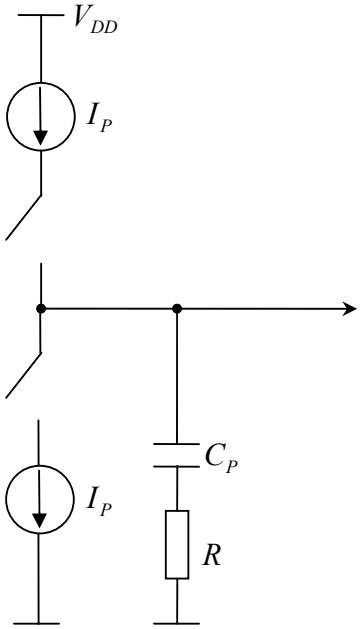

Figure 2.6. Addition of a zero to a charge pump

To perform a small signal analysis, we note that the switching operation of the charge pump and the lack of a discharge path between phase comparison instants make the PLL a discrete time system. However if the loop bandwidth is much less than the input frequency, we can assume the state of the PLL changes by a small amount during each cycle of the input. Using the "average" value of the discrete time parameters, we can then study the loop as a continuous time system.

Suppose the loop begins with a phase error

$$\phi_e = \phi_{in} - \phi_{out} \tag{2.23}$$

Then the average current charging the capacitor is given by $I_P\phi_e/(2\pi)$ and the average charge in the control voltage of the VCO equals

$$V_{cont}(s) = \frac{I_P\phi_e}{2\pi}\left(R + \frac{1}{C_P s}\right) \tag{2.24}$$

Noting that

$$\phi_{out}(s) = V_{cont}(s)\frac{K_{VCO}}{s} \tag{2.25}$$

we obtain the following closed loop transfer function:

$$H(s) = \frac{\frac{I_P}{2\pi C_P}(RC_P s + 1)K_{VCO}}{s^2 + \frac{I_P}{2\pi}K_{VCO}Rs + \frac{I_P}{2\pi C_P}K_{VCO}} \tag{2.26}$$

which has the same form as (2.16). Thus the system is characterized by a zero at

$$\omega_Z = -\frac{1}{RC_P} \tag{2.27}$$

with

$$\omega_n = \sqrt{\frac{I_P}{2\pi C_P}K_{VCO}} \tag{2.28}$$

and

$$\zeta = \frac{R}{2}\sqrt{\frac{I_P C_P}{2\pi}K_{VCO}} \tag{2.29}$$

In many applications, it is desirable to maximize the loop bandwidth, which is usually propotional to ω_n. Equations (2.28) and (2.29) suggest that in a CPPLL both ω_n and ζ can be increased if I_P or K_{VCO} is increased. However, as the loop bandwidth becomes comparable with the input frequency, the continuous time approximation used above breaks down, necessitating discrete time analysis. Using such an analysis, Gardner has derived a stability limit [3] that can be reduced to

$$\omega_n^2 < \frac{\omega_{in}^2}{\pi\left(RC_P\omega_{in} + \pi\right)} \tag{2.30}$$

The above charge pump suffers from a critical effect. Since the charge pump drives the series combination of a resistor and a capacitor, each time a current is injected into the filter, the control voltage experiences a large jump which is detrimental for the transient behavior of the VCO [4]. Therefore a second capacitor is placed in parallel to the series combination of the resistor and capacitor to suppress the initial step (Figure 2.7).

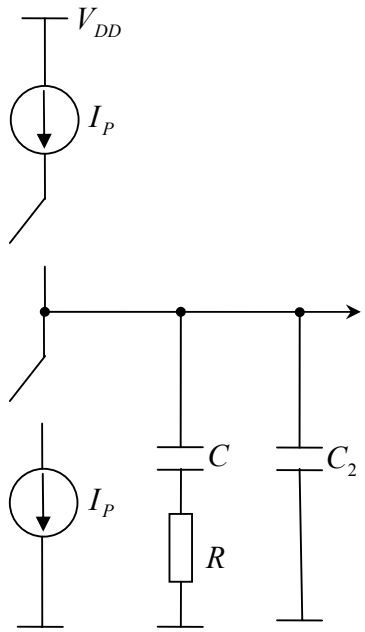

Figure 2.7. Addition of C_2 to suppress the initial step

Addition of C_2 introduces a third pole in the PLL, resulting in the following loop filter impedance.

$$Z(s) = \left(\frac{b-1}{b}\right)\frac{s\tau + 1}{sC\left(\frac{s\tau}{b} + 1\right)}; b = 1 + \frac{C}{C_2}; \tau = RC \tag{2.31}$$

and we obtain the following closed loop transfer function.

$$H(s)=\frac{K\left(\frac{b-1}{b}\right)\left(s+\frac{1}{\tau}\right)}{\frac{s^3\tau}{b}+s^2+K\left(\frac{b-1}{b}\right)s+\frac{K}{\tau}\left(\frac{b-1}{b}\right)};K=\frac{I_p}{2\pi}K_{VCO}R \tag{2.32}$$

Introduction of third pole in the PLL requires further study of stability issues. Gardner provides criteria for the stability of such systems [3].

2.4. Secondary Effects in CPPLLs

In practice, the charge pump is not ideal and has secondary effects such as the output impedance of the current mirror, the on resistance of the transistor switches and the current mismatch of the sourcing and sinking parties (Figure 2.8).

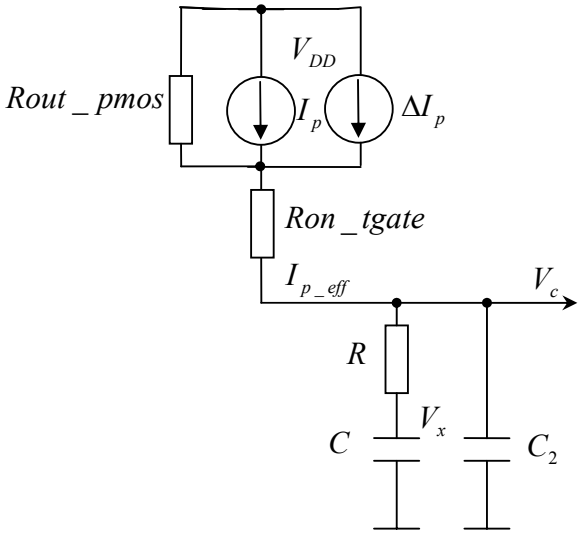

Figure 2.8. The secondary effects in the charge pump

These secondary effects can be included to the loop analysis by using the following set of equations.

$$
\begin{aligned}
&I_{P\_eff} = I_P + \Delta I_{P\_PMOS} + \frac{\Delta V_{C\_MIRROR}}{Rout\_pmos} \\
&\Delta V_{C\_MIRROR} = V_{DD} - V_{UP_{TGATE}} \\
&V_{UP_{TGATE}} = V_C + I_{P\_eff} Ron\_tgate \\
&\Delta V_{C\_MIRROR} \geq V_{SD_{SAT}}
\end{aligned}
\tag{2.33}
$$

$$
\frac{\partial V_C}{\partial t} = \frac{I_{P\_eff}}{C_2} - \frac{1}{RC_2} V_C + \frac{1}{RC_2} V_X \tag{2.34}
$$

$$
\frac{\partial V_X}{\partial t} = \frac{1}{RC} V_C - \frac{1}{RC} V_X \tag{2.35}
$$

$$
V_X(s) = \frac{V_C(s) + RCV_X(0)}{RCs + 1} \qquad \text{(2.36) solving (2.35)}
$$

$$
V_C(s) = \frac{RI_{P\_eff}(s) + V_X(s) + RC_2 V_C(0)}{RC_2 s + 1} \qquad \text{(2.37) solving (2.34)}
$$

$$
I_{P\_eff}(s) = \frac{(I_P + \Delta I_{P\_PMOS}) Rout\_pmos + V_{DD}}{(Rout\_pmos + Ron\_tgate)s} - \frac{V_C(s)}{Rout\_pmos + Ron\_tgate} \qquad \text{(2.38) solving (2.33)}
$$

Solving (2.36), (2.37) and (2.38), the following expression for the control node is obtained.

$$
V_C(s) = \frac{R(Rout\_pmos + Ron\_tgate)CC_2 V_C(0)s^2}{R(Rout\_pmos + Ron\_tgate)CC_2 s^3 + [(Rout\_pmos + Ron\_tgate)(C + C_2) + RC]s^2 + s} +
$$

$$
\frac{[RRout\_pmosC(I_P + \Delta I_{P\_PMOS}) + (Rout\_pmos + Ron\_tgate)(C_2 V_C(0) + CV_X(0)) + RCV_{DD}]s}{R(Rout\_pmos + Ron\_tgate)CC_2 s^3 + [(Rout\_pmos + Ron\_tgate)(C + C_2) + RC]s^2 + s} +
$$

$$
\frac{Rout\_pmos(I_P + \Delta I_{P\_PMOS}) + V_{DD}}{R(Rout\_pmos + Ron\_tgate)CC_2 s^3 + [(Rout\_pmos + Ron\_tgate)(C + C_2) + RC]s^2 + s} \tag{2.39}
$$

By using $Rout\_pmos + Ron\_tgate = Rcp\_out$, and rearranging Equation (2.39) to separate the zero input, zero state deterministic and probabilistic responses, Equation (2.39) simplified as

$$V_C(s) = \frac{RRcp\_outCC_2V_C(0)s^2 + Rcp\_out\left[C_2V_C(0) + CV_X(0)\right]s}{RRcp\_outCC_2s^3 + \left[Rcp\_out(C + C_2) + RC\right]s^2 + s} \quad \text{(zero input)}$$

$$+ \frac{\left[RRout\_pmosCI_P + RCV_{DD}\right]s + Rout\_pmosI_P + V_{DD}}{RRcp\_outCC_2s^3 + \left[Rcp\_out(C + C_2) + RC\right]s^2 + s} \quad \text{(zero state, deterministic)}$$

$$+ \frac{Rout\_pmos(RCs + 1)\Delta I_{P\_PMOS}}{RRcp\_outCC_2s^3 + \left[Rcp\_out(C + C_2) + RC\right]s^2 + s} \quad \text{(zero state, probabilistic)} \quad (2.40)$$

Equation (2.40) can be used to analyze the effects of different second order parameters on the control voltage. The effects of various charge pump output impedances and various tranmission gate on resistances are simulated in MATLAB 6.0.0.88 [5] and depicted in Figures (2.9 – 2.10). These simulations are 20ns long transient simulations, simulating the behavior of the control voltage of the vco for a 10ns long pumping of charge to the loop filter, i.e. a 10ns wide up pulse on the PFD output. The MATLAB file and the output figures are given in the companion CD-ROM (APPENDIX A).

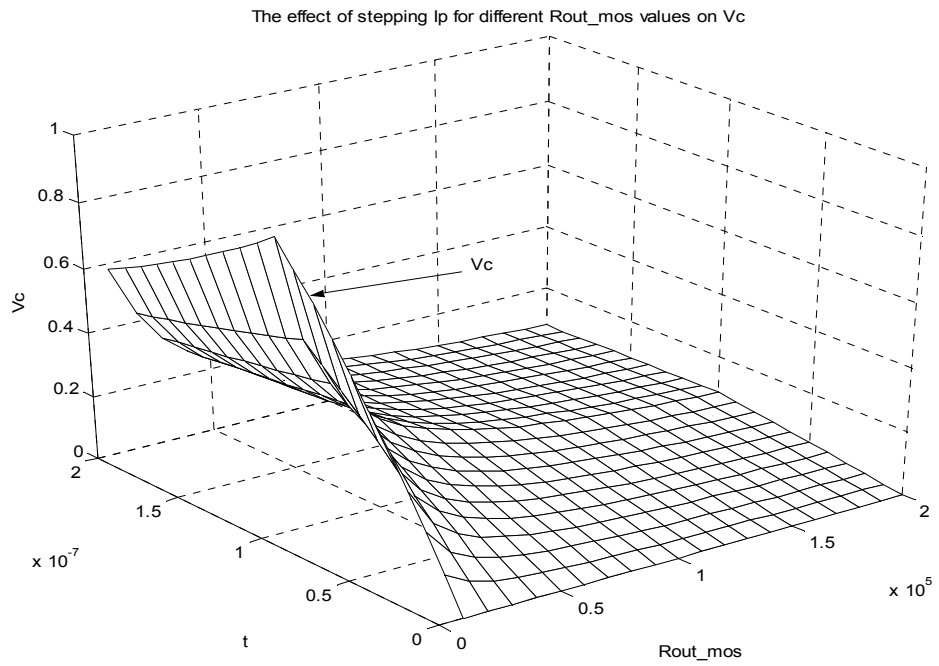

Figure 2.9. The effect of stepping Ip for different Rout_mos values on Vc

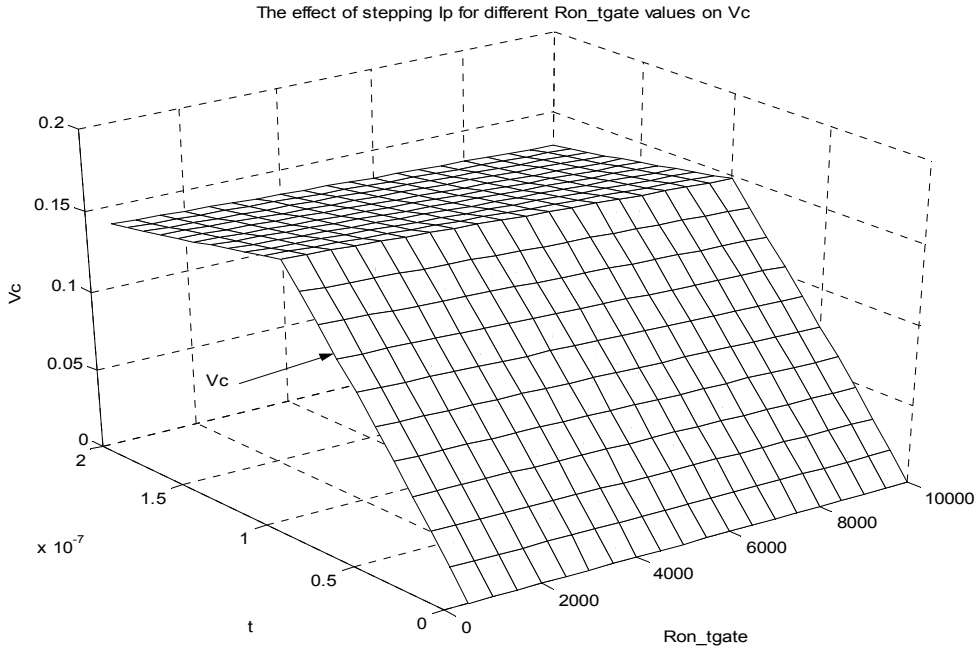

Figure 2.10. The effect of stepping Ip for different Ron_tgate values on Vc

3. NOISE ANALYSIS OF SIMPLE LOOP PLL

In this chapter, techniques borrowed from linear noise analysis is used to predict the output phase noise spectrum and the relative importance of VCO phase noise and reference signal phase noise as a function of the loop bandwidth. Furthermore, this analysis is extended to include the PLL circuit noise by using the techniques from nonlinear and stochastic noise analysis.

3.1. Linear Noise Analysis

Since PLLs operate on the phase of signals, they are susceptible to phase noise or jitter. If the input signal or the building blocks of a PLL exhibit noise, then the output signal will also suffer from noise. In general, all the loop components, including the phase detector, the LPF, the VCO, and the frequency divider may contribute noise [6]. The goal is to understand how the spectrum of a given noise source is shaped as it propagates to the output. We examine two important cases: 1) the input signal contains noise, and 2) the VCO introduces noise; in each case, we find the transfer function from the noise source of interest to the PLL output. In monolithic implementations, the phase noise of the VCO is typically much more significant than that of other loop components.

3.1.1. Phase Noise at Input

Consider the PLL in Figure 2.2 where the transfer function $\phi_{out}(s)/\phi_{in}(s)$ is

$$H(s)=\frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{3.1}$$

If $\phi_{in}(t)$ varies so slowly, $H(s)$ remains close to unity, indicating that the output phase (or frequency) follows the input phase (or frequency), a natural property of the PLL as a tracking system. For fast variations of the input excess phase or frequency, the PLL fails to track the input. In summary, the input phase noise spectrum of a PLL is shaped by the

characteristic low pass transfer function when it appears at the output (Figure 3.1). In order to minimize this noise, the loop bandwidth must be as small as possible, although it slows down the lock, limits the capture range, and degrades the stability.

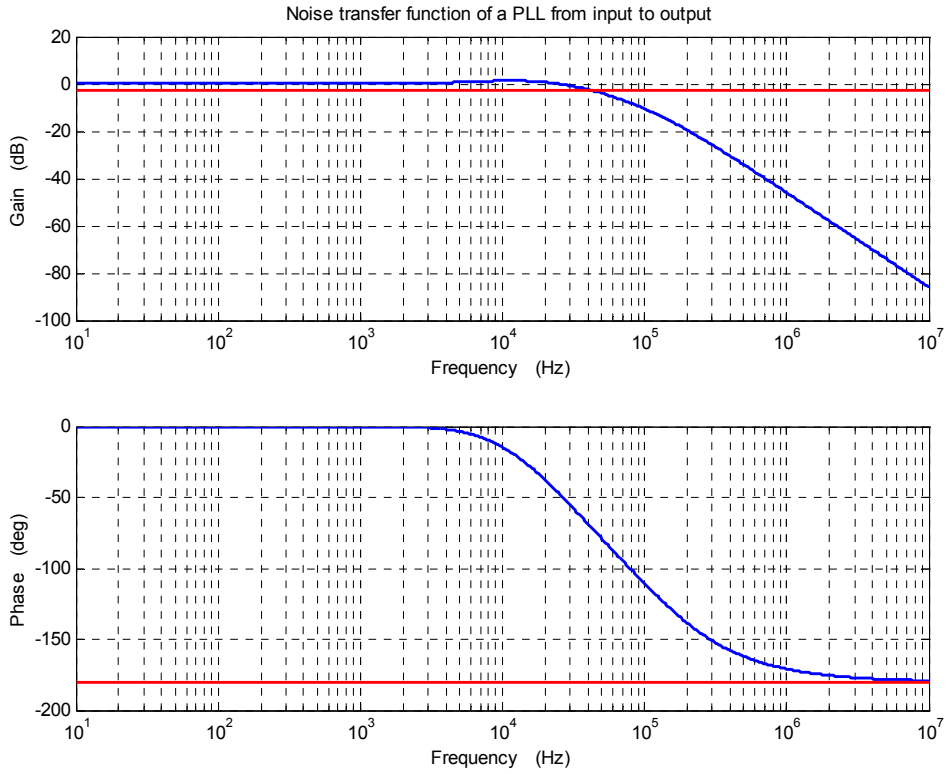

Figure 3.1. Noise transfer function of a PLL from input to output

3.1.2. Phase Noise of VCO

The phase noise of the VCO can be modeled as an additive component, ϕ_{VCO}, as shown in Figure 3.2. Assuming ϕ_{VCO} and ϕ_{in} are uncorrelated, we set ϕ_{in} to zero and compute the transfer function from ϕ_{VCO} to ϕ_{out}. Note that $\phi_{in}(t)=0$ means the *excess* phase of the input is zero, not the input signal itself; i.e., we must apply a strictly periodic signal at the input.

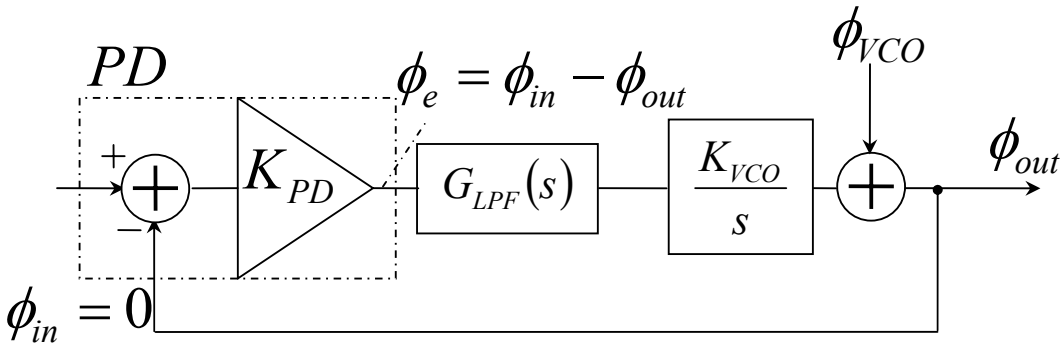

Figure 3.2. Noise transfer function of a PLL from VCO to output

With $\phi_{in} = 0$ and a simple LPF, we have

$$\frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{s(s+\omega_{LPF})}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.2}$$

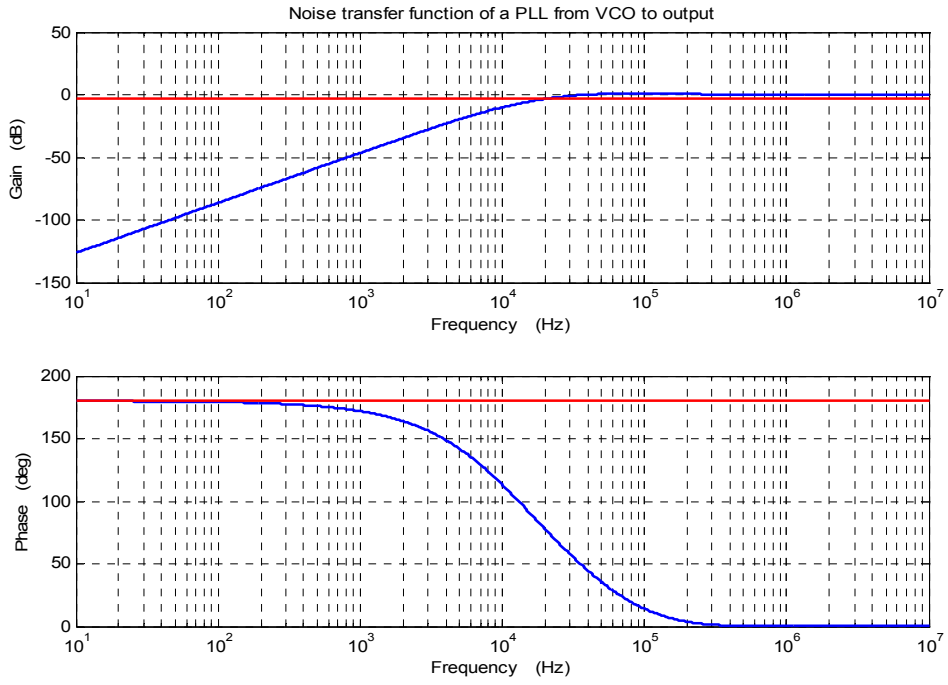

Figure 3.3. Noise transfer function of a PLL from VCO to output

As expected, this transfer function has the same poles as Equation (3.1), but it also contains two zeros at $\omega_{z1} = 0$ and $\omega_{z2} = -\omega_{LPF}$, making the characteristic a *high pass* filter (Figure 3.3).

A common test of noise immunity in PLLs entails applying a small step to the power supply and finding the time required for the input-output phase difference to settle within a certain error band [7]. Since such a step predominantly affects the VCO output, we can use Equation (3.2) to predict the behavior of the circuits. For a phase step of height ϕ_1, the output assumes the following form:

$$\phi_{out}(t) = \phi_1 \left[\cos\sqrt{1-\zeta^2}\,\omega_n t + \frac{\zeta}{\sqrt{1-\zeta^2}} \sin\sqrt{1-\zeta^2}\,\omega_n t \right] \times e^{-\zeta\omega_n t} \tag{3.3}$$

Thus, the output initially jumps to ϕ_1 and subsequently decays to zero with a time constant $(\zeta\omega_n)^{-1}$. It is therefore desirable to maximize $\zeta\omega_n$ for fast recovery of the PLL.

From the above analysis, we conclude that to minimize the VCO phase noise contribution, the loop bandwidth must be maximized, a requirement in conflict with that of the case where the PLL input contains noise. In applications where the input has negligible noise (e.g., because it is derived from a crystal oscillator), the loop bandwidth is maximized to reduce both the VCO phase noise and the lock time. The phase noise characteristics of a PLL for input and VCO noise sources are are simulated in MATLAB and depicted in Figure 3.4. The MATLAB file and the output figure are given in the companion CD-ROM (APPENDIX A).

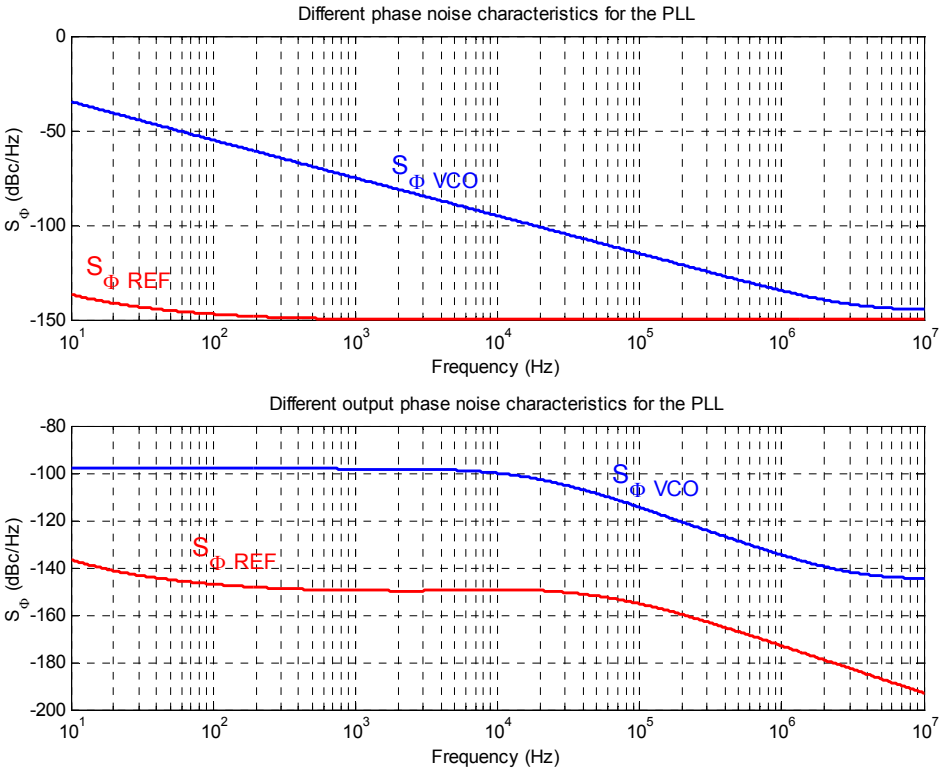

Figure 3.4. Phase noise characteristics of a PLL for input and VCO noise sources

3.2. Nonlinear Noise Analysis

The starting point of this work is [8-10] where noise analysis of open loop oscillators based on a novel perturbation analysis of an oscillatory system of equations was presented. The results presented in [8-10] for noise in open loop VCOs are summarized below.

- The phase deviation of the open loop VCO output is governed by the following stochastic differential equation:

$$\frac{d\alpha_{open\_loop\_vco}}{dt} = v^T\left(t + \alpha_{open\_loop\_vco}(t)\right)\xi_p(t) \tag{3.4}$$

where $\xi_p(t) \in R^p$ is a vector of p uncorrelated VCO white noise sources and $v(.) \in R^p = \left[v_1(.) \quad v_2(.) \quad . \quad . \quad v_p(.)\right]$ is a periodic function which depends on the noise source intensities and the response of the linearized oscillator circuit [8].

- It was shown that asymptotically $\alpha_{open\_loop\_vco}(t)$ becomes a Brownian motion process whose variance increases linearly with time at a rate c, i.e., $\alpha_{open\_loop\_vco} = \sqrt{c}B(t)$, where c is the time average of the inner product of the vector $v(.)$, i.e.

$$c = \frac{1}{T}\int_0^T v^T(t)v(t)dt \tag{3.5}$$

- The noisy oscillator output was shown to be of the form $x_s\left(t + \alpha_{open\_loop\_vco}(t)\right)$ where, $x_s(t)$ is the noiseless, periodic, steady state response of the oscillator.

Here we present the results of the work [11], which are a system of stochastic differential equations governing the behavior of the PLL VCO phase and a general expression for the power spectral density (PSD) of the PLL output. This expression used to derive the PSD of the PLL output for some specific loop filter configurations with various noise sources.

In a PLL, the difference of the reference and the VCO phase is filtered and applied to the VCO control node. Hence, Equation (3.4) is modified as follows:

$$\frac{d\alpha_{vco}}{dt} = v^T\left(t + \alpha_{vco}(t)\right)\xi_p(t) + v_{control}\left(t + \alpha_{vco}(t)\right)\gamma(t) \tag{3.6}$$

Here $\gamma(t)$ is the VCO input and $v_{control}(.) \in R$ is the component of $v(.)$ which corresponds to the unit noise source present at the control node of the VCO. The form of Equation (3.6) is valid only if the variance of $\gamma(t)$ is bounded for all t [11].

Now the important assumption that the PLL is in lock with the reference signal is introduced. By this, it is implied that the VCO output is *locked* to the same frequency as the reference signal or a multiple thereof if frequency dividers are used. $\beta(t)$ is defined as follows:

$$\beta(t) = \alpha_{vco}(t) - \alpha_{in}(t) \tag{3.7}$$

where $\alpha_{in}(t) = \sqrt{c_{in}} B_{in}$ and $B_{in}(t)$ is a one-dimensional(1-D) Brownian motion process Further, it is also assumed that $\beta(t)$ has *bounded* variance for all *t* [11].

Since $\gamma(t)$ is a filtered version of $\beta(t)$, $\beta(t)$ and $\gamma(t)$ are related by the following differential equation:

$$G\frac{dx}{dt} = Ex + F\xi_q(t) \tag{3.8}$$

where $x = [\beta(t) \quad \gamma(t) \quad . \quad . \quad .]^T$ is a vector of state variables, $x \in R^n, n = 1 + o_{lpf}, o_{lpf} > 0$ is the order of the LPF, $G, E \in R^{n-1 x n}$, and $F \in R^{n-1 x q}$, q is the number of noise sources in the LPF and the PD. Note that the coefficient matrices *G*, *E* and *F* are *independent* of time. This assumes that the reference signal frequency is not drifting with time and the VCO remains locked to the reference.

Equations (3.6)-(3.8) are solved using stochastic differential equation techniques and the following expression of $\beta(t)$ is obtained.

$$\frac{d\beta}{dt} = C_{VCO}^T \xi_p(t) + \sqrt{c_{control}}\,\gamma(t) - \sqrt{c_{in}}\,\xi_{in}(t) \tag{3.9}$$

Where $\xi_{in}(t)$ is the white noise process which is the time derivative of $B_{in}(t)$,

$$C_{VCO}^T = \left[\sqrt{c_1} \quad \sqrt{c_2} \quad . \quad . \quad \sqrt{c_p}\right]^T \tag{3.10}$$

$$c_i = \frac{1}{T}\int_0^T v_i^2(t)dt \tag{3.11}$$

and

$$c_{control} = \frac{1}{T}\int_0^T v_{control}^2(t)dt \tag{3.12}$$

Equations (3.8) and (3.9) can be combined to obtain a linear differential equation of the form

$$\dot{x} = -Ax + D\xi_{p+q+1} \tag{3.13}$$

for appropriate $A \in R^{nxn}$ and $D \in R^{nx(p+q+1)}$ where $\xi_{p+q+1}(t) = \left[\xi_p(t) \quad \xi_q(t) \quad \xi_{in}(t)\right]^T$ is a vector of *(p+q+1)* uncorrelated white noise processes.

PSD of the output is given by

$$S_{x_s,x_s}(\omega) = \sum_{i=-\infty}^{\infty} \sum_{k_1,\ldots,k_n=0}^{\infty} 2X_i X_i^* \exp\left[-\omega_0^2 i^2 \sum_{l=1}^{n}(\mu_l + v_l)\right]$$

$$\times \frac{\left[\prod_{l=1}^{n}\left[i^2\omega_0^2(\mu_l + v_l)\right]^{k_l}\right]\left(\frac{1}{2}\omega_0^2 i^2 c_{in} + \sum_{l=1}^{n} k_l\lambda_l\right)}{\left[\prod_{l=1}^{n} k_l!\right]\left[\left(\frac{1}{2}\omega_0^2 i^2 c_{in} + \sum_{l=1}^{n} k_l\lambda_l\right)^2 + (\omega + i\omega_0)^2\right]} \tag{3.14}$$

where

$$\mu_i = \sqrt{c_{in}}\,\frac{w_{1_i} d_{(p+q+1)_i}}{\lambda_i} \tag{3.15}$$

where w_1 is the first row of W, d_{p+q+1} is the last column of $W^{-1}D$, w_{1_i} and $d_{(p+q+1)_i}$ are the i th components of w_1 and d_{p+q+1}, respectively.

$A = W\Lambda W^{-1}$ where $\Lambda = diag(\lambda_1,...,\lambda_n)$ is a diagonal matrix of eigenvalues of A and W is a matrix of the corresponding eigenvectors.

Let $X = W^{-1}DD^TW^{-T}$ then,

$$v_i = \frac{w_{1_i}^2 x_{ii}}{2\lambda_i} + \sum_{j=1, j\neq i}^{n} \frac{w_{1_i} w_{1_j} x_{ij}}{2(\lambda_i + \lambda_j)} \tag{3.16}$$

In practice, one is usually interested in the PSD around the first harmonic which is defined (in dBc/Hz) as

$$10\log_{10}\left(\frac{S_{x_s,x_s}(\omega-\omega_0)}{|X_1|^2}\right) \tag{3.17}$$

3.2.1. PLL Examples

The algorithm for computing the PLL output spectrum is implemented in MATLAB. From Equation (3.9), it follows that the noise analysis of VCO need not be a part of the PLL noise analysis. The VCO parameters required for PLL noise analysis are $c_{vco} = \sum_i c_i$ and $c_{control}$, and these can be computed separately for the open loop VCO using the techniques presented elsewhere [9]. Note that the size of the matrix in Equation (3.13) is very small (typical values of *n* are 4-5). Therefore, the spectrum calculation involves the diagonalization of a very small matrix and this process is very efficient. In practice, infinite summations in Equation (3.14) are truncated to some finite integer. Unlike the noise analysis of many other periodic circuits, PLL noise analysis *does not* require a transient analysis of the entire circuit. Transient analysis of a PLL is very expensive because of widely separated time constants present in the circuit and CPU times of the order of a few hours are common. Assuming that the PLL locks to the reference frequency, the VCO

control voltage can be computed such that the VCO output is also at the appropriate frequency and its noise analysis can then be performed.

PLL without LPF, with a first order filter, CPPLL (first and second order) examples already exist in [11]. In this section, three specific examples of noise sources in charge pump PLLs are analyzed. These noise sources are:

- transmission gate on resistance,
- current mirror output resistance,
- any mismatch between charge pump up and down currents.

3.2.1.1. CPPLL with R_{TG}. A three-state charge pump can be studied in conjunction with a three-state phase/frequency detector (Figure 2.5). The pump itself consists of two switched current sources driving a capacitor. These switches are composed of a NMOS device and a PMOS device in parallel arrangement, and are not ideal switches, because they have series resistance associated with them. When analyzing them, the simplifying assumption that the switch has a constant resistive value is acceptable as in Figure (3.5).

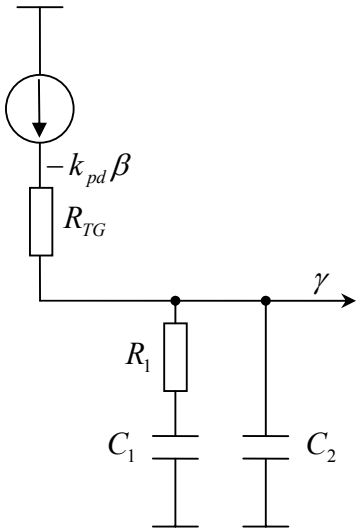

Figure 3.5. CPPLL with R_{TG}

For the above case Equation (3.13) can be written as

$$\frac{d}{dt}\begin{bmatrix}\beta\\ \bar{\gamma}\\ \delta\end{bmatrix}=-\begin{bmatrix}0 & -\sqrt{c_{pll}} & 0\\ 0 & 0 & -1\\ \dfrac{\omega_{lpf}\omega_2\zeta}{R_{TG}} & \dfrac{\omega_2\zeta\left(\sqrt{c_{pll}}+\omega_{lpf}\right)}{R_{TG}} & \dfrac{\omega_2\left(\zeta+R_{TG}\right)}{R_{TG}}\end{bmatrix}\begin{bmatrix}\beta\\ \bar{\gamma}\\ \delta\end{bmatrix}+$$

$$\begin{bmatrix}C_{VCO}^T & -\sqrt{c_{in}}\\ 0 & 0\\ \dfrac{-\omega_2\zeta C_{VCO}^T}{R_{TG}} & \dfrac{\omega_2\zeta\sqrt{c_{in}}}{R_{TG}}\end{bmatrix}\begin{bmatrix}\xi_p(t)\\ \xi_{in}(t)\end{bmatrix} \tag{3.18}$$

where

$$\zeta=\frac{R_1C_1}{\left(C_1+C_2\right)},\omega_{lpf}=\frac{1}{R_1C_1},\omega_2=\left(1+\frac{C_2}{C_1}\right)\omega_{lpf},\bar{\gamma}=\frac{\gamma}{k_{pd}},\sqrt{c_{pll}}=k_{pd}\sqrt{c_{control}}$$

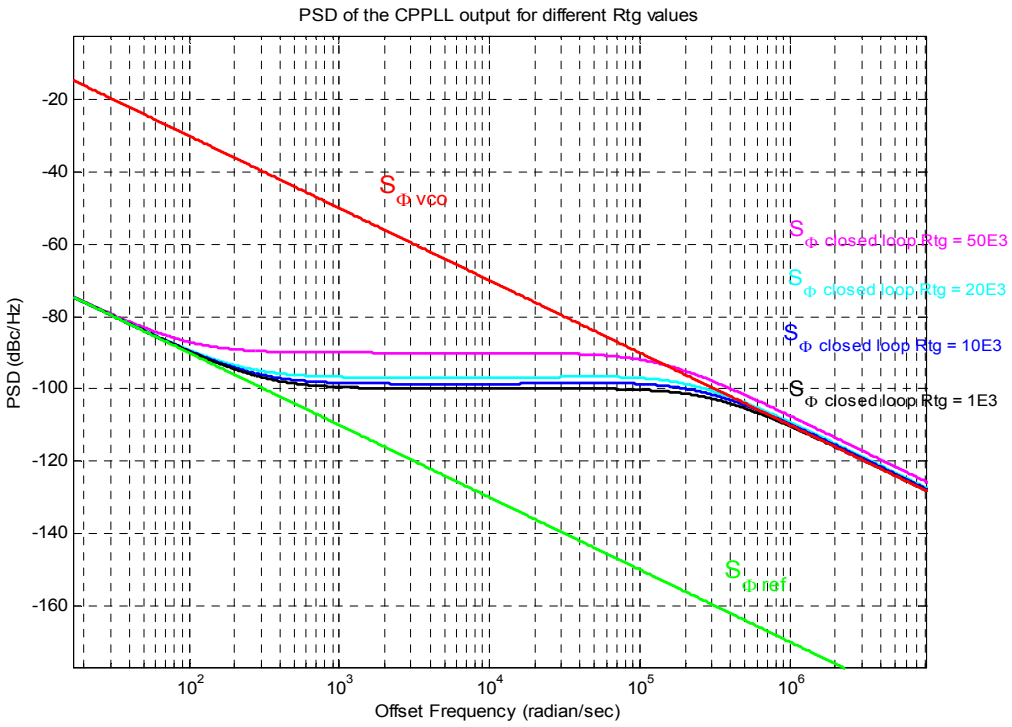

Figure 3.6. Power spectrum density of CPPLL for different R_{TG} values

Table 3.1. PSD values for different Rtg vaules

Offset Frequency(rad/sec)	$R_{TG}\ (\Omega)$	PSD(dBc/Hz)
10^4	10^3	-100
10^4	10^4	-98
10^4	2×10^4	-95
10^4	5×10^4	-88

CPPLL power spectrum density computation for different R_{TG} values are implemented in MATLAB and, the results are given in Figure (3.6) and Table (3.1). The MATLAB file and the output figure are given in the companion CD-ROM (APPENDIX A).

3.2.1.2. CPPLL with R_{TG} and R_O. The current sources in the charge pump are not ideal and they have output impedances associated with them.

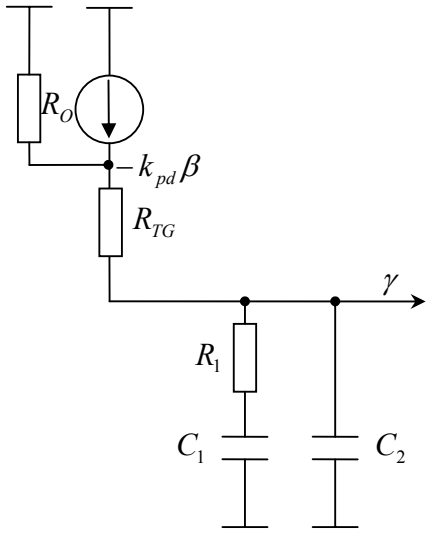

Figure 3.7. CPPLL with R_{TG} and R_O

For the above case Equation (3.13) can be written as

$$\frac{d}{dt}\begin{bmatrix}\beta\\ \overline{\gamma}\\ \delta\end{bmatrix}=-\begin{bmatrix}0 & -\sqrt{c_{pll}} & 0\\ 0 & 0 & -1\\ \dfrac{\omega_{lpf}\omega_2\zeta R_O}{R_{TG}+R_O} & \dfrac{\omega_2\zeta\omega_{lpf}+\omega_2\sqrt{c_{pll}}R_O(R_{TG}+\zeta)}{R_{TG}+R_O} & \dfrac{R_O R_{TG}\sqrt{c_{pll}}+\omega_2(\zeta+R_{TG}+R_O)}{R_{TG}+R_O}\end{bmatrix}\begin{bmatrix}\beta\\ \overline{\gamma}\\ \delta\end{bmatrix}$$

$$+\begin{bmatrix}C_{VCO}^T & -\sqrt{c_{in}}\\ 0 & 0\\ \dfrac{-\omega_2 R_O(\zeta+R_{TG})C_{VCO}^T}{R_{TG}+R_O} & \dfrac{\omega_2 R_O\sqrt{c_{in}}(R_{TG}+\zeta)}{R_{TG}+R_O}\end{bmatrix}\begin{bmatrix}\xi_p(t)\\ \xi_{in}(t)\end{bmatrix}+$$

$$\begin{bmatrix}\dfrac{-R_O R_{TG}C_{VCO}^T}{R_O+R_{TG}} & \dfrac{R_O R_{TG}\sqrt{c_{in}}}{R_O+R_{TG}}\end{bmatrix}\begin{bmatrix}\dfrac{d\xi_p(t)}{dt}\\ \dfrac{d\xi_{in}(t)}{dt}\end{bmatrix} \tag{3.19}$$

where

$$\zeta=\frac{R_1C_1}{(C_1+C_2)},\omega_{lpf}=\frac{1}{R_1C_1},\omega_2=\left(1+\frac{C_2}{C_1}\right)\omega_{lpf},\overline{\gamma}=\frac{\gamma}{k_{pd}},\sqrt{c_{pll}}=k_{pd}\sqrt{c_{control}}$$

CPPLL power spectrum density computation for different R_O values for a nominal R_{TG} value of $5K\Omega$ are implemented in MATLAB, and the results are given in Figure (3.8) and Table (3.2). The MATLAB file and the output figure are given in the the companion CD-ROM (APPENDIX A).

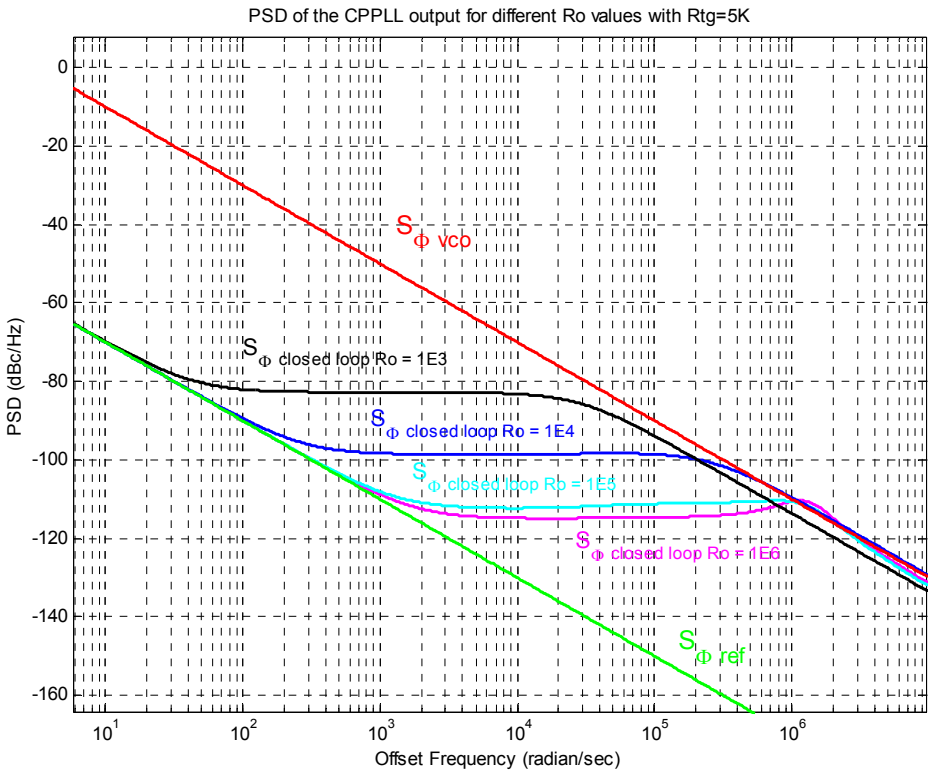

Figure 3.8. Power spectrum density of CPPLL for different R_O values

Table 3.2. PSD values for different R_O vaules with R_{TG} = 5K

Offset Frequency(rad/sec)	R_O (Ω)	PSD(dBc/Hz)
10^4	10^3	-84
10^4	10^4	-98
10^4	10^5	-112
10^4	10^6	-114

CPPLL power spectrum density computation for different R_O and R_{TG} values are implemented in MATLAB and the results are depicted in Figure (3.9) and Table (3.3) for an offset frequency of 10^4 rad/sec. The MATLAB file and the output figure are given in the companion CD-ROM (APPENDIX A). Note that, in Figure (3.9) the R_O scale is logarithmic for a better visualization.

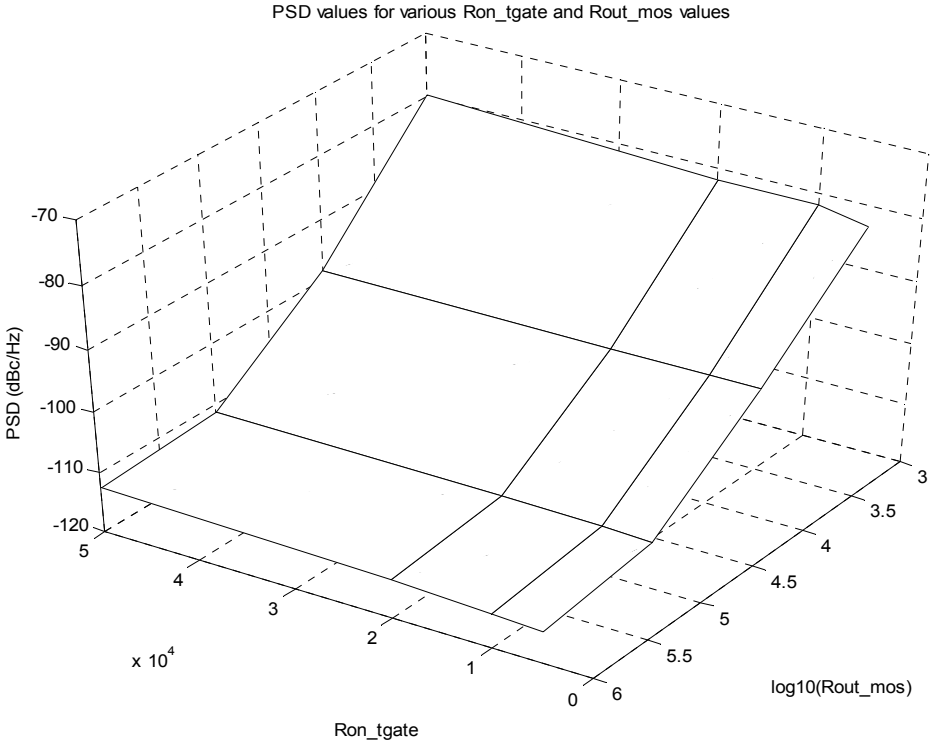

Figure 3.9. Power spectrum density of CPPLL for different R_O and R_{TG} values

Table 3.3. Power spectrum density of CPPLL for different R_O and R_{TG} values

PSD(dBc/Hz)		$R_O\ (\Omega)$			
		10^3	10^4	10^5	10^6
$R_{TG}\ (\Omega)$	5×10^3	-83.2	-98.6	-112.3	-114.8
	10^4	-81.8	-98.55	-112	-114.25
	2×10^4	-81.8	-98.5	-111.63	-113.49
	5×10^4	-79.64	-98.33	-111.3	-112.6

3.2.1.3. CPPLL with R_{TG}, R_O and ΔI_{CP}. One of the non-idealities of the current sources in the charge pump is the mismatches in the currents of the sinking and sourcing parties. Usually these mismatches are process dependent, and stochastic. For that reason these mismatches are modeled as stochastic as $\Delta I_{CP} = \sqrt{c_{CPUMP}}\,\xi_q(t)$ (Figure 3.10).

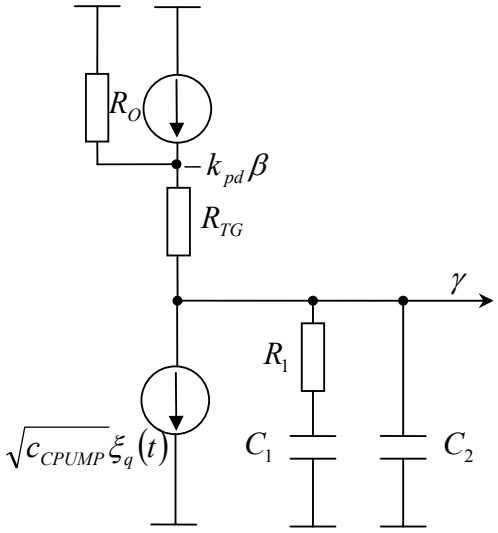

Figure 3.10. CPPLL with R_{TG}, R_O and $\Delta I_{CP} = \sqrt{c_{CPUMP}}\xi_q(t)$

For the above case Equation (3.13) can be written as

$$\frac{d}{dt}\begin{bmatrix}\beta\\ \gamma\\ \delta\end{bmatrix} = -\begin{bmatrix} 0 & -\sqrt{c_{pll}} & 0 \\ 0 & 0 & -1 \\ \dfrac{\omega_{lpf}\omega_2\zeta R_O}{R_{TG}+R_O} & \dfrac{\omega_2\zeta\omega_{lpf}+\omega_2\sqrt{c_{pll}}R_O(R_{TG}+\zeta)}{R_{TG}+R_O} & \dfrac{R_O R_{TG}\sqrt{c_{pll}}+\omega_2(\zeta+R_{TG}+R_O)}{R_{TG}+R_O}\end{bmatrix}\begin{bmatrix}\beta\\ \gamma\\ \delta\end{bmatrix}$$

$$+\begin{bmatrix} C_{VCO}^T & 0 & -\sqrt{c_{in}} \\ 0 & 0 & 0 \\ \dfrac{-\omega_2 R_O(\zeta+R_{TG})C_{VCO}^T}{R_{TG}+R_O} & \dfrac{-R_O\zeta\sqrt{c_{CP}}\omega_{lpf}\omega_2}{R_O+R_{TG}} & \dfrac{\omega_2 R_O\sqrt{c_{in}}(R_{TG}+\zeta)}{R_{TG}+R_O}\end{bmatrix}\begin{bmatrix}\xi_p(t)\\ \xi_q(t)\\ \xi_{in}(t)\end{bmatrix}$$

$$+\begin{bmatrix}\dfrac{-R_O R_{TG}C_{VCO}^T}{R_O+R_{TG}} & -R_O\sqrt{c_{CP}}(R_{TG}+\zeta) & \dfrac{R_O R_{TG}\sqrt{c_{in}}}{R_O+R_{TG}}\end{bmatrix}\begin{bmatrix}\dfrac{d\xi_p(t)}{dt}\\ \dfrac{d\xi_q(t)}{dt}\\ \dfrac{d\xi_{in}(t)}{dt}\end{bmatrix}+$$

$$\left[-\frac{\sqrt{c_{pll}}R_O R_{TG}}{\omega_2}\right]\left[\frac{d^2\xi_q(t)}{dt^2}\right] \tag{3.20}$$

where

$$\zeta=\frac{R_1C_1}{(C_1+C_2)},\omega_{lpf}=\frac{1}{R_1C_1},\omega_2=\left(1+\frac{C_2}{C_1}\right)\omega_{lpf},\bar{\gamma}=\frac{\gamma}{k_{pd}},\sqrt{c_{pll}}=k_{pd}\sqrt{c_{control}},\sqrt{c_{cp}}=\frac{\sqrt{c_{CPUMP}}}{k_{pd}}$$

CPPLL power spectrum density computation for different ΔI_{CP} values and for the nominal values of $R_{TG}=5K\Omega$ and $R_O=100K\Omega$ are implemented in MATLAB, and the results are given in Figure (3.11) and Table (3.4). The MATLAB file and the output figure are given in the companion CD-ROM (APPENDIX A).

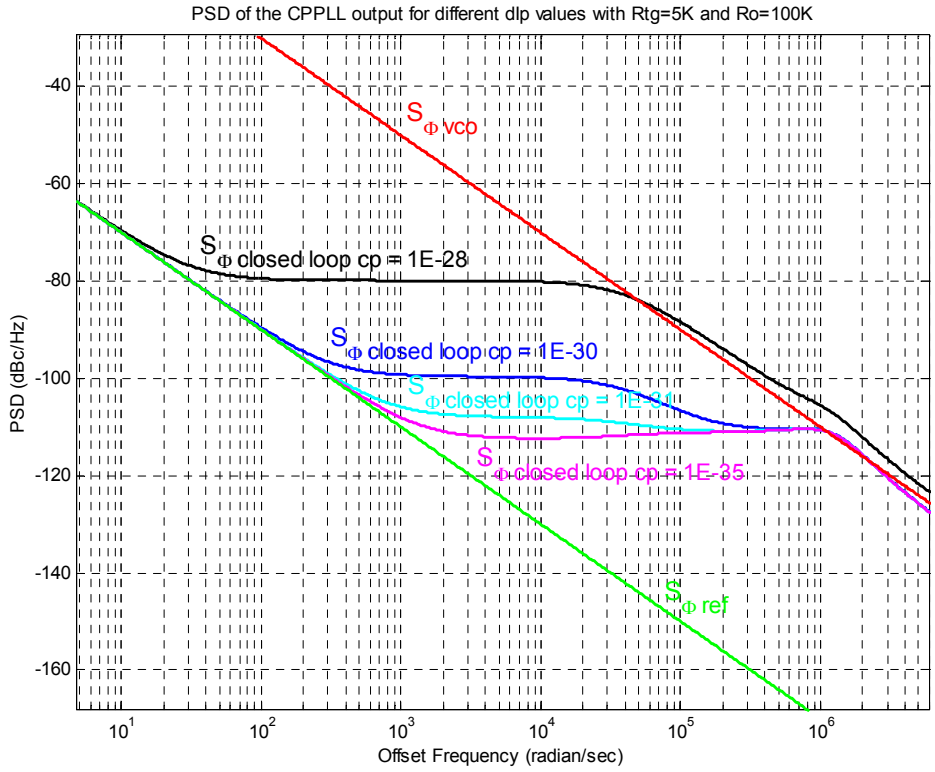

Figure 3.11. Power spectrum density of CPPLL for different ΔI_{CP} values

Table 3.4. PSD values for different ΔI_{CP} vaules with R_{TG} = 5K and $R_O = 100K\Omega$

Offset Frequency(rad/sec)	c_{cp}	PSD(dBc/Hz)
10^4	1×10^{-28}	-80
10^4	1×10^{-30}	-100
10^4	1×10^{-31}	-108
10^4	1×10^{-35}	-114

4. SIMULATIONS AND CORRELATIONS

In this chapter, output spectrum of a classical charge pump PLL is computed by using the noise analysis techniques presented in Chapter 3, and correlated with VHDL-AMS simulations.

4.1. Behavioral Modeling of Phase Noise and Jitter in VCOs

The behavioral modeling technique [12] is used to simulate Voltage Controlled Oscillators. It permits to minimize simulation runtime required to evaluate oscillator performances. The VCO model is developed using the standard description language VHDL-AMS and simulated with Smash 5.3.1 [13]. Because there is no possibility to do phase noise simulations, the jitter effect is introduced in the developed model. Therefore a transient simulation permits to calculate the jitter and then to deduce the phase noise characteristics. The steps of the modeling technique are explained in following.

4.1.1. Fluctuated Output Period Calculation

The jitter represents a random fluctuation of the ideal output period T_0. So it is modeled by adding random variation to T_0.

$$T_n = T_0\left(1 + A_0 J_n\right) \tag{4.1}$$

where T_n is the output period, A_0 is a parameter defining the maximum perturbation and J_n a random signal $\left(J_n \in [-1,1]\right)$ obtained from a random signal generator.

4.1.2. Random Signal Generator

To generate the real J_n, the following random signal generator, which is based on the random function proposed by Park and Miller [14], is used.

$$x_n = 16807 x_{n-1} \bmod\left[2^{31}\right] \tag{4.2}$$

It returns a pseudo random number *x* with uniform distribution and only white noise sources have been considered in the developed model.

4.1.3. Jitter Adjustment

In the time domain representation, the spacing between oscillator output transitions is ideally constant. In practice, however, the transition spacing is variable due to noise fluctuations. This uncertainty is known as timing jitter and defined as

$$\Delta T_n = T_n - \overline{T} \tag{4.3}$$

where T_n as the n^{th} period of the output and $\overline{T}$ is the mean period. The RMS value of the timing error ΔT_n defines the *cycle jitter* ΔT_c.

$$\Delta T_c = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2} \tag{4.4}$$

Phase noise and jitter characterize the same phenomenon, and they have the following relationship [15].

$$S_\phi(\omega_m) = \frac{1}{2\pi}\frac{\omega_0^3}{\omega_m^2}\Delta T_c^2 \tag{4.5}$$

Considering Equation (4.3), ΔT_c can be expressed as the following:

$$\Delta T_c = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \left(A_0 J_n T_0\right)^2} = A_0 T_0 \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} J_n^2}$$

$$= \frac{1}{\sqrt{3}} A_0 T_0 \tag{4.6}$$

By substituting Equation (4.6) in Equation (4.5), the following power spectrum density equation is obtained.

$$S_\phi(\omega_m) = \frac{4\pi^2}{3} A_0^2 \frac{1}{\omega_m^2} \frac{1}{T_0} \tag{4.7}$$

So by adjusting the parameter A_0, we can adjust ΔT_c and $S_\phi(\omega_m)$.

4.1.4. The VCO Model Example

A VCO is modeled for the case $A_0 = 0.008$ and $T_0 = 5ns$, which gives

$$\Delta T_c = \frac{1}{\sqrt{3}} A_0 T_0 = 0.008 \times 5ns = 23.1ps$$

The VCO model is simulated with Smash 5.3.1. The obtained signal *cycle jitter* after a $5us$ transient simulation is depicted in Figure (4.1). ΔT_c corresponds to the curve limit $22.5ps$, which is very close to the calculated $23.1ps$ value. The simulation file and the output figure are given in the companion CD-ROM (APPENDIX A).

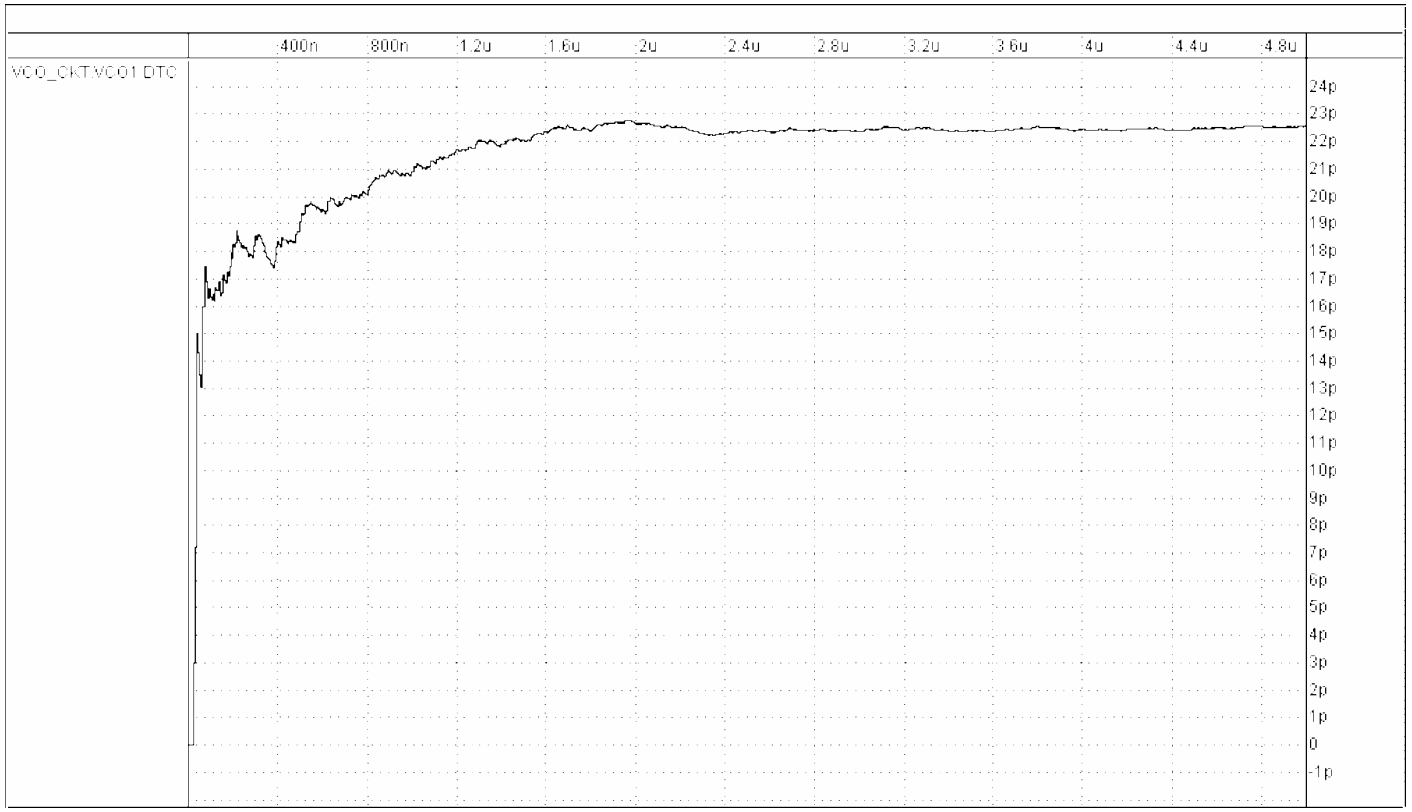

Figure 4.1. Cycle jitter simulation output

4.2. CPPLL Example

In this section, the phase noise of a CPPLL is calculated by using the techniques given in Chapter 3, and the same PLL is simulated by using the VCO model given in Section 4.1, then the results are correlated.

4.2.1. CPPLL PSD Calculations

The computed output spectrum around the first harmonic is shown in Figure (4.2) for the case $\omega_0 = 12.566\times10^6\ rad/\sec, c_{in} = 1.58\times10^{-12}\ \sec, c_{vco} = 1.412\times10^{-9}\ \sec$ and $c_{pll} = 1.849\times10^9\ 1/\sec^2$. This corresponds to a phase noise performance of -78 dBc/Hz at 20 KHz offset for the reference signal, -48 dBc/Hz for the open loop VCO and -52 dBc/Hz for the PLL. The PLL output spectrum follows that reference input spectrum for low offset frequencies and open loop VCO spectrum for large offset frequencies. Note that the offset frequency beyond which the PLL output spectrum follows the open loop VCO spectrum is approximately $\sqrt{c_{pll}}/2\pi = 6843Hz$ i.e. the *bandwidth* of the PLL.

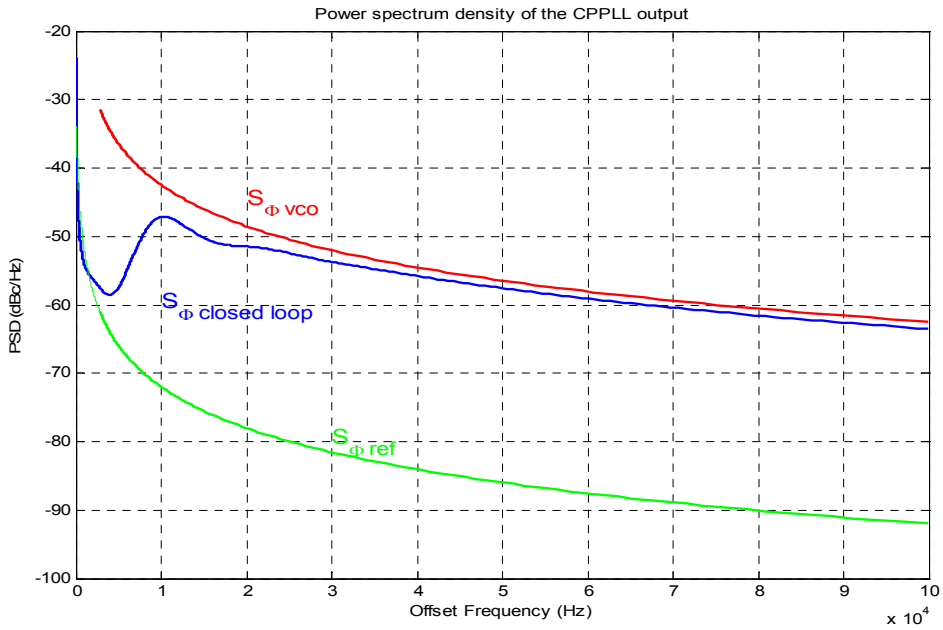

Figure 4.2. CPPLL output spectrum

4.2.2. CPPLL PSD Simulations

In Figures (4.4 - 4.8), the simulated CPPLL, open loop VCO and reference input spectra (both double side band (DSB) and single side band (SSB) waveforms) are presented. The simulation file and the output figures are given in the companion CD-ROM (APPENDIX A). The calculated response (Figure 4.2) is also given in the same x-y axis range as in the simulated response (Figure 4.4) in Figure 4.3 to ease the correlation. Note the same characteristic in both calculated and simulated closed loop responses. In Figure 4.6, VCO has a phase noise performance of -62 dBc/Hz at 100KHz offset, which is the same as both computed (Figures 4.2 - 4.3) and simulated (Figure 4.4) CPPLL spectrums. In Figure 4.6 reference input has a phase noise performance of -55 dBc/Hz around 2 KHz offset, which is also close to both the computed (Figures 4.2 - 4.3) and simulated (Figure 4.4) CPPLL spectrums. So the simulated CPPLL output spectrum also follows that reference input spectrum for low offset frequencies and open loop VCO spectrum for large offset frequencies. As a result, a good agreement is obtained between the analytically computed and simulated output spectrums.

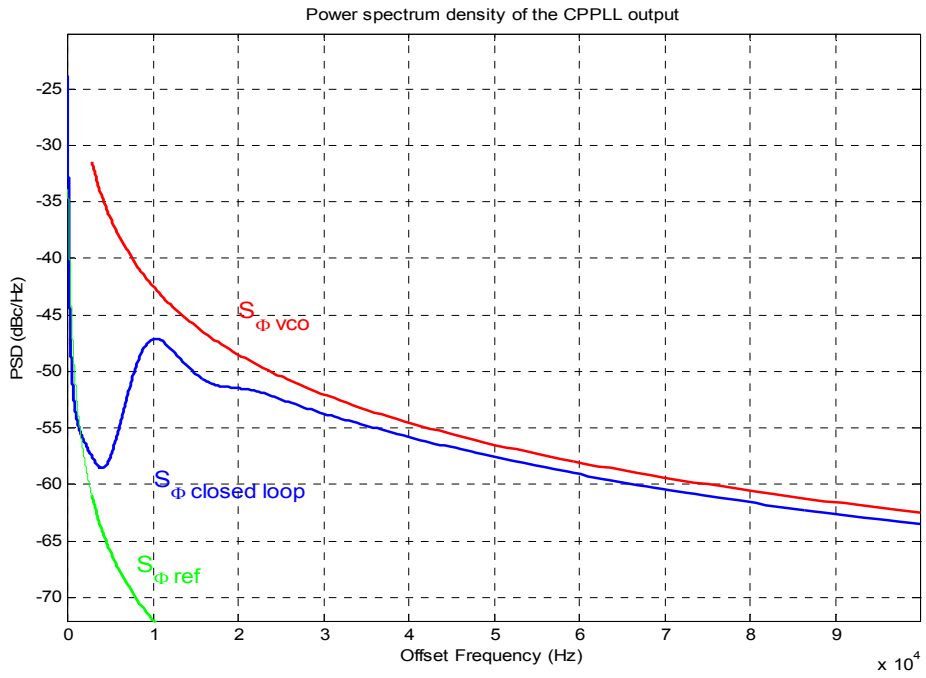

Figure 4.3. CPPLL output spectrum with same x-y axis range as Figure 4.4

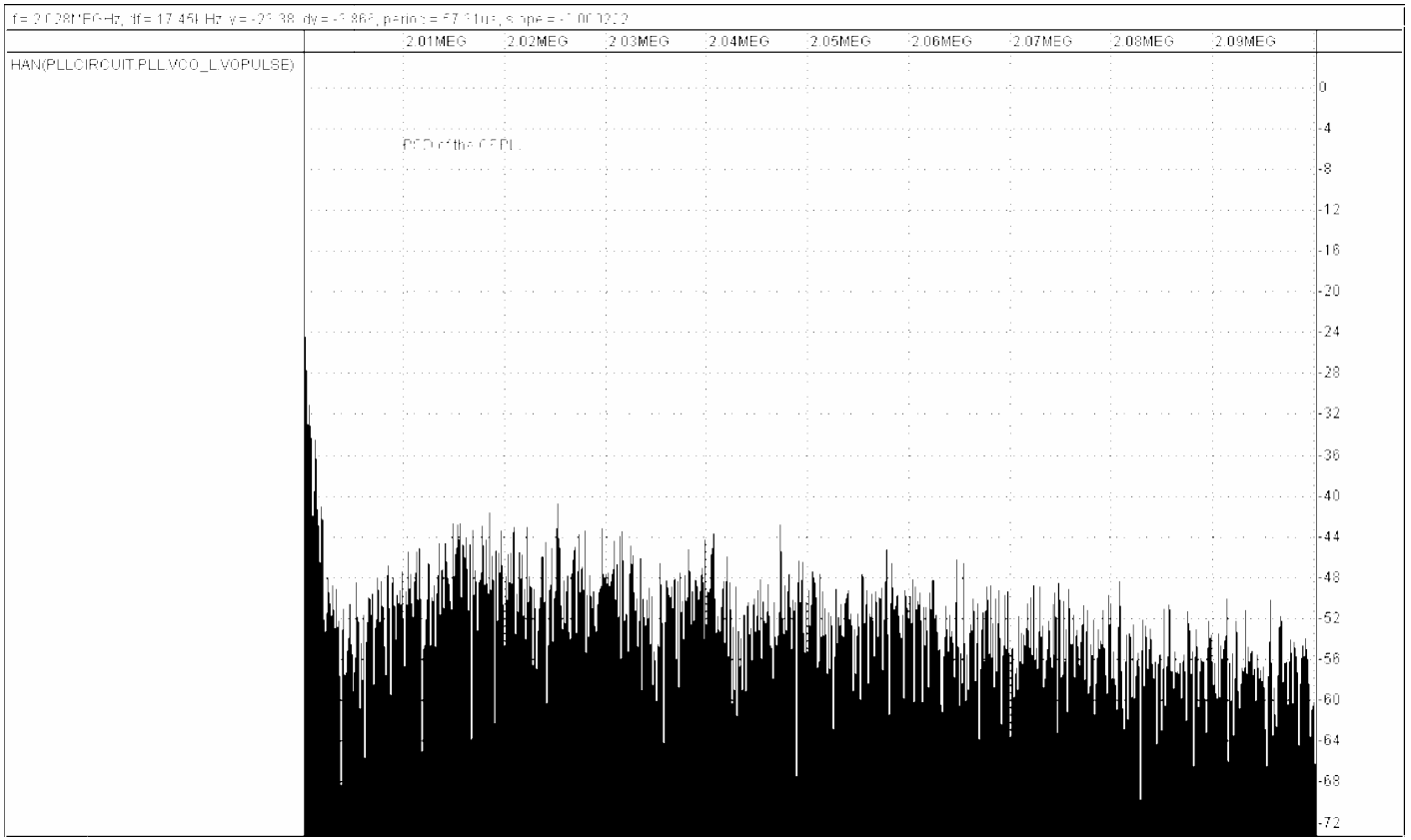

Figure 4.4. VHDL-AMS simulation output of CPPLL spectrum (SSB)

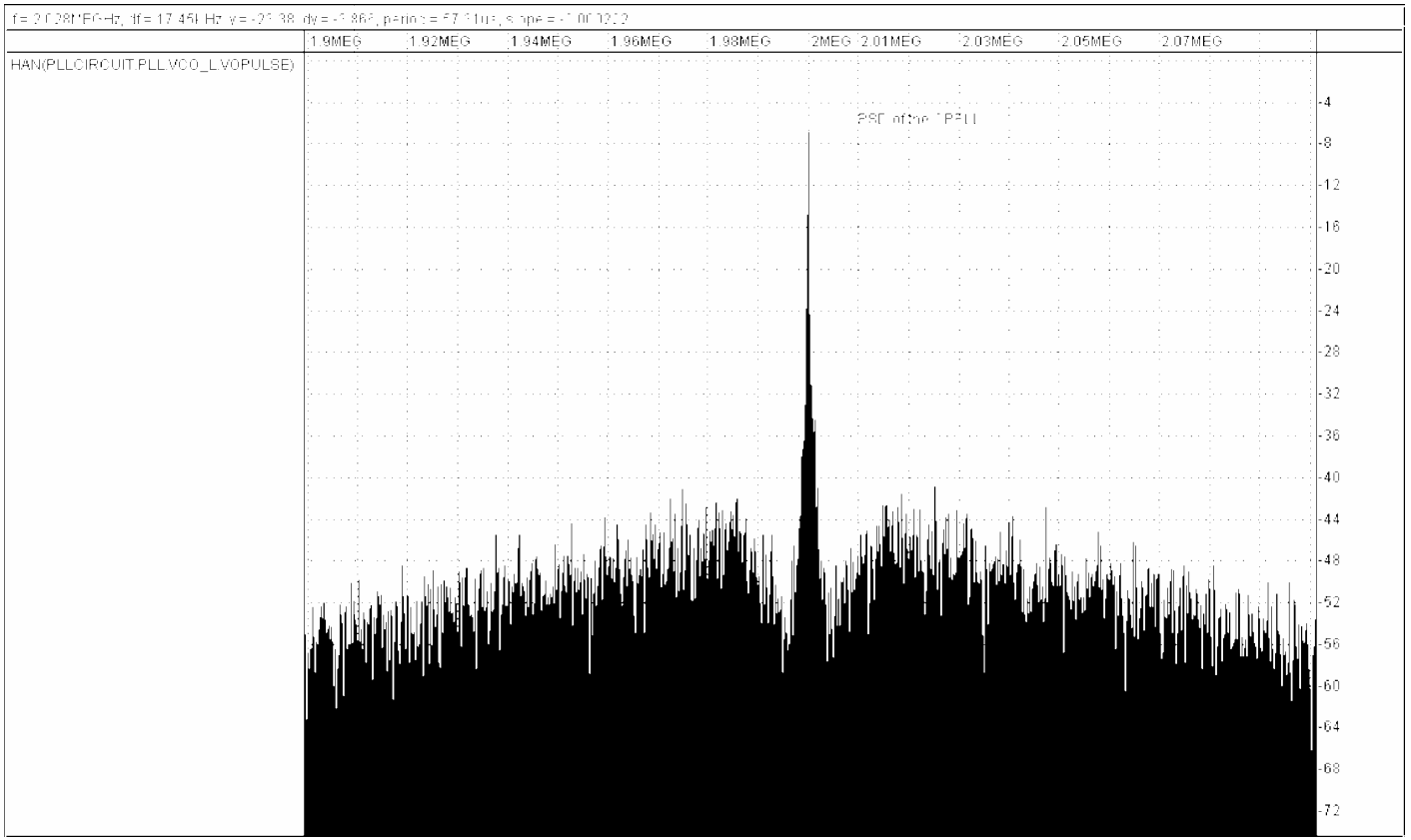

Figure 4.5. VHDL-AMS simulation output of CPPLL spectrum

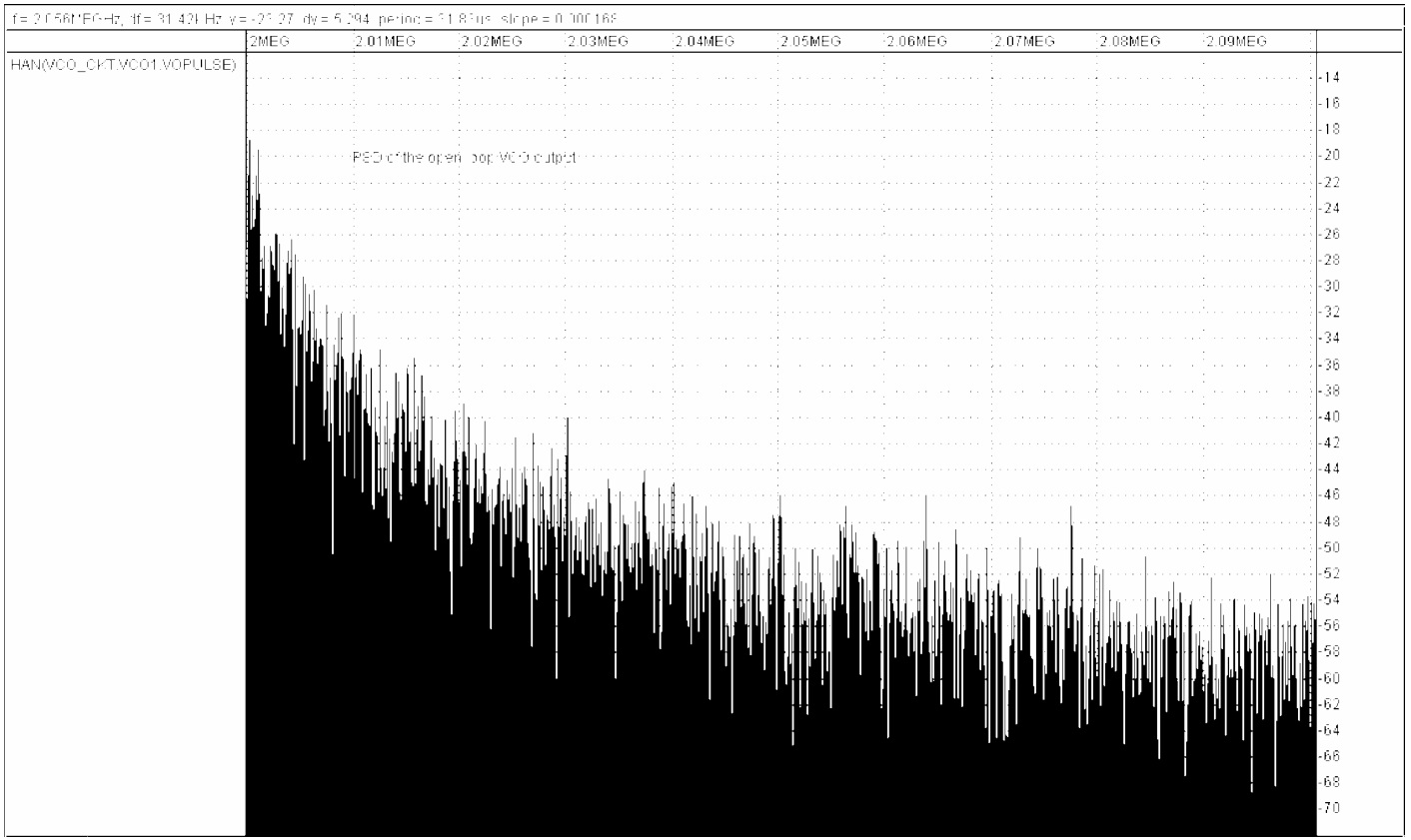

Figure 4.6. VHDL-AMS simulation output of open loop VCO spectrum (SSB)

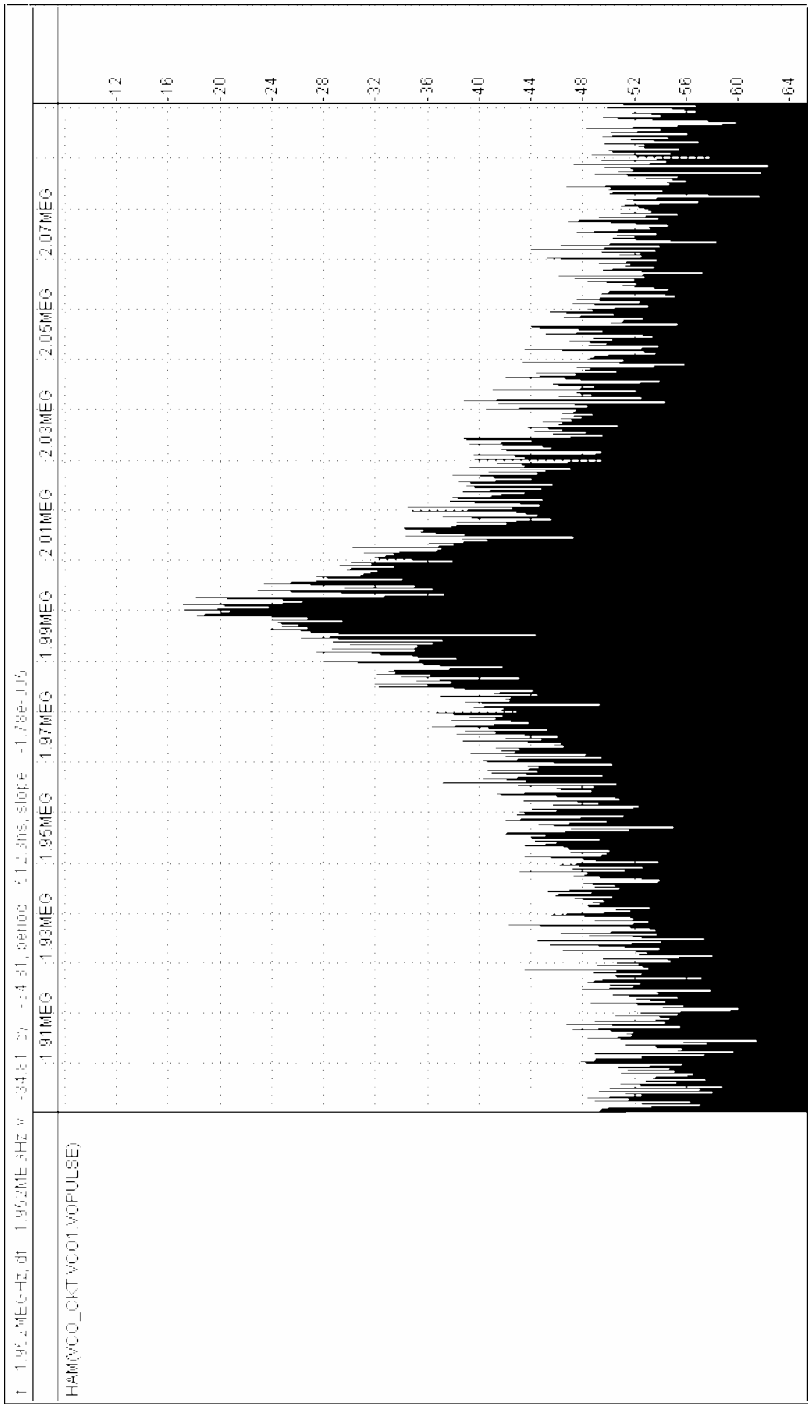

Figure 4.7. VHDL-AMS simulation output of open loop VCO spectrum

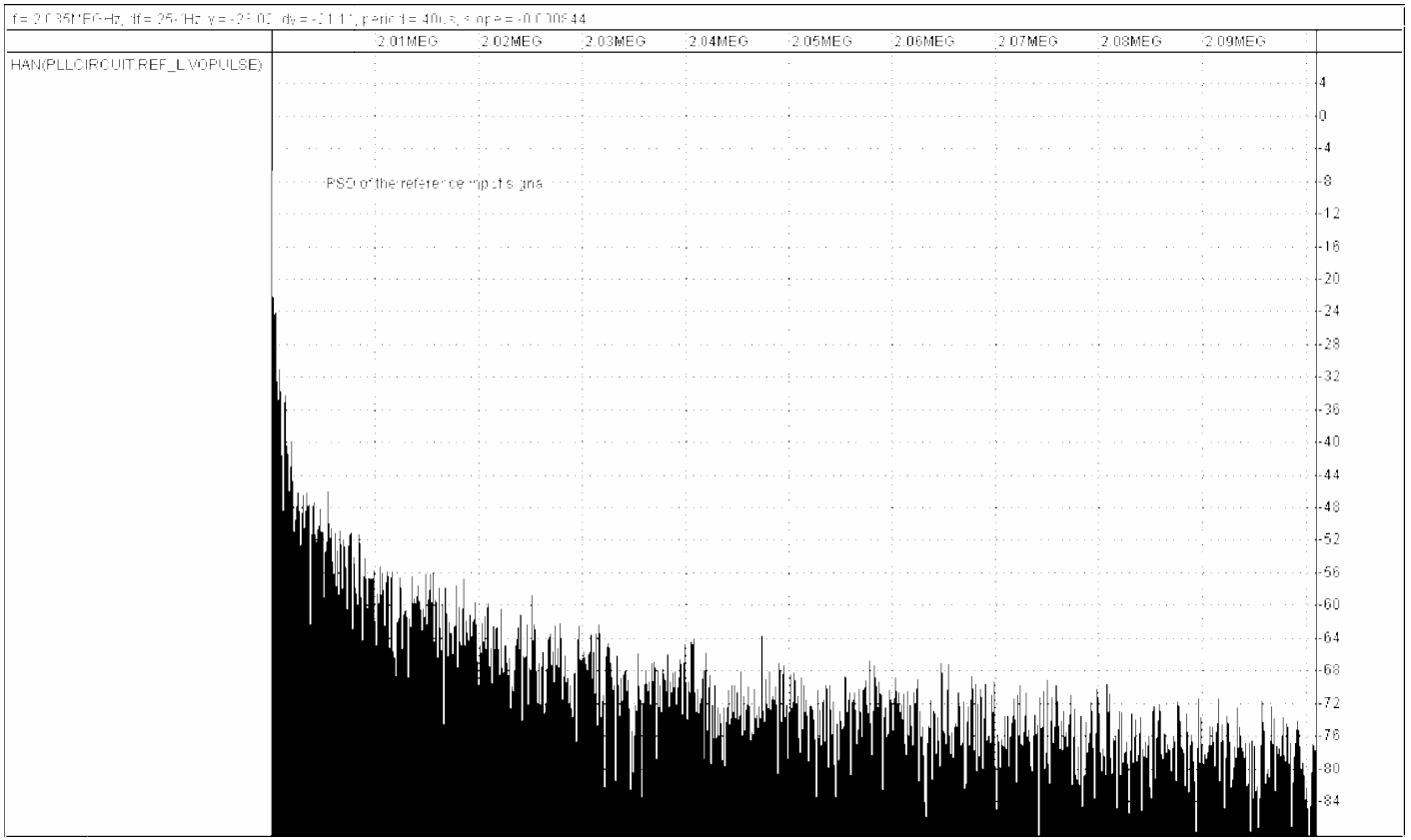

Figure 4.8. VHDL-AMS simulation output of reference input spectrum (SSB)

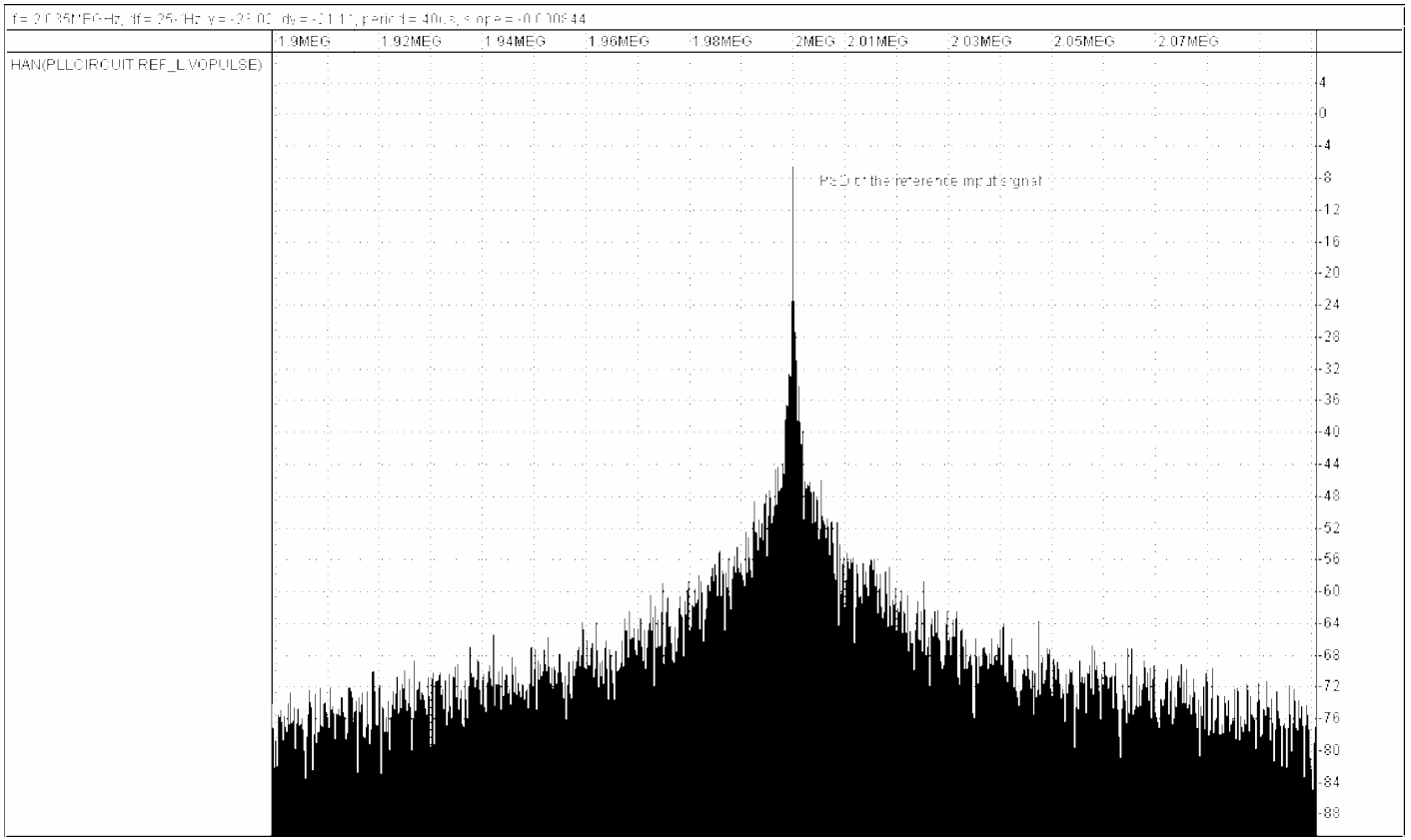

Figure 4.9. VHDL-AMS simulation output of reference input spectrum

5. CONCLUSIONS AND FUTURE WORK

Designing a low jitter clock synthesizer is not a trivial task. Multiple noise and disturbance sources combine together in the nonlinear blocks of the PLL affecting its performance. Moreover, deceptively small circuit nonideal characteristics can have nonnegligable effects in the behavior of the whole system. In this thesis, PLL noise analysis and modeling techniques are presented to develop an approach allowing the systematic design of PLLs. This approach allows the designer to maintain a grasp of the fundamentals using the coarse models at the early stage of the design and eventually to gain insight on the lower order effects by gradually increasing the level of detail as the design develops.

The noise analysis technique presented here only handles white noise sources. Future work can focus on the modeling of the other noise sources such as $1/f$, i.e. flicker noise, and other circuit noises such as phase detector and frequency divider noises. The effect of relaxing the assumptions stated in [11] can be investigated on the PLL noise performance. Gradual refinements of the model complexity and block parameters can lead to realistic design specifications for the actual circuits and provide accurate predictions of the overall system performance, which can lead to the design automation of PLLs.

APPENDIX A: THE COMPANION CD-ROM

Inside the back cover of this thesis, the companion CD-ROM is included. The companion CD-ROM contains the full text of this thesis in portable document format (PDF). All MATLAB and SMASH simulation files and output figures are stored in the subfolder corresponding to the section number.

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