DESIGN OF LOW NOISE CCII BASED CURRENT MODE CIRCUITS TO BE USED IN HIGH FREQUENCY APPLICATIONS

by

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ABSTRACT

DESIGN OF LOW NOISE CCII BASED CURRENT MODE CIRCUITS TO BE USED IN HIGH FREQUENCY APPLICATIONS

High performance analog circuits need to be modified according to modern telecommunication needs such as higher frequency (GHz regions), low power, low voltage, low noise and higher relative dynamic range. The attractive attributes of current mode approaches such as higher speed, greater linearity, larger bandwidth, etc., made them very popular in the design of high performance analog circuits. The second generation current conveyor (CCII) is the most widely used active element in high performance current mode design.

In this work, new high performance, low noise CMOS CCII circuit implementations are proposed. The first implementation, which is based on differential pairs, has high voltage swings on ports X and Y, very small equivalent impedance on port X, high equivalent impedances on ports Y and Z and also high-valued voltage and current transfer bandwidths. The second CCII implementation, which replaces the source follower transistors of the first implementation with super source follower ones, has very small equivalent impedance on port X, higher voltage and current transfer bandwidths compared to the first implementation. The final implementation is a self biased one which uses no additional biasing voltage or current sources other than the two supply rails. The proposed circuits are laid-out using Mentor Graphics IC Station Layout Editor and post layout simulations are performed with HSpice using AMS 0.35μm technology parameters. In addition, a common noise model of the proposed circuits is obtained which is composed of an input referred noise voltage source at high impedance port Y and an input referred noise current source at low impedance port X. The noise values are optimized by adjusting the g_m values of the transistors. Furthermore, the noise reduction techniques are tested on both current mode and voltage mode filter circuits. Considerable noise reductions are obtained especially for high order filter circuits.

ÖZET

YÜKSEK FREKANSLI UYGULAMALAR İÇİN DÜŞÜK GÜRÜLTÜLÜ CCII TABANLI AKIM MODLU DEVRELERİN TASARIMI

Modern telekomünikasyon gereksinimlerine bağlı olarak analog devrelerin daha yüksek frekans (GHz mertebesinde), düşük güç, düşük besleme gerilimi, düşük gürültü ve yüksek dinamik aralık elde edilecek şekilde yeniden tasarlanmaları gerekir. Akım modlu yaklaşımlar daha yüksek hız, daha geniş doğrusallık, daha büyük bant genişliği, vb., gibi çekici özellikleri yüzünden analog devre tasarımında tercih edilmektedir. İkinci kuşak akım taşıyıcı (CCII), akım modlu tasarımda en yaygın kullanılan aktif elemandır.

Bu çalışmada, yüksek başarımlı yeni CMOS CCII devre gerçekleştirmeleri önerilmiştir. Fark kuvvetlendiricisi tabanlı olan birinci gerçekleştirme, X ve Y düğümlerinde yüksek gerilim salınımları, X düğümünde çok düşük eşdeğer empedans, Y ve Z düğümlerinde yüksek eşdeğer empedans ve aynı zamanda yüksek değerli gerilim ve akım aktarım bant genişliklerine sahiptir. İlk gerçekleştirmedeki kaynak çıkışlı devrelerin yerine süper kaynak çıkışlı devreler kullanan ikinci gerçekleştirme, birinci gerçekleştirmeye nazaran, daha düşük X düğümü empedansı ve daha geniş gerilim ve akım aktarım bant genişliklerine sahiptir. Kendinden kutuplamalı olan üçüncü gerçekleştirme ise iki besleme hattından başka hiçbir gerilim veya akım kutuplama kaynağı kullanmamaktadır. Önerilen devrelerin, "Mentor Graphics IC Station Layout Editor" ile serimleri yapılmış ve serim sonrası benzetimleri HSpice ile AMS 0.35µm teknoloji parametreleri kullanılarak yapılmıştır. Ek olarak, önerilen devrelerin, yüksek empedanslı Y düğümünde girişe indirgenmiş gürültü gerilim kaynağı ve düşük empedanslı X düğümünde girişe indirgenmiş gürültü akım kaynağından oluşan ortak bir gürültü modeli elde edilmiştir. Transistörlerin g_m değerleri ayarlanarak gürültü değerlerinin en aza indirilmesi sağlanmıştır. Gürültü azaltma teknikleri hem akım kipli hem de gerilim kipli süzgeç

devrelerinde sınanmıştır. Özellikle yüksek dereceli süzgeç devrelerinin gürültü değerlerinde önemli derecede azalma elde edilmiştir.

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LIST OF SYMBOLS/ABBREVIATIONS

g_m	Transconductance of a MOS transistor
k	Boltzman constant
V_{DD}	Positive supply voltage
V_{SS}	Negative supply voltage
$V_{GS/DS}$	(Gate/drain)-to-source voltage of a MOS transistor
α	Current transfer ratio between ports X and Z
β	Voltage transfer ratio between ports Y and X
γ	Current transfer gain between ports X and Y
ASIC	Application specific integrated circuit
ADC	Analog-to-digital converter
AF	Frequency exponent
CAD	Computer aided design
CC	Current conveyor
CCI	First generation current conveyor
CCII	Second generation current conveyor
CCIII	Third generation current conveyor
CDBA	Current differencing buffered amplifier
CFOA	Current mode operational amplifier
CMOS	Complementary metal oxide semiconductor
DAC	Digital-to-analog converter
DOCC	Dual output current conveyor
DVCC	Differential voltage current conveyor
ECL	Emitter coupled logic
EF	Flicker exponent
EM	Saturation field
FDCC	Fully differential current conveyor
FTFN	Four-terminal floating nullor
IC	Integrated circuit

KF	Flicker noise parameter
MOS	Metal-oxide Semiconductor
NF	Noise figure
NMOS	N-type metal-oxide semiconductor
NOIA	Noise parameter A
NOIB	Noise parameter B
NOIC	Noise parameter C
NOIMOD	Noise model flag
OFCC	Operational floating current conveyor
OPAMP	Operational amplifier
OTRA	Operational transresistance amplifier
PDF	Probability density function
PMOS	P-type metal-oxide semiconductor
PSD	Power spectral density
SC	Switched-capacitor
SNR	Signal-to-noise ratio
UCC	Universal current conveyor
VLSI	Very Large Scale Integration

1. INTRODUCTION

The development of very large scale integrated (VLSI) technology has led to significant interest in analog integrated circuit (IC) design. The emergence of IC's incorporating mixed analog and digital functions on a single chip has given strong and decisive boost toward the design of low voltage, low power and high performance analog integrated circuits. Analog circuits are used in many VLSI systems some of which are data converters, amplifiers, filters, comparators and oscillators. The strategies for implementing new circuit designs especially for portable system applications are very important in low-cost CMOS technology.

Voltage mode circuits, as compared with current mode circuits, have received a much greater attention and found a much wider range of applications despite the fact that the concept of ideal current mode circuits, similar to that of ideal voltage mode circuits, emerged nearly few tens of years ago. Some reasons for such popularity of voltage mode circuits can be summarized as follows [1-5]: (i) The node voltages of electric networks can be measured very easily using voltmeters without disturbing the circuit topology and affecting the operation of the circuit. On the other hand, the measurement of the branch current is less convenient and often requires a change of the configuration of the circuit topology to connect the ammeter properly. (ii) In cascade configurations, the infinite impedance seen at the gate of MOS transistors makes them ideal choices for the realization of voltage-mode circuits, such as multistage amplifiers. (iii) The ease of having a high voltage gain in voltage mode circuits using techniques such as cascade and regulated cascade circuits. (iv) High supply voltages in the past were not of critical concern. (v) Switching noise was not a critical issue in the presence of a high supply voltage. (vi) Low speed requirements allow charging and discharging of node capacitances over a long period of time.

Traditionally, signal processing applications have been restricted to voltage mode operations only. As a result, the voltage mode op-amp has been the main analog block and has rapidly dominated the market since the advent of the first analog integrated circuits [1-3]. However in recent years, current mode signal processing techniques have been applied

to various kinds of electronic circuits. Rather than representing the signals by voltage mode quantities, the current mode technique includes current mode signals. Current mode signal processing can be defined as the processing of current signals where voltage signals are irrelevant in determining the performance of the circuit. This may be the case for circuits that are specifically designed to operate with low impedance nodes such that voltage swings and time constants are small [4]. By using amplifiers utilizing current mode techniques, performance in terms of supply voltage, bandwidth and slew-rate can be maximized. State-of-the-art current mode analog design can provide solutions to many circuit and system problems. Internal node impedances determine the signal range in current mode design and the signal range is not restricted by the supply voltages. Low-impedance internal nodes, higher slew-rate performance, minimized capacitive charging and discharging, increase the operation frequency range in current mode circuits. The need for low-voltage, low-power and high-frequency of operation is enormous in portable electronic equipments like laptop-computers, pace-makers, cellular phones, etc. Current mode circuits are suitable for low-voltage of operations and also they allow the design of the systems that can operate in higher frequencies with wider dynamic ranges. As a summary, the advantages of the current mode circuits are:

- Extended bandwidth
- Low-voltage and low-power operation
- Higher dynamic range
- Ease of arithmetic operations of signals
- Simpler circuit structure

Current mode approach includes variety of applications some of which are A/D and D/A converters, microwave and optical system applications, neural networks, continuous-time filters, sampled-data filters, disk drive read-channel ICs, current mode logic circuits, etc. Some of the current mode active devices are current conveyors (CC), current mode operational amplifiers (COA), four-terminal floating nullor (FTFN), current differencing buffered amplifiers (CDBA), current-feedback amplifiers (CFA), etc. Among these, the

most widely used active device is the current conveyor, especially the second generation current conveyor, abbreviated as CCII, due to its improved characteristics [5].

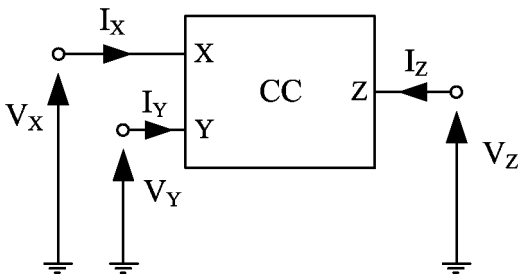

Figure 1.1. Block diagram of a CC

1.1. The Current Conveyor

A CC is a three (or more) port device which can perform many useful analog signal processing functions when arranged with other active and passive electronic circuit elements. In many ways the CC simplifies circuit design in much the same way as the conventional op-amp. This stems largely from the fact that the CC offers an alternative way of abstracting complex circuit functions, thus aiding in the creation of new and useful implementations [1]. Current conveyors allow the design of circuits operating in the current, voltage or hybrid mode. These building blocks have found many application areas such as continuous and discrete time filters, instrumentation amplifiers, non-linear circuits, current mode logic circuits, data converters, neural networks, etc. The block representation of current conveyor circuit is shown in Figure 1.1. It is made up of two follower stages:

- A current follower stage between ports X and Z
- A voltage follower stage between ports Y and X

Mathematically, the port relations of a CC can be described by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & A & 0 \\ B & 0 & 0 \\ 0 & \pm C & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{1.1}$$

where A, B and C assume a value 1, 0 or -1 depending on the type of the CC.

1.2. Classification of Current Conveyors

Current conveyor topologies can be classified depending on the characteristics of its X, Y and Z ports [5]. Similar to power amplifiers, they can also be classified based on the quiescent current flow.

1.2.1. Classification Based on the X Port

When used as voltage buffer, the voltage signal applied to high-impedance input port Y is copied to low-impedance output port X. If the voltage copied to X port has same polarity with Y port (B=1) the current conveyor is called non-inverting type and $V_X = V_Y$. If the output voltage is copied to X port with opposite polarity (B=-1), the CC is called inverting type and $V_X = -V_Y$.

1.2.2. Classification Based on the Y Port

The type of the current conveyor is determined by port Y. If the current flowing on this port is equal to the current injected at port X with same polarity (A=1), the CC is called first generation CC (CCI). If no current flows through Y port (A=0), the CC is called the second generation CC (CCII). If the current of Y port is equal to the current injected at X port with opposite polarity (A=-1), then it is the third generation CC (CCIII). The most widely used CC is the second generation one.

1.2.3. Classification Based on the Z Port

High-impedance Z port is the current output port of the CC. The direction of the current on Z port determines whether the CC is a positive or negative type. If the current

on Z port has the same polarity as the current injected at the X port then the CC is called positive type CC (CC+) and if the current has an opposite polarity then the CC is called negative type CC (CC-). If the CC has multiple output current port Z (both positive and negative) then the CC is called composite port CC [5].

1.2.4. Classification Based on the Quiescent Current

Current conveyors are classified according to their circuit configurations and methods of operation into different classes such as Class A, Class AB and Class B. In Class A CC, the device is on at all times and it is constantly carrying current, which represents a continuous loss of power. However, the Class B CC operates ideally with zero quiescent current, so that the dc power is small. Compared to Class A mode operation, the bandwidth is smaller. Class AB CC is the best alternative with small quiescent current, higher bandwidth and small dc power consumption.

1.2.5. Other Types of Current Conveyors

Other types of CC configurations are fully differential CC (FDCC), universal CC (UCC), differential voltage CC (DVCC), differential difference CC (DDCC), dual output CC (DOCC), operational floating CC (OFCC), etc.

1.3. Design with the CCII

Second generation current conveyor (CCII) is the most popular current mode circuit structure among all CCs and can be used in almost all analog circuit operations. Since its first presentation in 1970, many authors have proved its versatility and flexibility in analog circuit design for both linear and non-linear applications. In this work, among other CC structures, only the CCII circuit structure is used because of its popularity, versatility and flexibility [9,10].

1.3.1. The Ideal CCII

Basically, the CCII is a three terminal active device with the port relations as:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta & 0 & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1.2)$$

Ideally β =1 and α=1 and they represent the voltage and current transfer ratios of the conveyor, respectively. The sign of α, + or -, denotes positive type (CCII+) or negative type (CCII-) CCII, respectively. Port Y has ideally infinite impedance, so there is no current flowing through it. The voltage applied to Y port is copied to the low impedance port X and the current injected to port X is copied to the high impedance port Z. So, the CCII is composed of two followers:

- A voltage follower between ports Y and X
- A current follower between ports X and Z

1.3.2. The Real CCII

The ideal conveyor, defined by the matrix equation above, allows only a rough analysis of a circuit implemented with CCIIs. Thus, when an electronic function will have to be determined and notably its performance at frequencies above the MHz range, it will be necessary to consider a simplified relatively accurated non-ideal model for the CCII. This model will have to include the different parasitic impedances of the circuit as well as the possible variations, according to the frequency, of the voltage and current transfers. Some of the high performance parameters of the CCII can be listed as: wide voltage and current input ranges, high accuracy in voltage and current transfers, wide voltage and current transfer bandwidths, low input impedance at port X and also high output impedances at ports Y and Z. Fig. 1.2 shows the complete equivalent model of the CCII which takes into account the non-ideal characteristics at ports X, Y and Z, the capacitive parasitic impedances on ports Y and Z and also non-ideal voltage and current transfer parameters β and α. When high-frequency electronic functions have to be implemented with a CCII, accurate macro models on a large frequency range are needed to explain the limitations. (G_y+sC_y) constitutes the input admittance on port Y when output X of the voltage follower is left open. The controlled voltage source βV_y copies the voltage of port

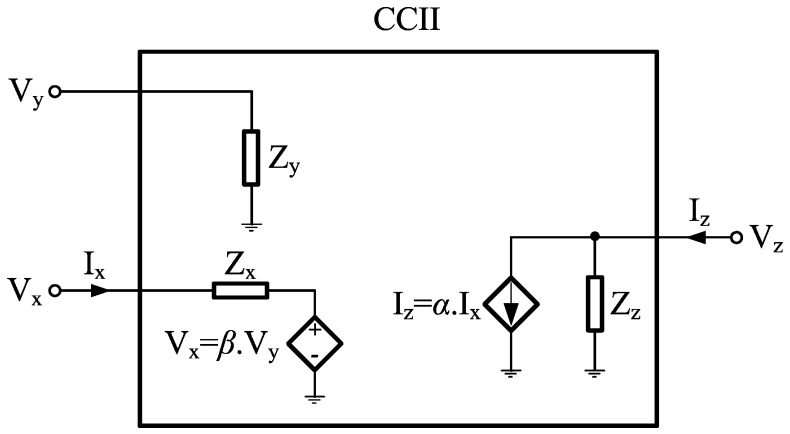

Figure 1.2. CCII+ equivalent model

Y to port X. R_x is the equivalent resistance seen on port X measured at low frequencies. (G_z+sC_z) is the output admittance on port Z [11,12].

1.4. High Frequency Continuous-Time Filters

High-frequency, high-precision, high-order filters have found many application areas in communications including AM and FM IF filtering, video processing, data communications and local area networks. Voltage mode filters have previously been successfully applied to high-frequency applications both by utilizing the two well-known techniques: switched-capacitor (SC) and the continuous-time filtering. One of the main disadvantages in high frequency SC filter design is that, in order to preserve a high unity-gain frequency, the G_m of an op-amp has to be as large as possible which results in large power dissipation. Another disadvantage is that, high transconductance requirement increases the input capacitance of the op-amp. The most important disadvantage of continuous-time filters is that, due to the dependence of the center-frequency of the filter on the absolute value of passive components, such as capacitors and resistors, some extra circuitry is required to control the center frequency [6,7].

With the trend toward mixed-analog/digital ICs fabricated using low-voltage digital CMOS technologies; it is becoming more difficult to design high-frequency, high-linearity and wide-dynamic-range voltage-mode analog circuits. Current-domain signal processing

is potentially faster because of the comparably low node impedances. This principle forms the guideline of many current-mode analog circuits some of which are:

- Current-steering DAC's
- Current conveyors
- Bipolar emitter coupled logic (ECL) gates
- High speed current-mode amplifiers

Thus, using digital CMOS technologies, current mode signal processing is viable for applications near the MOSFET transition frequency [8].

1.5. High Frequency Limitations in CCII

Fig. 1.2 illuminates the equivalent circuit that can be used to embody the behavior of the non-ideal CCIIs. The voltage and current transfer ratios, β(s) and α(s), will generally be described by the following first order functions:

$$\beta(s) = \frac{\beta_0}{1 + s/\omega_\beta} \tag{1.3}$$

$$\alpha(s) = \frac{\alpha_0}{1 + s/\omega_\alpha} \tag{1.4}$$

β_0 and α_0 are the values of these transfer functions at low frequencies (close to unity), ω_β and ω_α represent corresponding poles. The input impedances for the ideal CCII are respectively infinite on port Y and zero on port X, respectively. The current output port Z exhibits high equivalent impedance. The circuit in Fig. 1.2 allows us to determine the matrix equation in order to describe correctly the real (or non-ideal) CCII. It finally becomes:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} G_y + sC_y & 0 & 0 \\ \beta(s) & R_x & 0 \\ 0 & \pm\alpha(s) & G_z + sC_z \end{bmatrix} \times \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{1.5}$$

It is clearly seen from the matrix equation that the parasitic impedances of the conveyor tend to modify the true actual behavior of the transfer function and causes deviation from the expected behavior.

1.6. High Order Active Filters

Often the simple two-pole (quadratic) active filter designs do not meet the signal conditioning requirements. In these cases, quadratic filters may be cascaded to form high order filters having four or more poles. Such high order filters are described according to how they perform in time and frequency domains. Commonly used high order active filters are Butterworth, Chebyshev, Elliptic or Cauer and Bessel or Thompson filters [32].

The Butterworth filter is designed to have a frequency response which is flat (has no ripples) in the pass-band. Another name for a Butterworth filter is maximally flat magnitude filter. Compared with a Chebyshev or Elliptic filter, the Butterworth filter has a slower roll-off and thus requires a higher order to implement a particular stopband specification. However, Butterworth filters have a more linear phase response in the pass-band than the Chebyshev and Elliptic filters. There is considerable output overshoot in the time domain response of this kind of filters of order greater than n=4 to transient inputs.

In the frequency domain, the Chebyshev filter has more pass-band ripple (type I) or stop-band ripple (type II) than Butterworth filters. Generally, a Chebyshev low-pass filter having the same attenuation slope in the stop-band as a comparable Butterworth low-pass filter requires fewer poles.

An elliptic filter (or a Cauer filter) is a signal processing filter with equalized ripple behavior in both the pass-band and the stop-band. The amount of ripple in each band is independently adjustable, and no other filter of equal order can have a faster transition in gain between the pass band and the stop band, for the given values of ripple. High-order elliptic filters have oscillatory transient responses.

A Bessel filter is a type of linear filter with a maximally flat group delay (maximally linear phase response). Bessel filters are often used in audio systems. Analog Bessel filters

are characterized by almost constant group delay across the entire pass band, thus preserving the wave shape of filtered signals in the pass band. For any order, Bessel filters make good low-pass filters where faithful time domain signal reproduction is required [13].

1.7. Scope of the Thesis

This thesis has two main objectives. The first one is to design high performance differential-pair based CMOS CCII circuits to be used in high-order, high-frequency filter applications. The second aim is to obtain the analytical noise model which will be used to reduce the input referred noise values of the proposed CMOS CCII circuits. As a result, based on these noise reduction techniques, the output signal-to-noise ratio of CCII based filter applications will be maximized.

Initially, three high-performance, differential-pair based CMOS CCII implementations are proposed and compared with the circuits proposed previously in terms of voltage and current follower bandwidths, port X parasitic impedance and voltage swings on ports Y and X. The first CCII implementation is based on differential-pair based voltage follower stage and current mirror based current follower stage. The proposed circuit has high voltage and current transfer bandwidths, high voltage swings on ports X and Y, very low equivalent resistance on port X and high resistances on ports Y and Z for a wide frequency range. As for the second circuit, some additional feedback techniques are applied to the source follower transistors of the first circuit to reduce the equivalent resistance on X port and very good reduction is obtained. The third one is a self biased CMOS CCII implementation which does not use any voltage or current biasing sources other than the two supply rails. A start-up circuit is designed to guarantee the current flow in differential pairs when the supply is turned on.

Next, noise analysis of the proposed circuits is performed. Input referred noise voltage at high impedance port Y and input referred noise current at low impedance port X are obtained to form the noise model of the CCII. Using the analytical noise equations, which are formed by the well known quantities and the g_m values of the transistors, some techniques are recommended in order to reduce the noise values.

Finally, high order Butterworth and Chebyshev type filter circuits are designed. The validity of the proposed noise reduction techniques are tested on these filter applications. Considerable noise reductions are obtained and verified with HSpice simulations.

2. BACKGROUND

Since their introduction in 1970, the CCIIs have been exploited in a huge number of applications in multifarious designs for analog electronics, like amplifiers, filters, oscillators, A/D and D/A converters or more generally signal processing circuits. Several configurations have been introduced to implement current conveyors. The most important difference between the CCIIs is the implementation of the voltage follower stage. The properties of two commonly used current conveyor implementations (translinear loop based and differential pair based) are discussed in this section.

2.1. Class AB (Translinear-Loop Based) CCII

The translinear loop based configuration seems to be the most suitable configuration for a higher degree of control of the design characteristics [14-16]. Since their introduction, they have demonstrated recuperated high frequency performances. When the input stage (voltage follower) of the conveyor is implemented using mixed translinear-loop composed of complementary transistors, the conveyor will have high bandwidth voltage transfer gain

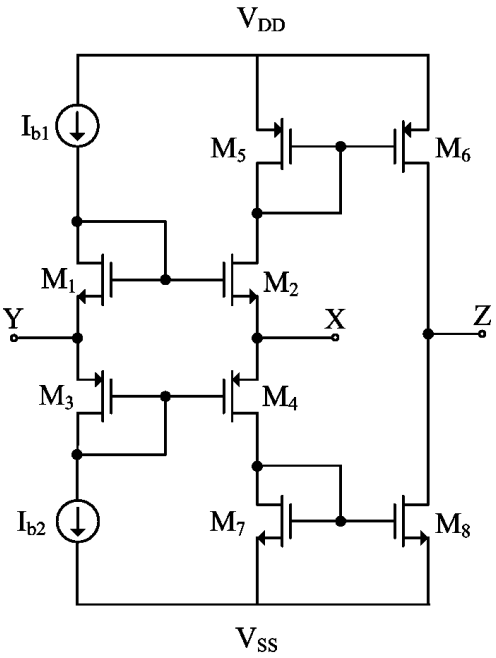

Figure 2.1. Class AB CCII

from Y port to X port. The translinear-loop based CMOS CCII circuit is shown in Fig. 2.1 [14].

Assuming transistors with equal bulk-source voltages, transistors M_1-M_4 provide a translinear loop which accurately reflects the DC voltage of Y port on X port. In fact, process tolerances do not appreciably modify the operating point. The parasitic impedance on port X has a non-negligible value which leads to conversion errors when a load resistance or capacitance is connected to this port. The resistance seen from this port is approximately:

$$R_X \cong \frac{1}{g_{m2} + g_{m4}} \tag{2.1}$$

To achieve low impedance on port X, large aspect ratios or high biasing currents must be used for transistors M_2 and M_4. The equivalent resistance seen at port Z is typically high and can be given by:

$$R_Z \cong \frac{r_{o6}.r_{o8}}{r_{o6} + r_{o8}} \tag{2.2}$$

If the current sources, I_{b1} and I_{b2}, have equal values, the circuit exhibits high input impedance on Y port. For this condition, the equivalent impedance is the parallel combination of the output impedances of these two current sources.

The circuit provides class AB operation and has a simple implementation and standard single-well process is sufficient. Besides the high equivalent impedance at X port, another disadvantage of the circuit is the signal swing on this port. As it can be seen from the circuit, the voltage swing on port X has a limited value which can be calculated as:

$$V_{SS} + \left|V_{DSb2}\right| + \left|V_{GS4}\right| \le V_X \le V_{DD} - \left|V_{DSb1}\right| - V_{GS2} \tag{2.3}$$

where V_{DSb1} and V_{DSb2} stands for the V_{DS} voltages of the current sources I_{b1} and I_{b2}, respectively.

2.2. Improved Class AB CCII

In [15], an improved translinear loop based CCII circuit is proposed. The authors deal with optimizing second generation current conveyors. In order to reduce its equivalent resistance at X port, an improved topology is considered. In this configuration, an additional feedback is applied to source follower transistors, M_2 and M_4, and as a result very low impedance on port X is obtained. In that way, the proposed circuit can be used in higher frequency applications. The improved class AB CCII circuit is shown in Fig. 2.2.

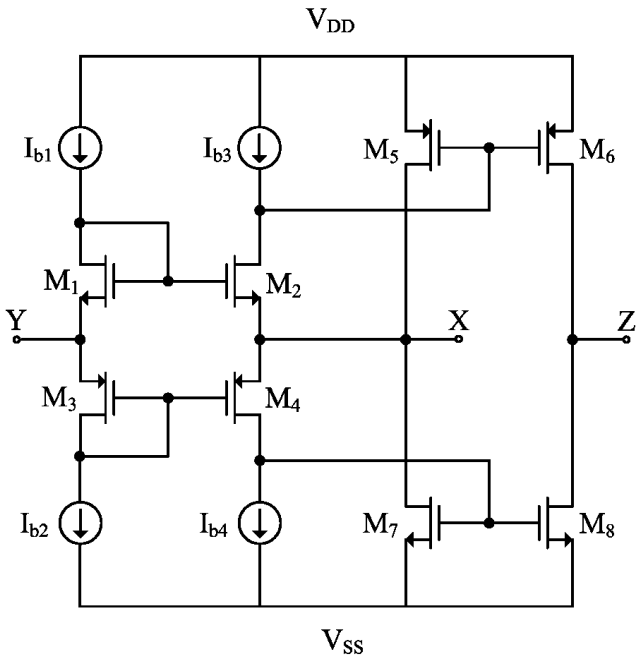

Figure 2.2. Improved class AB CCII

With the improved configuration, the equivalent resistance seen at port X is reduced to:

$$R_X \cong \frac{1}{g_{m5}\left(1+g_{m2}.r_{o2}\right)} \left\| \frac{1}{g_{m7}\left(1+g_{m4}.r_{o4}\right)} \right. \tag{2.4}$$

When compared to the parasitic impedance of the basic translinear loop based CCII, a very good reduction of the port X impedance is obtained. This parasitic impedance is decreased by at least a factor of ten compared to the basic class AB CCII. However, the

voltage swing on this port doesn't change and it also has a limited value as described in (2.3).

2.3. Differential Pair Based CCII

Another important classification category of the CCII circuits is based on differential pair based realizations. In the literature, a large number of current conveyors employing a differential-pair have been proposed [17-22]. The basic topology which operates in class A is shown in Fig. 2.3.

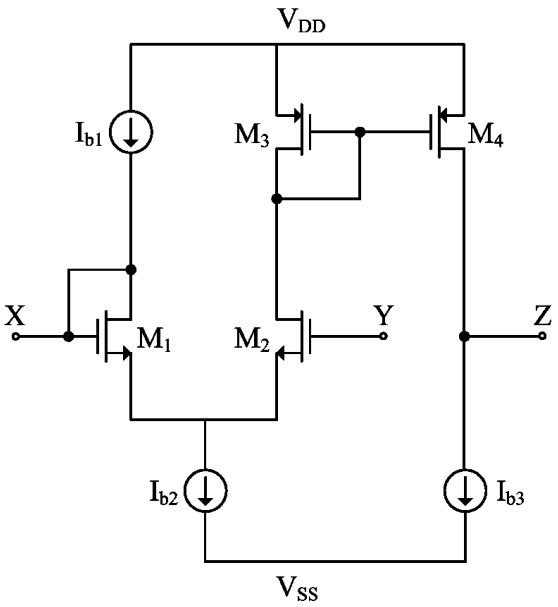

Figure 2.3. Differential pair based CCII in [3]

Low impedance at X port is obtained by the feedback connection. The differential pair M_1 and M_2 form the voltage follower from port Y to port X. If transistors with large output resistances are used, the voltage transfer ratio, β, will be closer to unity. For this circuit it is equal to:

$$\beta = \frac{V_X}{V_Y} = \frac{r_{o2}.g_{m2}}{1+r_{o1}.g_{m1}} \cong \frac{g_{m2}}{g_{m1}} \tag{2.5}$$

The equivalent impedance at X port is low and it is inversely proportional to the input transistor g_m. The value of R_X is equal to:

$$R_X \cong \frac{g_{m1} + g_{m2}}{g_{m1}.g_{m2}} \tag{2.6}$$

The input impedance of Y port is formed by the gate of transistor M_2 which is quite large. Its value can be evaluated knowing the sizes of this transistor. The value of the parasitic resistance seen on port Z is equal to:

$$Z_Z \cong \frac{r_{o4}.R_{Ib3}}{r_{o4} + R_{Ib3}} \tag{2.7}$$

A different, differential-pair based CMOS CCII circuit is shown in Fig. 2.4. This circuit shows improved characteristics at lower supply voltages.

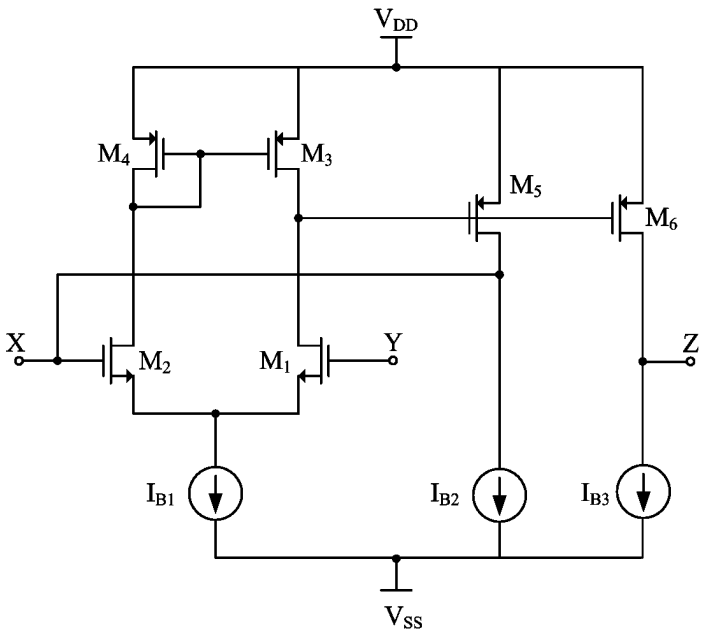

Figure 2.4. Differential pair based CCII in [2]

The output voltage at X port is taken from the drain of M_5. This voltage is directly connected to X port to implement the feedback which guarantees low impedance at X port. The β parameter, which is very similar to the previous circuit, is equal to:

$$\beta = \frac{V_X}{V_Y} \cong \frac{g_{m1}}{g_{m2}} \tag{2.8}$$

The current transfer ratio, α, depends on the load impedances connected to X and Z ports. If the output impedances of transistors M_5 and M_6 are notably greater than the load impedances, then the α parameter can be calculated as:

$$\alpha = \frac{I_Z}{I_X} \cong \frac{g_{m6}}{g_{m5}} \tag{2.9}$$

The equivalent resistance seen at X port has a resistive contribution given by:

$$R_X \cong \frac{2}{g_{m2}.g_{m5}.r_O} \tag{2.10}$$

When compared to Fig. 2.3, a considerable reduction is obtained at X port equivalent impedance. The equivalent resistance on Z port is typically high and it can be given as:

$$R_Z \cong \frac{r_{o6}.R_{Ib3}}{r_{o6} + R_{Ib3}} \tag{2.11}$$

The circuit in Fig. 2.3 can be easily modified in order to obtain a class AB current conveyor. This can be done replacing the two biasing sources with two NMOS transistors, as in the circuit in Fig. 2.5. With respect to the class A CCII, the topology reported in Fig. 2.19 shows that port X and Z currents can flow both out and into the CCII itself. Moreover, the limitation on the dynamic range is overcome. The voltage transfer gain, β, is only due to the mismatch between the input transistors M_1 and M_2 and it can be given by:

$$\beta = \frac{V_X}{V_Y} \cong \frac{g_{m2}}{g_{m1}} \tag{2.12}$$

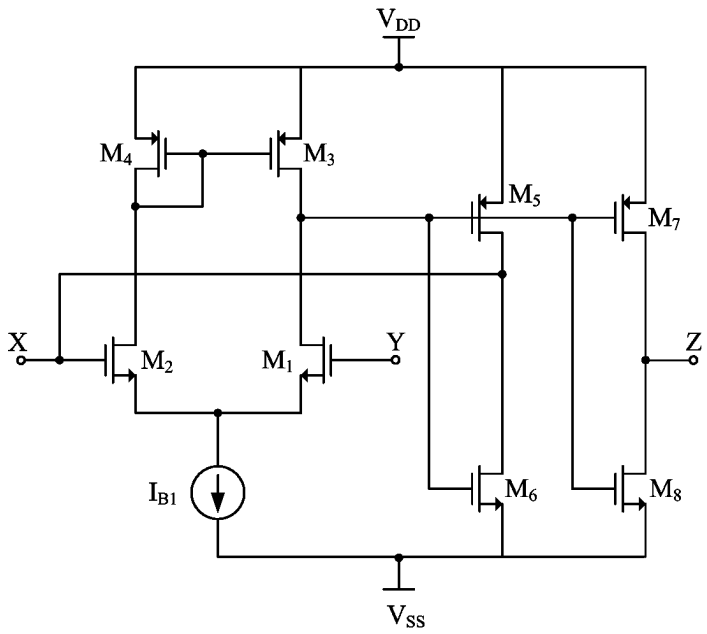

Figure 2.5. Differential pair based CCII in [34]

The load resistances connected at ports X and Z affect the current transfer bandwidth. If the load resistances are not very high when compared to the MOS output resistance, α can be given as:

$$\alpha = \frac{I_Z}{I_X} \cong \frac{g_{m7} + g_{m8}}{g_{m5} + g_{m6}} \tag{2.13}$$

Similar to (2.10), the equivalent resistance on X port can be calculated as:

$$R_X \cong \frac{2}{g_{m2} r_o \left(g_{m5} + g_{m6}\right)} \tag{2.14}$$

While the Z port output resistance is ensured to be high because it is given by the parallel combination of two transistor output resistances:

$$R_Z \cong \frac{r_{o7} . r_{o8}}{r_{o7} + r_{o8}} \tag{2.15}$$

There are many other studies concerning differential pair based CCIIs, both class A and class AB, in the literature [17-22]. The main objective of these studies is to design CMOS CCIIs with low parasitic impedance on port X, high equivalent impedances on ports Y and Z, high signal swings, especially high voltage swing on port X and also large voltage and current transfer bandwidths with transfer gains close to unity.

In [17], the proposed CCII includes two transconductance amplifiers with differential inputs. The first is implemented by the long-tail pair and the second is implemented by a single transistor. The voltage following action is the result of the negative feedback closed-loop structure. In this manner, both accuracy in the voltage transfer gain and low resistance at port X are achieved for high open loop gains. The circuit suffers limited voltage swing at port X.

A simplified CMOS realization of the differential-pair based CCII is proposed in [18]. The circuit includes three main blocks: a transconductance amplifier with a differential input and two matched inverting transconductance output stages connected in parallel. The proposed circuit uses an offset cancellation technique which which can only be achieved at I_X=0A otherwise the circuit exhibits larger offset, which is a critical disadvantage.

The CMOS CCII realization proposed in [19] consists of two differential pairs. Two matched differential input transconductance amplifiers, which are implemented by long tail pairs, are used. The implementation of the circuit is based on first generation current conveyor. An excellent current following action can be seen over the wide current range. The proposed circuit is also an excellent current follower that can widely be used in current-mode signal processing.

A CMOS current conveyor suitable for high-precision analog signal processing is presented in [20]. Based on the application of local negative feedback to reduce the voltage variations of the nodes affecting voltage transfer accuracy, high precision in voltage tracking and very low small signal resistance of the port X can be obtained simultaneously. Additionally, high precision in current transfer can be easily achieved by using high swing cascode current mirrors. Compared to the previous circuits, Yodprasit CCII exhibits the

highest accuracy in voltage following regarding the transfer gain and offset and the lowest input resistance. However, the circuit features the lowest input voltage range and the lowest voltage and current transfer bandwidths [23].

A novel, compact configuration of a CMOS current conveyor has been described in [21]. It is a versatile design which may also be used as an operational floating conveyor in various applications, because an additional output may be easily included using current mirrors. The circuit exhibits improved precision performance characteristics both in the DC and AC domains. Compared to Yodprasit CCII [20], the circuit has larger voltage offset, and higher input resistance at the X port. However, the circuit features higher input voltage and current ranges as well as lower current offset.

The proposed circuit in [22] has rail to rail swing capability with high linearity. The circuit requires no compensating capacitors and it has high bandwidths which are independent of the gain. The operation of the given circuit is insensitive to the threshold voltage variation resulting from the body effect. The circuit is considered to be the rail to rail version of Liu CCII [18]. The same offset cancellation technique applied for Liu CCII is used here. However, unfortunately, the some disadvantages that appear in Liu CCII reappear here. Firstly, the voltage offset cancellation is dependent on the input current. The circuit is designed to cancel the offset at zero input current only. Also, to achieve offset cancellation at zero input current a constraint equation should be satisfied as pointed in the paper. According to the reported realization, this equation is hardly achieved with a high level of precision which is another disadvantage. The circuit supports the rail to rail operation. It shows the largest input voltage range known so far. Compared to Liu CCII, the circuit provides higher input voltage range and higher voltage and current transfer bandwidths while keeping all other parameters in the same range.

The differential-pair based circuits which are designed during this work are compared with the circuits from the literature in terms of voltage and current transfer bandwidths, port X resistances and voltage swings of ports Y and X.

3. THE PROPOSED DIFFERENTIAL PAIR BASED CMOS CURRENT CONVEYOR CIRCUITS

In this chapter, high performance differential-pair based CMOS CCII circuits suitable for high frequency applications are introduced. They provide accurate voltage and current trackings as well as low equivalent impedances on port X. The proposed circuits use complementary differential pairs to realize the voltage follower stage. This solution allows high voltage swings on ports Y and X. The current follower stage is based on simple current mirror pairs.

3.1. Differential Pair Based CMOS CCII

The structure of this newly proposed circuit contains two follower stages: a differential pair based voltage follower with large voltage swings on X and Y ports and a current follower which is based on two simple current mirror pairs. The operational description of the proposed CCII circuit is given in detail by describing the voltage and current follower stages individually.

3.1.1. Voltage Follower Stage

The voltage follower stage of the proposed CMOS CCII circuit is shown in Fig. 3.1. Assuming that all the transistors operate in saturation region and all the transistor pairs are matched, the operation of the voltage follower stage can be explained as follows. Transistors M_7 and M_{10} conduct when the input voltage is positive, while transistors M_8 and M_9 conduct when the input voltage is negative. Current mirrors formed by M_2, M_3 and M_{16}, M_{17} force equal currents in the transistors M_7-M_{10} which function as source coupled pairs. This operation drives the gate-to-source voltages $v_{gs7}=v_{gs10}$ and $v_{gs8}=v_{gs9}$ and, as a result, forces the voltage at port X to follow the voltage at port Y. Transistors M_{11} and M_{12} are connected to form source followers in order to reduce the equivalent impedance on port X. The ideal voltage follower circuit has infinite input impedance, zero output impedance, unity voltage gain and also rail to rail voltage swings at input and output ports. With the assumptions that all the transistors are perfectly matched and each transistor operates in

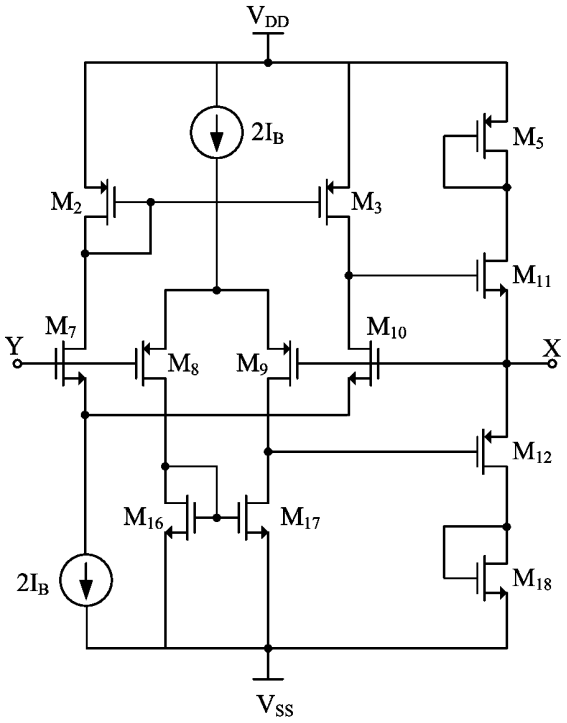

Figure 3.1. Voltage follower stage

saturation region, the proposed voltage follower circuit has very high input impedance at port Y, very low output impedance at port X, voltage transfer gain which is very close to unity and also high voltage swings (very close to supply rails) at ports X and Y. However, in a practical realization, several non-idealities that force deviation from the ideal performance are presented. The major factors that must be considered here are due to a finite value of transistor g_m and transistor mismatch. M_5 and M_{18} are mirror transistors to copy the current flowing through X port to Z port.

The β parameter of the voltage follower stage can be easily derived and it is equal to:

$$\beta = \frac{v_X}{v_Y} \cong \frac{g_{m7,8}}{g_{m9,10}} \tag{3.1}$$

Transistors with large output resistances are required to obtain a β value dependent only on the input pair transconductance ratios. The β parameter is given by the transconductance ratios of the input transistors, so it is very close to the ideal unitary value. If we consider the differential pair having the same small signal parameters (equal r_o's), the equivalent resistance seen on port X can be calculated as follows:

$$R_x = \frac{1}{g_{m11}(1+g_{m10}r_o/2)} \Big\| \frac{1}{g_{m12}(1+g_{m9}r_o/2)} \tag{3.2}$$

3.1.2. Current Follower Stage

The current follower stage of the proposed CMOS CCII circuit is shown in Fig. 3.2. The current mirrors M_5-M_6 and M_{18}-M_{19} have unity gains and they are used to sense the current flowing through X port and to mirror it to the high-impedance Z port. The ideal current follower circuit has zero input impedance, infinite output impedance and unity current gain. With the assumptions that all the transistors are perfectly matched, each transistor operates in saturation region and the current mirror pairs have unity gain, the

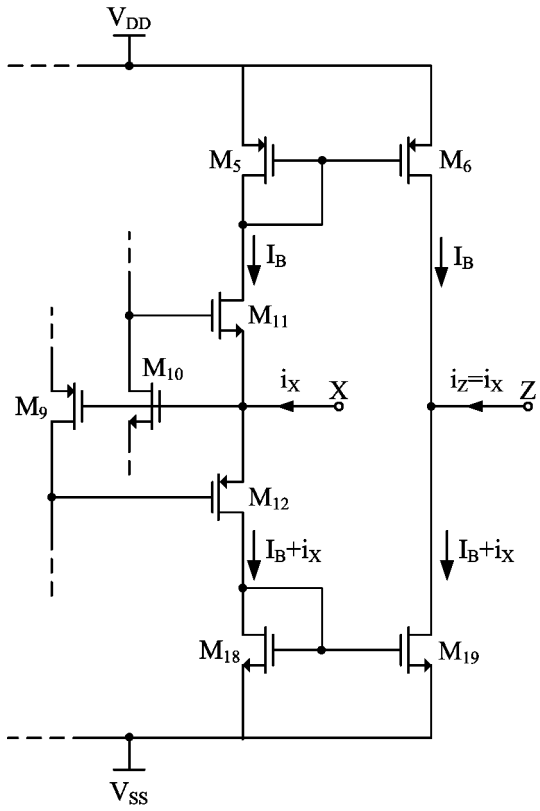

Figure 3.2. Current follower stage

proposed current follower circuit has very low input impedance at port X, which is calculated as in (3.2), very high output impedance at port Z and a current transfer gain which is very close to unity.

The α parameter of the current follower stage can be easily derived and it is equal to:

$$\alpha = \frac{i_Z}{i_X} \cong \frac{g_{m6,19}}{g_{m5,18}} \tag{3.3}$$

If the load impedance connected to high impedance port Z is negligible with respect to the transistor output resistances, the α parameter can be given by the transconductance ratios of the current mirror transistors and it is very close to the ideal unitary value. The equivalent resistance seen at port Z can be calculated as:

$$R_z \cong \frac{r_{o6} r_{o19}}{r_{o6} + r_{o19}} \tag{3.4}$$

3.1.3. The Complete Schematic

The proposed CMOS CCII circuit is composed of voltage and current followers as

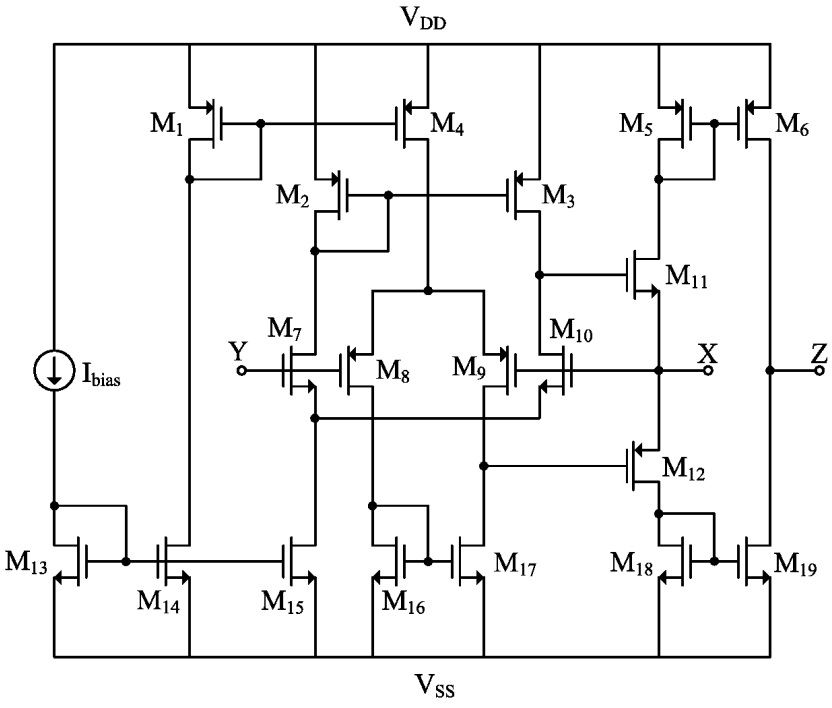

Figure 3.3. Differential pair based CMOS CCII

depicted in the above sections. The complete circuit is shown in Fig. 3.3. Transistors M_4 and M_{15} serve as DC current source for the differential pair transistors. Source coupled transistors M_7-M_{10} copy the voltage applied to high impedance port Y to low impedance port X. Current mirror transistors M_5-M_6 and M_{18}-M_{19} have unity gains and they sense the current through X port and copies it to high impedance Z port.

3.1.4. Simulation Results

For the proposed circuit, the voltage follower gain, β, is determined as a function of the frequency, an infinite load R_L connected at port X, the conveyor driven at port Y by an ideal voltage source and output port Z grounded. The current follower gain, α, is determined with an input current applied to port X. The current I_Z is then the current that flows through port Z grounded; port Y also grounded. The value of the equivalent impedance at port X is determined with outputs Y and Z grounded. When an input current I_X is applied at port X, the resulting voltage V_X allows determining the impedance. The values for R_Z and C_Z, which constitute the output impedance of the current source at port Z, will be determined for the conveyor driven by a current Ix at port X, and with port Y grounded. Then the voltage V_Z, which results in at port Z loaded by infinite impedance, allows determining R_Z at low frequencies: $R_Z = V_Z/\alpha.I_X \approx V_Z/I_X$ (since the value of α is very close to the unity) [12]. The value of C_Z is then deduced from the -3 dB cutoff frequency, f_Z, for this voltage.

Table 3.1. Aspect ratios

Transistor	**W[µm]/L[µm]**
M_{13}, M_{14}, M_{18}, M_{19}	10/0.5
M_{16}, M_{17}	20/0.35
M_7, M_{10}, M_{15}	20/0.5
M_{11}	30/0.35
M_1, M_5, M_6	30/0.5
M_2, M_3	60/0.35
M_4, M_8, M_9	60/0.5
M_{12}	90/0.35

The characteristics of the CMOS CCII circuit have been determined from HSpice simulations by using AMS 0.35µm, 3.3V process parameters. ±1.65V supply voltages and

25μA biasing current are used during simulations. Aspect ratios of the transistors are given in Table 3.1. Lengths of the transistors that need to be matched are selected as 0.5μm.

The variation of the ports X and Z impedances with frequency are shown in Fig. 3.4 and Fig. 3.5, respectively. Impedance values of the proposed circuit are very close to ideal values in a wide frequency range.

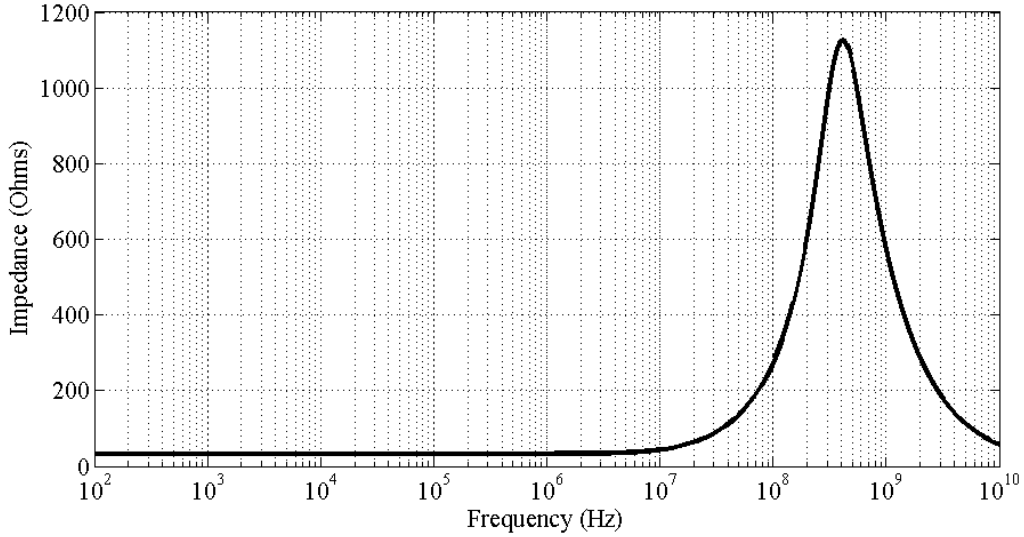

Figure 3.4. Port X impedance variation with frequency

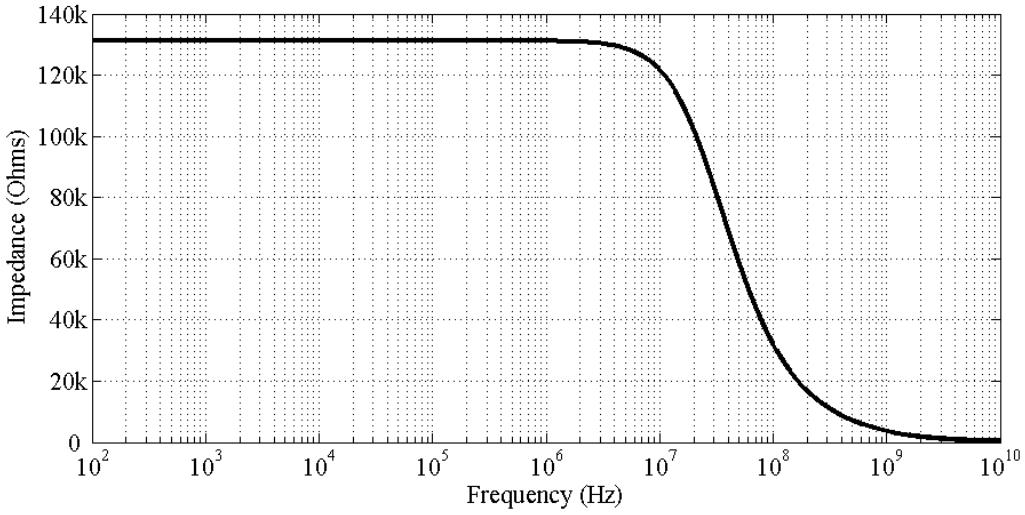

Figure 3.5. Port Z impedance variation with frequency

The equivalent impedance at port X has very small values up to 100MHz. The value of the impedance is 33.2Ω at 1MHz, 43.5Ω at 10MHz and 273.8Ω at 100MHz. Port Z impedance value is about 130kΩ at low frequencies and its value decreases as the frequency increases. Its value is about 122kΩ at 10MHz and 32kΩ at 100MHz.

In Fig. 3.6 and 3.7, the linear operation regions of the voltage and current follower stages are given for the ideal CCII and the proposed CCII. The difference between the two is also plotted.

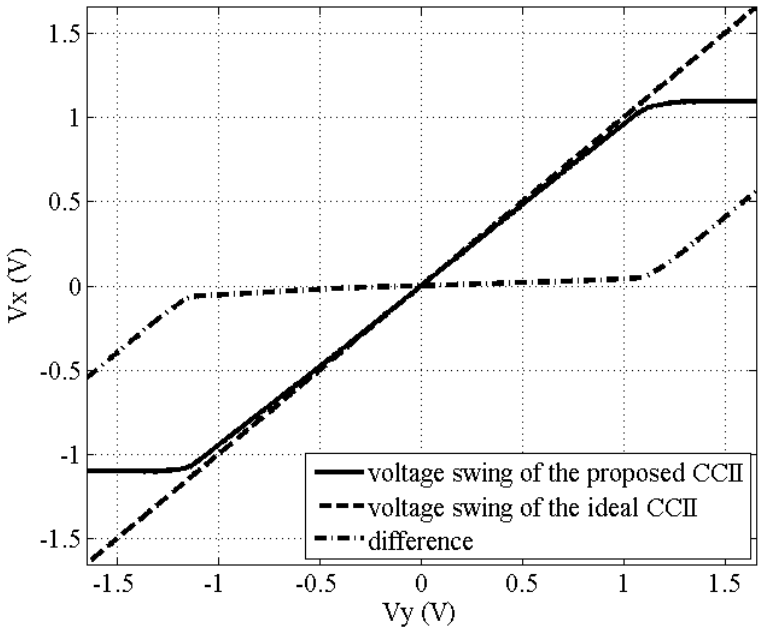

Figure 3.6. DC voltage transfer characteristics from port Y to port X

It is shown that the proposed circuit has a linear voltage swing up to ±1.1V owing to differential pair based voltage follower stage, with less than ±6% error. The proposed current follower stage has a linear current swing up to ±4mA with using basic current mirror transistors. From the DC transfer characteristics, offset voltage on port X and offset current on port Z are obtained. When port Y is grounded, the offset voltage obtained at port X is about 0.8mV and when the current applied at port X is zero, the offset current flowing through port Z is obtained as 2.2μA.

Fig. 3.8 and 3.9 illustrates the AC transfer characteristics of the voltage and current followers, respectively. The voltage and current transfer ratios, β and α, are found to be

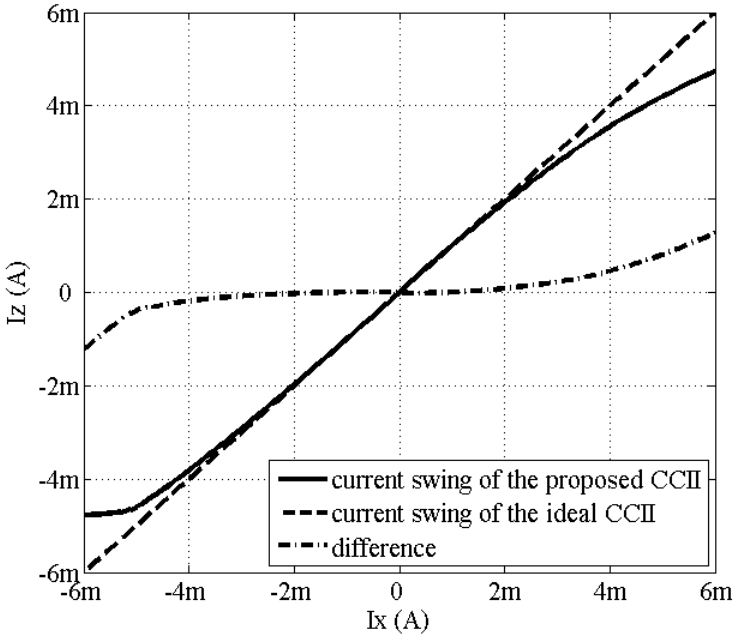

Figure 3.7. DC current transfer characteristics from port X to port Z

0.97 and 1.08, respectively. 475MHz voltage transfer bandwidth and 430MHz current transfer bandwidth are obtained with about only 670μW power consumption. The bandwidth of the circuit may be increased further if the power consumption of the circuit is allowed to be increased. Simulation results of the proposed differential pair based CMOS CCII circuit are also given in Table 3.2.

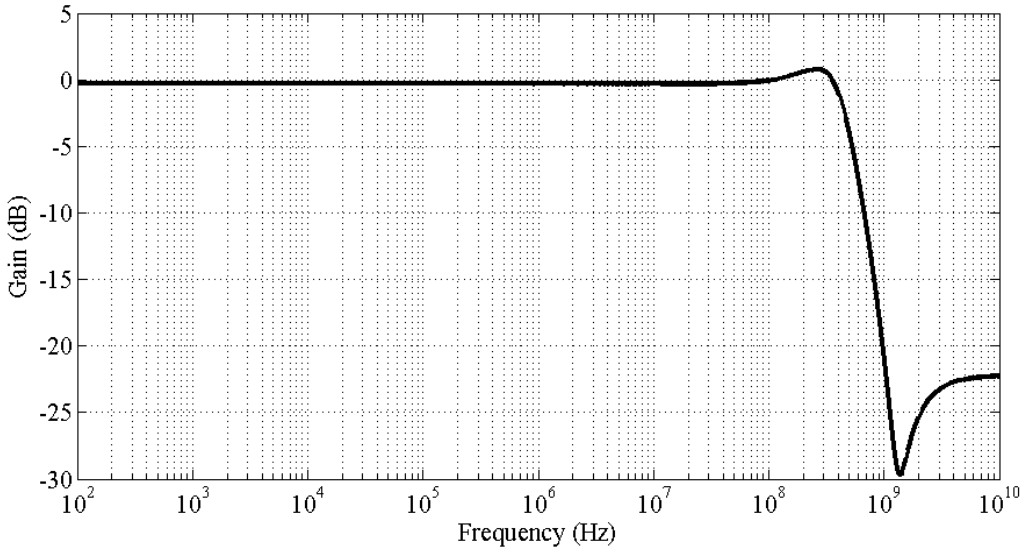

Figure 3.8. Voltage transfer gain between ports Y and X

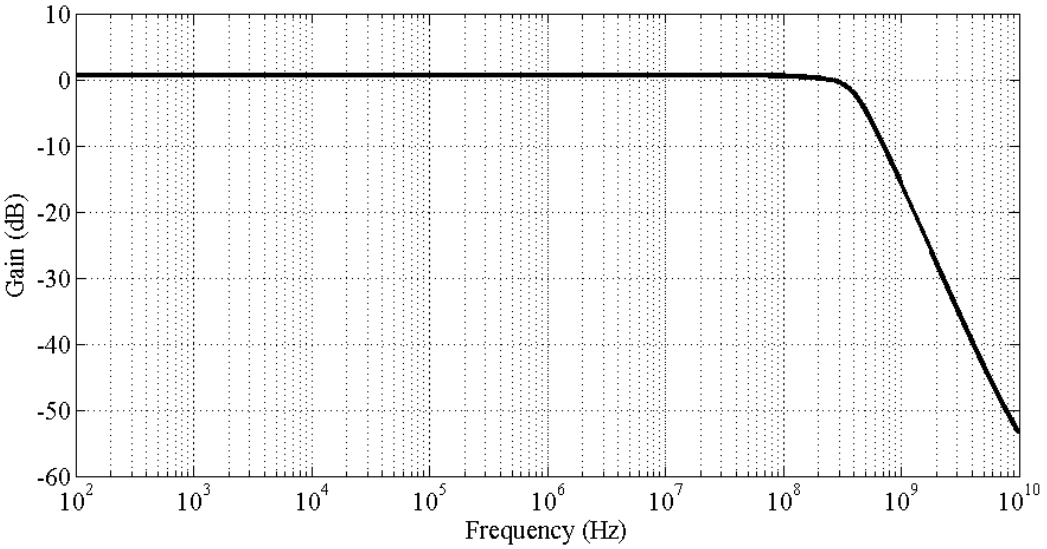

Figure 3.9. Current transfer gain between ports X and Z

Table 3.2. Simulation results of the differential pair based CMOS CCII

Summary of the CCII Performance	
Supply voltage	±1.65V
Biasing current	25µA
Power dissipation	670µW
Voltage gain, V_X / V_Y	0.97
Voltage transfer BW	475MHz
Voltage swing on port X	±1.1V
Current gain, I_Z / I_X	1.08
Current transfer BW	430MHz
Current swing on port Z	±4mA
Offset voltage on port X	0.8mV
Offset current on port Z	2.23µA
Port X resistance	33.2Ω
Port Z resistance	130kΩ

3.2. Improved Differential Pair Based CMOS CCII

The proposed circuit in Fig. 3.3 employs differential pair based voltage follower stage and simple current mirror based current follower stage. The voltage follower stage in Fig. 3.1 employs two source followers on output port to obtain low equivalent impedance. A well known method to reduce the output impedance is to use feedback. This technique can be conveniently applied to the source followers M_{11} and M_{12} in Fig. 3.1.

3.2.1. Improved Voltage Follower Stage

When local feedback is applied to the source follower transistors M_{11} and M_{12}, improved output stages can be obtained. These new configurations are called super source followers [46] and they are shown in Fig. 3.10.

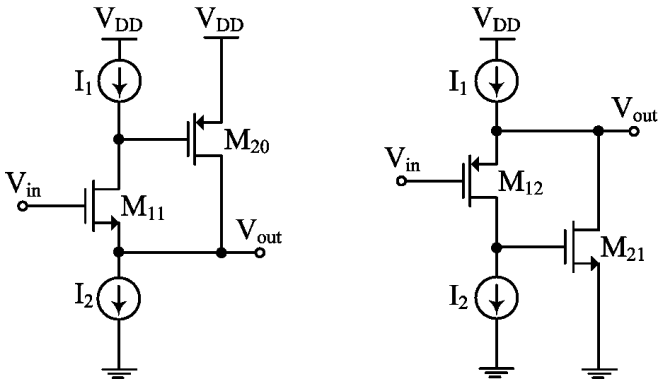

Figure 3.10. Source followers with local feedback (super source followers)

The gain stage amplifies the difference between the input and output of the source follower, thus reducing the output impedance by the amplification factor of the gain stage itself. The improved differential-pair based voltage follower stage with super source followers is shown in Fig. 3.11. Just like the conventional source follower, the input signal is replicated at the sources of M_{11} and M_{12}, but it is also amplified at the drains of same transistors. The amplified signal is fed to the inputs of M_{20} and M_{21} which operate as the input elements of the second gain stage [32]. Feedback loops are thus established through transistors M_{11}, M_{20} and M_{12}, M_{21}. With the improved configuration, the equivalent resistance on port X is decreased to:

$$R_x = \frac{1}{g_{m11}g_{m20}r_o(1+g_{m10}r_o/2)} \left\| \frac{1}{g_{m12}g_{m21}r_o(1+g_{m9}r_o/2)} \right. \tag{3.5}$$

When compared to (3.3), a very good reduction is obtained by applying additional local feedback to the source followers of Fig. 3.1.

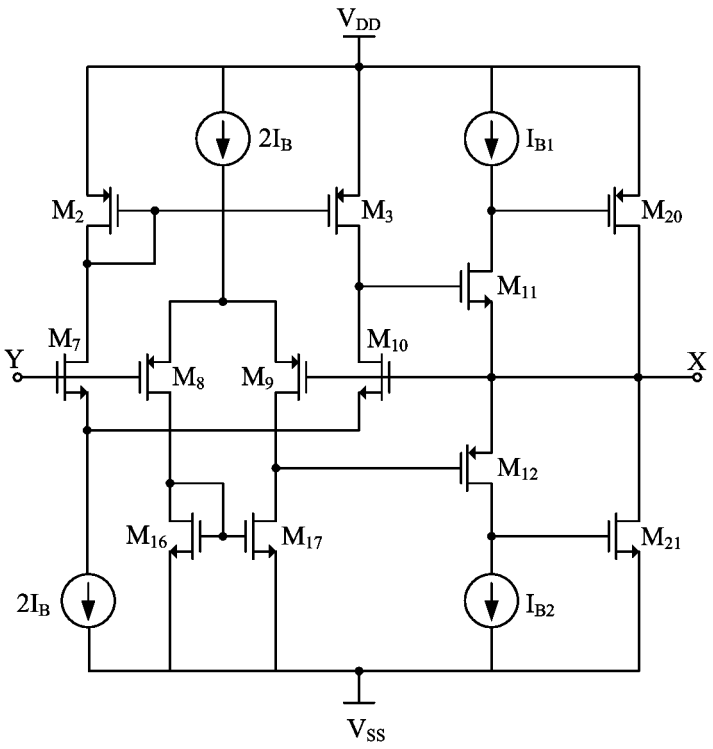

Figure 3.11. Improved voltage follower stage

3.2.2. Current Follower Stage

The current follower stage of the improved CCII topology is very similar to Fig. 3.2. The current flowing through X port is copied to high impedance Z port by the current mirror pairs M_{20}, M_6 and M_{21}, M_{19}. After applying local feedback to source follower transistors, a very good reduction for the input impedance of the current follower stage is obtained as shown in (3.5). The equivalent resistance on Z port is the parallel combination of the output resistances of transistors M_6 and M_{19}:

$$R_z \cong \frac{r_{o6} r_{o19}}{r_{o6} + r_{o19}} \tag{3.6}$$

In order to have high impedance values at port Z, transistors with bigger channel lengths are selected. The resultant current follower stage is shown in Fig. 3.12.

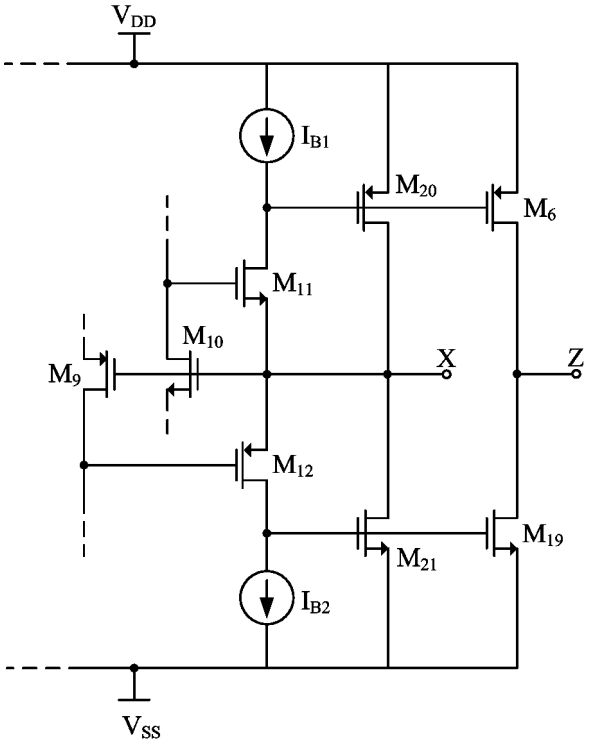

Figure 3.12. Current follower stage

The current transfer function is not independent from the load connected to port Z. If this load impedance is negligible compared to the output resistances of M_6 and M_{19}, the α parameter is very close to its ideal unitary value , as shown in the following expression:

$$\alpha = \frac{I_Z}{I_X} \cong \frac{g_{m6,19}}{g_{m20,21}} \tag{3.7}$$

3.2.3. The Complete Schematic

The complete schematic of the improved differential pair based CMOS CCII circuit is shown in Fig. 3.13. The source followers of Fig. 3.3 are replaced with the super source followers to obtain the proposed circuit. When compared to the circuit in Fig. 3.3, very good impedance reduction at port X is obtained. Voltage copying action from port Y to port X is carried out via the source coupled transistors M_7-M_{10}. Gates of transistors M_6, M_{20} and M_{19}, M_{21} are connected to each other. The current flowing through X port generates equal V_{GS} voltages for these transistors and as a result forces equal currents at ports X and Z.

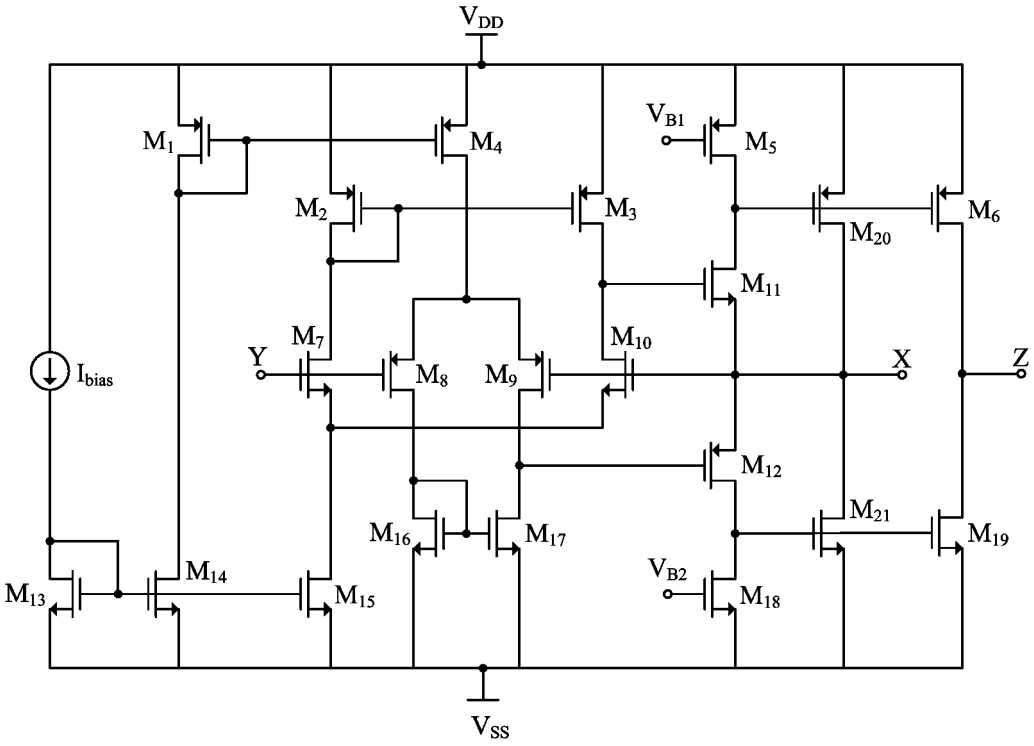

Figure 3.13. Improved differential pair based CMOS CCII

3.2.4. Simulation Results

The characteristics of the improved differential-pair based CMOS CCII circuit have been examined from HSpice simulations by using AMS 0.35µm, 3.3V process parameters. ±1.65V supply voltages and 25µA biasing current are used during simulations. Aspect ratios of the transistors are given in Table 3.3. Lengths of the transistors that need to be matched are selected as 0.5µm. Lengths of the transistors M_5 and M_{18}, which serve as DC

Table 3.3. Aspect ratios

Transistor	**W[µm]/L[µm]**
M_{13}, M_{14}, M_{18}, M_{19}, M_{21}	10/0.5
M_{16}, M_{17}	20/0.35
M_7, M_{10}, M_{15}	20/0.5
M_{11}, M_{20}	30/0.35
M_1, M_5, M_6	30/0.5
M_2, M_3	60/0.35
M_4, M_8, M_9	60/0.5
M_{12}	90/0.35

current sources for the source follower transistors, are selected as 0.5µm. Biasing voltages V_{b1} and V_{b2} are equal to 0.8V and -0.96V, respectively. The variation of the ports X and Z impedances with frequency are given in Fig. 3.14 and Fig. 3.15, respectively.

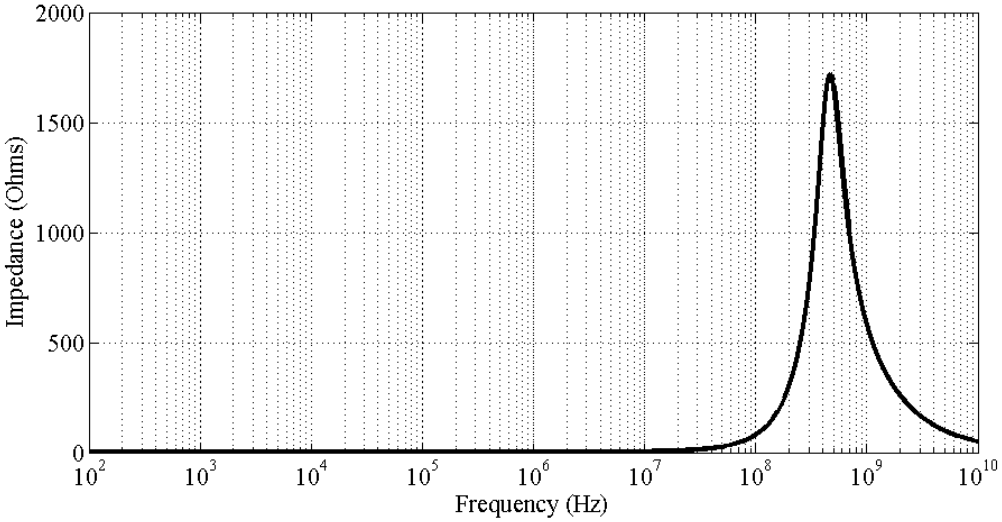

Figure 3.14. Port X impedance variation with frequency

The equivalent impedance on port X has very small values up to 100MHz. The value of the impedance is 1.65Ω at 1MHz, 4.5Ω at 10MHz and 80.3Ω at 100MHz. Port Z impedance value is about 147kΩ at low frequencies and its value decreases as the frequency increases. Its value is about 135kΩ at 10MHz and 34kΩ at 100MHz.

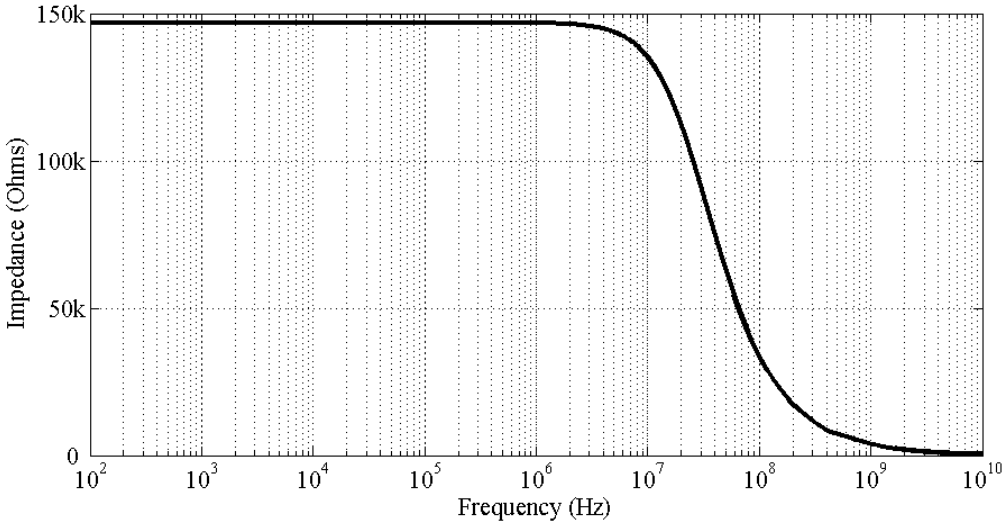

Figure 3.15. Port Z impedance variation with frequency

In Fig. 3.6 and 3.7, the linear operation regions of the voltage and current follower stages are given for the ideal CCII, the proposed CCII and the difference between the two.

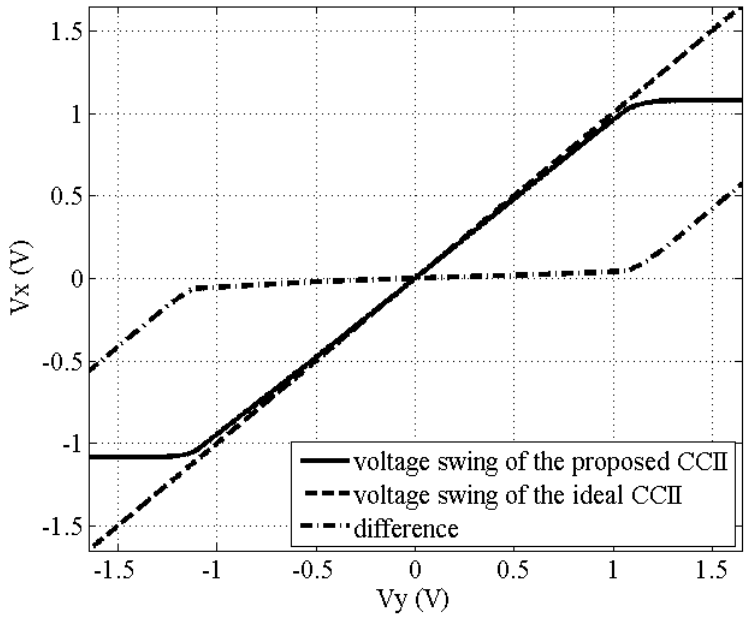

Figure 3.16. DC voltage transfer characteristics from port Y to port X

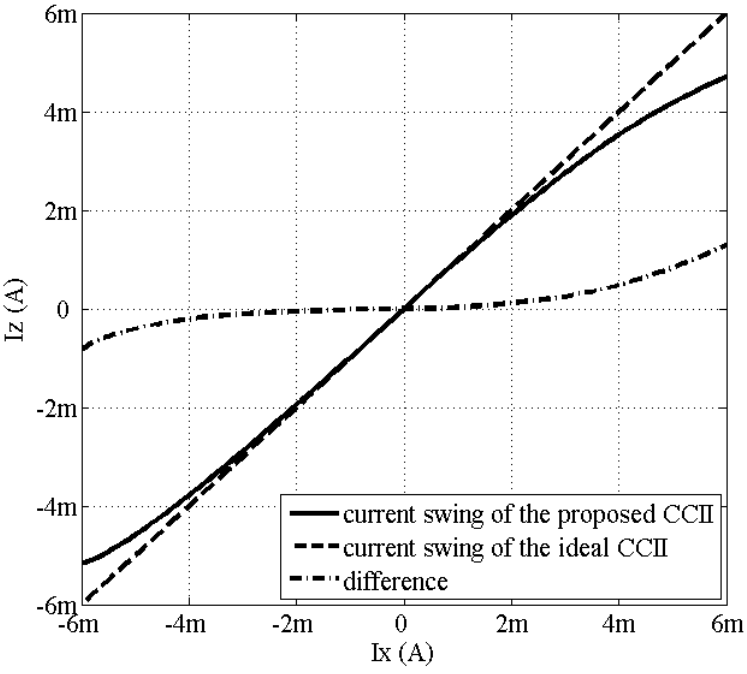

Figure 3.17. DC current transfer characteristics from port X to port Z

Very similar to the circuit in Fig. 3.3, the improved differential pair based circuit has a linear voltage swing between ±1.1V with less than ±6% error. The proposed current follower stage has a linear current swing up to ±4mA.

From the DC transfer characteristics, offset voltage on port X and offset current on port Z are obtained. When port Y is grounded, the offset voltage obtained at port X is about 0.8mV and when the current applied at port X is zero, the offset current flowing through port Z is obtained as 130nA.

Fig. 3.18 and 3.19 illustrates the AC transfer characteristics of the voltage and current followers, respectively. The voltage and current transfer ratios, β and α, are found to be 0.96 and 0.99, respectively. 550MHz voltage transfer bandwidth and 575MHz current transfer bandwidth are obtained with about only 740μW power consumption. Simulation results of the improved differential pair based CMOS CCII circuit are also given in Table 3.4.

When compared to differential pair based circuit in Fig. 3.3, two advantages are obtained with the proposed circuit. Firstly, the bandwidth of the current follower stage is increased from 430MHz to 575MHz. Secondly, about 20 times reduction is obtained for the equivalent impedance on port X and it is decreased from 33.2Ω to 1.6Ω.

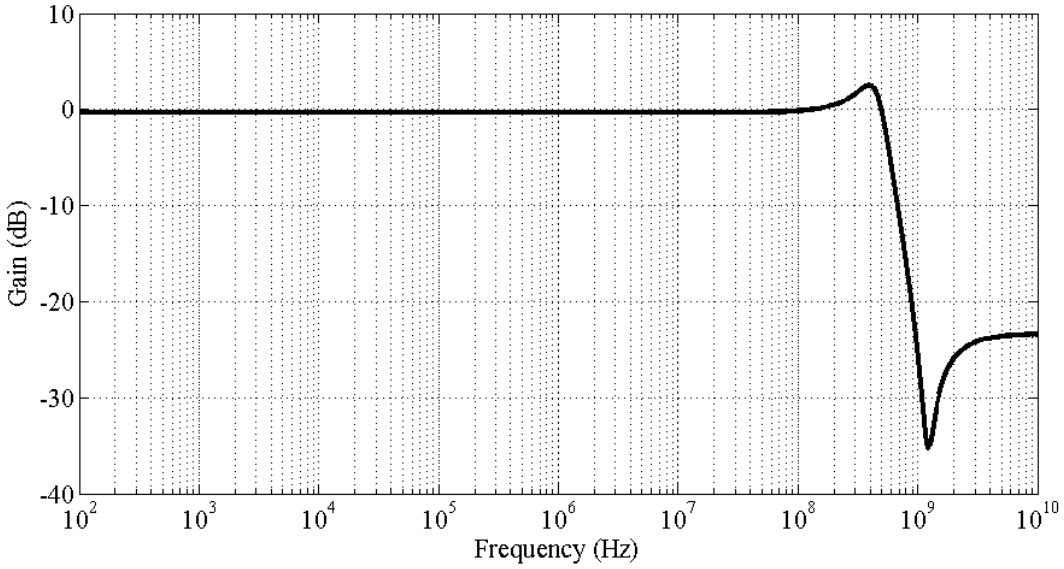

Figure 3.18. Voltage transfer gain between ports Y and X

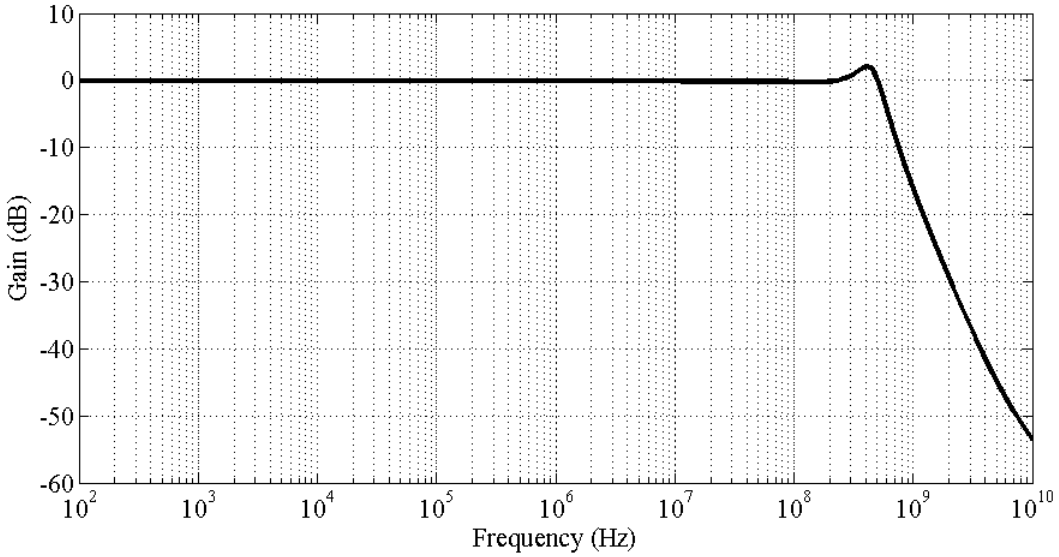

Figure 3.19. Current transfer gain between ports X and Z

Table 3.4. Simulation results of the improved differential pair based CMOS CCII

Summary of the CCII Performance	
Supply voltage	±1.65V
Biasing current	25µA
Power dissipation	740µW
Voltage gain, V_X / V_Y	0.96
Voltage transfer BW	550MHz
Voltage swing on port X	±1.1V
Current gain, I_Z / I_X	0.99
Current transfer BW	575MHz
Current swing on port Z	±4mA
Offset voltage on port X	0.8mV
Offset current on port Z	130nA
Port X resistance	1.6Ω
Port Z resistance	147kΩ

3.3. Self Biased Differential Pair Based CMOS CCII

In an analog circuit, different active devices should be properly biased to attain high performance. For instance, most of the transistors in a CMOS circuit should be biased for operation in the saturation region. Usually a separate circuit is used to bias the transistors. Using external bias voltage or current sources result in numerous drawbacks, namely, area and power overhead, susceptibility of the bias lines to noise cross-talk and high sensitivity of the bias point to process variations [25-27]. In this section, a self biased differential-pair

based CMOS CCII circuit is introduced, which uses no additional biasing voltage or current sources other than the two supply rails. The resulting self biased circuit is free from the above mentioned drawbacks and exhibits similar performance to previously mentioned CCII circuits, except for a small reduction in voltage swing on X port.

The circuit is composed of a self biased differential-pair based voltage follower stage and a current mirror based current follower stage. The operation of the circuit is given in detail by describing the operations of the voltage and current follower stages individually.

3.3.1. Self Biased Voltage Follower Stage

The structure of the self biased voltage follower stage is based on long tail differential pairs to provide large voltage swings on X and Y ports. Assuming that all the transistors operate in saturation regions, the operation of the proposed circuit can be explained as follows. Transistors M_1 and M_4 conduct when the input voltage is positive, while transistors M_2 and M_3 conduct when the input voltage is negative. By the current mirroring action of transistors M_9, M_{13} and M_{10}, M_{14} the current flowing through M_{11} and

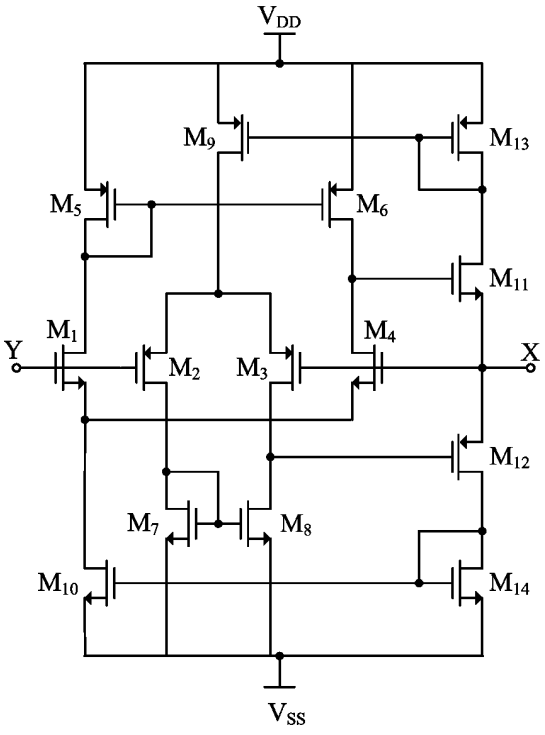

Figure 3.20. Self biased voltage follower stage

M_{12} is copied to M_9 and M_{10} which serve as DC current sources for the differential pairs. The current mirrors formed by M_5-M_8 force equal currents in the transistors M_1-M_4 which function as source-coupled pairs. This operation drives the gate-to-source voltages $v_{gs1}=v_{gs4}$ and $v_{gs2}=v_{gs3}$ and, as a result, forces the voltage at port X to follow the voltage at port Y. The proposed circuit is shown in Fig. 3.20.

An important issue in self-biasing CMOS circuits is the existence of degenerate bias points. In the proposed self biased voltage follower circuit, if all of the transistors carry zero current when the supply is turned on, they may remain off indefinitely because the loop can support a zero current in both differential pairs. This start-up problem is resolved by adding a start-up circuit which is shown in Fig. 3.21.

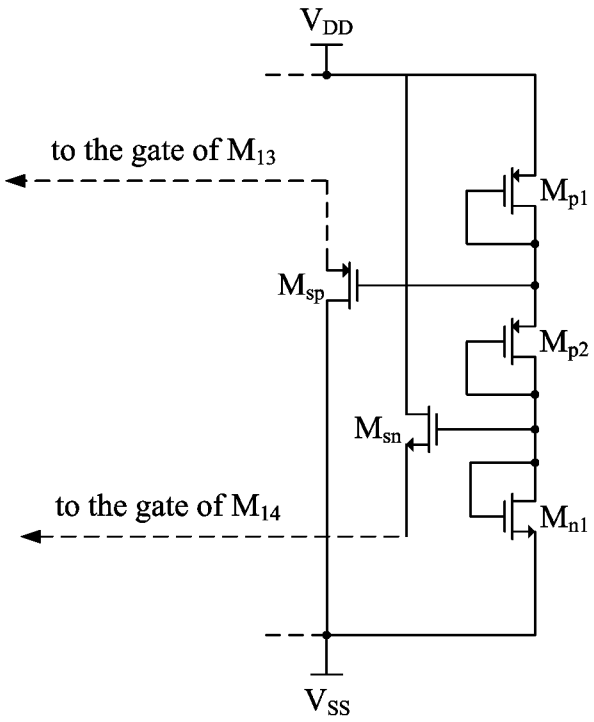

Figure 3.21. The start-up circuit

The possibility of the current flowing through the circuit being zero exists in all self-biased circuits. The current flowing through the voltage follower circuit will be zero when the gate voltages of M_9 and M_{13} are at or near V_{DD} or the gate voltages of M_{10} and M_{14} are at or near V_{SS}. The start-up circuit shown in Fig. 3.21 is used to avoid operation of the voltage follower circuit with zero current. If the gate voltage of M_{14} is at or near V_{SS}, M_{sn}

turns on and a current will flow from V_{DD} to V_{SS} through transistors M_{sn} and M_{14} which also support a V_{GS} voltage for M_{10}, the current source transistor of the NMOS input differential pair. The similar operation is valid for the PMOS input differential pair with the current source transistor M_9. If the gate voltage of M_{13} is at or near V_{DD}, M_{sp} turns on and a current will flow from V_{DD} to V_{SS} through transistors M_{13} and M_{sp} which generates a V_{GS} voltage for M_9. With the increase of the V_{GS} voltages of M_{13} and M_{14}, M_{sn} and M_{sp} will turn off and they will not affect the operation of the voltage follower circuit [24]. Transistors M_{11} and M_{12}, which are connected to form a source follower, provide low parasitic resistance on port X. The β parameter of the self biased voltage follower stage is equal to:

$$\beta = \frac{v_X}{v_Y} \cong \frac{g_{m1,2}}{g_{m3,4}} \tag{3.8}$$

The parasitic resistance at port X is the same as (3.2) and it is equal to:

$$R_x = \frac{1}{g_{m11}(1+g_{m4}r_o/2)} \left\| \frac{1}{g_{m12}(1+g_{m3}r_o/2)} \right. \tag{3.9}$$

3.3.2. Current Follower Stage

The current follower stage is shown in Fig. 3.22. The current mirrors M_{13}, M_{15} and M_{14}, M_{16} have unity gains and they are used to sense the current flowing through X port and to mirror it to the high impedance Z port. With the assumptions that all the transistors are perfectly matched, each transistor operates in its saturation region and the current mirror pairs have unity gain, the proposed current follower circuit has very low input impedance at port X, very high output impedance at port Z and a current transfer gain which is very close to unity. The α parameter of the current follower stage is equal to:

$$\alpha = \frac{i_Z}{i_X} \cong \frac{g_{m15,16}}{g_{m13,14}} \tag{3.10}$$

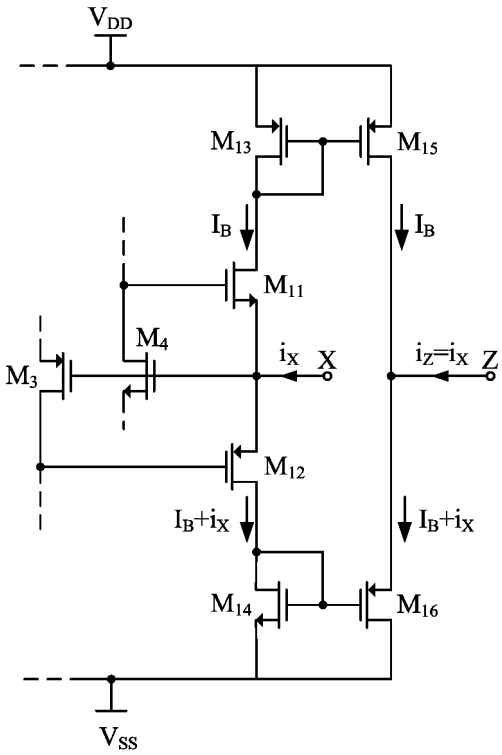

Figure 3.22. Current follower stage

If the load impedance connected to high impedance port Z is negligible compared to the transistor output resistances, the α parameter can be given by the transconductance ratios of the current mirror transistors and it is very close to the ideal unity value. The equivalent resistance seen at port Z can be calculated as:

$$R_z \cong \frac{r_{o15} r_{o16}}{r_{o15} + r_{o16}} \tag{3.11}$$

3.3.3. The Complete Schematic

The complete schematic of the self biased differential-pair based CMOS CCII including the start-up circuit is shown in Fig. 3.23. There are no any biasing voltage or current sources other than the two supply rails. The current flowing through the source follower transistors M_{11} and M_{12} generates V_{DS} voltages for the diode connected transistors M_{13} and M_{14}. These voltages are the V_{GS} voltages of M_9 and M_{10}, which serve as DC current sources for the differential pairs. Voltage copying action from port Y to port X is

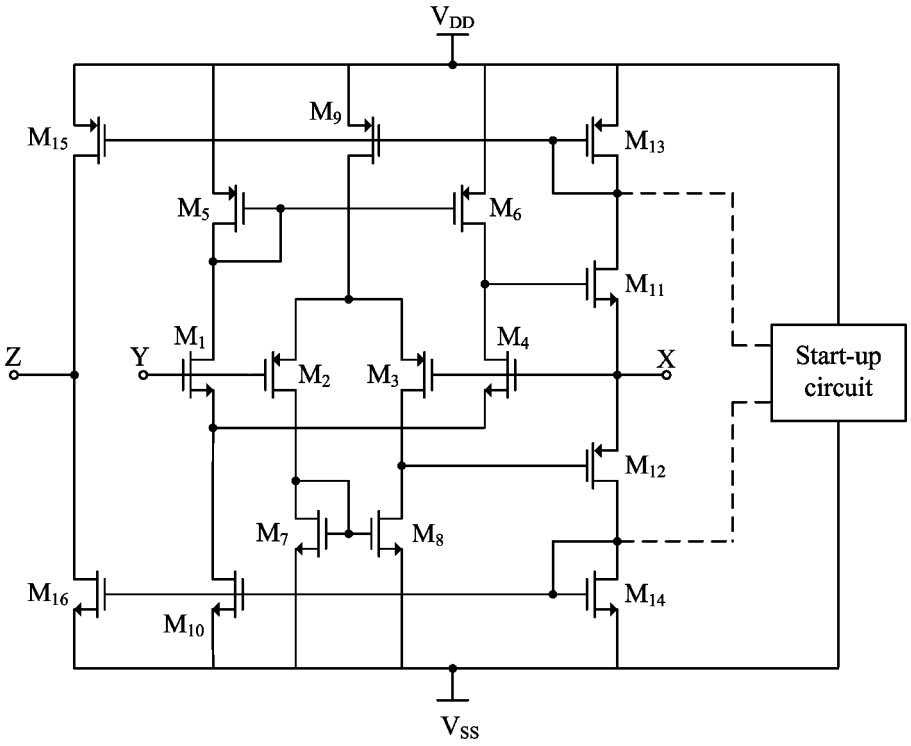

Figure 3.23. Self biased differential pair based CMOS CCII

performed via the source-coupled transistors M_1-M_4. The current flowing through X port is copied to high impedance Z port by the mirror transistor pairs M_{13}, M_{15} and M_{14}, M_{16}.

3.3.4. Simulation Results

The characteristics of the self biased differential pair based CMOS CCII circuit have been determined with HSpice simulations by using AMS 0.35µm, 3.3V process

Table 3.5. Aspect ratios

Transistor	**W[µm]/L[µm]**
M_{10}, M_{14}, M_{16}	10/0.5
M_7, M_8	20/0.35
M_1, M_4	20/0.5
M_{11}	50/0.35
M_9, M_{13}, M_{15}	30/0.5
M_5, M_6	60/0.35
M_2, M_3	60/0.5
M_{12}	150/0.35
M_{p1}	20/0.5
M_{p2}, M_{sp}, M_{sn}	1/5
M_{n1}	20/5

parameters. Neither voltage nor current biasing sources are used during simulations. The current which flows through differential pairs and the transistors that form X port, M_{11} and M_{12}, is about 25µA. The current flowing through the diode connected transistors of the start up circuit is 5µA and the power consumption of the start-up circuit is 16.5µW. Aspect ratios of the transistors are given in Table 3.5. In order to have high impedance value at port Z, lengths of transistors M_{13}-M_{16} are selected as 0.5µm.

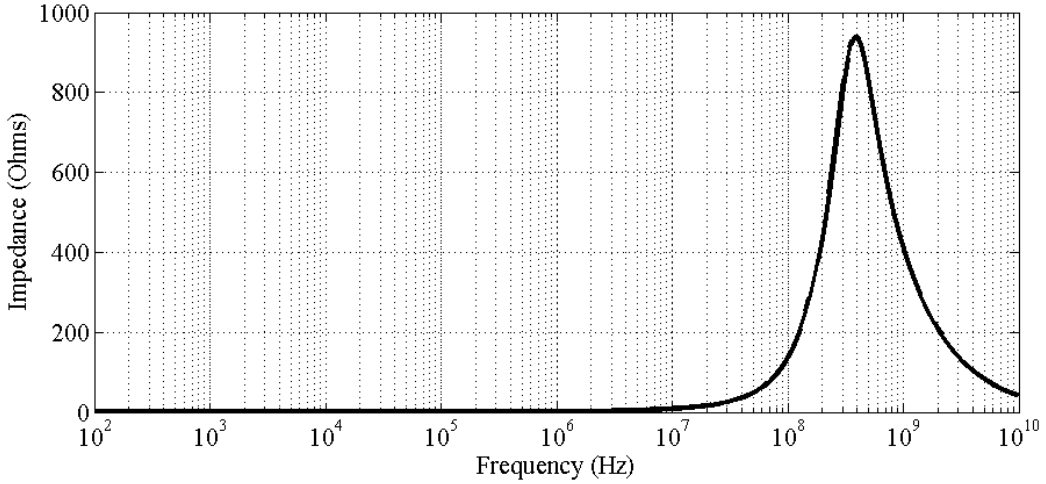

Figure 3.24. Port X impedance variation with frequency

The variation of the ports X and Z impedances with frequency are given in Fig. 3.24 and Fig. 3.25, respectively.

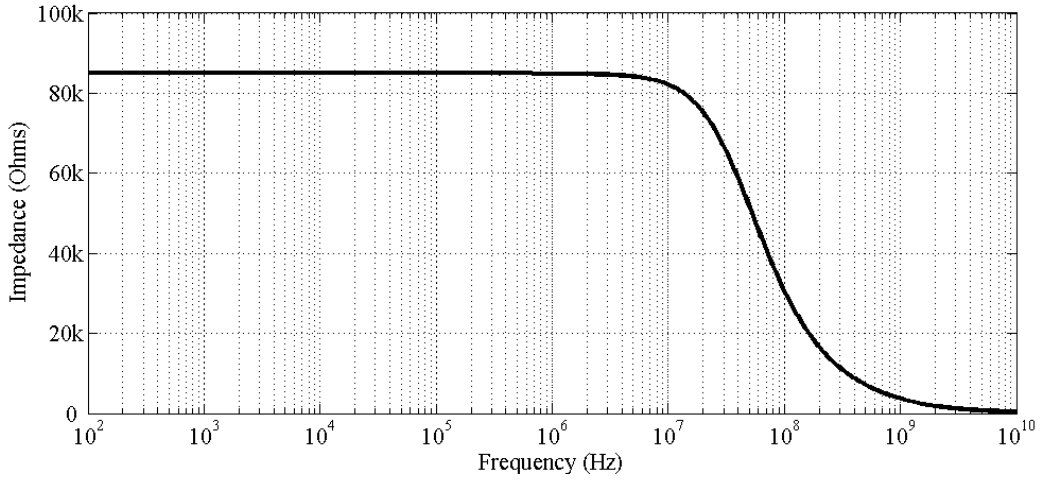

Figure 3.25. Port Z impedance variation with frequency

The value of the equivalent impedance on port X is 1.1Ω at 1MHz, 8.6Ω at 10MHz and 137.4Ω at 100MHz. Port Z impedance value is about 85kΩ at low frequencies and its value decreases as the frequency increases. Its value is about 82kΩ at 10MHz and 31kΩ at 100MHz. The impedance values of the proposed CMOS CCII circuit are very similar to the ideal CCII values in a wide frequency range and these properties allow the circuit to be used in high frequency applications.

In Fig. 3.26 and 3.27, the linear operation regions of the voltage and current follower stages are given, respectively. The offset voltage on port X is 0.9mV and the offset current flowing through port Z is 2.8μA. The proposed circuit has a linear voltage swing between ±1.1V with less than ±6% error and a linear current swing up to ±4mA with less than ±9% error.

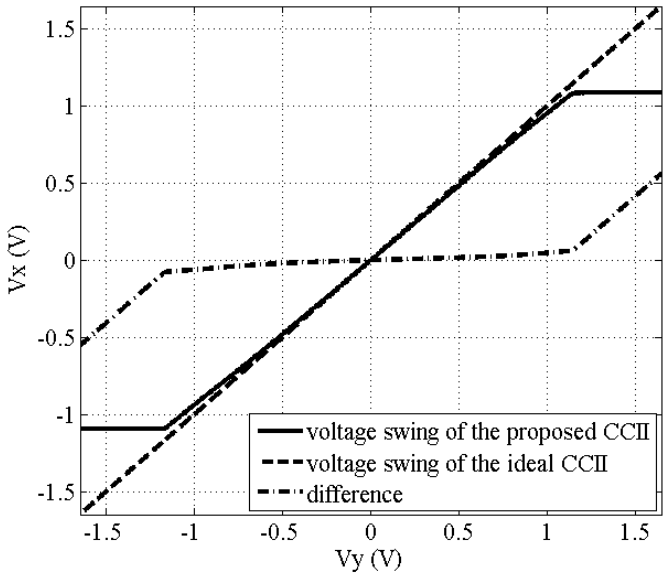

Figure 3.26. DC voltage transfer characteristics from port Y to port X

Fig. 3.28 and 3.29 illustrate the AC transfer characteristics of the voltage and current followers, respectively. The voltage and current transfer ratios, β and α, are found to be 0.97 and 1.07, respectively. 440MHz voltage transfer bandwidth and 400MHz current transfer bandwidth are obtained with about 650μW power consumption. Simulation results of the improved differential pair based CMOS CCII circuit are also given in Table 3.6.

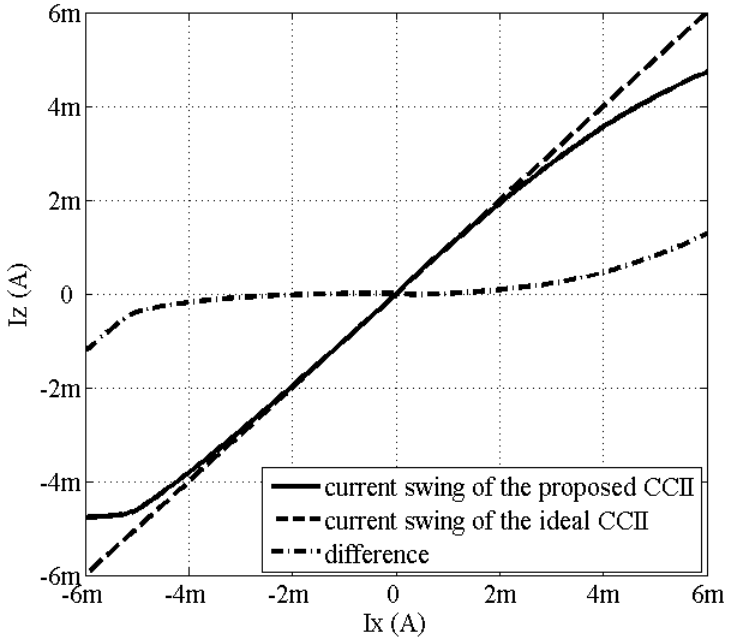

Figure 3.27. DC current transfer characteristics from port X to port Z

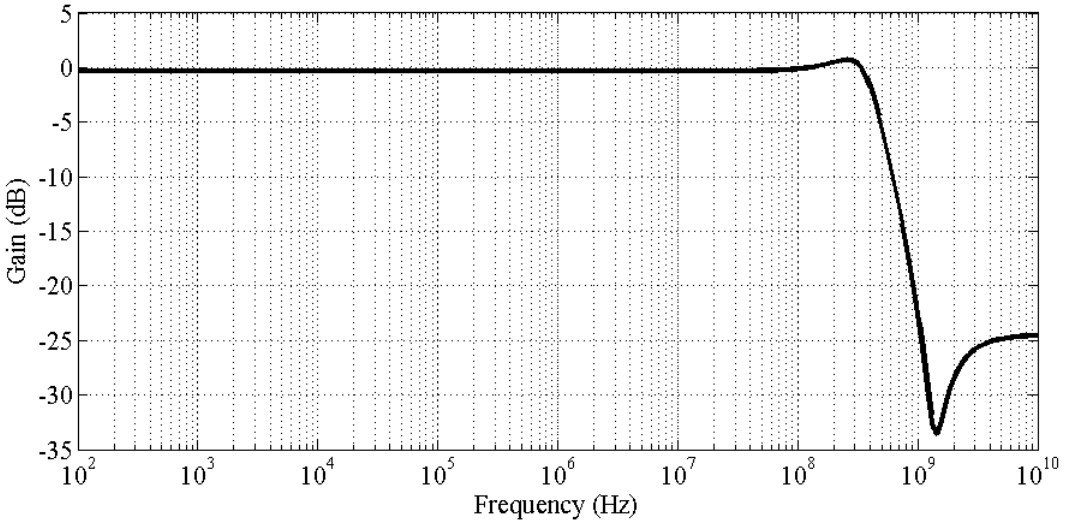

Figure 3.28. Voltage transfer gain between ports Y and X

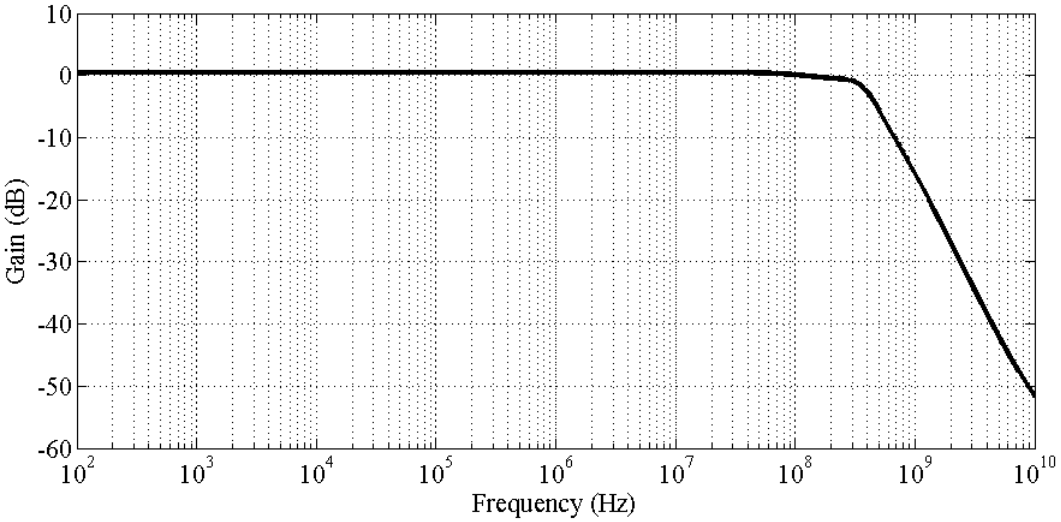

Figure 3.29. Current transfer gain between ports X and Z

Table 3.6. Simulation results of the self biased differential pair based CMOS CCII

Summary of the CCII Performance	
Supply voltage	±1.65V
Power dissipation	650µW
Voltage gain, V_X / V_Y	0.97
Voltage transfer BW	440MHz
Voltage swing on port X	±1.1V
Current gain, I_Z / I_X	1.07
Current transfer BW	400MHz
Current swing on port Z	±4mA
Offset voltage on port X	0.9mV
Offset current on port Z	2.8µA
Port X resistance	0.51Ω
Port Z resistance	84.9kΩ

3.4. CMOS Differential Pair Based Implementations of CCI and CCIII

The proposed circuits, which are already defined in the above sections, implement differential pair based CMOS CCII configurations. The proposed voltage follower circuits with their high impedances on ports Y and Z, very low impedances on ports X, high voltage and current transfer bandwidths with gains very close to unity, can be used to implement the input or output stages of other current mode circuits like CCI, CCIII, CDBA, FTFN, etc. In this section self biased CMOS implementations of first and third generation current conveyors (CCI and CCIII, respectively) will be introduced.

3.4.1. First Generation Current Conveyors

The first generation current conveyor (CCI) is a three terminal active device which ensures two functionalities between its terminals. The voltage applied to Y port is copied to X port and the current flowing through X port is copied to Y and Z ports all with unity gains. The commonly used block representation of a CCI is given in Fig. 1.1. In mathematical terms, the port relations of a CCI can be described by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & \gamma & 0 \\ \beta & 0 & 0 \\ 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{3.12}$$

where α, β and γ are unity for an ideal CCI and they represent the voltage and current transfer gains. The current flowing through Y port is the main difference between a CCI and a CCII. Fig. 3.30 shows the complete real equivalent model of the CCI which takes into account the non-ideal characteristics at three ports, the capacitive parasitic impedances on Y and Z nodes and also non-perfect voltage and current follower parameters α, β and γ.

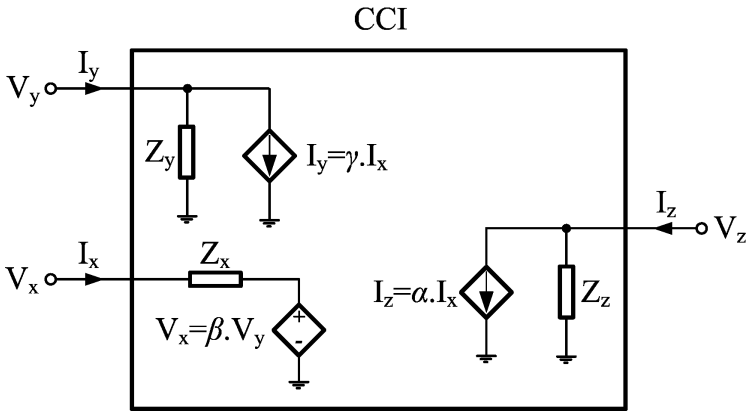

Figure 3.30. CCI+ equivalent model

$R_y//C_y$ constitutes the input impedance (Z_y) on port Y when output X of the voltage follower is open. The controlled voltage source $\beta.V_y$ reflects at port X, the voltage existing on port Y. The controlled current sources $\gamma.I_x$ at port Y and $\alpha.I_x$ at port Z copy the current

of port X. R_x is the intrinsic resistance on port X measured at low frequencies. $R_z//C_z$ is the output impedance (Z_z) on port Z [11,12].

3.4.1.1. Voltage and Current Follower Stage between Ports X and Y

The voltage follower stage of the proposed CCI circuit is very similar to Fig. 3.20. Current mirror pairs M_{13}, M_{17} and M_{14}, M_{18} sense the current flowing through X port and copy it to high impedance Y port with unity gain. The voltage applied to port Y is copied to low impedance X port by the source coupled transistors M_1-M_4. The circuit that performs voltage and current buffering between ports X and Y is shown in Fig. 3.31.

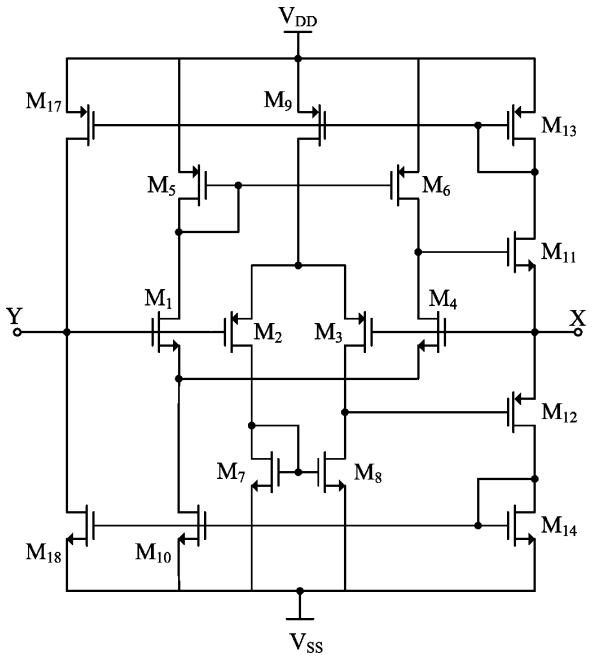

Figure 3.31. Buffer circuit used between ports X and Y

There is no difference of the port X impedance equation given in (3.9). Port Y equivalent resistance is the parallel combination of output resistances of transistors M_{17} and M_{18}.

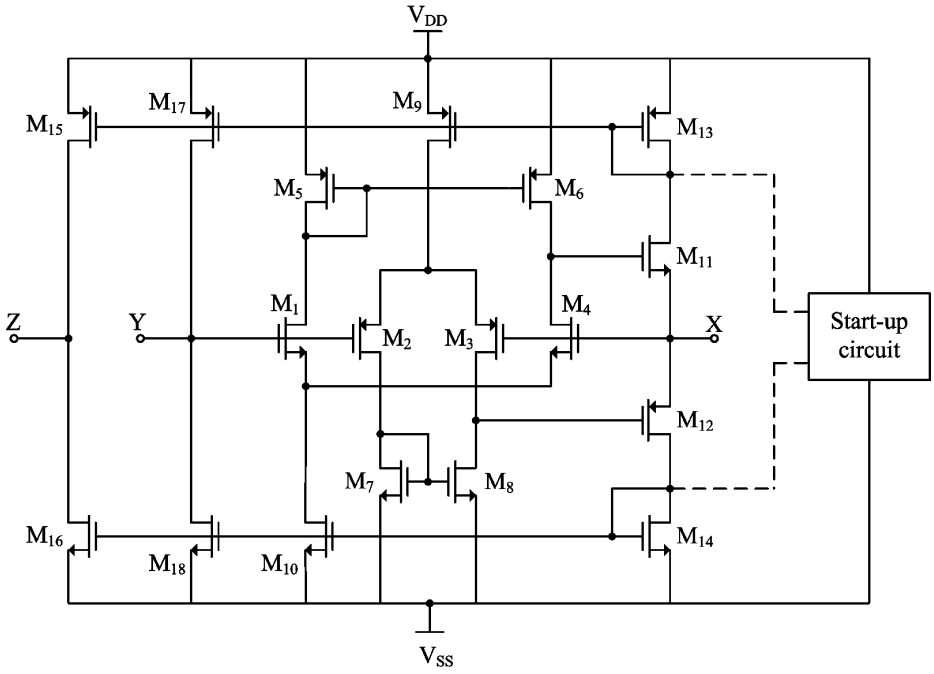

Figure 3.32. Self biased differential pair based CMOS CCI

Current follower stage given in Fig. 3.22 is used to copy the current flowing through X port to Z port with unity gain. The complete schematic of the self biased differential pair based CMOS CCI circuit is shown in Fig. 3.32.

3.4.1.2. Simulation Results

The characteristics of the proposed circuit have been determined from HSpice simulations by using AMS 0.35µm, 3.3V process parameters. Neither voltage nor current

Table 3.7. Aspect ratios

Transistor	**W[µm]/L[µm]**
M_{10}, M_{14}, M_{16}, M_{18}	10/0.5
M_7, M_8	20/0.35
M_1, M_4	20/0.5
M_{11}	30/0.35
M_9, M_{13}, M_{15}, M_{17}	30/0.5
M_5, M_6	60/0.35
M_2, M_3	60/0.5
M_{12}	90/0.35
M_{p1}	20/0.5
M_{p2}, M_{sp}, M_{sn}	1/5
M_{n1}	20/5

biasing sources are used during simulations. The current flowing through differential pairs is about 25µA. Aspect ratios of the transistors are given in Table 3.7.

Port Y is a current out - voltage in port. So the equivalent impedance seen at port Y must be as high as possible. In order to have high impedance values at ports Y and Z, lengths of transistors M_{13}-M_{18} are selected as 0.5µm. The current flowing through the diode connected transistors of the start up circuit is 5µA with about 16.5µW power consumption.

The proposed circuit is derived from the self biased CCII circuit which is given in Fig. 3.23 by adding two transistors, M_{17} and M_{18}, to copy the current of port X to port Y. Only the simulation results of current follower between these two ports are given in this section.

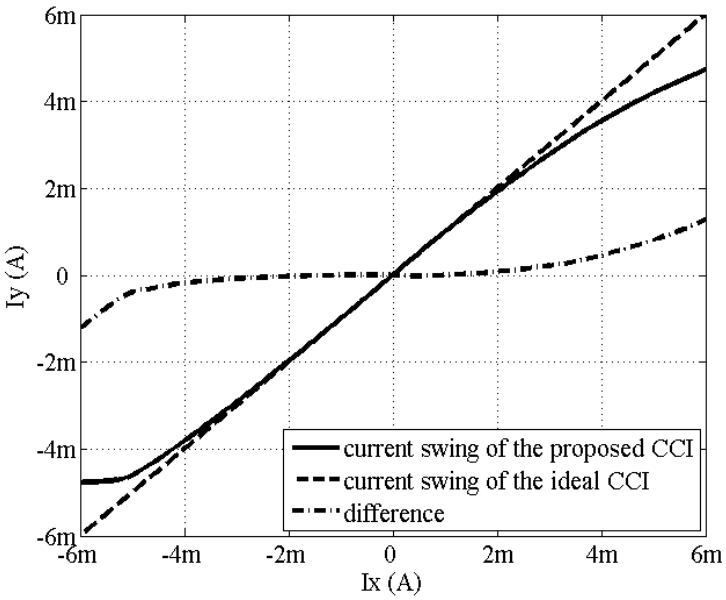

Figure 3.33. DC current transfer characteristics from port X to port Y

In Fig. 3.33 the linear operation region of the current follower stage is given. The offset current flowing through port Y is 2.8µA when port X is grounded. The current follower stage has a linear current swing between ±4mA with less than ±9% error. Fig. 3.34 illustrates the AC transfer characteristic of the current follower. The current transfer ratio γ is found to be 1.07. 430MHz current transfer bandwidth is obtained with about 640µW power consumption. Simulation results are also given in Table 3.8.

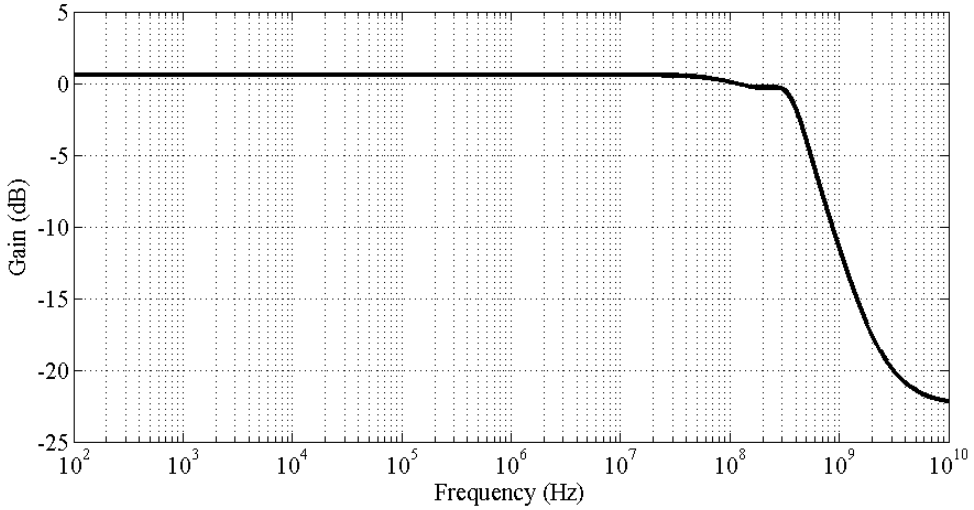

Figure 3.34. Current transfer gain between ports X and Y

Table 3.8. Simulation results of the self biased differential pair based CMOS CCI

Summary of the CCI Performance	
Supply voltage	±1.65V
Power dissipation	644µW
Voltage gain, V_X / V_Y	0.97
Voltage transfer BW	412MHz
Current gain, I_Z / I_X	1.07
Current transfer BW (α)	400MHz
Current gain, I_Y / I_X	1.07
Current transfer BW (γ)	430MHz
Offset voltage on port X	0.9mV
Offset current on port Z	2.8µA
Offset current on port Y	2.8µA
Port X resistance	3.15Ω
Port Y resistance	173kΩ
Port Z resistance	101.2kΩ

3.4.2. Third Generation Current Conveyors

Very similar to CCI, a third generation current conveyor (CCIII) is a three terminal device which ensures two functionalities between its terminals. The voltage applied to Y port is copied to X port and the current flowing through X port is copied to Y and Z ports all with unity gains. The current flowing through Y port is reversed in a CCIII. In mathematical terms, the port relations of a CCI are described by:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -\gamma & 0 \\ \beta & 0 & 0 \\ 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{3.13}$$

Fig. 3.35 shows the complete real equivalent model of the CCIII which take into account the non-ideal characteristics at three ports, the capacitive parasitic impedances on Y and Z nodes and also non-perfect voltage and current follower parameters α, β and γ.

The controlled current sources $\gamma.I_x$ at port Y and $\alpha.I_x$ at port Z copy the current of port X. The difference between the CCI and the CCIII is the direction of the current on port Y.

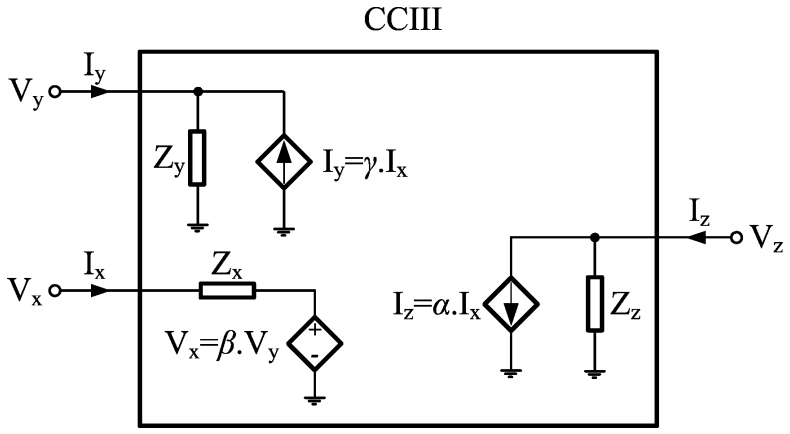

Figure 3.35. CCIII+ equivalent model

3.4.2.1. Current Follower Stage between Ports X and Y

The circuit to reverse the current on port Y is shown in Fig. 3.36. Cross coupled current mirror transistors, M_{19}-M_{22}, copy and change the direction of the current on X port with a gain very close to unity. The circuit which is used for current buffering between ports X and Z is very similar to the circuit in Fig. 3.22 with the similar analytical expressions. The complete schematic of the self biased differential pair based CMOS CCIII circuit is shown in Fig. 3.37.

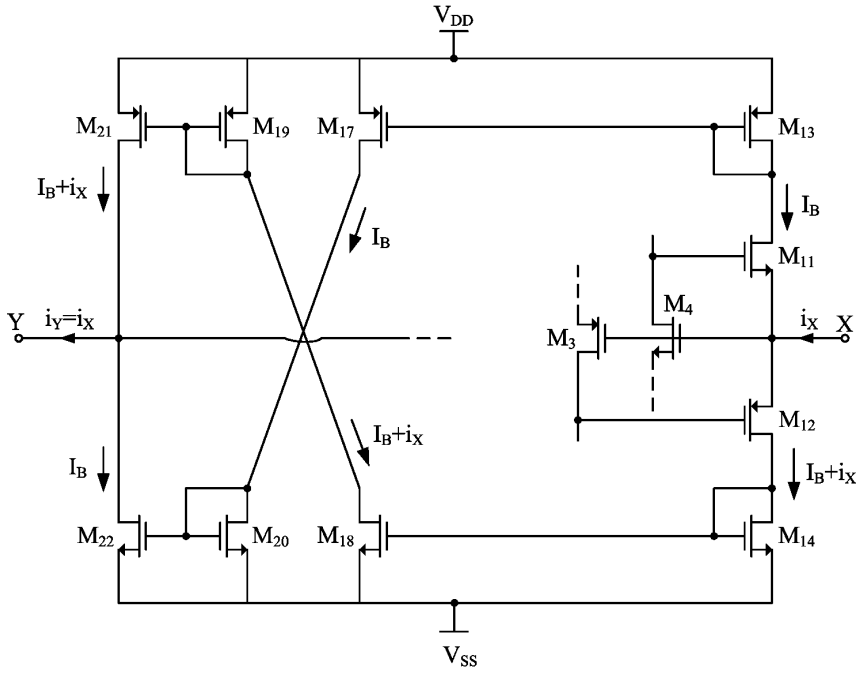

Figure 3.36. Inverting current follower stage between ports X and Y

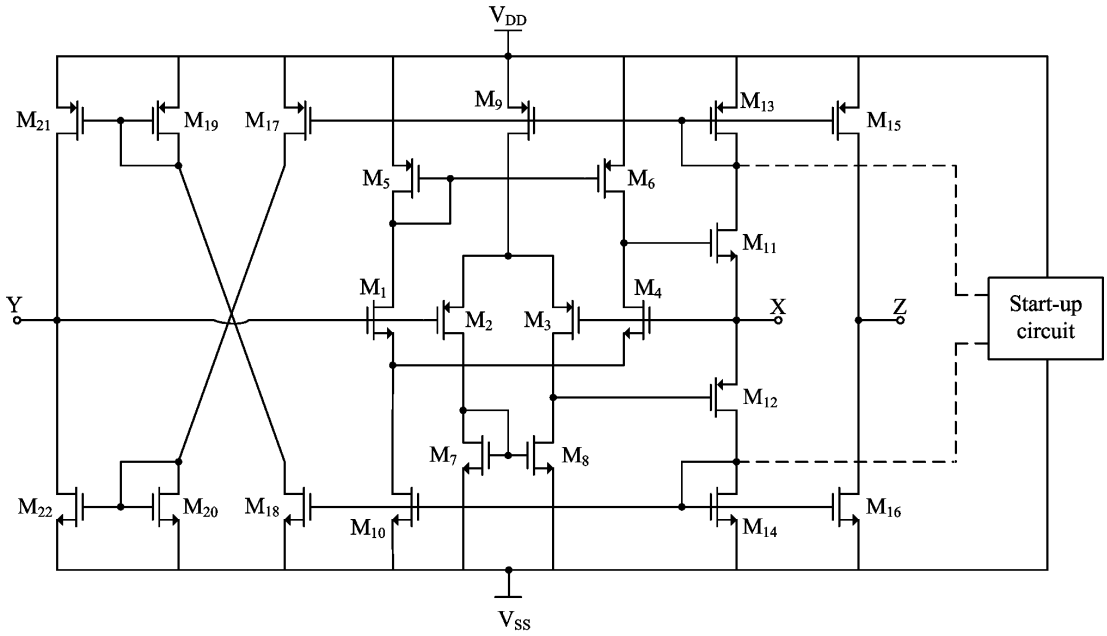

Figure 3.37. Self biased differential pair based CMOS CCIII

3.4.2.2. Simulation Results

The characteristics of the proposed circuit have been determined from HSpice simulations by using AMS 0.35μm, 3.3V process parameters. Neither voltage nor current

biasing sources are used during simulations. The current flowing through differential pairs is about 25µA. Aspect ratios of the transistors are given in Table 3.9.

Table 3.9. Aspect ratios

Transistor	**W[µm]/L[µm]**
M_{10}, M_{14}, M_{16}, M_{18}, M_{20}, M_{22}	10/0.5
M_7, M_8	20/0.35
M_1, M_4	20/0.5
M_{11}	30/0.35
M_9, M_{13}, M_{15}, M_{17}, M_{19}, M_{21}	30/0.5
M_5, M_6	60/0.35
M_2, M_3	60/0.5
M_{12}	90/0.35
M_{p1}	20/0.5
M_{p2}, M_{sp}, M_{sn}	1/5
M_{n1}	20/5

In order to have high impedance values at ports Y and Z, lengths of transistors M_{13}-M_{22} are selected as 0.5µm. The proposed CCIII circuit is derived from the self biased CCII circuit which is given in Fig. 3.23 by adding the cross coupled current mirror transistors, M_{17}-M_{22}, to copy and invert the current of port X.

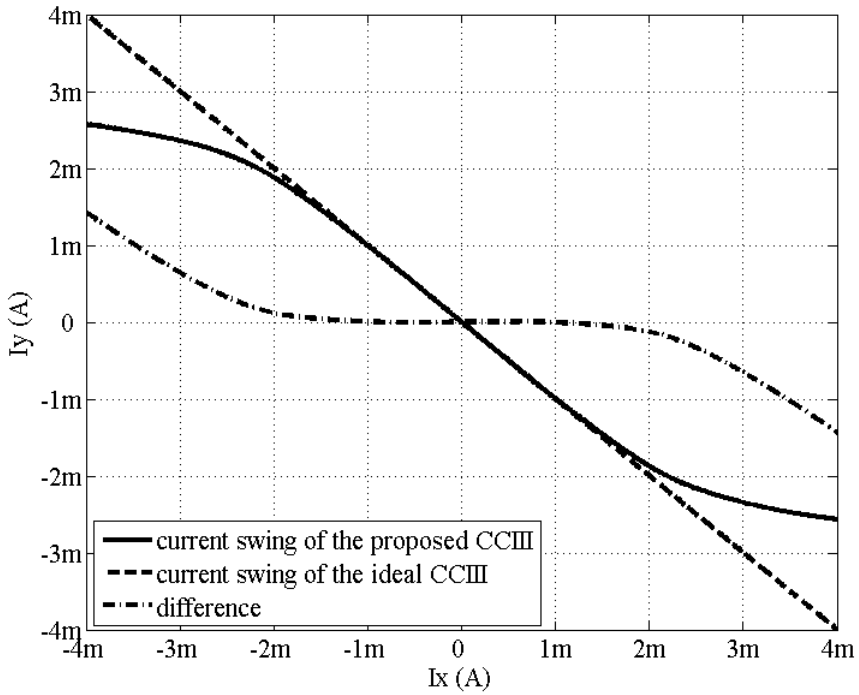

Figure 3.38. DC current transfer characteristics for the inverting current follower stage

In Fig. 3.38 the linear operation region of the inverting current follower stage between ports X and Y is given. The offset current flowing through port Y is 4.3µA when port X is grounded. The current follower stage has a linear current swing between ±2mA with less than ±5% error. Fig. 3.39 illustrates the AC transfer characteristic of the inverting current follower stage. The current transfer ratio between ports X and Y, γ, is found to be 1.1 and a bandwidth of 280MHz is obtained with about 971µW power consumption. Simulation results are also given in Table 3.10.

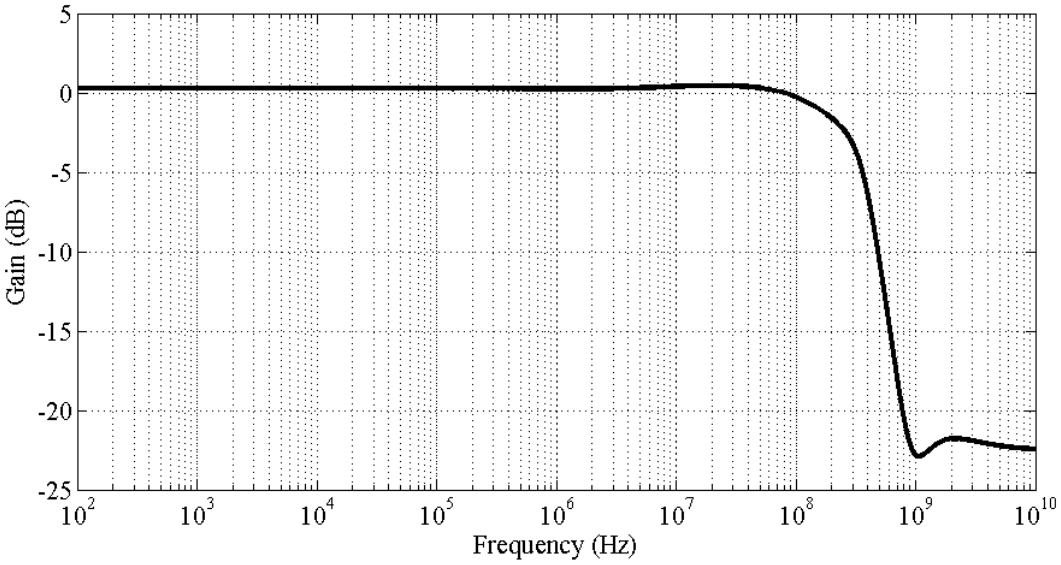

Figure 3.39. Current transfer gain between ports X and Y

Table 3.10. Simulation results of the self biased differential pair based CMOS CCIII

Summary of the CCIII Performance	
Supply voltage	±1.65V
Power dissipation	971µW
Voltage gain, V_X / V_Y	0.97
Voltage transfer BW	412MHz
Current gain, I_Z / I_X	1.07
Current transfer BW (α)	400MHz
Current gain, I_Y / I_X	1.1
Current transfer BW (γ)	280MHz
Offset voltage on port X	0.9mV
Offset current on port Z	2.8µA
Offset current on port Y	4.3µA
Port X resistance	3.15Ω
Port Y resistance	135kΩ
Port Z resistance	101.2kΩ

3.5. Comparison Results

In this section, the proposed circuits are compared with some previously proposed translinear-loop based [14] and differential pair based [17-19] circuits from the literature. A fair comparison criterion is adopted while designing the CMOS CCII circuits. This criterion has the following constraints [23]. Firstly, all the CCII circuits operate under the same supply voltages of ±1.65V. Secondly, aspect ratios of the equivalent transistors are equal and equivalent current sources are identical. The reference DC current source is taken as 25μA. Thirdly, the same model is used for all the circuits. HSpice simulations were carried out with AMS 0.35μ, 3.3V technology parameters. Port Z is grounded in all simulations, port X is open circuited while simulating the voltage transfer characteristics and port Y is grounded while simulating the current transfer characteristics. The comparison results are given in Table 3.11. Simulation results indicate that the designed circuits have superior performance compared to previous CCII designs.

Table 3.11. Comparison results of the CMOS CCIIs

Parameter	**CCIIs from literature**				**Proposed CCIIs**		
	[14]	[17]	[18]	[19]	Fig. 3.3	Fig. 3.13	Fig. 3.23
Type of the CCII	Trans-linear	Diff.	Diff.	Diff.	Diff.	Diff.	Diff.
Supply voltage, [V]	±1.65	±1.65	±1.65	±1.65	±1.65	±1.65	± 1.65
Biasing current, [μA]	25	25	25	25	25	25	25
Power dissipation, [μW]	357	392	362	466	670	740	650
Voltage gain, V_X / V_Y	0.97	0.93	0.99	0.96	0.97	0.96	0.97
Voltage transfer BW, [MHz]	520	263	235	420	475	550	440
Voltage swing on port X, [V]	±0.60	+0.6 -1.3	±1.4	+1.5 -0.9	±1.1	±1.1	±1.1
Current gain, I_Z / I_X	1.11	1.11	1.08	1.06	1.08	0.99	1.07
Current transfer BW, [MHz]	295	400	410	420	430	575	400
Port X resistance, [Ω]	1.58k	125	177	189	33.2	1.6	0.51
Noise current at 10MHz, [pA/√Hz]	3.4	3.5	3.4	6.4	3.8	4.7	3.6
Noise voltage at 10MHz, [nV/√Hz]	9.1	16.6	12.6	24.1	10.4	7.3	7.7

4. NOISE ANALYSIS

In this chapter, noise analysis of the proposed CMOS CCII circuits is performed. Input referred noise voltage at high-impedance port Y and input referred noise current at low impedance port X are obtained to form the noise model of the CCII. Using the analytical noise equations, which are formed by the g_m values of the transistors, some techniques are advised in order to reduce the noise values. For the proposed circuits, it is shown that using current gains greater than unity results in high noise reductions.

4.1. Definition and Types of Noise

Noise can be defined as any random interference unrelated to the signal of interest. This definition distinguishes between noise and deterministic phenomena such as harmonic distortion and intermodulation. As other random processes, noise is characterized by a probability density function (PDF) and a power spectral density (PSD). Analog signals processed by integrated circuits are corrupted by two different types of noise: device electronic noise and environmental noise. The latter refers to random disturbances that a circuit experiences through the supply or ground lines or through the substrate [28-30].

4.1.1. Thermal Noise

Thermal noise, which always exists at non-zero temperatures, originates from vibrations of the lattice atoms which are transferred to the free electrons. The electrons are thus performing an unsteady movement, being interrupted by collisions. This unsteady movement leads to an irregularly fluctuating voltage between both ends of the conductor. It will be seen that the available noise power of a resistor only depends on the absolute temperature of the resistor. The thermal noise is thus especially well suited to serve as a reference noise source. It is a relatively weak noise phenomenon which can be further reduced by cooling. For many systems it is often sufficient, if the overall noise, referred to the input of the system, is of a similar level as the thermal noise [30-33].

4.1.1.1. Resistor Thermal Noise

If the electrical resistance of a conductor is R, the noise power can be expressed in terms of the mean square noise voltage between the terminals of the resistor, or the mean square noise current flowing through the resistor as [29]:

$$P_n = \overline{v_n^2} \times \frac{1}{R} \text{ or } P_n = \overline{i_n^2} \times R \tag{4.1}$$

For what concerns the thermal noise, we have:

$$\overline{v_n^2} = 4kTR\left[V^2/Hz\right] \text{ or } \overline{i_n^2} = \frac{4kT}{R}\left[A^2/Hz\right] \tag{4.2}$$

where k is the Boltzman constant, T is the absolute temperature (Kelvin degrees). The polarity used for the voltage or current noise sources is unimportant because the noise is a random quantity. Nevertheless, once a polarity is chosen, it must be retained throughout the analysis of the circuit so as to obtain consistent results.

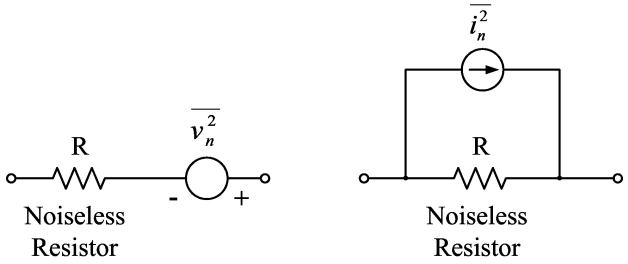

Figure 4.1. Thermal noise of a resistor

4.1.1.2. MOS Thermal Noise

MOS devices exhibit thermal noise. Thermal noise is also called white noise since its spectral density is constant over a given frequency. The thermal noise of MOS devices can be modeled as voltage source connected in series to the gate or a current source connected between the drain and the source with PSDs:

$$\overline{v_n^2} = \frac{4kT\gamma}{g_m}\left[V^2/Hz\right] \text{ or } \overline{i_n^2} = 4kT\gamma g_m\left[A^2/Hz\right] \tag{4.3}$$

where k is the Boltzman constant, T is the absolute temperature (Kelvin degrees) and g_m is the transconductance of the transistor. The parameter γ has a value of unity at zero drain–source voltage V_{DS}, and decreases towards a value of 2/3 in saturation in long channel devices [34].

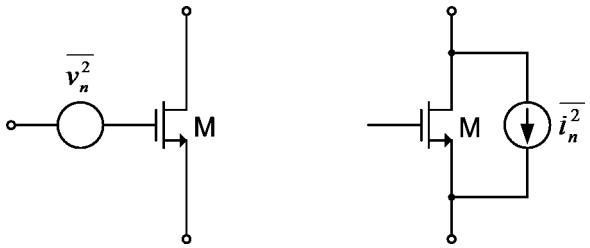

Figure 4.2. Thermal noise of a MOSFET

4.1.2. Flicker Noise

The electrical properties of surfaces or boundary layers are influenced energetically by so-called boundary layer states, which are also subject to statistical fluctuations. This leads to the so-called flicker noise or l/f noise for the current flow. Flicker noise arises due to random trapping of charge at the oxide-silicon interface of MOSFETs. This kind of noise is especially observable at low frequencies and generally decreases with increasing frequency f according to a l/f law until it is covered by frequency-independent noise mechanisms, e.g. thermal noise or shot noise. It will be seen, that flicker noise is of great importance for high-frequency oscillators, because it can modulate the carrier frequency by non-linear processes. Unwanted amplitude and phase fluctuations with a flicker noise characteristic will, therefore, be impressed on the oscillator signal. While the effect of flicker noise may seem negligible at high frequencies, we must note that nonlinearity or time variance in circuits such as mixers or oscillators can translate the 1/f - shaped spectrum to the RF range.

There exist two models for flicker noise: Spice2 flicker noise model and BSIM3 flicker noise model. For Spice2 model, the flicker noise is equal to [34]:

$$\overline{v_n^2} = \frac{KF}{2C_{OX}WLK'}\frac{1}{f}\left[V^2/Hz\right] \text{ or } \overline{i_n^2} = \frac{KFI_D}{C_{OX}L^2}\frac{1}{f}\left[A^2/Hz\right] \tag{4.4}$$

where KF and K′ are process-dependent parameters, C_{ox} is the unity gate capacitance and W and L are transistor sizes. For BSIM3 model, it is equal to:

$$\overline{i_n^2} = \frac{v_t q^2 I_{ds}\mu_{eff}}{f^{Ef}L_{eff}^2 C_{OX}10^8}\left[N_{oia}\,log\left(\frac{N_o + 2\times10^{14}}{N_l + 2\times10^{14}}\right) + N_{oib}\left(N_o - N_l\right) + 0.5N_{oic}\left(N_o^2 - N_l^2\right)\right] + \frac{v_t I_{ds}^2 \Delta L_{clm}}{f^{Ef}L_{eff}^2 W_{eff}10^8}\frac{N_{oia} + N_{oib}N_l + N_{oic}N_l^2}{\left(N_l + 2\times10^{14}\right)^2} \tag{4.5}$$

where v_t is the thermal voltage, μ_{eff} is the effective mobility at the given bias condition, L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source given by:

$$N_o = \frac{C_{OX}\left(V_{GS} - V_{TH}\right)}{q} \tag{4.6}$$

The parameter N_l is the charge density at the drain given by:

$$N_l = \frac{C_{OX}\left(V_{GS} - V_{TH} - V_{DS}'\right)}{q} \tag{4.7}$$

$$V_{DS}' = MIN\left(V_{DS}, V_{DSAT}\right) \tag{4.8}$$

ΔL_{clm} refers to channel length reduction due to channel length modulation (CLM). N_{oia}, N_{oib} and N_{oic} are the noise parameters.

4.1.3. Shot Noise

Another noise mechanism, which is particularly important for electronic devices, is the shot noise. The transition of electrical potential barriers is a statistical process, because the charge of the carriers, electrons or ions, is always an integer multiple of the elementary charge. Consequently, the current emitted by a cathode at constant temperature and voltage is not a pure d.c. current, rather it fluctuates around a time average. Because the emitted electrons arrive irregularly at the anode, the term shot noise became accepted for this phenomenon. A similar situation can be found for potential barriers in solid-state devices, i.e. junctions between semiconductors or between metals and semiconductors. Therefore, such junctions also show shot noise for the current flowing. In general, shot noise has the smaller available noise power compared to the thermal noise [30, 43].

4.1.4. Avalanche Noise

Very high noise is generated by a semiconductor junction operated at breakdown. This noise mechanism is called avalanche noise. Accelerated electrons generate new electron-hole pairs by collision. In particular, the electrons are able to generate further electron-hole pairs after acceleration, so that the current increases very rapidly. In low-noise devices breakdown must be strictly avoided. On the other hand calibrated noise sources utilize the breakdown mechanism of a pn- or Schottky-junction in order to achieve a high well-defined noise power for measurement purposes [30, 43, 44].

4.1.5. Burst Noise

Burst noise, also called pop-corn noise, impulse noise or bi-stable noise, is related to imperfections in semiconductor material and heavy ion implants. It is characterized by discrete high-frequency pulses. The pulse rates may vary, but the amplitudes remain constant at several times the thermal noise amplitude. Burst noise makes a popping sound at rates below 100 Hz when played through a speaker, it sounds like popcorn popping, hence the name. Low burst noise is achieved by using clean device processing, and therefore is beyond the control of the designer [43, 44].

4.1.6. Transit Time Noise

In semiconductor devices, the transit time is the time taken by the carriers to cross a junction. The periodic time of the signal is equal to reciprocal of signal frequency. When the signal frequency is high, periodic time becomes very small and hence may be comparable to transit time of carriers. In such situation, some of the carriers may diffuse back to the source, i.e. emitter. Due to this, conductance component of input admittance increases with frequency. This conductance has associated with a noise current generator. Since the conductance increases with frequency, the noise spectrum density increases at high frequencies [42].

4.1.7. Induced Gate Noise

The noise at the gate of a FET is very important when the FET is used as the input device of an amplification stage. The referred back to the gate channel noise is composed by the narrow band excessive noise mechanisms along with the wide band thermal noise fluctuations in the channel. For MOSFETs, because of the absence of a D.C. gate current, the gate noise is dominated by the referred back to the gate wide band noise produced in the channel (the noise of the drain current). Existing models, such as BSIM3 and BSIM4, are based on the Van der Ziel model and underestimate the induced gate noise for short channel devices. At the RF-frequencies used, besides the drain current thermal noise also the induced gate noise plays an important role.

It was shown by van der Ziel that the gate noise of a FET is [43-45]:

$$\overline{i_{ng}^2} = 4kT\frac{\delta\omega^2 C_{GS}^2}{5g_m} \tag{4.9}$$

where k is the Boltzman constant, T is the absolute temperature (Kelvin degrees) and δ is a bias-dependent factor of a MOSFET.

Gate-to-source capacitance (C_{GS}) has two contributors: the overlap capacitance due to the overlap between the gate and the source and the intrinsic capacitance which depends on the operating mode of the device. In saturation mode, C_{GS} is equal to:

$$C_{GS} = C_{GSO}W + \frac{2}{3}C_{ox}WL \tag{4.10}$$

C_{GSO} parameter depends on the technology and account for the overlap capacitance per unit width. C_{OX} is the value of the capacitance per unit area in the active region.

The transconductance, g_m, can be expressed as:

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \tag{4.11}$$

From (4.11):

$$W = \frac{g_m^2 L}{2\mu_n C_{ox} I_D} \tag{4.12}$$

Substituting (4.10) and (4.12) in (4.9) and simplifying, we get:

$$\overline{i_{ng}^2} = \frac{1}{5}kT\frac{\delta\left(C_{GSO} + \frac{2}{3}C_{OX}L\right)^2}{\mu_n^2 C_{ox}^2 I_D^2}\omega^2 L^2 g_m^3 \tag{4.13}$$

It is seen that, the induced gate noise strongly depends on the device dimensions and especially the g_m value of the transistor.

4.1.8. Noise Figure

In many analog circuits, the signal to noise ratio (SNR), defined as the ratio of the signal power to the total noise power, is an important parameter. In RF design, on the other

hand, even though the ultimate goal is to maximize the SNR for the received and detected signal, most of the front-end receiver blocks are characterized in terms of their "noise figure" (NF) rather than the input-referred noise. This is partly for computational convenience and partly from tradition. NF has been defined in a number of different ways. The most commonly accepted definition is [29-30]:

$$NF = \frac{SNR_i}{SNR_o} \tag{4.14}$$

where SNR_i and SNR_o are the signal to noise ratios measured at the input and output, respectively. Thus the NF of a network is the decrease or degradation in the SNR as the signal goes through the network. A perfect amplifier would amplify the noise at its input along with the signal, maintaining the same signal-to-noise ratio at its input and output (the source of input noise is often thermal noise associated with the earth's surface temperature or with losses in the system). A realistic amplifier, however, also adds some extra noise from its own components and degrades the SNR. A low noise figure means that very little noise is added by the network. The concept of noise figure only fits networks (with at least one input and one output port) that process signals. This note is mainly about two-port networks; although mixers are in general three-port devices, they are usually treated the same way as a two-port device with the local oscillator connected to the third port.

The output signal (S_o) is equal to the input signal (S_i) times the gain: $S_o = S_i \times G$. The output noise is equal to the noise delivered to the input (N_i) from the source plus the input noise of the device (N_a) times the gain: $N_o = (N_i + N_a) \times G$. Substituting into (4.14) and simplifying, we get:

$$NF = \frac{SNR_i}{SNR_o} = \left[\frac{S_i / N_i}{\dfrac{G \times S_i}{G(N_i + N_a)}} \right] = 1 + \frac{N_a}{N_i} \tag{4.15}$$

Once the input spectral density of the device has been determined, it is a simple matter to calculate the NF.

4.2. Representation of Noise in Circuits

In a general two port circuit as shown in Fig. 4.3, the natural approach of quantifying the effect on noise would be to set the input to zero and calculate the total noise at the output, or output referred noise, due to various sources of noise in the circuit. This is indeed the way to simulate the noise or measure it in the laboratory [29].

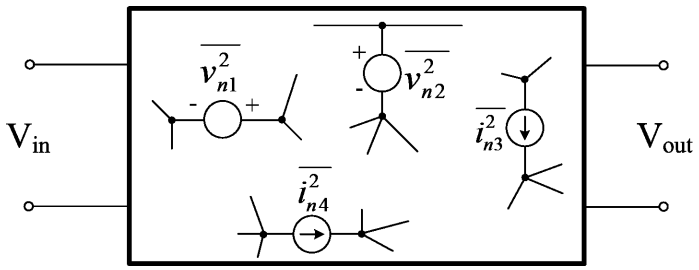

Figure 4.3. Two port network with noise sources

While intuitively appealing, the output-referred noise does not allow a fair comparison of the performance of different circuits because it depends on the gain. Forming the noise model by using the input-referred noise sources, allows both a fair noise comparison and easier NF calculation as shown in (4.14). The input-referred noise and the input signal are both multiplied by the gain as they are passing through the circuit. Thus, the input-referred noise indicates how much the input signal is corrupted by the circuit's noise, i.e. how small an input the circuit can detect with acceptable SNR. For this reason input-referred noise allows a fair comparison of different circuits. If the circuit has finite input impedance, modeling the input-referred noise by only a voltage source shows that the output noise vanishes as the source impedance becomes large. To resolve this issue, the circuit must be modeled by a series voltage source and a parallel current source, as shown in Fig. 4.4, so that if the output impedance of the preceding stage has large values, the noise current source still flows through the finite impedance, thus producing noise at the input of the circuit.

Generally, an equivalent input noise source or generator is obtained by evaluating the output noise and dividing it by the gain of the circuit. For high-gain amplifiers, this leads to

the well-known characteristic of input transistors as main contributors to noise. In contrast, CCIIs are made up of two followers, therefore we expect all the transistors to contribute to noise to a similar extent. The evaluation of the output noise is further complicated by the fact that a CCII is a three-terminal device where port X acts as an input and output terminal at the same time. Therefore, care must be taken when evaluating the equivalent output voltage noise at port X, to separate the component due to noise voltage from that due to noise current.

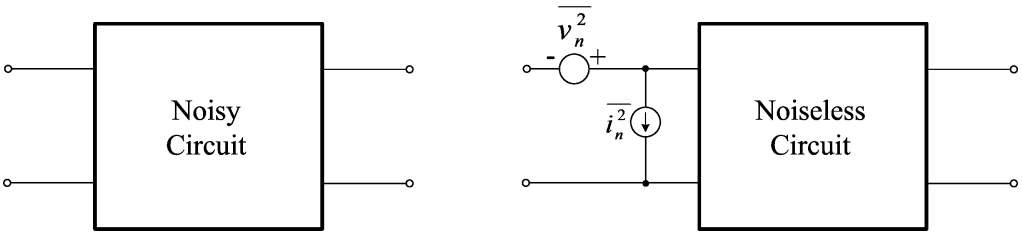

Figure 4.4. Two port network with input referred noise sources

4.3. Noise Analysis of the Proposed Circuits

In this section, noise analysis of the proposed CMOS CCII circuits is studied. Input referred noise voltage at high impedance node Y and input referred noise current at low impedance node X are obtained to form the noise model. Using the analytical noise equations, some techniques are advised in order to reduce the noise values.

4.3.1. The Noise Model

An important performance parameter of CCIIs is noise. In general, noise in a CCII can be completely modeled by three noise generators as shown in Fig. 4.5. Note that noise voltage is only associated with the Y port since any noise voltage in series with the X port can be directly transferred to the Y port. Moreover, any noise current in parallel with the Z port can be directly transferred to the X port. Hence X port is characterized by only one current noise generator. In a conveyor employed as the input stage of a current mode amplifier, the Y port is always grounded. In addition, especially for the differential pair based CCIIs, the input impedance on port Y is extremely high, so the equivalent current

noise source at Y port can be neglected [3, 29-30]. In this case the noise model can be simplified by omitting the current noise generator on Y port. Hence, the noise model in Fig. 4.5 reduces to a simpler model given in Fig. 4.6.

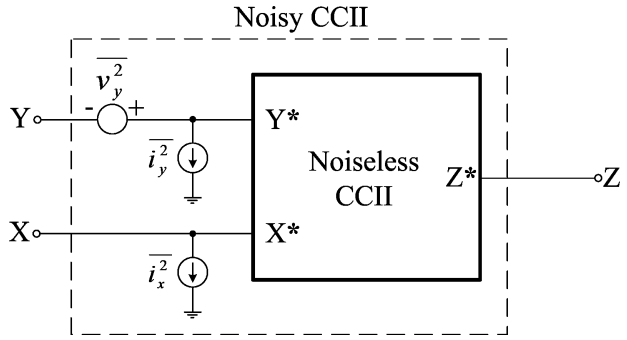

Figure 4.5. Current conveyor with equivalent noise generators

A previous study [34] gives some design guidelines for the noise evaluation in differential pair based CCIIs. It evaluates the input equivalent noise components using the well known quantities and the g_m values of the transistors. A useful and simple noise model of the current conveyor includes noise generators referred to X and Y nodes as shown in Fig. 4.5. Especially for the differential pair based CCIIs, the input impedance on Y node is extremely high, so the equivalent current noise source at Y node can be neglected [3, 34].

There are two methods of representing the input-referred noise sources at ports X and

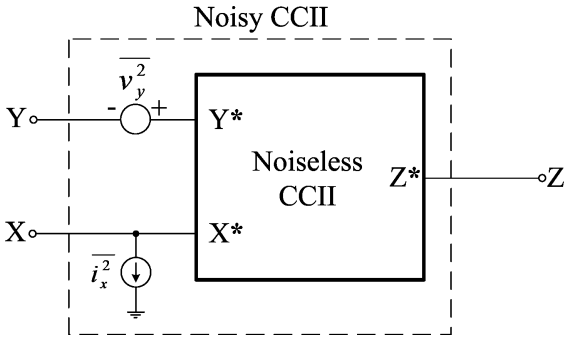

Figure 4.6. Current conveyor with simplified noise model

Y. One method is the use of noise voltage generators attached to the gates of the transistors and the other one is the use of noise current generators connected between the drains and the sources. Both of the methods give the same results and they will be applied

individually in order to obtain the noise models. The CMOS CCII circuit in Fig. 3.3 is selected for the noise evaluation.

4.3.2. Thermal Noise Evaluation Using Current Noise Sources

Thermal noise analysis will be carried out for each stage and then overall noise generators will be calculated considering the connected blocks of the conveyor circuit. The first block considered is the input differential pair. It is important to note that, noise due to biasing transistors of the rail-to-rail stage is cancelled by symmetry and matching. Only devices on the signal path are important. The noise analysis of the input stage is based on the individual noise determination of each differential block and then overall noise determination using the connection of these two block in parallel which form the rail-to-rail stage of the proposed circuit. NMOS and PMOS input differential pairs are shown in Fig. 4.7 and Fig. 4.8 with the related current noise generators.

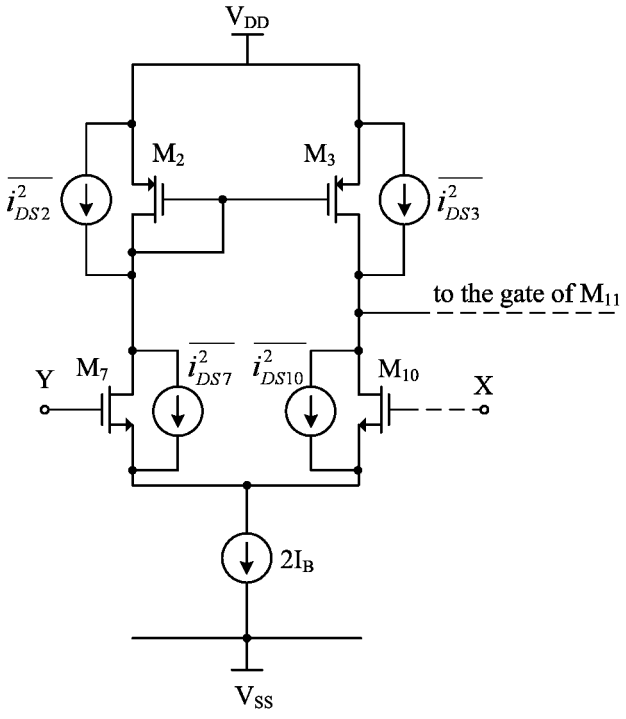

Figure 4.7. NMOS input differential pair with related noise current sources

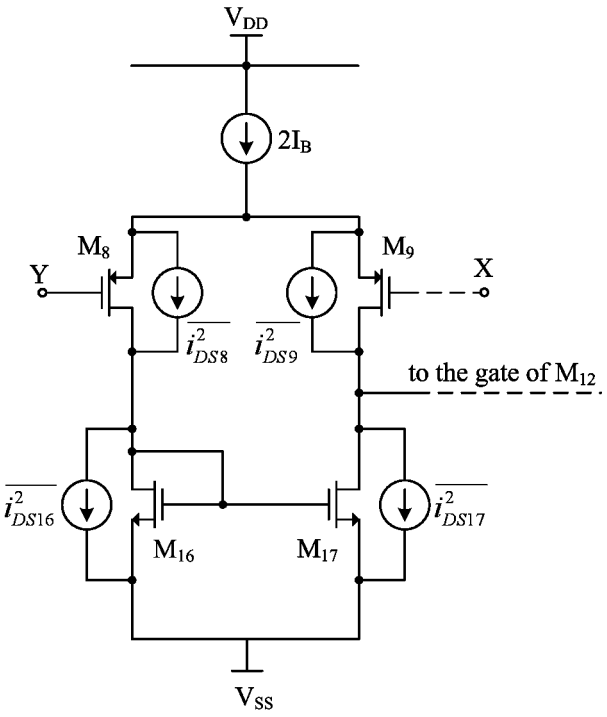

Figure 4.8. PMOS input differential pair with related noise current sources

The calculation of equivalent noise values at Y port is done with the help of nodal equations. For the NMOS input differential pair, the equivalent input noise value at Y port is equal to:

$$\overline{v_{yN}^2} = \frac{\overline{i_{DS2}^2} + \overline{i_{DS3}^2} + \overline{i_{DS7}^2} + \overline{i_{DS10}^2}}{g_{m10}^2} \tag{4.16}$$

Using the thermal noise equation:

$$\overline{i_{DSn}^2} = 4kT\gamma g_{mn} \tag{4.17}$$

(4.16) can be rewritten as:

$$\overline{v_{yN}^2} = 4kT\gamma\left(\frac{g_{m2} + g_{m3} + g_{m7} + g_{m10}}{g_{m10}^2}\right) \tag{4.18}$$

If the transistors are perfectly matched and they carry equal amount of current, then transconductances of the matched transistors will be equal:

$$g_{m2} = g_{m3} \text{ and } g_{m7} = g_{m10} \tag{4.19}$$

Then (4.18) will have a simplified form as:

$$\overline{v_{yN}^2} \cong 4kT\gamma\left[\frac{1}{g_{m10}}\left(2 + 2\frac{g_{m2}}{g_{m10}}\right)\right] \tag{4.20}$$

It is important to note that, transistors M_2, M_3 and M_{16}, M_{17} contribute to noise, whilst the noise terms due to M_{11} and M_{12} are suppressed by the local feedback formed by M_{10}, M_{11} and M_9, M_{12}. Very similar to NMOS input differential pair, the PMOS input differential pair has a thermal noise at Y port which is equal to:

$$\overline{v_{yP}^2} = \frac{\overline{i_{DS8}^2} + \overline{i_{DS9}^2} + \overline{i_{DS16}^2} + \overline{i_{DS17}^2}}{g_{m9}^2} \tag{4.21}$$

Transistors M_8, M_9 and M_{16}, M_{17} are matched and they have equal currents, so:

$$g_{m8} = g_{m9} \text{ and } g_{m16} = g_{m17} \tag{4.22}$$

(4.21) can be rewritten in a simpler form as:

$$\overline{v_{yP}^2} \cong 4kT\gamma\left[\frac{1}{g_{m9}}\left(2 + 2\frac{g_{m16}}{g_{m9}}\right)\right] \tag{4.23}$$

The total noise voltage at port Y is the combination of thermal noises of NMOS and PMOS input differential pairs, with the assumption that they are all uncorrelated:

$$\overline{v_y^2} \cong 4kT\gamma\left[\frac{1}{g_{m9,10}}\left(1 + \frac{g_{m2,16}}{g_{m9,10}}\right)\right] \tag{4.24}$$

The current follower stage is shown in Fig. 4.9 with the related current noise generators. The calculation of equivalent thermal noise values at X port is also done with the help of nodal equations. On inspection, it is easy to see that only transistors M_5, M_6, M_{18} and M_{19} contribute to the noise current.

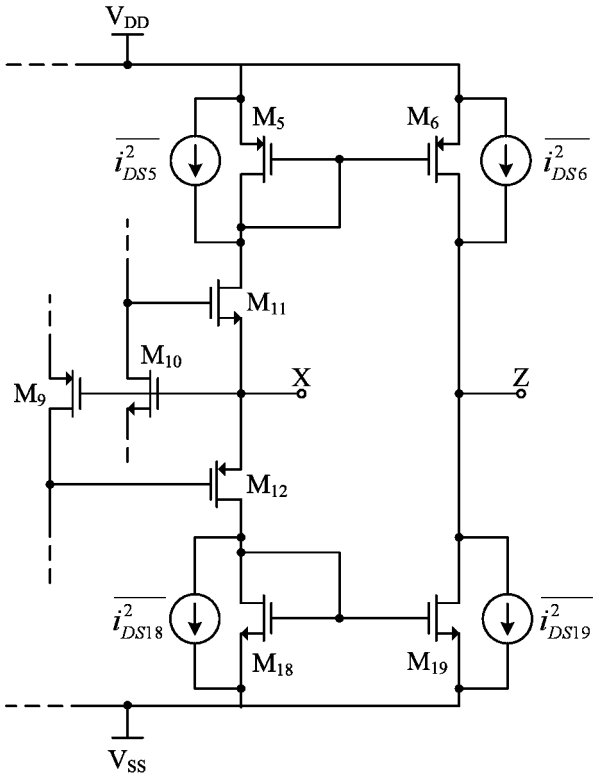

Figure 4.9. Current follower stage with related current noise sources

$$\overline{i_x^2} \cong \overline{i_{DS5}^2} + \overline{i_{DS18}^2} + \left(\frac{g_{m5}}{g_{m6}}\right)^2 \overline{i_{DS6}^2} + \left(\frac{g_{m18}}{g_{m19}}\right)^2 \overline{i_{DS19}^2} \tag{4.25}$$

$$\overline{i_x^2} \cong 4kT\gamma\left(g_{m5} + g_{m18} + \frac{g_{m5}^2}{g_{m6}} + \frac{g_{m18}^2}{g_{m19}}\right) \tag{4.26}$$

4.3.3. Thermal Noise Evaluation Using Voltage Noise Sources

Another way of evaluating the noise values is using voltage noise sources. The differential pairs with related voltage noise sources attached to the gates of the transistors are shown in Fig. 4.10 and Fig. 4.11.

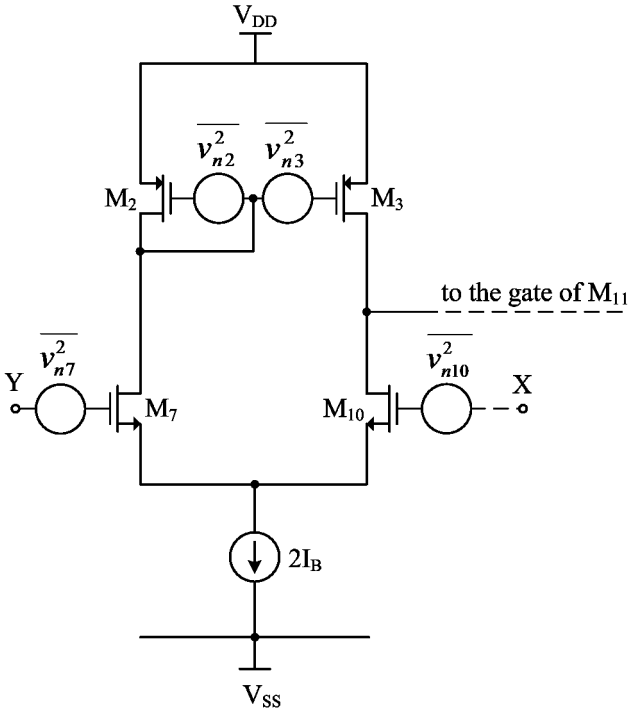

Figure 4.10. NMOS input differential pair with related voltage noise sources

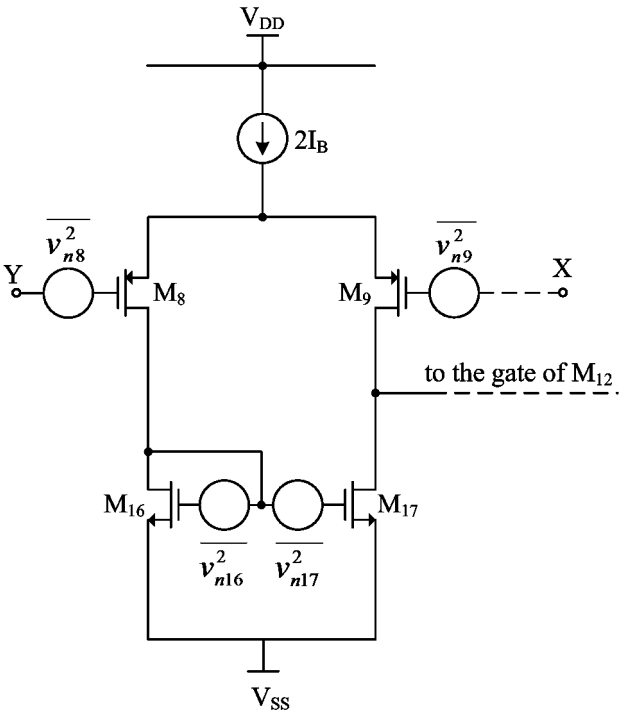

Figure 4.11. PMOS input differential pair with related voltage noise sources

The calculation of equivalent thermal noise voltage at Y port is also done with the help of nodal equations.

$$\overline{i_{yN}^2} \cong g_{m2}^2 \overline{v_{n2}^2} + g_{m3}^2 \overline{v_{n3}^2} + g_{m7}^2 \overline{v_{n7}^2} + g_{m10}^2 \overline{v_{n10}^2} \tag{4.27}$$

$$\overline{i_{yP}^2} \cong g_{m8}^2 \overline{v_{n8}^2} + g_{m9}^2 \overline{v_{n9}^2} + g_{m16}^2 \overline{v_{n16}^2} + g_{m17}^2 \overline{v_{n17}^2} \tag{4.28}$$

Because of symmetry and matching:

$$\overline{i_{yN}^2} \cong 2g_{m2}^2 \overline{v_{n2}^2} + 2g_{m10}^2 \overline{v_{n10}^2} \tag{4.29}$$

$$\overline{i_{yP}^2} \cong 2g_{m9}^2 \overline{v_{n9}^2} + 2g_{m16}^2 \overline{v_{n16}^2} \tag{4.30}$$

To refer back to the input:

$$\overline{v_{yN}^2} \cong 2\left[\overline{v_{n10}^2} + \left(\frac{g_{m2,3}}{g_{m7,10}}\right)^2 \overline{v_{n2}^2}\right] \tag{4.31}$$

$$\overline{v_{yP}^2} \cong 2\left[\overline{v_{n9}^2} + \left(\frac{g_{m16,17}}{g_{m8,9}}\right)^2 \overline{v_{n16}^2}\right] \tag{4.32}$$

The total noise voltage at port Y is the combination of thermal noises of NMOS and PMOS input differential pairs, again with the assumption that they are all uncorrelated:

$$\overline{v_y^2} \cong 4kT\gamma\left[\frac{1}{g_{m9,10}}\left(1 + \frac{g_{m2,16}}{g_{m9,10}}\right)\right] \tag{4.33}$$

As can be seen, (4.33) is equal to (4.24). The current follower stage is shown in Fig. 4.12 with the related voltage noise generators.

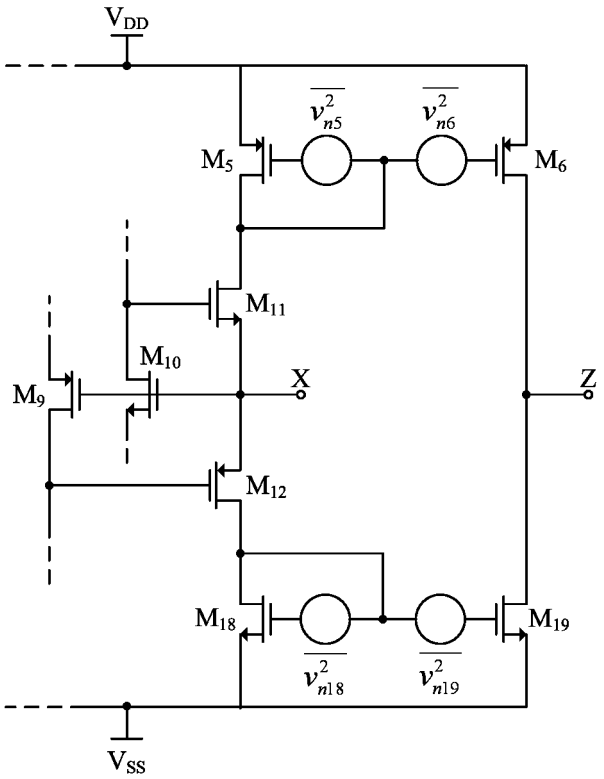

Figure 4.12. Current follower stage with related voltage noise sources

Similarly, the noise current on port X can be obtained as:

$$\overline{i_X^2} \cong g_{m5}^2 \overline{v_{n5}^2} + g_{m18}^2 \overline{v_{n18}^2} + \left(\frac{g_{m5}}{g_{m6}}\right)^2 g_{m6}^2 \overline{v_{n6}^2} + \left(\frac{g_{m18}}{g_{m19}}\right)^2 g_{m19}^2 \overline{v_{n19}^2} \tag{4.34}$$

$$\overline{i_X^2} \cong 4kT\gamma\left(g_{m5} + g_{m18} + \frac{g_{m5}^{\ 2}}{g_{m6}} + \frac{g_{m18}^{\ 2}}{g_{m19}}\right) \tag{4.35}$$

4.4. Noise Optimization

In the previous chapter, analytical expressions for the input-referred thermal noise expressions were obtained for the proposed circuits. The input-referred noise voltage at high impedance port Y and input referred noise current at low impedance port X are given in terms of the g_m values of the transistors. In this section, some noise reduction techniques are proposed, which depend on the adjustment of g_m values of the transistors. Noise analysis of current mode and voltage mode filter applications that employs the proposed

CMOS CCII circuits are studied. Input referred noise expressions for the filter applications, before and after g_m adjustment, are compared and it is shown that, with the proposed technique, very good noise reductions are obtained especially on high order filter applications.

4.5. Noise Optimization of the Proposed CCII Circuits

4.5.1. Thermal Noise Optimization at High Impedance Port Y

The input referred noise voltage at high impedance port Y was obtained as:

$$\overline{v_y^2} \cong 4kT\gamma\left[\frac{1}{g_{m9,10}}\left(1+\frac{g_{m2,16}}{g_{m9,10}}\right)\right] \tag{4.36}$$

Differential pair transistors M_7-M_{10} and active load transistors M_2-M_3 and M_{16}-M_{17} determine the noise value. In order to reduce this noise component, the input differential pairs have to be designed with high g_m transistors and the active load transistors should have smaller g_m values. The g_m values can be adjusted by changing the widths of the transistors. Increasing the width of the transistor results in an increase in the g_m value. The initial g_m values of the transistors are selected to make the CCII as close as possible to ideal CCII, i.e. to make the current and voltage gains equal to 1, maximize the bandwidth and minimize the X port parasitic input resistance.

4.5.1.1. Simulation Results

The noise voltage at Y port is simulated as shown in Fig. 4.13. Y and Z ports are

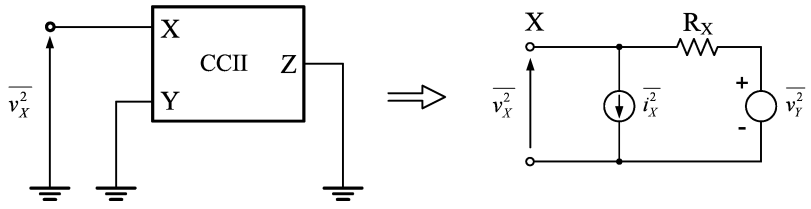

Figure 4.13. Circuit configuration to simulate the noise voltage at Y port

connected to ground and the total noise voltage at X port is evaluated. Since v_X=v_Y, the noise value at X port can be given by [34]:

$$\overline{v_X^2} = \overline{v_Y^2} + \overline{i_X^2} R_X^2 \tag{4.37}$$

R_X is the equivalent resistance at X port. From theory and simulations, it is known that the noise current value at X port (i_X) is in pA range and the noise voltage value at Y port (v_Y) is in nV range. Moreover, it is known that the value of R_X is in tens of Ω range. So the term $i_X^2 R_X^2$ can be neglected. With this assumption, the noise voltage at Y port (v_Y^2) is equal to v_X^2.

The noise current at X port is simulated using the circuit in Fig. 4.14. X and Y ports are grounded and Z port is terminated using a small valued (compared to equivalent resistance of Z port) resistance, R_{Zload}. The noise voltage at Z port is equal to:

$$\overline{v_Z^2} = \frac{R_Z^2}{\left(R_Z + R_{Z,load}\right)^2} R_{Z,load}^2 \overline{i_Z^2} \tag{4.38}$$

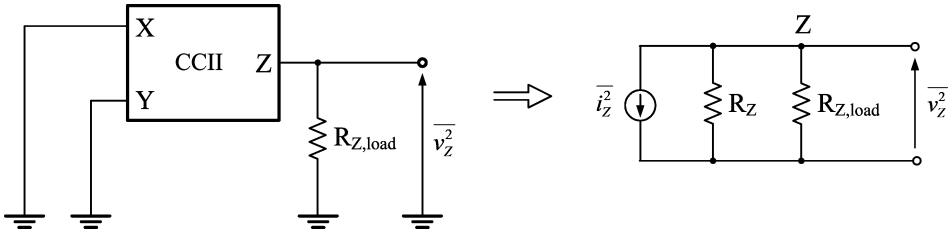

Figure 4.14. Circuit configuration to simulate the noise current at X port

Being the load resistance ($R_{Z,load}$) much lower than parasitic resistance at port Z (R_Z), it can be assumed that all the current noise flows through $R_{Z,load}$, so the measured voltage divided by $R_{Z,load}$ gives the value of the noise current at *Z* port. Since i_Z=i_X, the noise current flowing through X port is equal to:

$$\overline{i_X^2} = \frac{\overline{v_Z^2}}{R_{Z,load}^2} \tag{4.39}$$

The simulation results for the input-referred noise voltage at high impedance port Y, before and after g_m adjustment, are given. During hand calculations, it is assumed that the noise sources are uncorrelated. The theoretical noise expressions are compared with the simulated counterparts and the comparison results are shown in Table 4.1. It is observed that, theoretical results are in very good agreement with simulations. A thermal noise voltage contribution of about 11.52nV/√Hz is obtained by simulation. This value is obtained as 10.41nV/√Hz analytically with only 9.63 % error.

Table 4.1. Noise values at high impedance port Y

Noise Value	Calculated	Simulated	Difference
$\overline{v_y^2}$ (nV/√ Hz)	10.41	11.52	9.63 %

Equations 4.23 through 4.32 show that it is possible to decrease the noise value by adjusting the g_m values of the related transistors. The contribution of the differential pair transistors when determining the input referred thermal noise value is dominant when compared to the active load transistors. If the g_m values of the differential pair transistors are increased and the g_m values of the active load transistors are reduced a noise reduction can be obtained. As the widths of the differential pair transistors increase, the voltages at their respective sources also increase. Increasing the g_m values more than a certain value drives the transistors into cut-off region; because their V_{GS} voltages fall below the threshold voltage. The simulation results before and after the g_m adjustments are given in

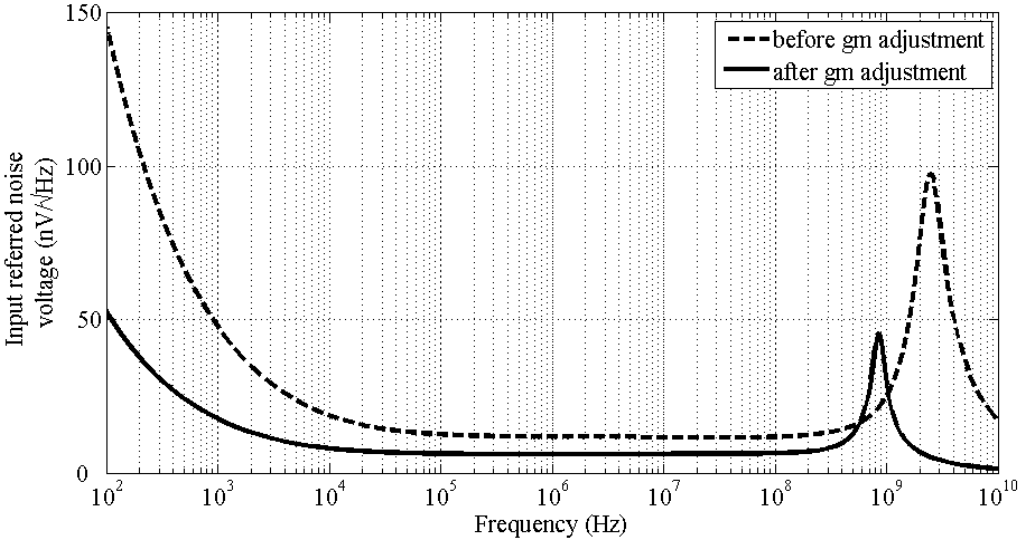

Figure 4.15. Noise voltage at high impedance port Y

Fig. 4.15. The results are also given in Table 4.2. It is shown that, by adjusting the g_m values of the transistors, the input referred noise voltage is decreased from 11.52nV/√Hz to 6.07nV/√Hz which means about 47% reduction.

Table 4.2. Noise values at port Y before and after g_m optimization

Noise Value		Before g_m optimization	After g_m optimization	Reduction
$\overline{v_y^2}$ (nV/√ Hz)	Calculated	10.41	5.65	45.73 %
	Simulated	11.52	6.07	47.31 %

4.5.2. Thermal Noise Optimization at Low Impedance port X

The input referred noise current at low impedance port X was obtained as:

$$\overline{i_X^2} \cong 4kT\gamma\left(g_{m5} + g_{m18} + \frac{g_{m5}^{\ 2}}{g_{m6}} + \frac{g_{m18}^{\ 2}}{g_{m19}} \right) \tag{4.40}$$

Mirror transistors M_5-M_6 and M_{18}-M_{19} determine the noise value at low impedance port X. In order to reduce this noise component, the transistors that form the high impedance port Z, M_6 and M_{19}, have to be designed with higher g_m values and the mirror transistors M_5 and M_{18} with smaller g_m values. The g_m values can be adjusted by changing the widths of the transistors. Increasing the width of the transistor results in an increase in the g_m value. The initial g_m values of these transistors are selected to ensure the current gain equal to 1, maximize the equivalent impedance on port Z and also maximize the current transfer bandwidth. A careful g_m adjustment of mirror transistors M_5, M_6 and M_{18}, M_{19} must be made; because both the values of parasitic impedances at ports X and Z and also the current transfer bandwidth depend on these transistors.

Thermal noise optimization at port X is done by adjusting the g_m values of the transistors. As mentioned before, g_m adjustment is done by decreasing or increasing the widths of the transistors. By doing this adjustment, it is important to note that, the values of

the other two noise components, flicker noise and induced gate noise, are also changed. The induced gate noise of a transistor is equal to:

$$\overline{i_{ng}^2} = \frac{1}{5}kT\frac{\delta\left(C_{GSO}+\frac{2}{3}C_{OX}L\right)^2}{\mu_n^2 C_{ox}^2 I_D^2}\omega^2 L^2 g_m^3 \tag{4.41}$$

It depends strongly on the frequency, device dimensions and also the g_m value of the transistor. The input referred noise current at low impedance port X was determined especially by the g_m values of the transistors M_5 and M_{18}. Reducing the g_m values of these transistors not only decreases the value of the thermal noise but also decreases the value of the induced gate noise rapidly. It is clearly observed from (4.41) that, for the fixed values of L, I_D and ω, halving g_m decreases the induced gate noise 8 times.

On the other hand, the flicker noise component is inversely proportional to W_{eff}, or g_m, as given in (4.42).

$$\begin{aligned}\overline{i_n^2} = {} & \frac{v_t q^2 I_{ds}\mu_{eff}}{f^{Ef}L_{eff}^2 C_{OX}10^8}\left[N_{oia}\,log\left(\frac{N_o+2\times10^{14}}{N_l+2\times10^{14}}\right)+N_{oib}\left(N_o-N_l\right)+0.5N_{oic}\left(N_o^2-N_l^2\right)\right] \\ & +\frac{v_t I_{ds}^2 \Delta L_{clm}}{f^{Ef}L_{eff}^2 W_{eff}10^8}\frac{N_{oia}+N_{oib}N_l+N_{oic}N_l^2}{\left(N_l+2\times10^{14}\right)^2}\end{aligned} \tag{4.42}$$

Charge densities N_l and N_o, which are given in equations (4.6) and (4.7), depend on the overdrive voltages. Decreasing the g_m values of M_5 and M_{18} increases the overdrive voltages; because the currents of these two transistors remain unchanged during g_m adjustment. As a result, the increase in charge densities also increases the flicker noise. What is more, as can be seen from the second term of the equation, flicker noise is inversely proportional to W_{eff}. The flicker noise will increase for the smaller values of W_{eff}. To sum up, decreasing g_m values reduces the thermal and induced gate noise components but it increases the flicker noise. It is important to note that, the flicker noise value decreases rapidly as the frequency increases. So the effect of the flicker noise component may be neglected at high frequencies.

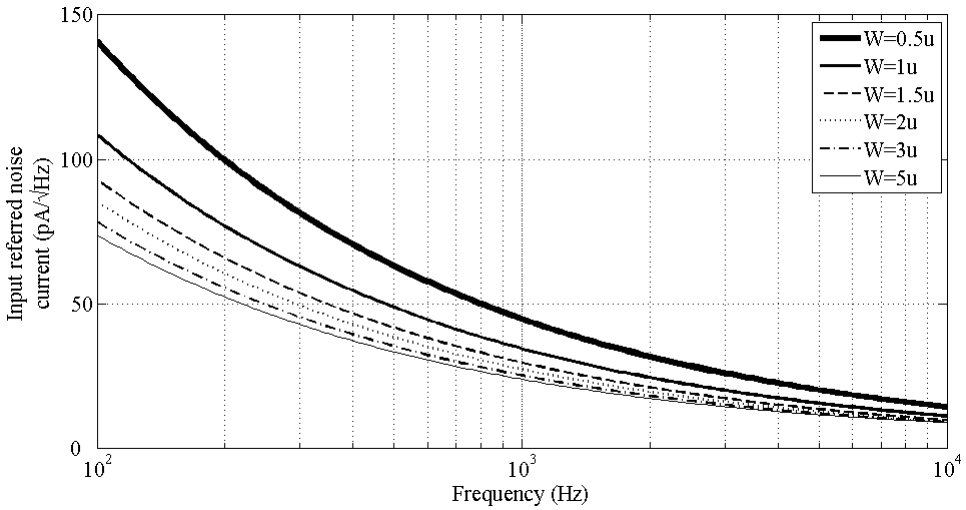

Figure 4.16. Flicker noise variations with transistor widths and the frequency

The flicker noise variations with different transistor widths of M_5 for the circuit in Fig. 3.3 are given in Fig. 4.16. As the width (or g_m) of the transistor M_5 (or M_{18}) decreases the flicker noise increases because the flicker noise is inversely proportional to W_{eff} as described above.

4.5.2.1. Simulation Results

The simulation results of the input referred current noise at low impedance port X, before and after g_m adjustment, are given. The theoretical noise expressions are compared with the simulated ones and the comparison results are shown in Table 4.3. It is observed that, the theoretical results are in very good agreement with the simulation results. A thermal noise current contribution of about 3.92pA/√Hz is obtained by simulation. This value is obtained as 3.86pA/√Hz analytically with only 1.53% error.

Table 4.3. Noise values at low impedance port X

Noise Value	Calculated	Simulated	Difference
$\overline{i_x^2}$ (pA /√ Hz)	3.86	3.92	1.53 %

The input referred noise current is mainly determined by transistors M_5, M_6, M_{18} and M_{19}. According to analytical expressions, $g_{m6,19}$ should be increased and $g_{m5,18}$ should be decreased in order to decrease the noise current. Increasing $g_{m6,19}$ or decreasing $g_{m5,18}$ both increase the current gain from X port to Z port. In order to support the analytical results,

some simulations are performed with different current gains. As a first step, while reducing the g_m values of mirror transistors M_5 and M_{18}, all other g_m values are kept constant. Input referred noise values decrease as the g_m values decrease. When the g_m values reach to half of their initial values, the input referred noise current reaches its minimum value with a current gain of about 3.7 as shown in Fig. 4.17. Then, all other g_m values kept constant and the g_m values of transistors, M_6 and M_{19}, are increased. Input referred noise values continue decreasing as the g_m values of M_6 and M_{19} increase. Minimum noise value is obtained at a current gain of about 5 as shown in Fig. 4.18. After the current gain of 5, increasing the g_m values of M_6 and M_{19} affects very little on the noise value but the current transfer bandwidth continues decreasing. The results are also given in Table 4.4. It is shown that, by adjusting the g_m values of the transistors, the input referred noise current is decreased from 3.91pA/√Hz to 2.16pA/√Hz which means a 45% reduction.

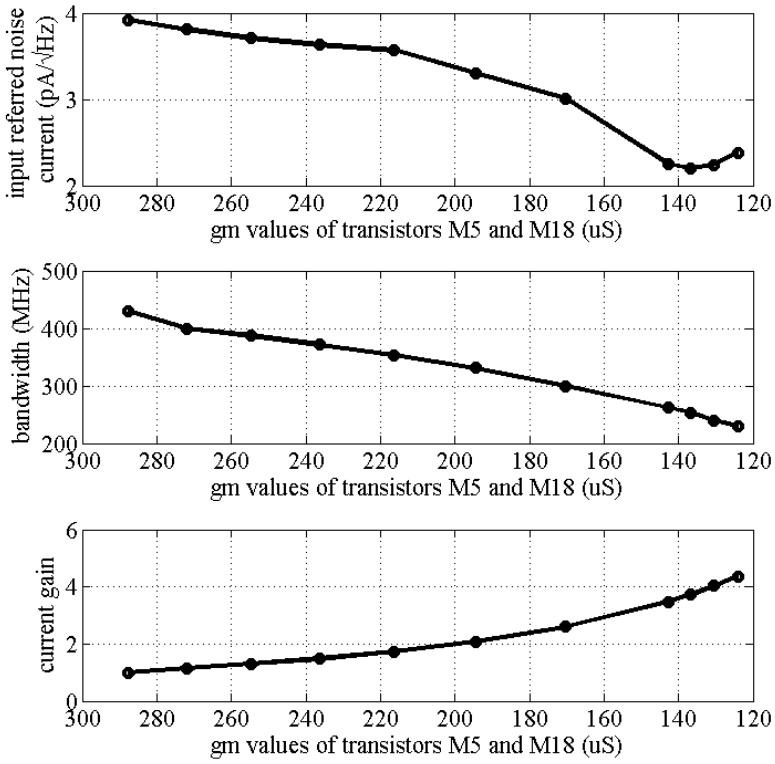

Figure 4.17. Noise, bandwidth and current gain variations with g_{m5} and g_{m18}

A careful g_m adjustment of mirror transistors M_5, M_6 and M_{18}, M_{19} must be made; because both the values of parasitic impedances at ports X and Z and also the current transfer bandwidth depend on these transistors. Changes in parasitic impedance values are listed in Table 4.5.

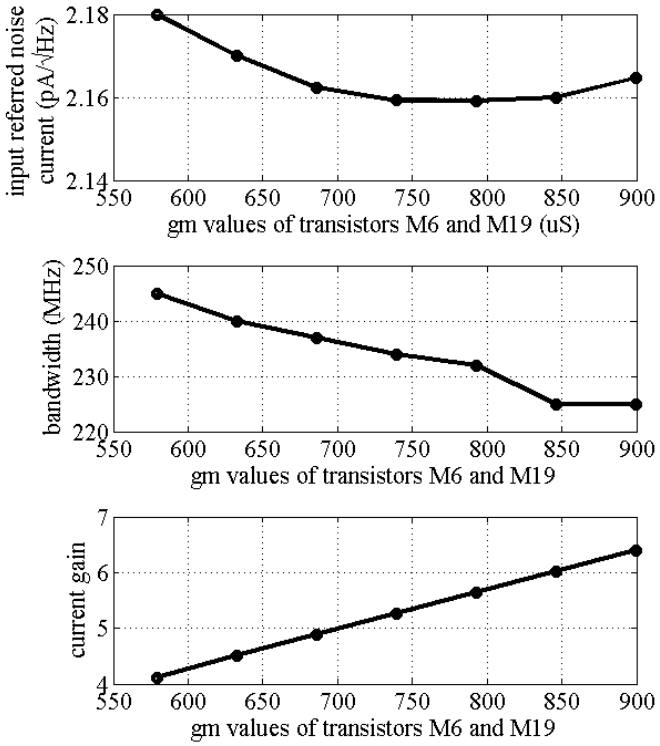

Figure 4.18. Noise, bandwidth and current gain variations with g_{m6} and g_{m19}

Table 4.4. Noise values at port X before and after g_m optimization

Noise Value		**Before g_m optimization**	**After g_m optimization**	**Reduction**
$\overline{v_y^2}$ (nV/√ Hz)	Calculated	3.86	2.07	46.37 %
	Simulated	3.92	2.16	44.89 %

Table 4.5. Resistance values before and after g_m optimization

Resistance	**Before g_m Optimization**	**After g_m Optimization**
R_X	33.2 Ω	38.9 Ω
R_Z	130 kΩ	47.1 k Ω

4.6. Noise Optimization of Filter Circuits

In the previous section, the noise model, which is formed by the input referred noise voltage source at high impedance port Y and the input referred noise current source at low impedance port X, was obtained. The noise values depend on the g_m values of the

transistors. The g_m values of the transistors were optimized to have minimum noise values and 47% reduction was obtained for the input referred noise voltage and 45% reduction was obtained for the input referred noise current. In this section, some current mode and voltage mode filter circuits are compared in terms of their input referred noise values. The validity of the noise reduction method is tested for the filter circuits. In addition, noise analysis of higher order filter circuits are also studied and it is shown that much higher reductions of input referred noise values are obtained with using optimized g_m values.

4.6.1. Noise Optimization of Current Mode Filter Circuits

Noise optimizations of current mode filter circuits are performed and the techniques, proposed in the above section, are applied to decrease the noise values. The first example of a current mode, band-pass (BP) filter circuit is shown in Fig. 4.19 with the related noise sources.

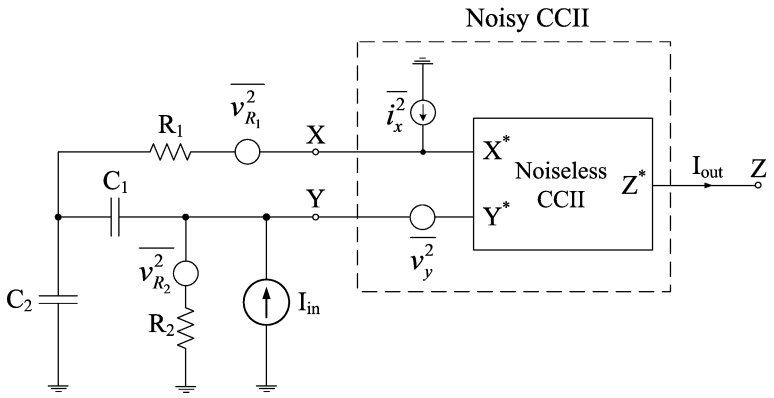

Figure 4.19. Current mode BP filter circuit with related noise sources

The transfer function of the BP filter circuit is:

$$\frac{I_{out}}{I_{in}} = \frac{C_2 G_1 s}{G_1 G_2 + G_2 (C_1 + C_2) s + C_1 C_2 s^2} \tag{4.43}$$

which has a center frequency of:

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \tag{4.44}$$

and a quality factor of:

$$Q = \frac{\sqrt{G_1 G_2 C_1 C_2}}{G_2 (C_1 + C_2)} \tag{4.45}$$

The filter circuit is simulated with the passive element values of R_1=2kΩ, R_2=4kΩ, C_1=C_2=1pF which determine the center frequency as 56.3MHz. The simulation results are shown in Fig. 4.20.

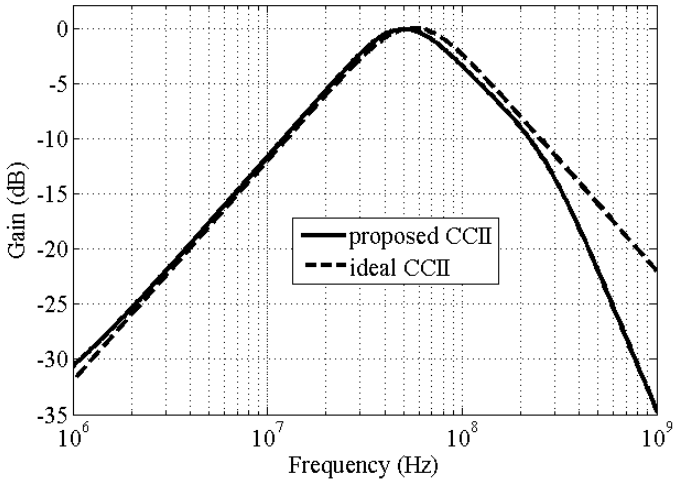

Figure 4.20. Frequency responses of the current mode 2nd order BP filter

The filter circuit has an input referred noise current of about 9.48pA/√Hz at the center frequency. If the noise values of the current conveyor are decreased, the total input referred noise current of the filter circuit can also be decreased. It is important to note that, g_m optimization at Y port does not change the current gain and as a result it does not affect the transfer function. Only optimization at X port increases the current gain and results in a change in the gain of the transfer function. By using the optimized g_m values, the transfer function of the filter circuit, for non-unity gain CCII turns into:

$$\frac{I_{out}}{I_{in}} = \frac{5 C_2 G_1 s}{G_1 G_2 + G_2 (C_1 + C_2) s + C_1 C_2 s^2} \tag{4.46}$$

The transfer function of the filter circuit does not change by using optimized g_m values except the gain factor of 5. The center frequency and the quality factor remain unchanged and they are equal to (4.44) and (4.45), respectively. After g_m optimization at Y port, the input referred noise current is decreased from 9.48pA/√Hz to 7.06pA/√Hz with a 26% reduction. With the g_m optimization both at Y and X ports a 36% reduction is obtained and the noise value is decreased to 6.00pA/√Hz. Simulation results are shown in Fig. 4.21 and also they are given in Table 4.6.

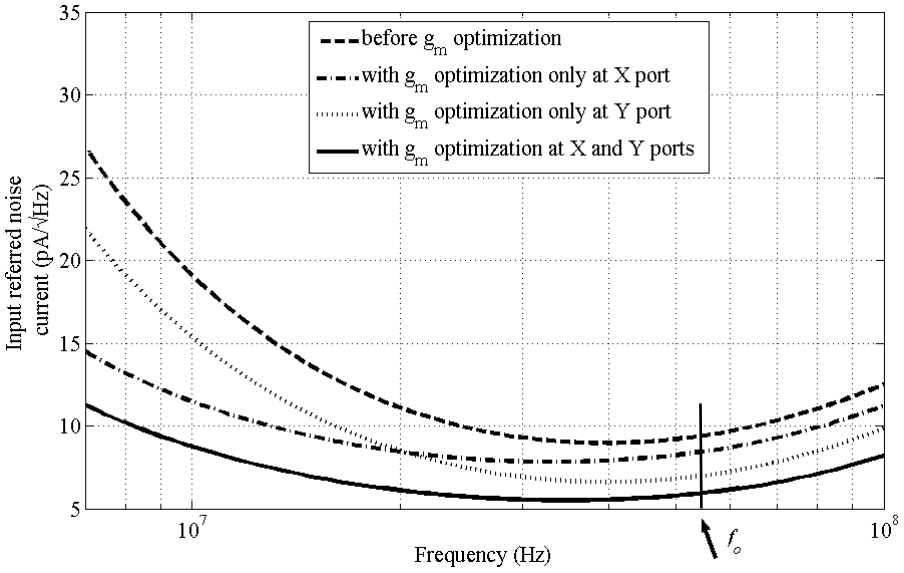

Figure 4.21. Input referred noise currents of the 2nd order filter circuit

Table 4.6. Noise values for the 2nd order filter circuit before and after g_m optimization

Noise Value	**Before g_m optimization**	**After g_m optimization**	**Reduction (%)**
$\overline{i_n^2}$ (pA /√ Hz)	9.48	6.00	36

4th and 6th order current mode filter circuits are also realized and their noise performances are studied. The identical filter circuits of Fig. 4.19 are cascaded to form the 4th and 6th order current mode filter circuits. The center frequency remains unchanged. Fig. 4.22 shows the frequency responses of the filter circuits. The input referred noise values of the 4th and 6th order filter circuits are 14.32pA/√Hz and 18.85pA/√Hz, respectively. After optimizing the g_m values of the transistors, the input referred noise values are decreased to 6.13pA/√Hz (58% reduction) for the 4th order filter circuit and 6.14pA/√Hz (68% reduction) for the 6th order filter circuit. The simulation results are shown in Fig. 4.23 and Fig. 4.24 and also they are given in Table 4.7.

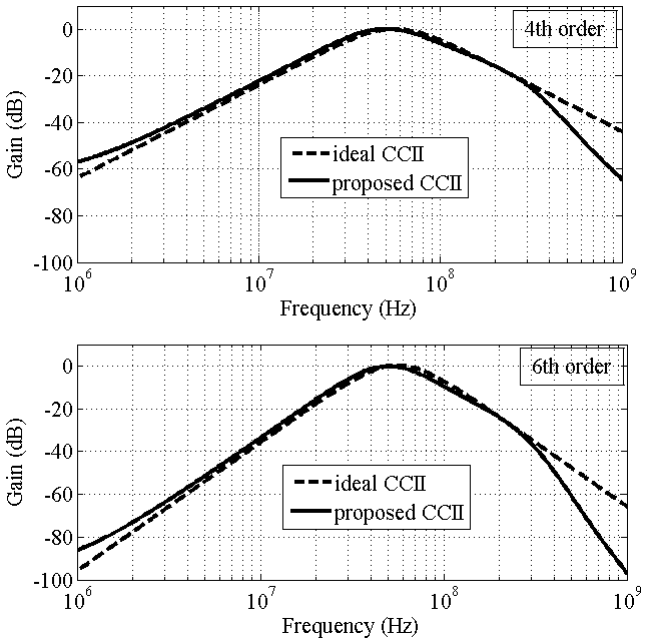

Figure 4.22. Frequency responses of the current mode 4th and 6th order BP filter circuits

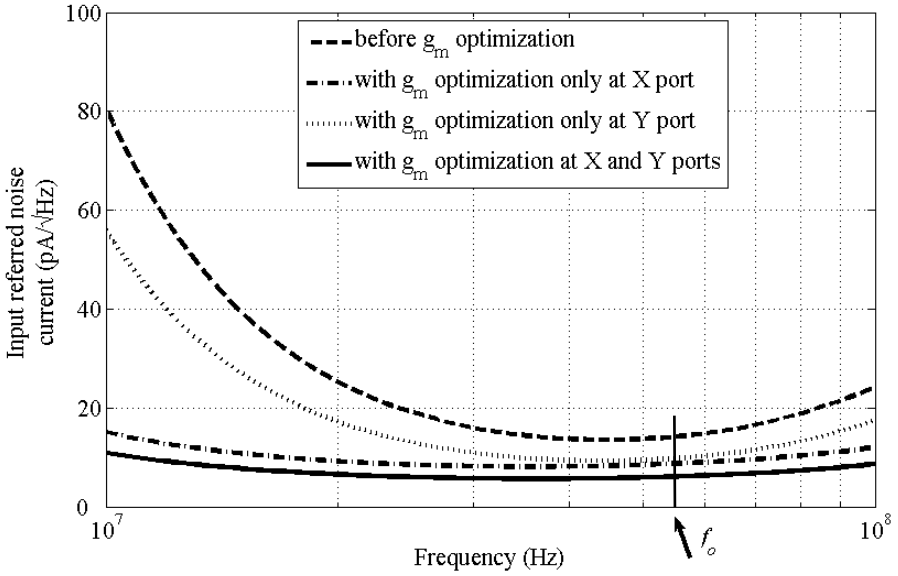

Figure 4.23. Input referred noise currents of 4th order filter circuit

Table 4.7. Noise values for the 4th and 6th order filter circuits before and after g_m optimization

Filter Order	Input Referred Noise Current (pA/√Hz)		
	Before g_m optimization	After g_m optimization	Reduction
4	14.32	6.13	58%
6	18.85	6.14	68%

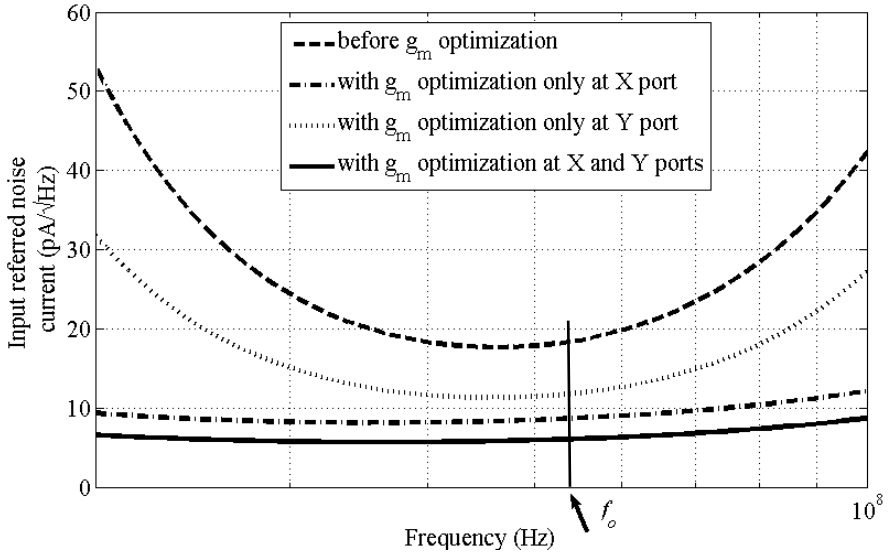

Figure 4.24. Input referred noise currents of 6th order filter circuit

The second example of a current mode, band-pass (BP) filter circuit is shown in Fig. 4.25 with the related noise sources.

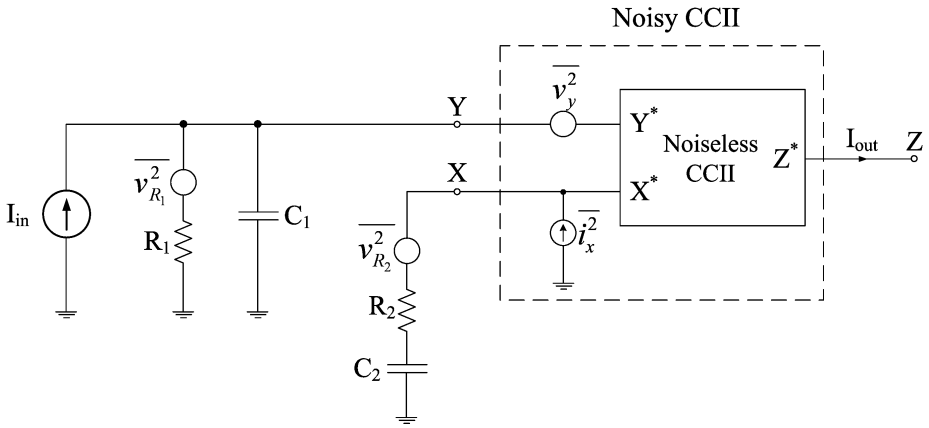

Figure 4.25 Current mode BP filter circuit with related noise sources

The transfer function of the BP filter circuit is:

$$\frac{I_{out}}{I_{in}} = -\frac{C_2 G_2 s}{G_1 G_2 + (C_2 G_1 + C_1 G_2)s + C_1 C_2 s^2} \tag{4.47}$$

which has a center frequency of:

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \tag{4.48}$$

and a quality factor of:

$$Q = \frac{\sqrt{G_1 G_2 C_1 C_2}}{C_2 G_1 + C_1 G_2} \tag{4.49}$$

The circuit is simulated with the passive element values of R_1=R_2=1.5kΩ, C_1=C_2=2pF which determine the center frequency as 53.1MHz. The simulation results are shown in Fig. 4.26.

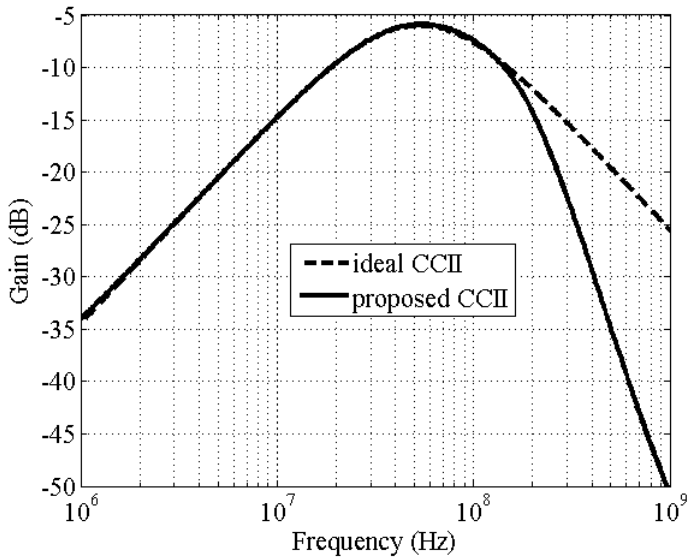

Figure 4.26. Frequency responses of the current mode 2nd order BP filter

The filter circuit has an input referred noise current of about 14.91pA/√Hz at the center frequency. With using the optimized g_m values, the transfer function of the filter circuit turns into:

$$\frac{I_{out}}{I_{in}} = -\frac{5C_2 G_2 s}{G_1 G_2 + (C_2 G_1 + C_1 G_2)s + C_1 C_2 s^2} \tag{4.50}$$

The transfer function of the filter circuit does not change except the gain factor of 5. The center frequency and the quality factor remain unchanged and they are equal to (4.48) and (4.49), respectively. After g_m optimization only at Y port, the input referred noise current is decreased from 14.91pA/√Hz to 11.45pA/√Hz with a 23% reduction. With the g_m optimization both at Y and X ports a 38% reduction is obtained and the noise value is decreased to 9.18pA/√Hz. Simulation results are shown in Fig. 4.27 and also they are given in Table 4.8.

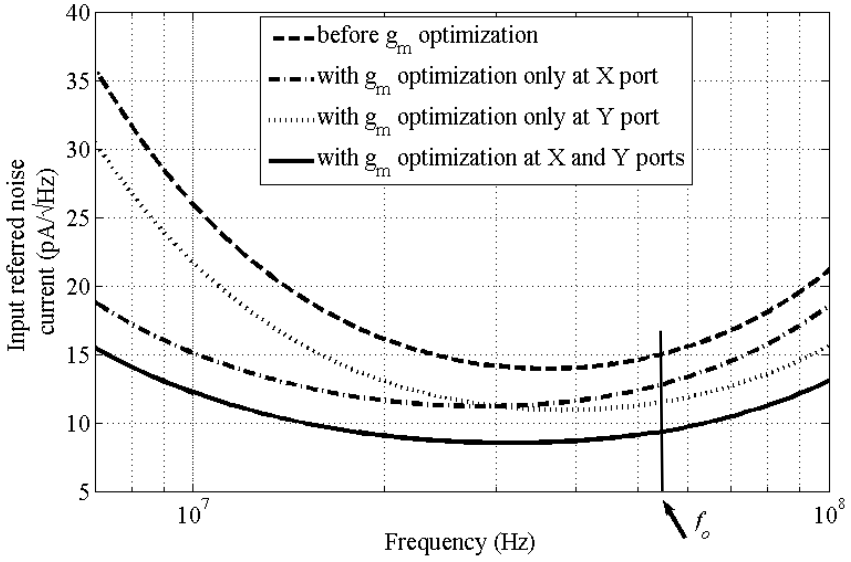

Figure 4.27. Input referred noise currents of the 2nd order filter circuit

Table 4.8. Noise values for the 2nd order filter circuit before and after g_m optimization

Noise Value	Before g_m optimization	After g_m optimization	Reduction (%)
$\overline{i_n^2}$ (pA /√ Hz)	14.91	9.18	38

4th and 6th order current mode filter circuits are also realized and their noise performances are studied. The identical filter circuits of Fig. 4.25 are cascaded to form the 4th and 6th order current mode filter circuits. The center frequency remains unchanged. Fig. 4.28 shows the frequency responses of the filter circuits. The input referred noise values of the 4th and 6th order filter circuits are 32.94pA/√Hz and 66.60pA/√Hz, respectively. After optimizing the g_m values of the transistors, the input referred noise values are decreased to 9.87pA/√Hz (70% reduction) for the 4th order filter circuit and 9.98pA/√Hz (85%

reduction) for the 6th order filter circuit. The simulation results are shown in Fig. 4.29 and Fig. 4.30 and also they are given in Table 4.9.

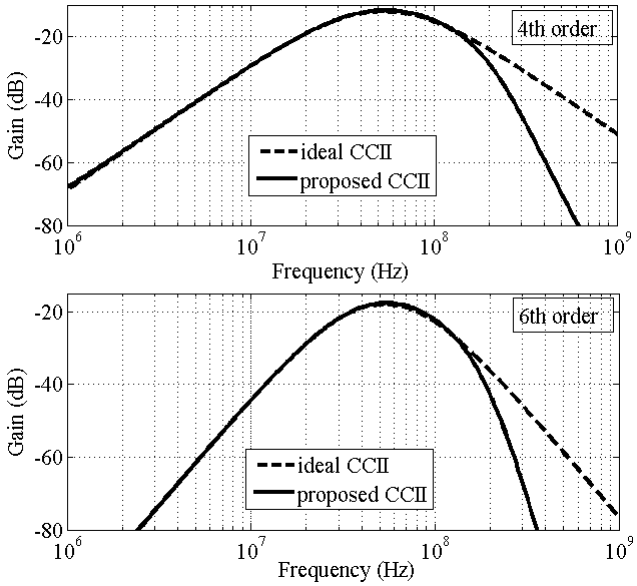

Figure 4.28. Frequency responses of the current mode 4th and 6th order BP filter circuits

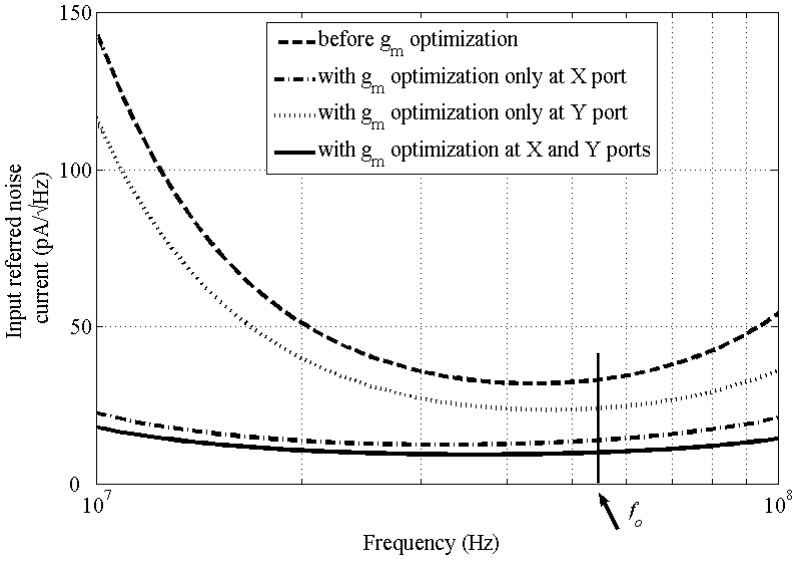

Figure 4.29. Input referred noise currents of the 4th order filter circuit

Table 4.9. Noise values for the 4th and 6th order filter circuits before and after g_m optimization

Filter Order	Input Referred Noise Current (pA/√Hz)		
	Before g_m optimization	After g_m optimization	Reduction
4	32.94	9.87	70%
6	66.60	9.98	85%

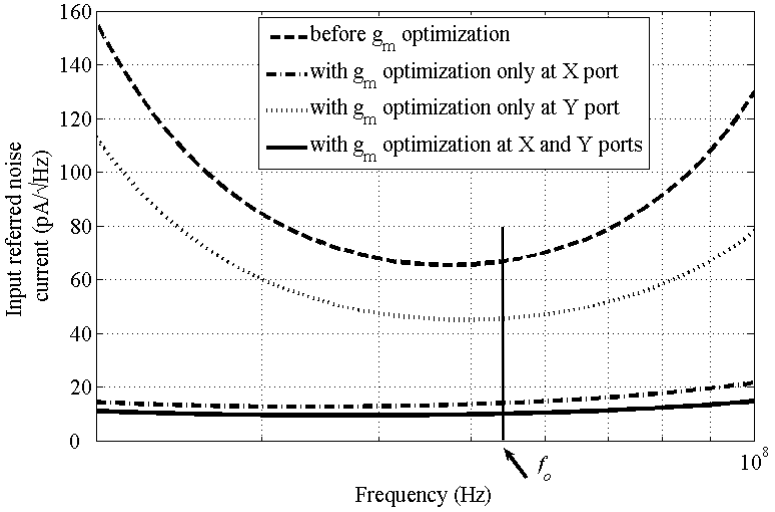

Figure 4.30. Input referred noise currents of the 6th order filter circuit

Optimization of the g_m values not only decrease the input referred noise value at center frequency but also suppresses it in a wide frequency range. A 6th order Chebyshev type-I, 1 dB ripple low-pass filter is also realized as shown in Fig. 4.31 and its noise analysis is studied in a lower frequency range. The passive element values of the filter are selected as: R_1=0.062kΩ, R_2=16.077kΩ, R_3=0.305kΩ, R_4=5.885kΩ, R_5=1.863kΩ, R_6=4.308kΩ and all the capacitance values are selected as 10pF which determine the center frequency as 1.63MHz. The simulation results are shown in Fig. 4.32.

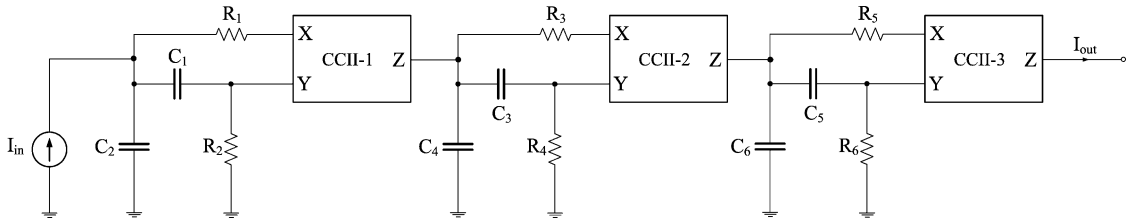

Figure 4.31. Chebyshev, type-I, 1-dB ripple, 6th order LP filter circuit

Fig. 4.33 shows the frequency responses of the filter circuit which uses the optimized g_m values. The gain of the circuit is increased to 19.2dB because the g_m optimization increases the current gain of the CCII. The filter circuit has an input referred noise current of about 33pA/√Hz in the pass-band. With using optimized g_m values, a reduction of 80% is obtained and the noise value is decreased to 6.5pA/√Hz as shown in Fig. 4.34.

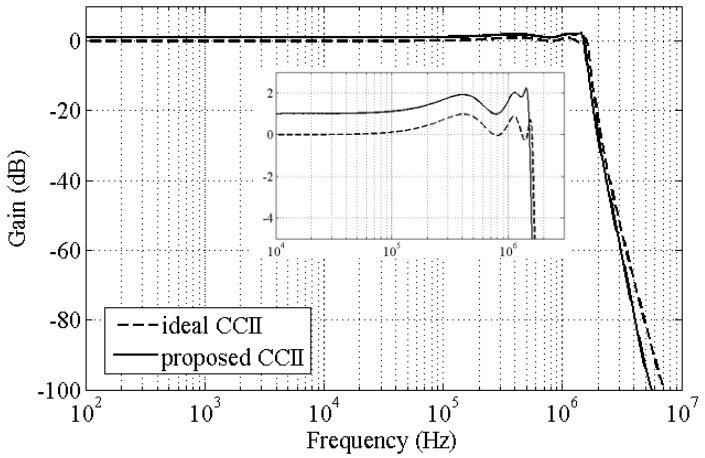

Figure 4.32. Frequency responses of the 6th order Chebyshev LP filter circuit before g_m optimization

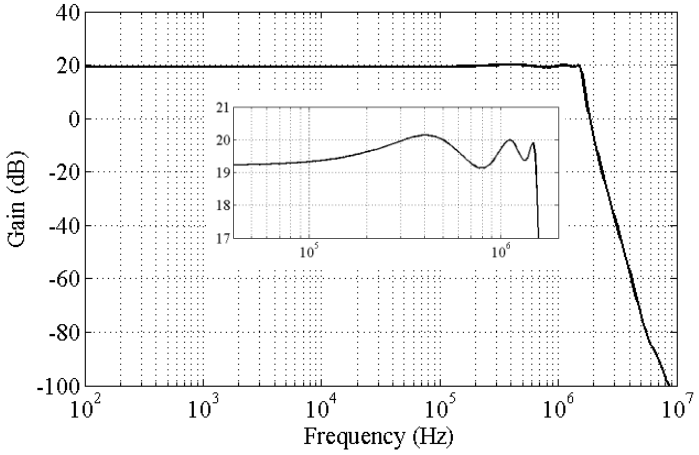

Figure 4.33. Frequency response of the 6th order filter circuit after g_m optimization

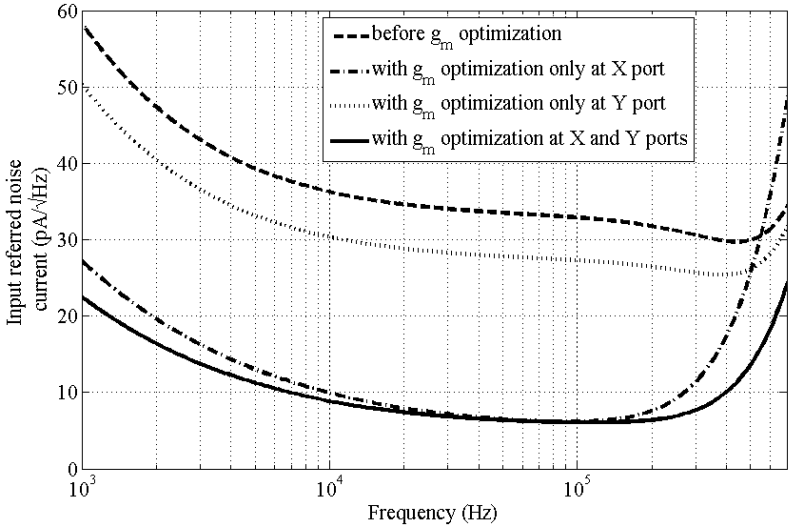

Figure 4.34. Input referred noise currents of the 6th order Chebyshev LP filter circuit

4.6.2. Noise Optimization of Voltage Mode Filter Circuits

Noise comparisons of voltage mode filter circuits are also performed and the noise techniques, proposed in the above section, are applied in order to decrease the noise values. Both of the filter circuits use equal number of active and passive elements and also equal valued resistance and capacitance values with center frequencies very close to each other. The filter topologies are taken from the literature [39, 40]. Selected filter circuits with all related noise sources are shown in Fig. 4.35 and Fig. 4.36.

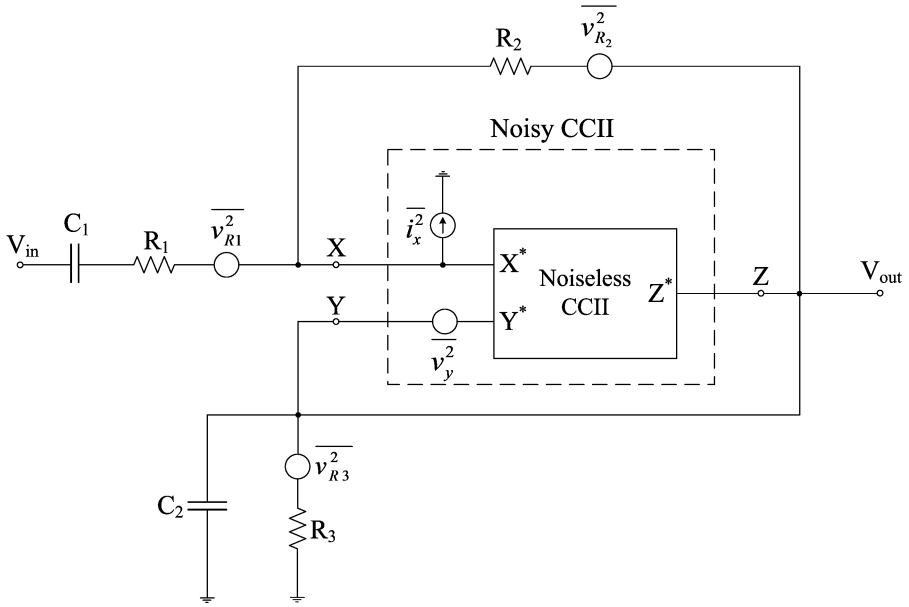

Figure 4.35. Band-pass filter circuit in [39] with related noise sources

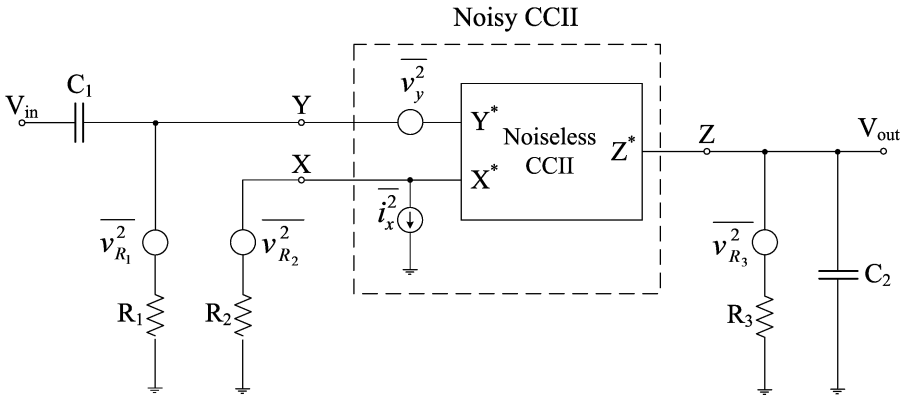

Figure 4.36. Band-pass filter circuit in [40] with related noise sources

The transfer function for the filter circuit in Fig. 4.35 is:

$$\frac{V_{out}}{V_{in}} = -\frac{C_1 G_1 s}{G_1 G_3 + (C_1 G_3 + C_2 G_1 - C_1 G_1)s + C_1 C_2 s^2} \tag{4.51}$$

which has a center frequency of:

$$\omega_o = \sqrt{\frac{G_1 G_3}{C_1 C_2}} \tag{4.52}$$

and a quality factor of:

$$Q = \frac{\sqrt{C_1 C_2 G_1 G_3}}{C_1 G_3 + C_2 G_1 - C_1 G_1} \tag{4.53}$$

During simulations of the filter circuit in Fig. 4.35, the values of the passive elements are selected as R_1=R_3=2kΩ, R_2=4kΩ and C_1=C_2=2pF, respectively which determine the center frequency as 39.8MHz.

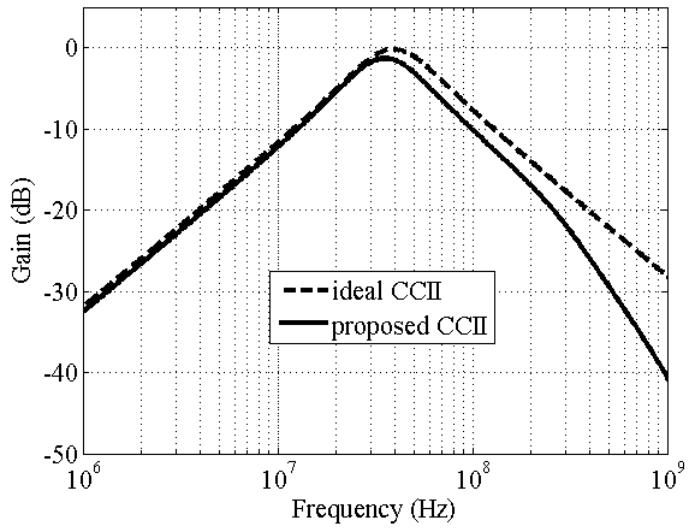

Figure 4.37. Frequency responses of the 2nd order BP filter circuit in [39]

In Fig. 4.37, the frequency responses of the filter circuit are shown. The filter circuit has an input referred noise voltage of about 39.75nV/√Hz at the center frequency. If the

noise values of the current conveyor are decreased, the total input referred noise voltage of the filter circuit can also be decreased. After applying the g_m adjustment method to the filter circuit, the transfer function turns into:

$$\frac{V_{out}}{V_{in}} = -\frac{5C_1G_1s}{G_1G_3 + (C_1G_3 + C_2G_1 - 5C_1G_1)s + C_1C_2s^2} \tag{4.54}$$

The center frequency of the filter circuit doesn't change and it is the same as (4.38). The quality factor is exposed to a small change and its new value is:

$$Q = \frac{\sqrt{C_1C_2G_1G_3}}{C_1G_3 + C_2G_1 - 5C_1G_1} \tag{4.55}$$

It is important to note that, adjusting the g_m values of the CCII circuit does not change the center frequency of the filter, only the gain of the overall circuit changes. The resultant circuit is again a BP filter with a lower input referred noise. The input referred noise voltages, before and after g_m adjustment, at centre frequencies are shown in Fig. 4.38 and also they are given in Table 4.10.

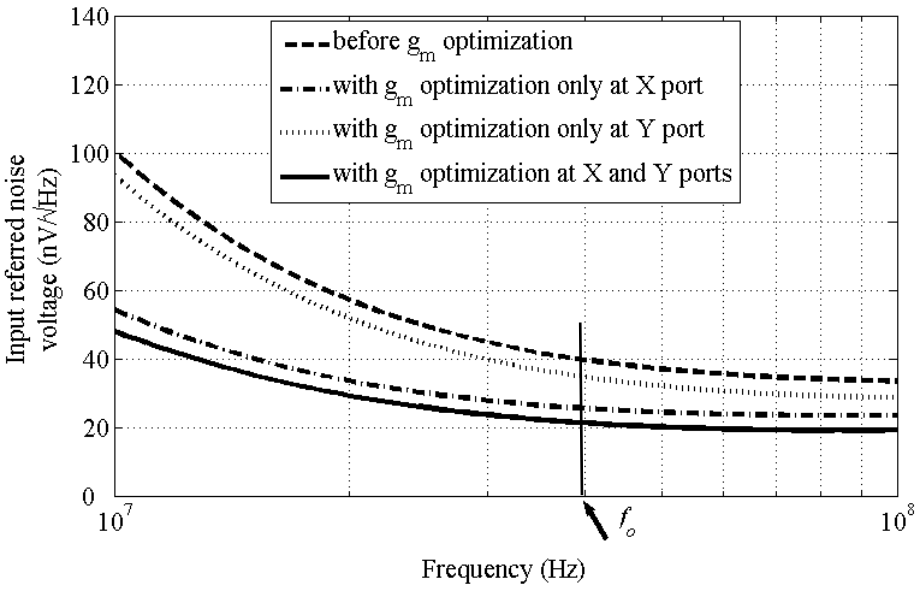

Figure 4.38. Input referred noise values of the 2nd order BP filter circuit in [39]

Table 4.10. Noise values for the 2nd order filter circuit before and after g_m optimization

Noise Value	Before g_m adjustment	After g_m adjustment	Reduction (%)
$\overline{v_n^2}$ (nV /√ Hz)	39.75	21.30	47

Firstly, only g_m optimization at port Y is performed, which doesn't change the current gain between ports X and Z and as a result doesn't affect the transfer function of the filter. The input referred noise voltage is decreased from 39.75nV/√Hz to 34.75nV/√Hz. With the g_m optimization both at ports Y and X, the input referred noise voltage is decreased to 21.3nV/√Hz which means a 47% reduction. It is important to note that, the g_m optimization at port X brings a gain factor of 5 to the filter circuit. That is to say, at center frequency, the filter circuit amplifies the input current with a gain of 5.

During simulations of the filter circuit in Fig. 4.36, the passive element values are selected as $R_1=R_2=R_3=2.5k\Omega$ and $C_1=C_2=1pF$, respectively which determine the center frequency as 63.7MHz. The transfer function of the filter circuit is:

$$\frac{V_{out}}{V_{in}} = \frac{C_1 G_2 s}{G_1 G_3 + (C_1 G_3 + C_2 G_1)s + C_1 C_2 s^2} \tag{4.56}$$

which has a center frequency of:

$$\omega_o = \sqrt{\frac{G_1 G_3}{C_1 C_2}} \tag{4.57}$$

and a quality factor of:

$$Q = \frac{\sqrt{C_1 C_2 G_1 G_3}}{C_1 G_3 + C_2 G_1} \tag{4.58}$$

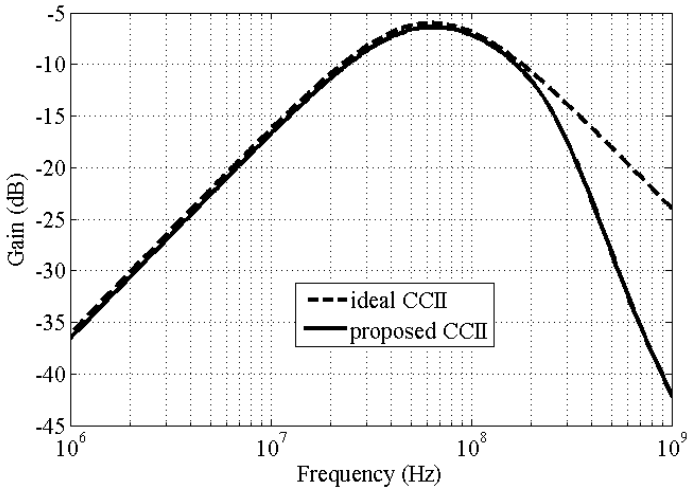

Figure 4.39. Frequency responses of the 2nd order BP filter circuit in [40]

In Fig. 4.39 the frequency response of the filter circuit is shown. The filter circuit has an input referred noise voltage of about 27.41nV/√Hz at the center frequency. After applying the g_m adjustment method, the transfer function of the filter becomes:

$$\frac{V_{out}}{V_{in}} = \frac{5C_1G_2s}{G_1G_3 + (C_1G_3 + C_2G_1)s + C_1C_2s^2} \tag{4.59}$$

The transfer function of the filter circuit does not change after g_m adjustment except the gain factor of 5. The center frequency and the quality factor remain unchanged and

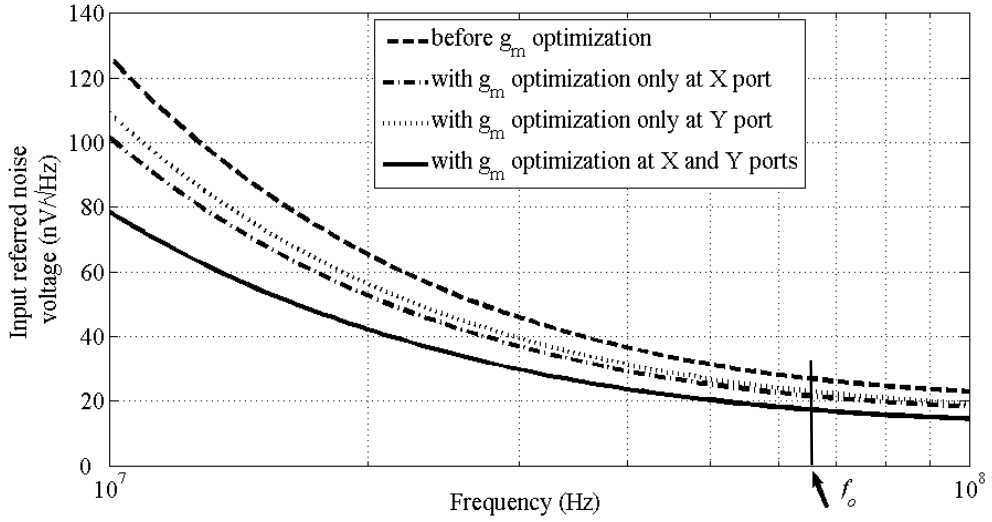

Figure 4.40. Input referred noise values of the 2nd order BP filter circuit in [40]

they are equal to (4.57) and (4.58), respectively. The input referred noise voltages, before and after g_m adjustment, at centre frequencies are shown in Fig. 4.40 and also they are given in Table 4.11.

Table 4.11. Noise values for the 2nd order filter circuit before and after g_m optimization

Noise Value	Before g_m optimization	After g_m optimization	Reduction (%)
$\overline{v_n^2}$ (nV /√ Hz)	27.41	17.63	36

With the g_m optimization at port Y, the input referred noise voltage is decreased from 27.41nV/√Hz to 23.42nV/√Hz. With the addition of the g_m optimization at port X, the noise voltage is decreased to its minimum value of 17.63nV/√Hz with a totally 36% reduction.

4th and 6th order voltage mode filter circuits are also realized and their noise performances are studied. The circuit in Fig. 4.36 is selected for the following simulations. Identical filter circuits of Fig. 4.36 are cascaded to form the 4th or 6th order voltage mode filter circuits. The center frequencies remain unchanged. Fig. 4.41 shows the frequency responses of the 4th and 6th order voltage mode BP filter circuits.

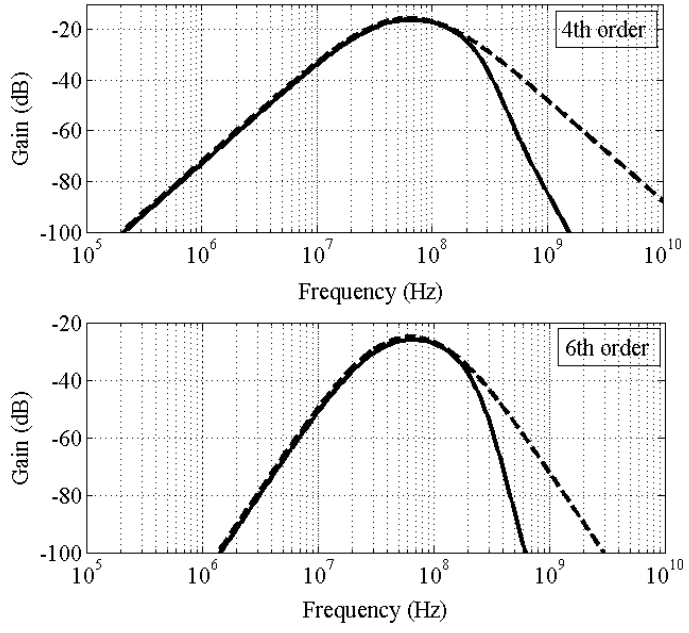

Figure 4.41. Frequency responses of the 4th and 6th order filter circuits

The 4th order filter circuit has an input referred noise voltage of about 91.37nV/√Hz before g_m optimization. When the noise value at port Y is optimized, it is decreased to 74.54nV/√Hz without disturbing the current gain of the CCII and also the transfer function of the filter. With the additional port X noise current optimization, a 77% reduction is obtained and the input referred noise voltage is decreased to 21.22nV/√Hz. The simulation results are shown in Fig. 4.42. Similar solutions are performed for the 6th order filter circuit. Initially the filter circuit has an input referred noise voltage of 291.21nV/√Hz. With

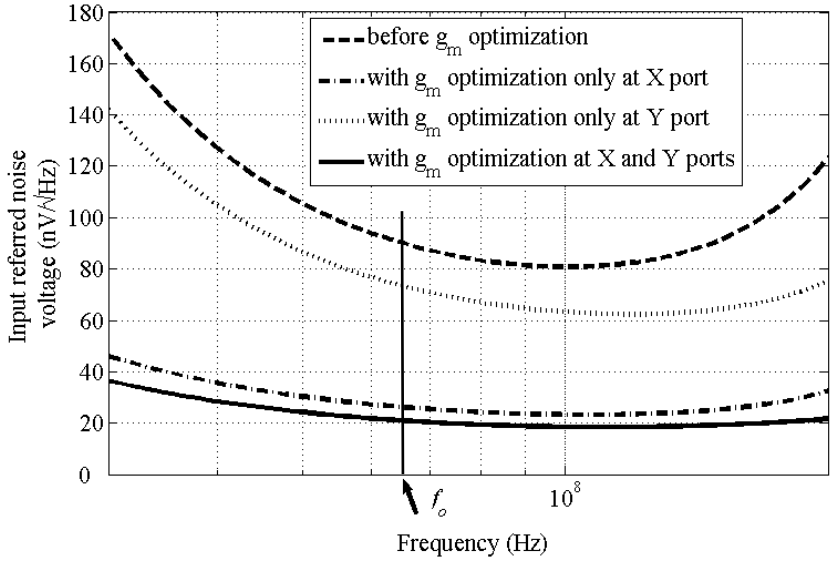

Figure 4.42. Input referred noise values of the 4th order BP filter circuit

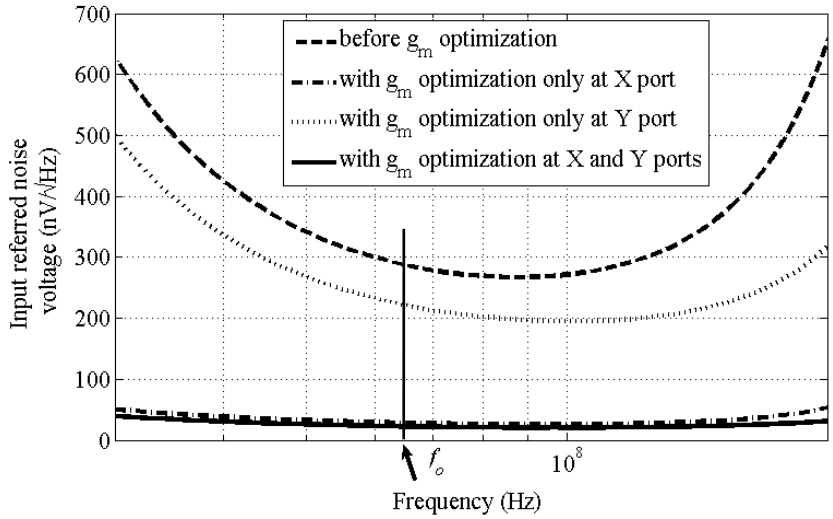

Figure 4.43. Input referred noise values of the 6th order BP filter circuit

the g_m optimization at port Y, it is decreased to 225.2nV/√Hz without changing the current gain of the CCII and the transfer function. With the additional g_m optimization at port X, totally 92% reduction is obtained and the value of the noise voltage is decreased to 22.60nV/√Hz as shown in Fig. 4.43. Simulation results are also given in Table 4.12.

Table 4.12. Noise values for the 4th and 6th order filter circuits before and after g_m optimization

Filter Order	Input Referred Noise Voltage (nV/√Hz)		
	Before g_m optimization	After g_m optimization	Reduction
4	91.37	21.22	77%
6	291.21	22.60	92%

Finally, the noise reduction technique is tested on another voltage mode, Butterworth type, 3rd order BP filter circuit. It is given in Fig. 4.44 with all related noise sources.

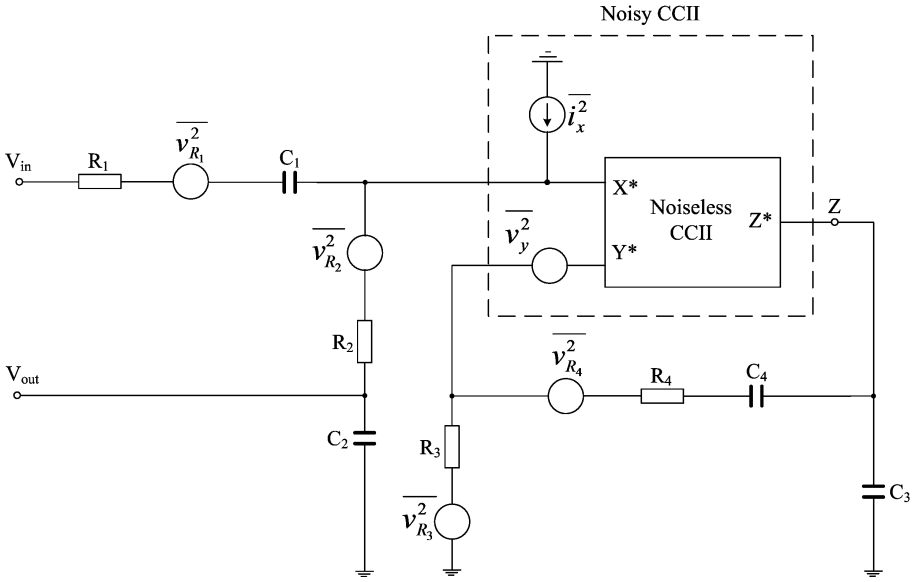

Figure 4.44. Voltage mode, Butterworth type, 3rd order BP filter circuit

The voltage transfer function of the circuit can be given as:

$$\frac{V_{out}}{V_{in}} = -\frac{1}{2}\frac{sCG^2}{G^3 + 2CG^2 s + 2C^2 G s^2 + C^3 s^3} \tag{4.60}$$

Taking G = 1 mho and C = 1 F,

$$\frac{V_{out}}{V_{in}} = -\frac{1}{2}\left(\frac{s}{1+2s+2s^2+s^3}\right) \tag{4.61}$$

Impedance and frequency scaling can be performed on the filter circuit to shift the center frequency to the desired value [41]. During simulations, resistance values and capacitance values are selected as 3kΩ and 1pF, respectively which determine the center frequency as 47.5MHz. Simulation results are given in Fig. 4.45. The input and output

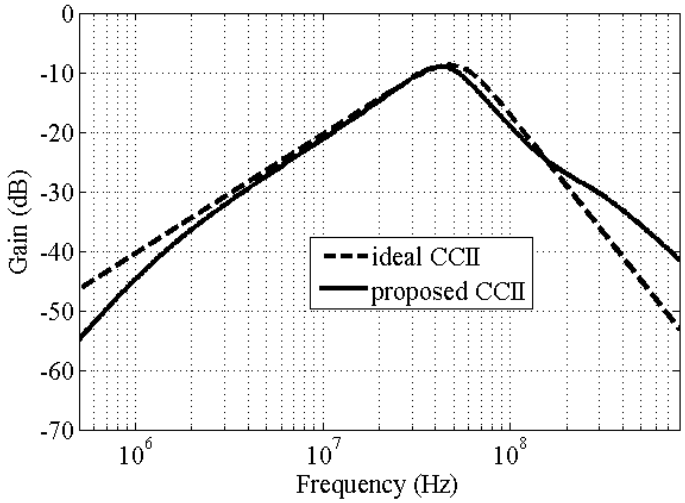

Figure 4.45. Frequency responses of the 3rd order Butterworth filter circuit

impedance values of the proposed CCII changes after 100MHz and this change results in a deviation between the filter responses that are realized with the ideal CCII and the proposed CCII. The filter circuit has an input referred noise voltage of about 58.56nV/√Hz at the center frequency. After optimizing the noise current at port X, the current gain is increased to 5 and the transfer function of the filter becomes:

$$\frac{V_{out}}{V_{in}} = -\frac{1}{2}\left(\frac{5CG^2 s}{G^3 - 2CG^2 s - 2C^2 Gs^2 + C^3 s^3}\right) \tag{4.62}$$

It is seen that increasing the current gain of the CCII disrupts the filter transfer function and the resultant transfer function no more belongs to any type of filter circuit. As a result, for this exceptional filter circuit, g_m optimization at port X cannot be applied. Only the noise voltage at port Y can be optimized which doesn't change the current gain of

the CCII and as a result doesn't disturb the transfer function. After optimizing the noise voltage at port Y, the input referred noise voltage of the filter circuit is decreased to 46.71nV/√Hz with a 21% reduction. Simulation results are shown in Fig. 4.46.

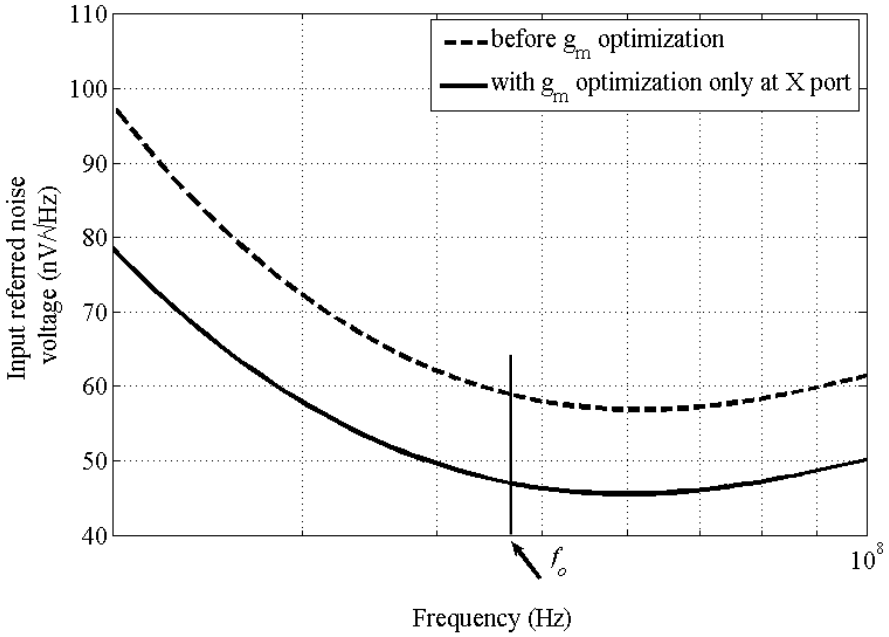

Figure 4.46. Input referred noise values of the 3rd order Butterworth filter circuit

5. CONCLUSION

In this thesis, novel CMOS implementations of second generation current conveyor (CCII) circuits are introduced. The first implementation is based on differential pairs and it has high voltage swings on ports X and Y, very low equivalent impedance on port X, high equivalent impedances on ports Y and Z and also high-valued voltage and current transfer bandwidths. When compared to translinear-loop based CCIIs or class A CCIIs, the main advantage of the circuit is the high voltage swings on ports X and Y. It is shown that, the voltage swings of the translinear-loop based CCIIs are limited to a very small value. The second implementation replaces the source followers of the first CCII implementation with super source followers (source followers with local feedback) to obtain smaller equivalent impedance value at port X. It has also higher voltage and current transfer bandwidths compared to the first implementation. The final implementation is a self biased one which uses no additional biasing voltage or current sources other than the two supply rails. A start-up circuit is also designed for the circuit. It is the first self-biased CMOS CCII implementation in the literature.

Noise analyses of the proposed CMOS CCII circuits are studied. Input referred noise voltage at high-impedance port Y and input referred noise current at low impedance port X are obtained to form the noise model of the CCII. Based on this noise model, noise values of the proposed circuits are optimized by adjusting the g_m values of the transistors. It is shown analytically and by simulations that, selecting the current gains from X port to Y port higher than unity results in high noise reductions. The input referred noise is reduced by increasing the circuit current gain up to 5. Increasing the gain more than 5 does not help to decrease the noise any more, but deteriorates the circuit performance by decreasing the bandwidth and increasing the X port input resistance. So it is chosen to be around 5. The validity of the noise reduction techniques are tested on both current mode and voltage mode filter circuits. Considerable noise reductions are obtained especially on higher order filter circuits. Filter design equations do not change with this modification, only a gain factor is added to the transfer functions.

The contribution of the thesis may be summarized as follows:

- In this work, new differential pair based CMOS CCII implementations are proposed. The proposed circuits exhibit better characteristics compared to its predecessors in terms of voltage swings on ports X and Y and especially equivalent impedance values at ports X in a wide frequency range. It is known that the ideal impedance levels of the CCII are infinite for Y and Z ports and zero for the X port. The CMOS CCII circuit can be used in a wide frequency range if the equivalent impedance values of the proposed circuit are very close to their ideal values.

- One of the important shortcomings of the current mode active filter design is the need for low noise. A noise model which is composed of an input referred noise voltage at high impedance port Y and an input referred noise current at low impedance port X, for the proposed CMOS CCII circuits, are obtained. The noise of the CMOS CCII circuit is minimized by using this model and choosing proper g_m values for the MOS transistors. It is shown that using current conveyors with current gains greater than unity, results in high noise reductions. CCII with a current gain greater than unity may be used for active filter circuits without ant modification in design procedure.

- Some current mode and voltage mode filter circuits are selected from the literature and they are realized by using our circuit to test the noise performance. The proposed noise reduction techniques are applied to the filter circuits and considerable noise reductions, up to 90%, are obtained especially for the high order filter circuits.

- In this work, it is seen that the 0.35μ technology is not usable to realize high frequency active filters beyond a few 10MHz. This limitation is due to the minimum input resistance and capacitances of the circuits. The maximum operation frequency may be increased by using new technologies with smaller dimensions in the expense of higher noise.

- The proposed CMOS CCII circuit in Fig. 3.3 employs 19 transistors. With this high number of transistors, it is difficult to obtain high operation frequency because each additional transistor adds additional pole, increases the power and the layout area and as a result decreases the bandwidth of the circuit. If the basic requirements of current-mode circuits can be ensured by using simpler current mode architectures with fewer

numbers of transistors, it will be possible to obtain low noise, low power and also high operation frequency.

APPENDIX A: NOISE EFFECT RELATED MODEL PARAMETERS

There exist two models for channel thermal noise. One is called as Spice2 thermal noise model. Another one is called as BSIM3v3 thermal noise model. Each of these can be toggled by the NOIMOD flag. The parameters in the models are listed in the tables below.

Table A.1. Noise parameters for 0.35μm AMS

Symbols used in SPICE	Description	NMOS	PMOS
NOIA	Noise parameter A	1.73e+19	1.52e+18
NOIB	Noise parameter B	7.000e+04	7.75e+03
NOIC	Noise parameter C	-5.64e-13	5.0e-13
AF	Frequency exponent	1.3600e+00	1.48e+00
KF	Flicker noise parameter	5.1e-27	8.5e-27
EF	Flicker exponent	1.000e+00	1.000e+00
NOIMOD	Noise model flag	3	3

Table A.2. Noise parameters for 0.18 μm UMC

Symbols used in SPICE	Description	NMOS	PMOS
NOIA	Noise parameter A	1.23857E+21	4.86325E+19
NOIB	Noise parameter B	44531.54732	142700
NOIC	Noise parameter C	-1.05E-14	1.04E-11
EF	Flicker exponent	0.93963	1.117
EM	Saturation field [V/m]	2063059.94272	5015000
NOIMOD	Noise model flag	2	2

For SPICE2, the thermal noise is equal to:

$$\frac{8kT}{3}\left(g_m + g_{ds} + g_{mb}\right) \tag{A.1}$$

For BSIM3V3, the thermal noise is equal to:

$$\frac{4KT\mu_{eff}}{L_{eff}^2}\left|Q_{inv}\right| \tag{A.2}$$

$$Q_{inv} = -W_{eff} L_{eff} C_{ox} V_{gsteff} \left(1 - \frac{A_{bulk}}{2\left(V_{gsteff} + 2vt\right)} V_{dseff} \right) \quad \text{(A.3)}$$

The NOIMOD flag is used to select different combination of flicker and thermal noise models as given in Table A.3.

Table A.3. NOIMOD flag for different noise models

NOIMOD flag	**Flicker noise model**	**Thermal noise model**
1	Spice2	Spice2
2	BSIM3v3	BSIM3v3
3	BSIM3v3	Spice2
4	Spice2	BSIM3v3

APPENDIX B: NOISE OPTIMIZATION RESULTS USING UMC TECHNOLOGY PARAMETERS

The 6th order current mode BP filter circuit, which is realized in Section 4.6.1 by cascading the filter circuit in Fig. 4.16, is also simulated at much higher frequencies using 3.3V, 0.18µm, UMC technology parameters. During simulations, passive element values are selected as R_1=0.5kΩ, R_2=1kΩ, C_1=C_2=1pF which determine the center frequency as 225MHz. Frequency responses are given in Fig. B.1.

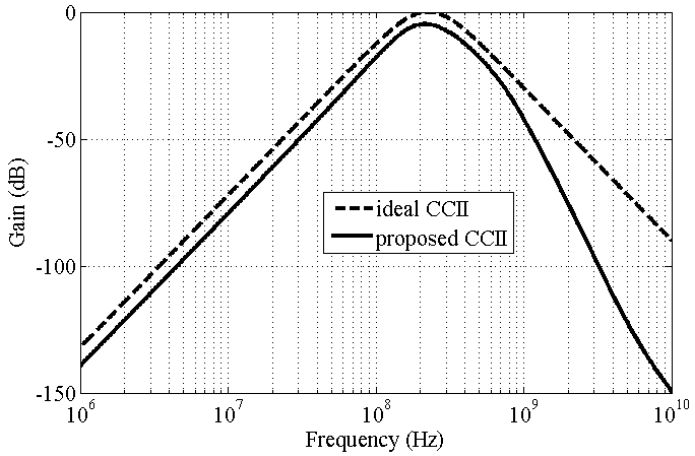

Figure B.1. Frequency responses of the current mode 6th order BP filter circuit

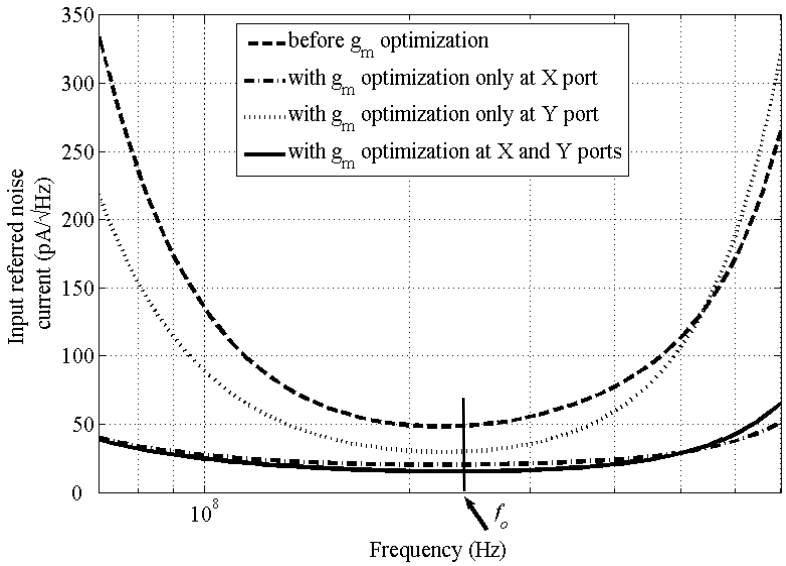

Figure B.2. Input referred noise values of the current mode 6th order BP filter circuit

The filter circuit has an input referred noise voltage of about 48.29nV/√Hz before g_m optimization. When the noise value at port Y is optimized, it is decreased to 29.53nV/√Hz without disturbing the current gain of the CCII and also the transfer function of the filter. With the additional port X noise current optimization, a 69% reduction is obtained and the input referred noise voltage is decreased to 15.26nV/√Hz. The simulation results are shown in Fig. B.2.

APPENDIX C: LAYOUT OF THE PROPOSED CIRCUIT

The proposed circuit in Fig. 3.3 is laid-out using Mentor Graphics IC Station Layout Editor, using AMS 0.35µm process parameters. The layout is shown in Fig. C.1 and the simulation results are given in Table C.1.

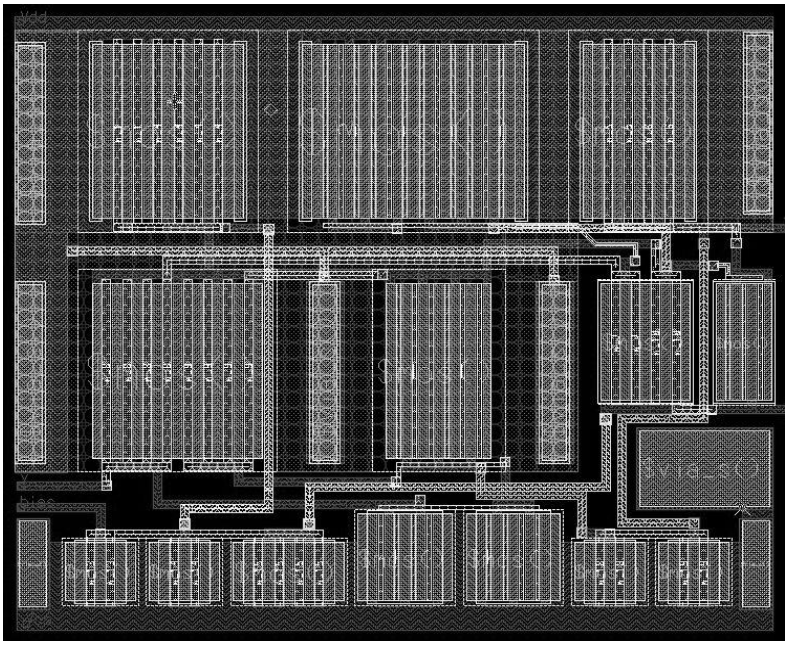

Figure C.1. Layout of the CMOS CCII circuit in Fig. 3.3

Table C.1. Post-layout simulation results

Parameter	**Schematic**	**Post-Layout**
Voltage gain, V_x / V_y	0.97	0.94
Voltage transfer BW	486 MHz	451 MHz
Noise at 100MHz	9.1nV/√ Hz	10.9nV/√ Hz
Current gain, I_z / I_x	1.03	1.06
Current transfer BW	467 MHz	420 MHz
Noise at 100MHZ	4.6pA/√ Hz	4.8pA/√ Hz
Offset voltage on *X*	-0.77 mV	10 mV
Offset current on *Z*	1.13 µA	1.7 µA
Port X resistance	23.4 Ω	98.7 Ω
Port X voltage swing	±1.05 V	±1.05 V
Power consumption	703 µW	714 µW

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