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MICROPROCESSOR APPLICATION
FOR ADAPTIVE POSICAST CONTROL
OF LIGHTLY DAMPED SYSTEMS

by

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ABSTRACT

The problem of compensating a feedback system which is very lightly damped has long confronted control engineers. Numerous schemes have been utilized with varying degrees of success. This work investigates and applies one such scheme, Half-cycle Posicast, which was introduced by Otto J. M. Smith. This scheme has several advantages. It reduces overshoot and resonant peaking thus allowing higher forward gain to be used. This in turn reduces steady-state errors.

The problem of compensating a second order, lightly damped linear feedback system by means of Half-cycle Posicast with microprocessor application is examined and the results of analog computer simulations are shown. The sensitivity of behavior to variations in system parameters is examined and some degree of adaptivity to changes of parameters is reached.

ÖZETÇE

Az sönümlü bir geribeslemeli denetim düzeneği tasarlama sorunu uzun zamanlar denetim mühendislerinin çözmesi gereken bir sorun olarak önlerine gelmiştir. Bu sorun için çok sayıda ve değişen başarı çizgilerinde çözümler önerilmiştir. Bu çalışmada bu yöntemlerden birisi olan ve ilk defa Otto J.M. Smith tarafından tanıtılan "Salın-dur" ("Posicast") çözüm yöntemi incelenmekte ve uygulanmaktadır. Bu yöntemin çeşitli üstünlükleri vardır. Yöntem sistemdeki salınımı yok ederek daha yüksek bir iletkenlik kazanç sabiti kullanılmasına olanak sağlamaktadır.

Bu çalışmada az sönümlü doğrusal geribeslemeli ikinci dereceden bir sistemde Salın-dur yönteminin mikro-işlemci ile tasarımı incelenmiş, analog bilgisayar benzetim sonuçları gösterilmiştir. Ayrıca geçici durum cevabı verilmiştir. Sistem parametrelerindeki değişikliklere duyarlılık davranışı incelenmiş ve parametre değişikliklerine karşı uyarlanabilirlik (adaptivity) sağlanmıştır.

1. INTRODUCTION

In recent years significant progress has been made in discrete-data and digital control systems. These systems have gained popularity and importance in all industries due in part to the advances made in digital computers, and more recently in microcomputers, as well as the advantages found in working with digital signals. The science and art of communications have profited from the realization and application of the fact that intelligence can be transmitted and stored in discrete pieces or as a sequence of numbers spaced in real time. Even though we treat sampled-data systems primarily from the viewpoint of the control function, it is not surprising that many concepts have been borrowed from the communications field. Furthermore, the same body of theory can be used to describe the over-all performance of the control systems, even though its primary function is the controlled actuation of power elements and processes.

Sampled-data systems are characterized by the fact that the signal data appear at one or more points in the system as a sequence of pulses or numbers. A central problem in the theory of such systems is that of describing the response of linear continuous elements, or pulsed filters, as they are sometimes called, to pulse sequences applied to their input.

The use of the z-transformation and the all important pulse transfer function of the pulsed filter makes the problem relatively straight forward. A unique component found in sampled-data control systems is the digital controller, which is a computer that accepts a sequence of numbers at its input, processes it in accordance with some logical program, and applies the resultant sequence to the controlled element. In view of the operation of this controller, it is possible to implement it by means of a conventional digital computer or its equivalent in the form of a mixed or wholly analog computer. If the numerical process programmed in the computer is linear, it can be expressed mathematically in terms of a recursion formula which is transformed into a generating function having similarity to the pulse transfer function of a pulsed linear filter.

The trend of the past few decades has been toward dynamical systems that operate with variables which are in the form of a sequence of numbers. These variables are generally quantized in amplitude and are available only at specified instants of time, which are usually equally spaced. The major point of difference between analog and discrete systems lies in the fact that analog or continuous systems have variables which are known at all instants of time,

whereas discrete systems have variables which are known only at sampling instants.

Many modern control systems contain intentional sampling and digital processors. Some of the advantages of sampled-data and digital control are:

1. Improved sensitivity,
2. Better reliability,
3. No drift,
4. Less effect due to noise and disturbance,
5. More compact and lightweight,
6. Less cost,
7. More flexibility in programming.

One distinct advantage of digital controllers is that they are more versatile than analog controllers. The program which characterizes a digital controller can be modified to accommodate design changes, or adaptive performances, without any variations on the hardware. Digital components in form of electronic parts, transducers and encoders are often more reliable, more rugged in construction, and more compact in size than their analog equivalents. These and other glaring comparisons are rapidly converting the control system technology into a digital one.

In recent years, parallel to the progress in discrete-data and digital control systems, problems of optimal

control have received a great deal of attention owing to increasing demand for systems of high performance and to the ready availability of the digital computer.

Along with interest and progress in control topics in general, interest in adaptive control systems has increased rapidly. The term adaptive implies that the system is capable of accomadating unpredictable environmental changes, whether these changes arise within the system or external to it. This concept has a great deal of appeal to systems designer since a highly adaptive system, besides accomadating environmental changes, would also accomodate moderate engineering design errors or uncertainties and would compensate for the failure of minor system components thereby increasing system reliability.

Under the light of above mentioned progresses we can try to improve transient response of control systems using switching techniques.

One basis for evaluating a system's performance is its time response to a step function input. A perfect response identical to the input with no error at any time. Such a response is impossible, therefore methods are studied to achieve the optimum performance of a system. There have been several criteria presented for optimizing the response of a system, using the step input as a reference. If the system is

required to produce a dead-beat response, one may write the equation describing such a response. The input to a given system producing this response can be obtained. Calling this a "modified input", one may then try to synthesize a network whose step response is the modified input. This network is called compensating network.

One method of compensating is using discrete compensators. This is done by modifying the input step signal into a two step staircase signal. This is known as Posicast compensators. In general, the step modification may be more complicated depending on the other features of the system.

The proposed compensating network modifies the input step by adding to it a pulse, or pulses. In order to achieve a dead-beat response, without overshoot, it is necessary to adjust the location, width and magnitude of this pulse. This mode of operation can be easily extended to higher-order systems.

Suppose a compensated system is in a changing environment causing the system's parameters to change. This will disturb the modified step response. To reobtain a dead-beat response under such variable conditions, it would be necessary to constantly adjust some parameters in the digital controller unit.

2- OPTIMAL CONTROL.

2.1. PROBLEMS OF OPTIMAL CONTROL.

By an optimal control system is meant a system which is the best in a certain sense. The optimality criteria on which a system is based can be most diverse and depend on the nature of the problem at hand. They include the accuracy of the control system against input signal variations, the transient process duration, integral criteria of a transient process, economic efficiency, productivity, complexity of the control system, and other technological and economic indices.

The principles of optimal control are being used on an ever increasing scale and they have helped in developing new automatic controllers, servos and other devices considerably improving the efficiency of industrial control systems.

Constraints on controls are chiefly attributable to limited power resources of the system. The phase coordinates, or the states of the system, are most frequently constrained for the sake of safety, strength, etc.

By plausible arguments and experimentation in the past it was believed that if a control system is being operated under limited power, then the system can be moved from one state to another in the shortest time by at all times properly utilizing all available power. This hypothesis is

called the "bang-bang principle". Although many time-optimal control systems with limited control power are of the bang-bang type, it is not true that all such systems are of this type. (For example, if the transfer function of a plant includes zeros, it can be shown that the strict bang-bang solution in which the control signal switches between the constant values u_0 and $-u_0$ is not optimal.)

For second-order systems, the phase-plane approach is the most convenient in determining the switching curve on which the sign of the control signal must be changed. For higher-order systems, however, in whatever approach is used, it can be quite difficult to find the switching surfaces in n -dimensional state space. In most cases, constructing explicitly the switching surfaces in n -dimensional state space is almost impossible.

The technical implementation of the optimal switching function is complicated even in primitive system, therefore practical problems are better solved by finding an equivalent switching function coinciding with in sign but easier to implement.

2.2. QUASI-OPTIMAL TECHNIQUES.

Although important results have been obtained in the theory of optimal control the practical use of this theory has been rather limited because the control systems for plants described by high order equations and subject to complex constraints are difficult to implement.

It is necessary to develop easily implementable approximate (quasi-optimal) control laws which do not differ much from the optimal ones as regards the criterion adopted. Quasi-optimal systems are also convenient for the following reasons.

1. Any control unit is made up of elements with limited possibilities and, consequently, certain constraints are imposed on selection of the control unit.

2. The mathematical model of the plant on which the control is based is often approximate because the structure and parameters of the plant are not always known in detail.

3. Strictly optimal control systems require detailed data on the system coordinates, input signals and their derivatives, which are very hard to come by in practical work. Thus, for instance, higher derivatives of the controlled coordinate cannot be measured without errors, which are often so large that prevent the use of the derivatives in the control law.

The ways of developing quasi-optimal systems can be classified into two groups: the use of an approximate model of the plant, ignoring the knowledge of strictly optimal control laws for an accurate model, and the use of simple hardware to approximate strictly optimal controls obtained in advance for the accurate model.

2.2.a. Simplified Mathematical Description of a Plant.

As an example of quasi-optimal control we will consider the following practical problem. A process includes a system used to control the parameter y . A control board carries only an indicator y and a setpoint unit with its own indicator of u . In this case the setpoint is the control action. To facilitate the operation, all controllers are made so that the readings of the indicators of y and u coincide in the steady state. If the controlled variable is to be changed from y_a to y_b , the simplest way to achieve this is to make the setpoint equal to u_b instead of u_a , which was associated with y_a . On completion of the transient process y will be equal to y_b .

However, an experienced operator who wishes to accelerate transition to new coordinates acts as follows. Precisely at the time t_0 when the conditions must be changed the maximal setpoint value $u = u_{\max}$ is set. Then $y(t)$ increases

sharply. At the time t_1 when y reaches the desired value, the setpoint is shifted to $u=u_b$. The time when the control is switched over is not calculated in advance and depends on the time taken to reach the desired point $y=y_b$.

A control action of this kind is strictly optimal for a first-order system. Indeed, at $t_0 \leq t \leq t_1$ the coordinate $y(t)$ changed under the effect of the greatest value of control while at the time t_1 the assignment of the setpoint $u=u_b=y_b$ stopped the change of $y(t)$, i.e. $y(t)=y_b$ at $t > t_1$. This can easily be verified by substituting $u=y$ into the equation of the system,

$$T \frac{dy}{dt} + y = u$$

then we obtain $dy/dt=0$, the coordinate $y(t)$ has ceased to change.

For higher-order plants with aperiodic transient process control of the above type is not strictly optimal because once $u=u_b$, the coordinate $y(t)$ may continue changing. Nevertheless, due to the forced operation in the time interval $[t_0, t_1]$ the transient process in such a system will achieve a steady state sooner than with conventional control given as a step from u_a to u_b .

The application of control which is strictly optimal for first-order systems to higher-order systems may

be interpreted as follows : replacement of actual equation of the system by a simpler one, determination of an extremal for this simple equation, and implementation of this extremal in order to control the original system. This approach to quasi-optimal control problems is the essence of simplified mathematical description.

Simplification does not , however, always lead to a first-order equation. In this case the extremal is a piecewise-constant function taking on the extreme values u_{\max} and u_{\min} , and the moments of switching are found from the solution of the associated variational problem of strictly optimal control.

2.2.b. Quasi-optimal Control of an Oscillatory Plant.

The above technique of quasi-optimal control in which the control action takes on extreme values while the moments of switching are found from a simplified mathematical model may prove unsatisfactory with oscillatory plants because even small errors in switching moments may result in large overshoots in the transient process.

For quasi-optimal control of oscillatory plants, the so called Posicast compensators can be proposed.

3. THE THEORY OF POSICAST CONTROL

To understand the theory of Posicast control, let us assume a frictionless pendulum as shown in Fig.(3.1). A weight is suspended as a pendulum and it is to be moved in the minimum time from vertical line i to the vertical line f . The control must be linear, and there must be no overshoot. The force can be applied only horizontally to the rolling support r . The support is moved initially to the midpoint m , as shown in Fig.(3.1.b), where it is held constant until the weight W swings to the final desired position f , as in Fig(3.1.c). Then suddenly the support is moved the remaining distance to f , as in Fig.(3.1.d), and the system will remain at rest.

The control motion is like casting a fly during fishing with a rod and reel; hence the name "Positive-cast" or Posicast control is given to this kind of control. The control mechanism is completely linear and limits the total transient time to one-half cycle, for the poles of the transfer function of a second-order system, without damping which we can also call it as half-cycle Posicast. There is no transient overshoot, and no oscillations. The impulse response of this type control is a sudden initial displacement and return

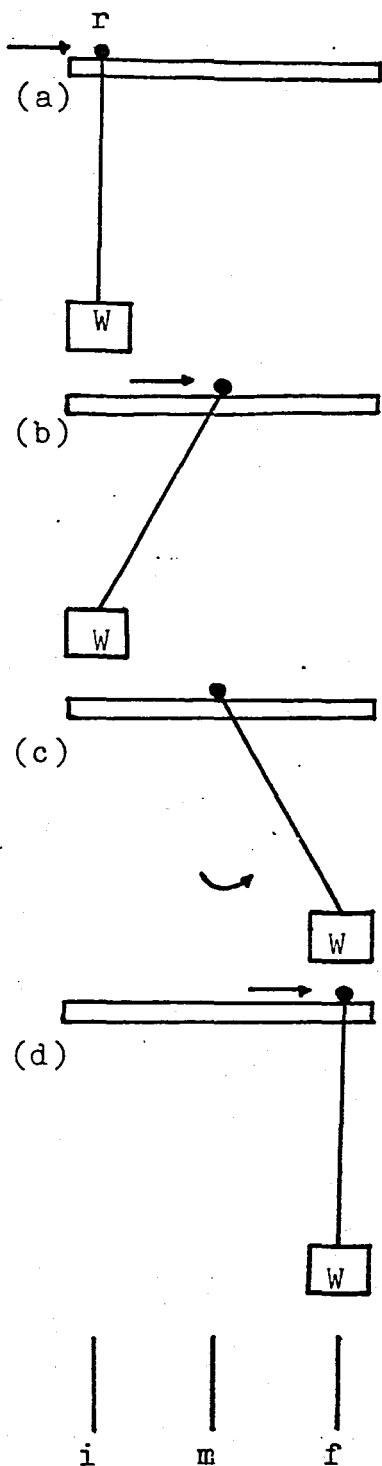


Fig.(3.1). Posicast control of a pendulum position through force application to the suspension only.

(a).Initial position.

(b).Control computer takes half of a unit input step and moves the support instantly to the midpoint m . Support remains fixed for one half period.

(c).Maximum swing of pendulum weight with support still fixed for one half period.

(d).Support suddenly moved to the final position f directly above the maximum swing point.

of r , delivering an impulse with momentum to weight W . The energy delivered is just sufficient to carry the weight to the maximum desired excursion. One fourth cycle later, it reaches i with maximum velocity. A second input impulse removes all the kinetic energy, and it remains stationary thereafter.

The secret of this type control is the division of the action into two times and two quantities. The second action time must follow the first action time by exactly one-half cycle of the transient if the superposition of the results is to be zero for all subsequent times. Any other action-spacing time would excite two oscillations whose vectors would not cancel, because they would always have the same phase-angle difference. The first quantity at the first action time must deliver exactly the amount of energy needed to swing the output to the desired final value in one-half cycle. The second quantity must remove all the remaining energy from the system. The energy must be in one form only, namely the kind initially delivered at the first action time. This is true if the natural transient half period is used to space the action times.

This kind of control can be used to control a

pair of complex poles with lightly damping. We can define a second-order system by the following differential equation

$$\ddot{c}(t) + 2\zeta\omega_n\dot{c}(t) + \omega_n^2c(t) = r(t) \quad (3.1)$$

where $r(t)$ is the input to the system and $c(t)$ is the corresponding output of the system.

As seen from the Eq.(3.1), the dynamical behavior of second order systems can be described in terms of two parameters ζ ; the damping ratio of the system, and ω_n ; the undamped natural frequency of the system.

The transfer function of such a system is

$$G(s) = \frac{C(s)}{R(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (3.2)$$

where the initial conditions are assumed to be zero.

If we try to apply posicast control to such a system with ζ in the range of $0 < \zeta < 1$ we must calculate peak time t_p and maximum overshoot M_p in order to find the magnitude of the first step and the application of time of the second step to be applied.

For the step input $r_1 u(t)$ we have

$$C(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{r_1}{s} \quad (3.3)$$

then the response in the time domain will be

$$c(t) = r_1 \left[1 - e^{-\zeta\omega_n t} \left(\cos\omega_d t + \frac{\zeta}{\sqrt{1-\zeta^2}} \sin\omega_d t \right) \right] \quad (3.4)$$

or

$$c(t) = r_1 \left[1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_d t + \phi) \right] \text{ for } t \geq 0 \quad (3.5)$$

which is shown in Fig.(3.2), where $\omega_d = \omega_n \sqrt{1-\zeta^2}$, $\phi = \tan^{-1} \left(\frac{\sqrt{1-\zeta^2}}{\zeta} \right)$

and $\sin \phi = \sqrt{1-\zeta^2}$, $\cos \phi = \zeta$

From Eq.(3.5), it can be seen that the frequency of the transient oscillations is the damped natural frequency which is equal to $\omega_n \sqrt{1-\zeta^2}$ and thus varies with the damping ratio; ζ .

From Eq.(3.5),

$$\begin{aligned} \frac{dc(t)}{dt} &= \frac{r_1 \omega_n e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \left[\zeta \sin(\omega_d t + \phi) - \sqrt{1-\zeta^2} \cos(\omega_d t + \phi) \right] \\ &= \frac{r_1 \omega_n e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_d t) \end{aligned} \quad (3.5)$$

At maximum overshoot; M_p , the derivative of the output must be zero

$$\left. \frac{dc(t)}{dt} \right|_{t=t_p} = \sin \omega_d t_p = 0 \quad (3.6)$$

that means

$$\sqrt{1-\zeta^2} \omega_n t_p = k\pi \quad (k=0,1,2,\dots)$$

where $k=1$ for maximum overshoot, then

$$t_p = \frac{\pi}{\omega_d} = \frac{\pi}{\omega_n \sqrt{1-\zeta^2}} \quad (3.7)$$

According to Posicast method we must obtain the desired value R , at time t_p and all $t_p < t$, from the output of the system. Then

$$c(t_p) = R = r_1 \left[1 - \frac{e^{-\pi\zeta/\sqrt{1-\zeta^2}}}{\sqrt{1-\zeta^2}} \sin(\pi - \phi) \right]$$

since

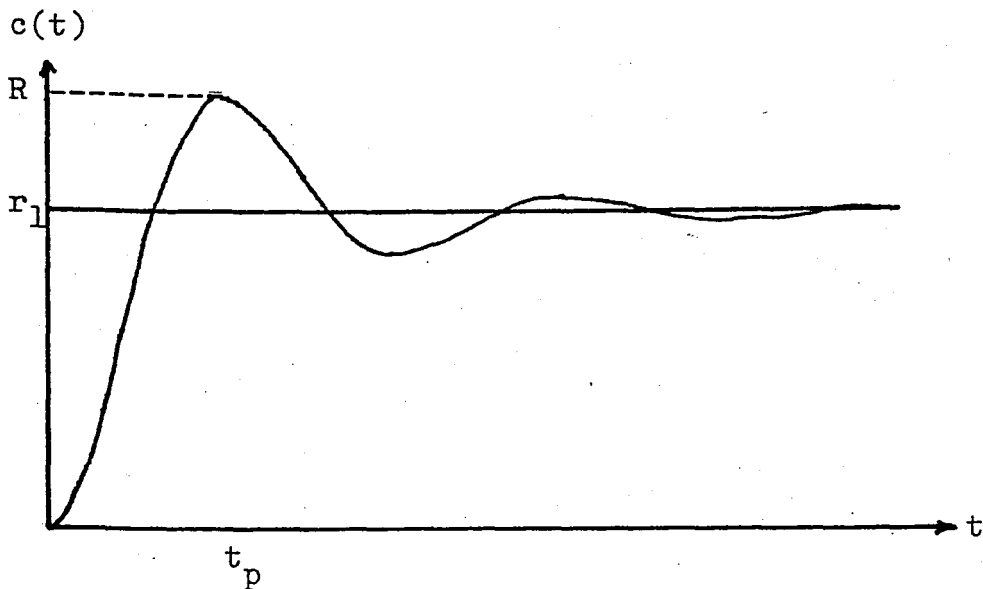
$$\sin(\pi - \phi) = -\sin \phi = -\sqrt{1-\zeta^2}$$

then

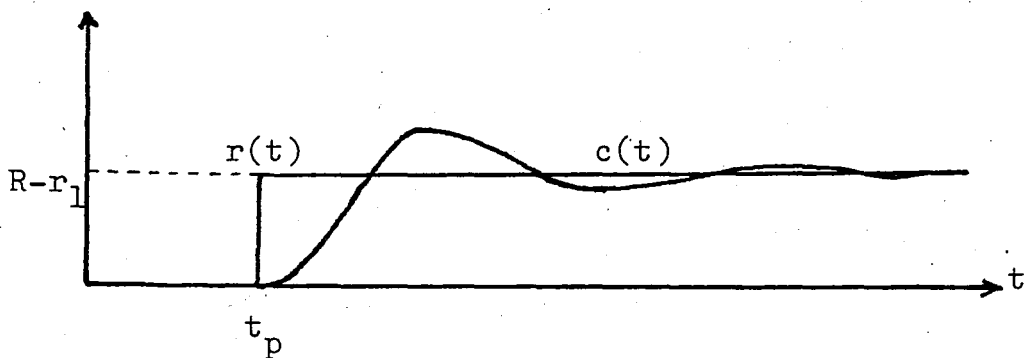
$$R = r_1 \left(1 + e^{-\frac{\pi\zeta}{\sqrt{1-\zeta^2}}} \right) = r_1 (1 + M_p)$$

that is

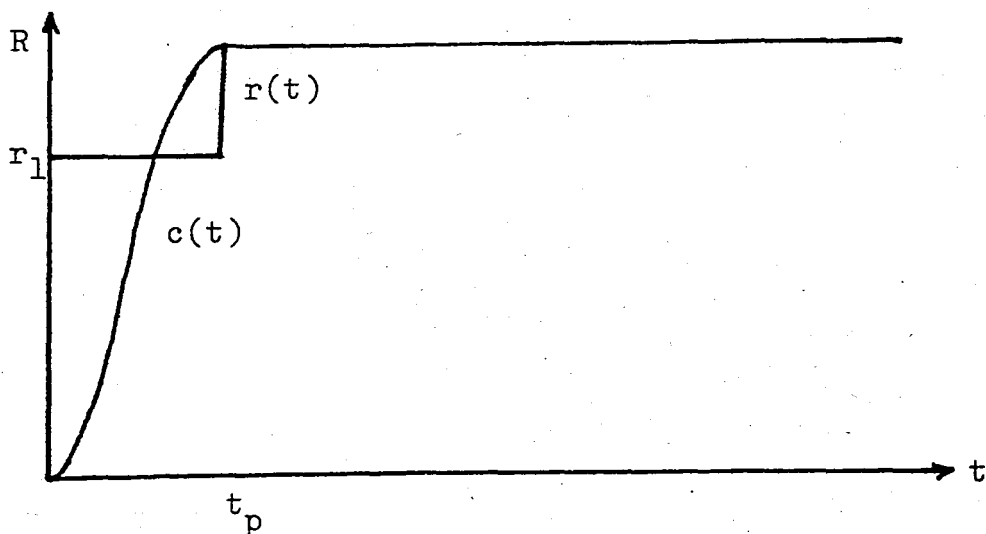
$$r_1 = \frac{R}{1 + M_p} \quad (3.8)$$



3.2.a. Response of the second order system to input, $r(t) = r_1 u(t)$



3.2.b. Response of the second order system to the input $r(t) = (R - r_1) u(t - t_p)$



3.2.c. Response of the system with Posicast control.

FIG. 3.2

The response to the input $r(t) = (R-r_1) u(t-t_p)$ is shown in Fig.(3.2.b).

So if we apply $r(t) = r_1 u(t)$ to the second order system the output function $c(t)$ has an overshoot at time t_p reaches a value R , i.e. $c(t_p) = R$. The moment t_p corresponds to the maximum of the function $c(t)$, i.e. $\dot{c}(t) = 0$, if the input receives a second step resulting in $r(t) = R$, then from Eq.(3.1) $\ddot{c}(t)$ becomes zero. The fact that the first and second derivatives are zeros for a second order system means that the transient process of $c(t)$ has set in, or that at $t > t_p$ $c(t) = \text{constant} = R$.

Consequently the input

$$r(t) = r_1 u(t) + (R-r_1) u(t-t_p) \quad (3.9)$$

ensures a transient process in an oscillatory plant, whose equation is given by Eq.(3.1), without an overshoot within the time given by Eq.(3.7) as shown in Fig.(3.2.c).

In an open loop system if we try to obtain the input function given by Eq.(3.9) from a step function of R/s we have to design a controller with the transfer function

$$D(s) = \frac{R(s)}{R/s} = \frac{r_1}{R} + \frac{R-r_1}{R} e^{-t_p s} \quad (3.10)$$

Fig.(3.3) shows the control system block diagram. Although this is a linear system, it is not possible to interchange the order of components. With the Posicast control first, the oscillations are prevented from starting. With the Posicast control following the complex poles, it only prevents the output from seeing the undesired oscillations.

As seen from Eq.(3.10), $D(s)$ may only has zeros.

Then

$$D(s) = \frac{r_1}{R} + \frac{R-r_1}{R} e^{-t_p s} = 0$$

we obtain

$$e^{-t_p s} = -\frac{r_1}{R-r_1}$$

where $s = a + jb$, which gives the following equation

$$e^{-at_p} \cdot e^{-jbt_p} = \frac{r_1}{R-r_1} e^{-j(2k+1)\pi}, \quad k=0, \pm 1, \pm 2, \dots$$

From the magnitude equality

$$e^{-at_p} = \frac{r_1}{R-r_1} = \frac{1+M_p^{-1}}{1+M_p} = M_p^{-1} = e^{+\zeta \omega_n t_p}$$

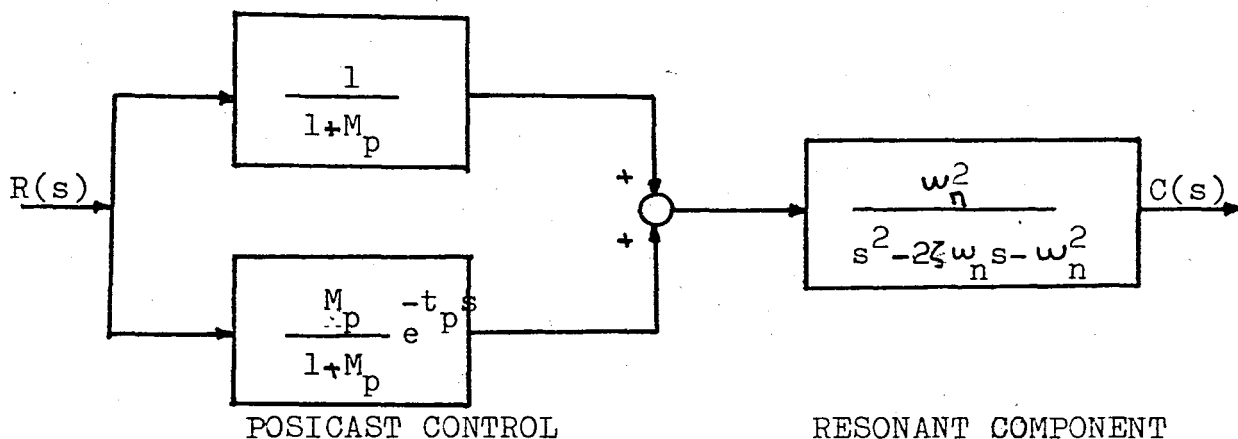


Fig.(3.3). Posicast control of a lightly damped second-order system.

that is

$$e^{-(a+\zeta\omega_n)t_p} = 1$$

which means

$$a = -\zeta\omega_n$$

From the phase equality of Eq.(3.11)

$$bt_p = (2k+1)\pi \quad k = 0, \bar{1}, \bar{2}, \dots$$

since $t_p = \frac{\pi}{\omega_n \sqrt{1-\zeta^2}}$

then

$$b = (2k+1)\omega_n \sqrt{1-\zeta^2} = (2k+1)\omega_d$$

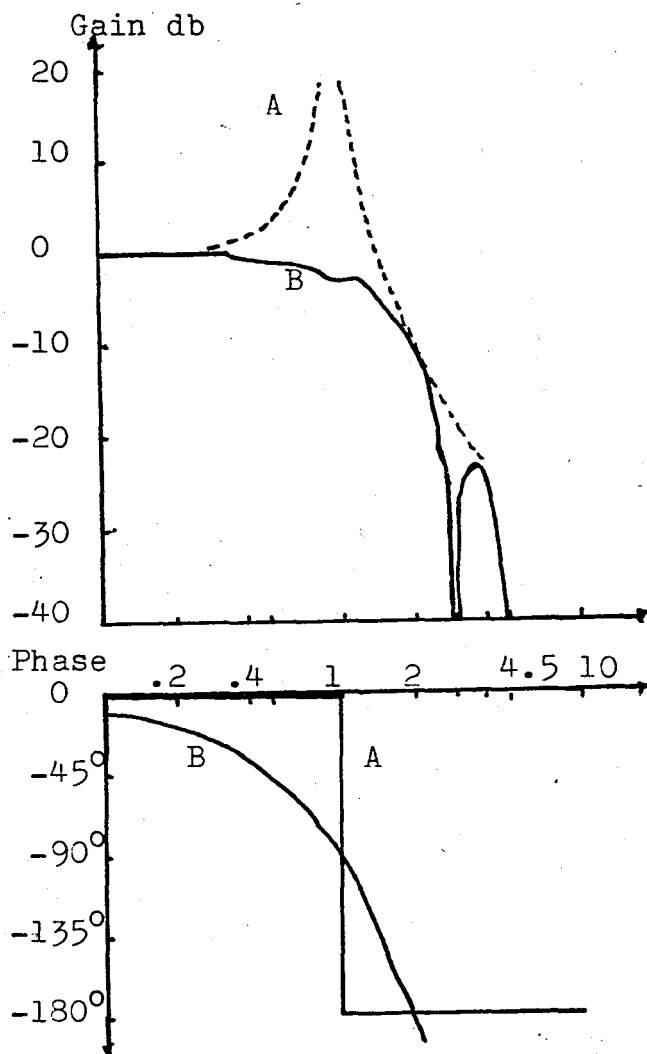
The over-all frequency response of the system is shown in Fig.(3.4). The high resonant peak has been

Fig.(3.4).

Frequency response
of system with

Posicast compensator
(A). Undamped resonant
pair of poles alone
without compensator.

(B). Undamped resonant
pair of poles with
Posicast compensator.



reduced to approximately -3 db. The formerly rapid change of phase of curve (A) near the resonant frequency has been converted into the linear phase lag with frequency of curve (B). This phase characteristics is ideal for good wave shape reproduction. The frequency response is excellently flat throughout the passband, and has its ripples or nulls only in the stopband.

Fig.(3.5)

s-plane patterns
for half-period
control of complex
pole pair.

(a).Original

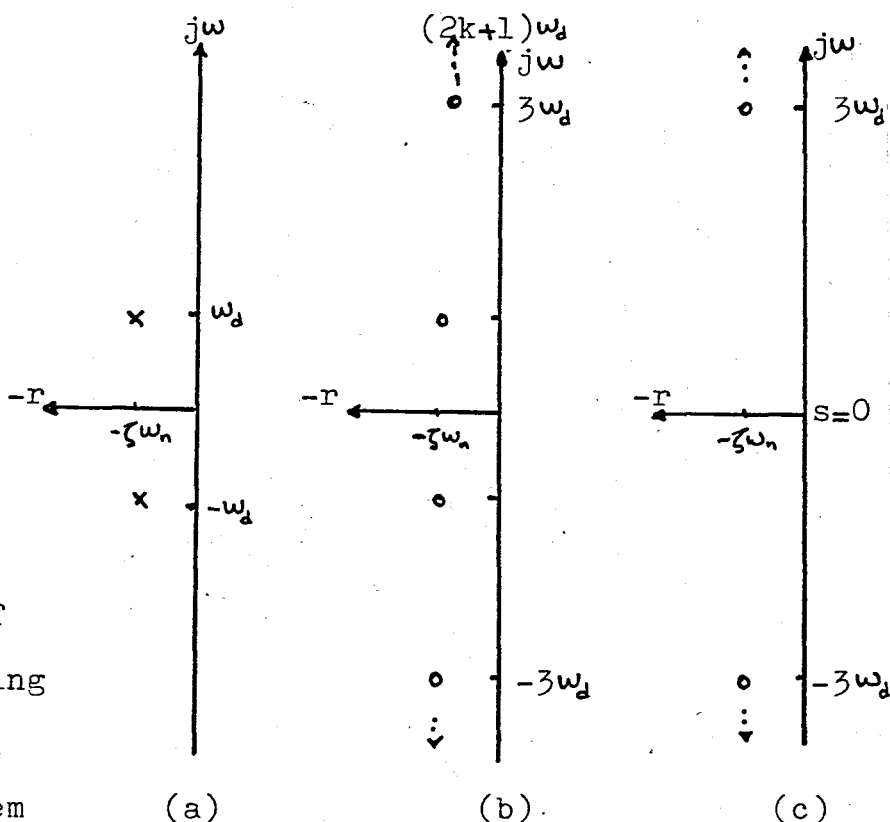
lightly damped
pole pair

(b).Transference of

Posicast compensating
section alone.

(c).Resultant system

with half period response.



The frequency response can also be interpreted from the s-plane plot shown in Fig.(3.5). The Posicast compensating section has an infinite column of complex zeros spaced at odd integers along the frequency scale. The lowest frequency complex zeros are made to coincide with the resonant poles. They cancel the poles completely from a frequency viewpoint. There still remains an infinite column of zeros outside of the useful frequency band. This passband characteristic can be compared with a maximally flat (Butterworth) or an equal

ripple (Chebyshev) design. In these classical designs, a band of poles is distributed through the frequency range, with nothing outside. The frequency response is therefore rippled in the useful frequency range and is smooth at the unimportant high frequencies. In the Posicast control the frequency response is smooth in the passband and rippled at the unimportant high frequencies. By slightly detuning the complex zeroes, an extremely flat frequency response can be obtained up through the resonant frequency. This causes a small transient overshoot.

4. DEVELOPMENT OF POSICAST METHOD.

A second order system given by the differential equation (3.1) can be represented by the compact notation of the state vector differential equation

$$\dot{\underline{x}}(t) = \underline{A} \underline{x}(t) + \underline{b} r(t) \quad (4.1)$$

where $\underline{x}(t) = \begin{bmatrix} c(t) \\ \dot{c}(t) \end{bmatrix}$, $\underline{A} = \begin{bmatrix} 0 & 1 \\ -\omega_n^2 & -2\zeta\omega_n \end{bmatrix}$

and $\underline{b} = \begin{bmatrix} 0 \\ \omega_n^2 \end{bmatrix}$

We can write the plant equation of second-order system with Posicast compensator by assuming an over all input to the whole system of $u_r(t) = R u(t)$ and from the equation (4.1) and Fig.(3.3)

$$\frac{d}{dt} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\omega_n^2 & -2\zeta\omega_n \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{\omega_n^2}{1+M_p} (1+M_p u(t-t_p)) \end{bmatrix} u_r(t)$$

(4.2)

As seen from Eq.(4.2) the system is a time varying system.

The state transition matrix $\Phi(t, t_0)$, is found as

$$\Phi(t, t_0) = \frac{e^{-\zeta \omega_n (t-t_0)}}{\omega_d} \begin{bmatrix} \omega_n \sin(\omega_d (t-t_0) + \phi) & \sin \omega_d (t-t_0) \\ -\omega_n^2 \sin \omega_d (t-t_0) & -\omega_n \sin(\omega_d (t-t_0) - \phi) \end{bmatrix} \quad (4.3)$$

If any time-varying system has $\Phi(t, t_0)$ and $\underline{b}(t)$ so that $\Phi(t, t_0) \underline{b}(t)$ has columns or rows which are linearly independent on $t_0 \ll t \ll t_1$ then this system is controllable on $t_0 \ll t \ll t_1$.

If we apply this criterion to our system we obtain

$$\Phi(t, t_0) \underline{b}(t) = \frac{\omega_n^2}{\omega_d} (1 + M_p u(t-t_p)) \frac{e^{-\zeta \omega_n (t-t_0)}}{1 + M_p} \begin{bmatrix} \sin \omega_d (t-t_0) \\ -\omega_n \sin(\omega_d (t-t_0) - \phi) \end{bmatrix} \quad (4.4)$$

since $\phi \neq 0$ Eq.(4.4) never becomes zero. Then the system given by Eq.(4.2) is controllable for $t \gg 0$.

By applying $u(t)$ to the in Fig.(3.3) in order to reach to the state of $(R \ 0)$ at time t_p , from the solution of Eq.(4.2) we can write

$$\underline{x}(t_p) = \underline{\Phi}(t_p, 0)\underline{x}(0) + \int_0^{t_p} \underline{\Phi}(t_p, \tau)\underline{b}(\tau)u(\tau) d\tau \quad (4.5)$$

where

$$\int_0^{t_p} \underline{\Phi}(t_p, \tau)\underline{b}(\tau)u(\tau) d\tau = \frac{1}{1+M_p} \frac{\omega_n^2}{\omega_d} \begin{bmatrix} \int_0^{t_p} e^{-\zeta\omega_n\tau} \sin\omega_d\tau d\tau \\ -\omega_n \int_0^{t_p} e^{-\zeta\omega_n\tau} \sin(\omega_d\tau - \phi) d\tau \end{bmatrix}$$

$$= \begin{bmatrix} R & 0 \end{bmatrix}^T$$

and

$$\underline{\Phi}(t_p, 0) = -e^{-\zeta\omega_n t_p} \underline{I}$$

then Eq.(4.5) becomes

$$\begin{bmatrix} R \\ 0 \end{bmatrix} = -e^{-\zeta\omega_n t_p} \begin{bmatrix} c(0) \\ \dot{c}(0) \end{bmatrix} - \begin{bmatrix} R \\ 0 \end{bmatrix} \quad (4.6)$$

To satisfy Eq.(4.6) $c(0)$ and $\dot{c}(t)$ must be equal to zero

From Eq.(4.5) and (4.6) we can say that in the configuration shown in Fig.(3.3) we can reach to the desired vector of state only when the initial conditions are zero. This configuration proposed by O. Smith is an open loop system. To obtain a closed loop automatic control system by the same method, we must develop Posicast method so that we can use it when the initial state vector is nonzero.

The solution of Eq.(3.1) by considering initial conditions $c(0) = c_0$ and $\dot{c}(t) = \dot{c}_0$ is

$$c(t) = r_1 - \frac{e^{-\zeta \omega_n t}}{\sqrt{1-\zeta^2}} \left[(r_1 - c_0) \sin(\omega_d t + \phi) - \frac{\dot{c}_0}{\omega_n} \sin \omega_d t \right] \quad (4.7)$$

At maximum peak $\dot{c}(t_p)$ must be equal to zero then

$$t_p = \frac{1}{\omega_d} \arctan \frac{\dot{c}_0 \sqrt{1-\zeta^2}}{\dot{c}_0 \zeta - (r_1 - c_0) \omega_n} \quad (4.8)$$

From Eq.(4.8) t_p is found to be dependent on the value of c_0 and \dot{c}_0 . We can calculate r_1 from $c(t_p) = R$

relation, but such a calculation is time consuming during application. So it is difficult to realize such a system. If we restrict the system so that c_0 is zero at the state we are going to apply Posicast control to reach another state, then

$$t_p = \frac{\pi}{\omega_d}$$

and from the condition $c(t_p) = R$

$$r_1 = \frac{R + c_0 e^{-\zeta \omega_n t_p}}{1 + e^{-\zeta \omega_n t_p}} \quad (4.9)$$

where

$$e^{-\zeta \omega_n t_p} = M_p$$

So the magnitude of the first step will be

$$r_1 = \frac{1}{1 + M_p} R + \frac{M_p}{1 + M_p} c_0 \quad (4.10)$$

Finally by controlling the derivative of output we can construct the closed-loop Posicast control of second order system as shown in Fig.(4.1).

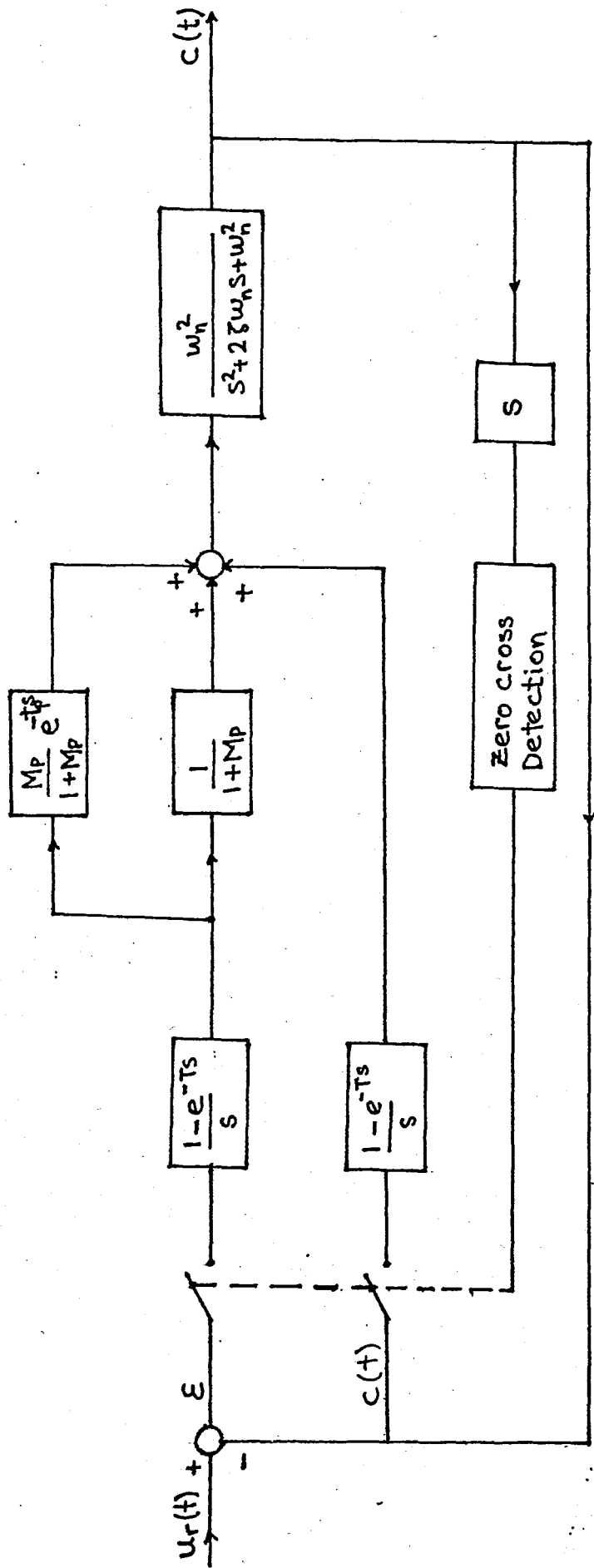


Fig. (4.1) Closed Loop Posicast Control of a Second-order System.

5. ANALOG COMPUTER SIMULATION OF A SECOND-ORDER SYSTEM

In course of analysis and design of complicated systems , analog computer simulation plays an important role. The effects of change in system parameters on the performance of the system can be easily determined.

To get a general result in application of Posicast control on second-order systems, analog computer simulation of the second order system shown in Fig.(5.1) is used.

To find the value of components used to realize the configuration shown in Fig.(5.1) we have to make some calculations in order not to saturate the outputs of the operational amplifiers, so that the linearity of the system is always achieved and furthermore scale the system variables to appropriate levels for observation and feedback purposes.

Mathematical solution of Eq.(3.1) is given in Eq.(3.5) and the derivative of the solution ,i.e. $\dot{c}(t)$ is given in Eq.(3.5)

From Eq.(3.5) $\ddot{c}(t)$ is calculated as follows

$$\ddot{c}(t) = - \frac{r}{\sqrt{1-\zeta^2}} e^{-\zeta \omega_n t} \sin(\omega_d t - \phi) \quad (5.1)$$

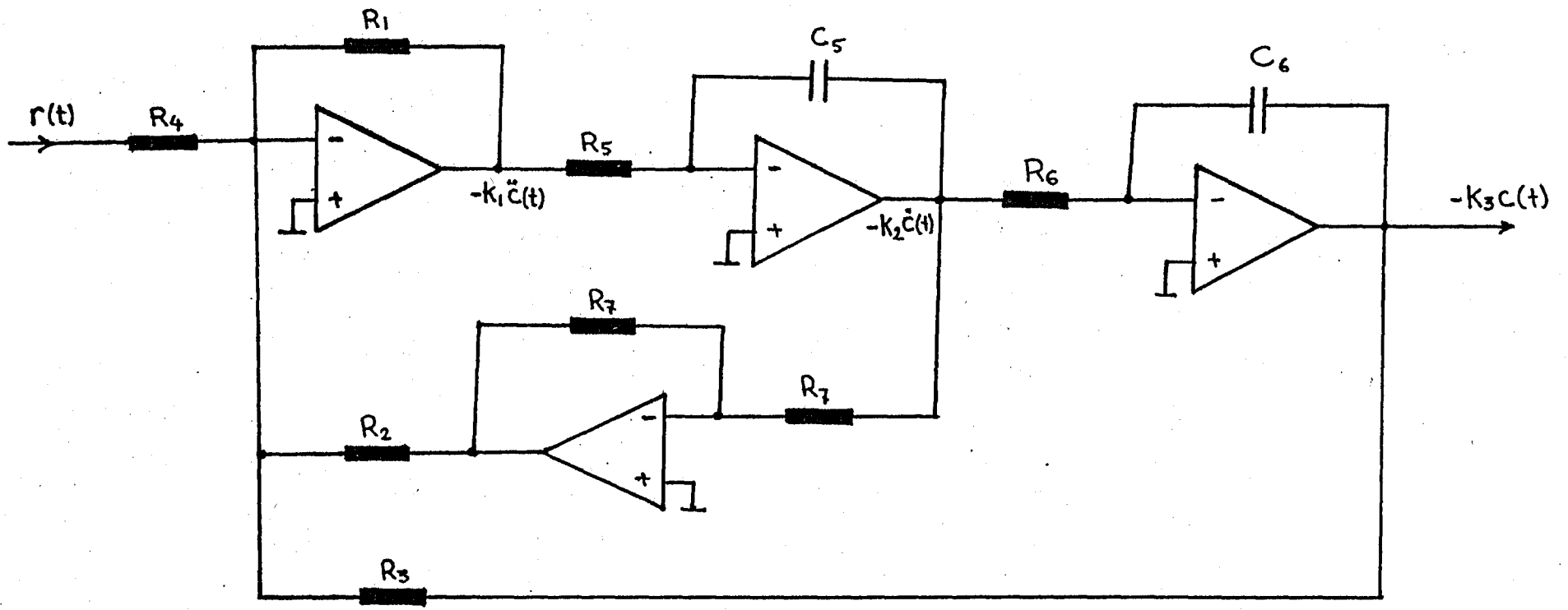


Fig.(5.1). Analog Computer Simulation of the Second-Order System

From equations (3.1) , (3.5) and (5.1) ,choosing $\zeta = 0.304$ and $\omega_n = 164.317$ rad/sec and by applying maximum input of 6volts we can calculate the maximum values of $c(t)$, $\ddot{c}(t)$ and $\dot{c}(t)$ as follows,

$$\text{Maximum value of } |c(t)| = 3.037 \times 10^{-4}$$

$$\text{Maximum value of } |\dot{c}(t)| = 2.440 \times 10^{-2} \text{ sec}^{-1}$$

$$\text{Maximum value of } |\ddot{c}(t)| = 6.299 \text{ sec}^{-2}$$

If we rewrite Eq.(3.1) by replacing the ζ and ω_n values and scaling the variables, we can write

$$k_1 \ddot{c}(t) + 100 \frac{k_1}{k_2} (k_2 \dot{c}(t)) + 27000 \frac{k_1}{k_3} (k_3 c(t)) = k_1 r \quad (5.2)$$

Each operational amplifier in the configuration shown in Fig.(5.1) has limited output of ± 6 volts. Then we can calculate the scaling factors by dividing maximum allowable output voltage of each operational amplifier to maximum value of each variable.

$$k_1 = \frac{\text{Max.output voltage}}{\ddot{c}_{\max}} = 0.953$$

$$k_2 = \frac{\text{Max.output voltage}}{c_{\max}} = 245.857$$

$$k_3 = \frac{\text{Max.output voltage}}{c_{\max}} = 197.57496$$

Finally from Fig.(5.1) and from the input stage of the configuration we can write

$$\ddot{c}(t) + \frac{k_2}{k_1} \frac{R_1}{R_2} \dot{c}(t) + \frac{k_3}{k_1} \frac{R_1}{R_3} c(t) = \frac{1}{k_1} \frac{R_1}{R_4} r \quad (5.3)$$

Then from equations (5.2) and (5.3) the component relations are as follows

$$\frac{R_1}{R_4} = 0.953$$

$$\frac{R_1}{R_3} = 27000 \frac{k_1}{k_3} = 1.301$$

$$\frac{R_1}{R_2} = 100 \frac{k_1}{k_2} = 0.337$$

$$\frac{1}{R_5 C_5} = \frac{k_2}{k_1} = 258.096$$

$$\frac{1}{R_6 C_6} = \frac{k_3}{k_2} = 80.362$$

by arbitrarily choosing $R_1 = 6800 \Omega$ and $C_5 = C_6 = 1 \times 10^{-6} \text{ F}$
we can find the values of other components as

$$R_4 = 7138.51 \Omega$$

$$R_3 = 5223.70 \Omega$$

$$R_2 = 17550.65 \Omega$$

$$R_5 = 3874.53 \Omega$$

and

$$R_6 = 12443.73 \Omega$$

However these values are approximated to some nearer values during construction of the circuit.

The step response of the simulated second-order system without any compensation is shown in Fig.(6.2) which is very close to the theoretical response.

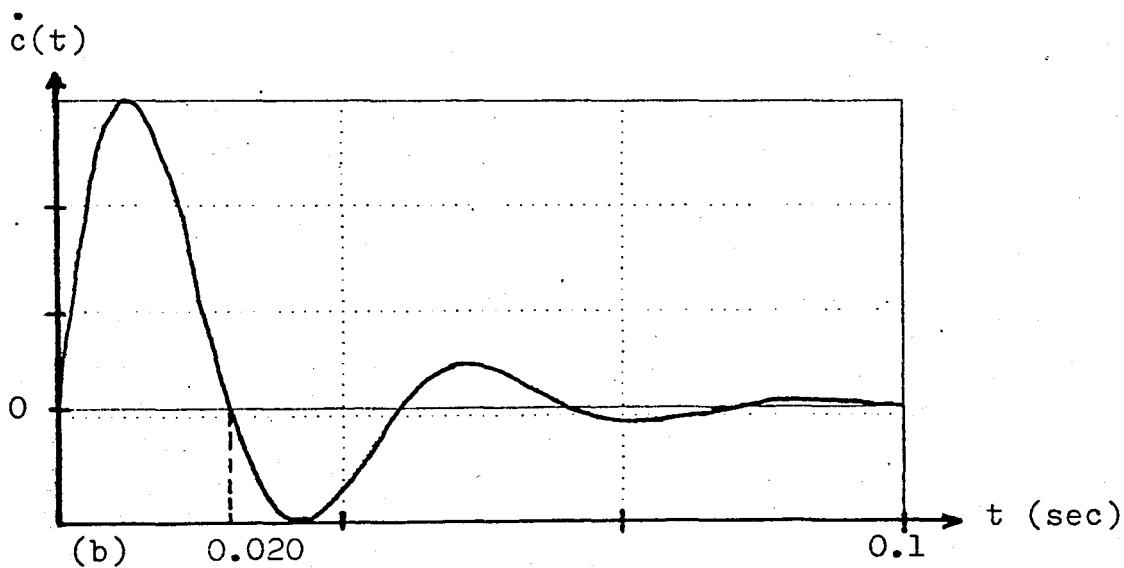
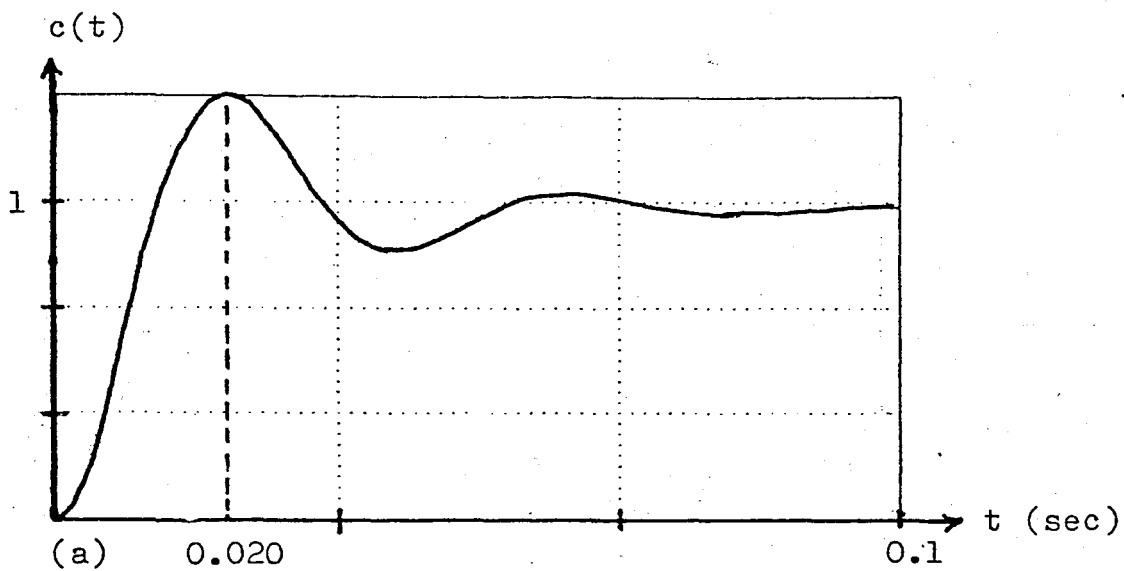


Fig.(5.2)

(a) Step response , (b) derivative of the step response of the system shown in Fig.(5.1)

6.DIGITAL CONTROLLER UNIT

6.1.DIGITAL CONTROLLER SPECIFICATIONS

The digital controller used in this work is a conventional Z80 system with 4K-memory capacity. The 2K of the memory is assigned to ROM (2716) area, the rest of the memory is assigned to RAM (6116) area. A Z80 PIO is used for controlling Digital to Analog and Analog to Digital converters. A Intel 8255 PPI can also be added to the controller to interface a simple keyboard and display combination for developing user programs in the RAM area. The system clock rate is 2.5 MHz.

The controller needs three different voltages of +5V, +12V and -12V. There are on board regulator ICs, 7805, 7812 and 7912 for power requirements of the digital controller as shown in Fig.(6.1).

The clock, address decoding, reset circuitries and connections of RAM, ROM and CPU are shown in Fig.(6.2).

The clock circuitry is a simple oscillator with a 2.4576 MHz crystal. Oscillation frequency is the crystal frequency. The output of the oscillator is called the system

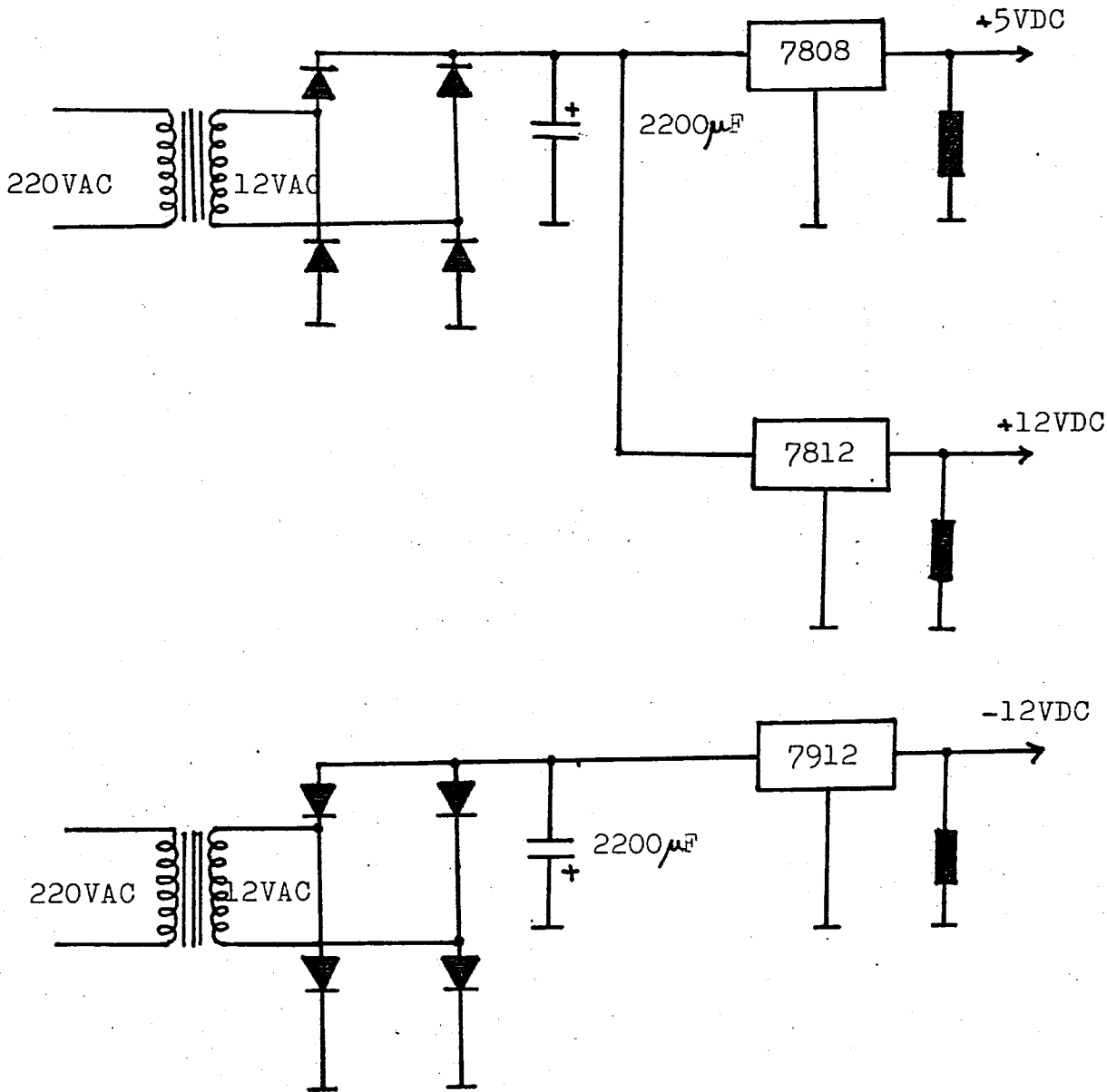


Fig.(6.1) Power supply of the digital controller.

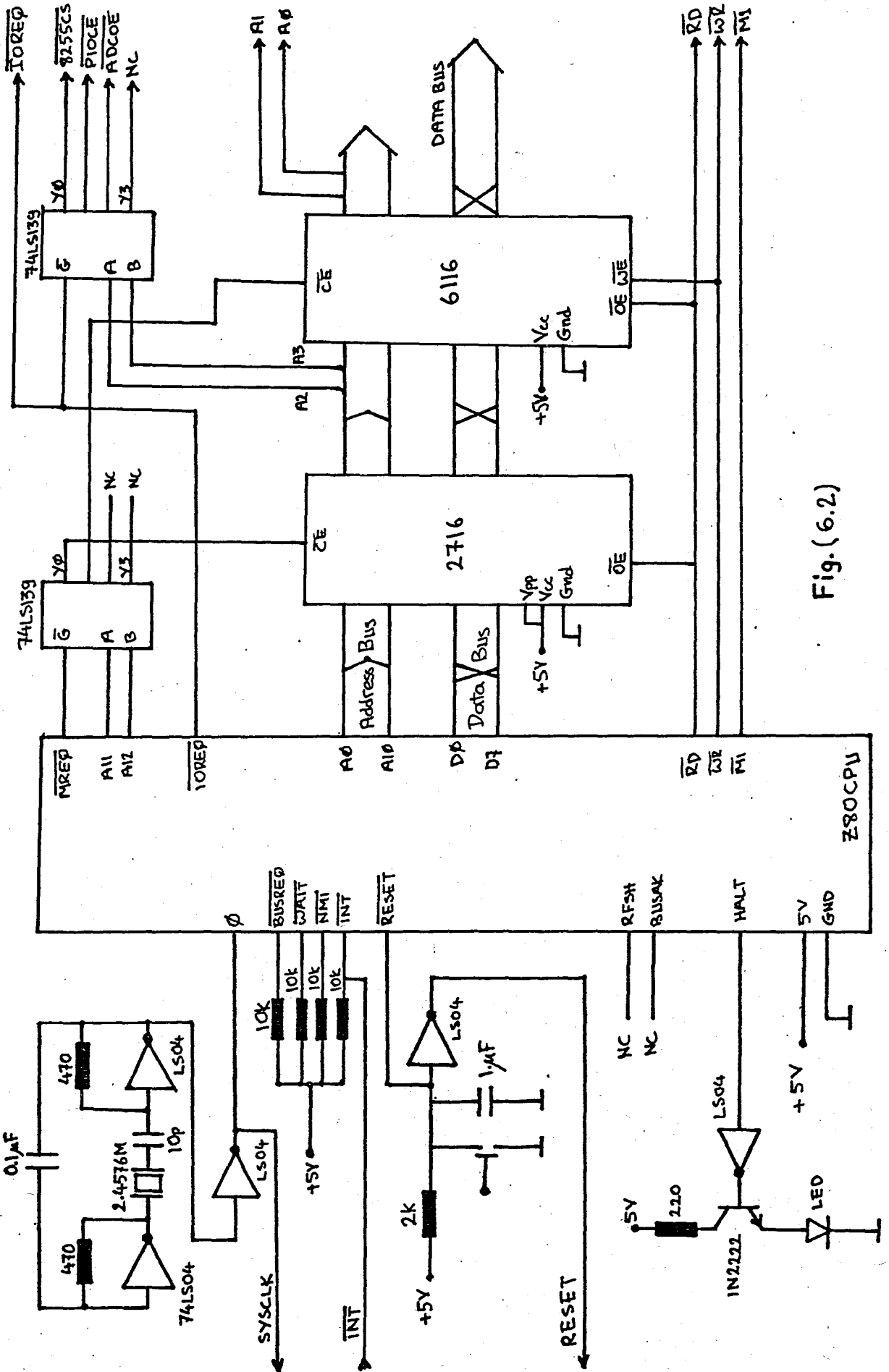


Fig. (6.2)

clock and is used by Z80 CPU and Z80 PIO.

Address decoding circuitry selects only one device during memory or I/O access of CPU. Address lines A11 and A12 and the control signal $\overline{\text{MREQ}}$ of CPU are used to select memory devices. Address decoding for memory devices is shown in the table below

$\overline{\text{MREQ}}$	A15	A14	A13	A12	A11	
0	X	X	X	0	0	EPROM is selected
0	X	X	X	0	1	RAM is selected
0	X	X	X	1	X	Not used
1	X	X	X	X	X	None of the memory devices is selected

where X stands for don't care conditions. Since the addresses of the devices is not full decoded, 8 different addresses may select the same memory location in the same device. However during programming A13, A14, A15 are assumed to be zero logic voltage level. Then the addresses from 0000H to 07FFH is assigned to EPROM and addresses from 0800H to 0FFFH is assigned to RAM.

Address lines A2, A3 and control signal $\overline{\text{IOREQ}}$

of CPU are used for selecting only one I/O device during I/O access of CPU. Address decoding for I/O devices is shown in the table below,

<u>IOREQ</u>	A7	A6	A5	A4	A3	A2	A1	A0	
0	X	X	X	X	0	0	X	X	8255 PPI is selected
0	X	X	X	X	0	1	X	X	Z80 PIO is selected
0	X	X	X	X	1	0	X	X	D/A Converter is selected
0	X	X	X	X	1	1	X	X	Not used
1	X	X	X	X	X	X	X	X	None of the I/O devices is selected.

This time because of not full decoding, 16 different addresses can address the same register of the same I/O device. Again during programming A4 to A7 lines are assumed to be in zero logic voltage level. Address lines A0 and A1 during I/O access are used to access the internal registers of the selected device. Then we can write the addresses of the I/O ports as

- 0 Port A of 8255 PPI
- 1 Port B of 8255 PPI
- 2 Port C of 8255 PPI
- 3 Control register of 8255 PPI

- 4 Port A-data register of Z80 PIO
- 5 Port A-control register of Z80 PIO
- 6 Port B-data register of Z80 PIO
- 7 Port B-control register of Z80 PIO
- 8 A/D converter \overline{OE} signal

Since \overline{BUSREQ} , \overline{WAIT} , \overline{NMI} pins of Z80 CPU are not used they are tied to 5-volt level.

A Z80 PIO is used to control A/D and D/A converters as shown in Fig.(6.3). The Z80 PIO is Zilog's parallel interface device. It 16 I/O pins, divided into two 8-bit I/o ports. Each I/O port has two associated control lines which are left open in this controller. The two Z80 PIO I/O ports may be separately specified as input, output or control ports.

Port A of Z80 PIO is specified as output and used as a latch device for D/A converter. Port B is specified as control port. The lower 4 bits of port B are specified as input signals and the 4 upper bits of port B are specified as output signals. Bit 0 of port B checks the end of conversion (EOC) status line of ADC0800. Bit 7 of port B starts conversion in ADC0800 by applying 5volts. Bit 1 of port B checks a signal DER which is a

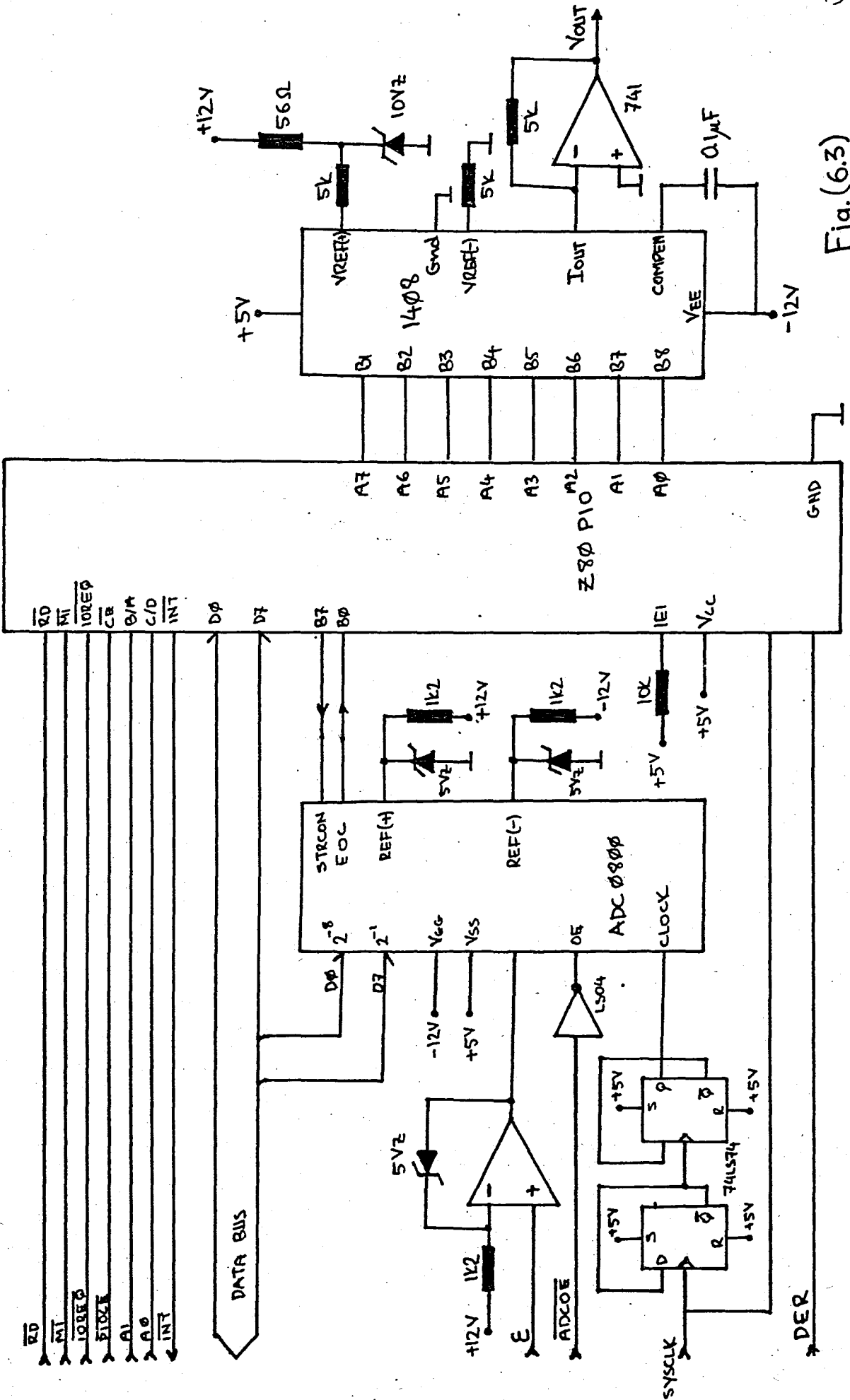


Fig.(6.3)

TTL level signal will be mentioned later.

6.2. THE 1408 8-BIT DIGITAL TO ANALOG CONVERTER

The 8-bit Digital to Analog Converter 1408DAC is used in this controller for analog signal output. The 1408 DAC is admittedly a relatively primitive, low-performance device when compared to other DAC devices, the wide availability and resultant low price justify its usage. It has a settling time of 300 nsecs.

The 1408 device provides a single output on pin 4 (I_O). This output is a current sink with a maximum rating of 4.2 milliamperes. An external op-amp is used by holding I_O pin DAC at virtual ground of the op-amp. The output compliance is extended to accommodate a range of 0 to 10 volts by using a negative supply voltage V_{EE} more negative than -10 volts, i.e. -12 volts. RANGE CONTROL pin is left open since extended output voltage compliance operation is needed.

The 1408 device can be operated in either a unipolar or a bipolar mode. In Fig.(6.3), it is operated in unipolar mode. Straight binary coding is used and expected output

values for various digital input codes are shown in the table below

Output Scale	B1	B2	B3	B4	B5	B6	B7	B8	I_{OUT} (mA)	V_{OUT}
Full scale	1	1	1	1	1	1	1	1	-1.992	9.960
Full scale-LSB	1	1	1	1	1	1	1	0	-1.984	9.920
Half scale+LSB	1	0	0	0	0	0	0	1	-1.008	5.040
Half scale	1	0	0	0	0	0	0	0	-1.000	5.000
Half scale-LSB	0	1	1	1	1	1	1	1	-0.992	4.960
Zero scale+LSB	0	0	0	0	0	0	0	1	-0.008	0.040
Zero scale	0	0	0	0	0	0	0	0	0.000	0.000

In this configuration the reference current is 2.0 mA which is recommended for this device.

6.3. THE ADC 0300 8-BIT ANALOG TO DIGITAL CONVERTER

The ADC 0300 8-bit A/D converter is used in Fig. (6.3). The ADC 0300 uses the successive approximation technique to perform an analog to digital conversion. It can perform a conversion of an analog value in a minimum of 50 microseconds. An 8-bit latch with three-state output is provided on the device, an external clock and voltage

reference must be supplied. The ADC 0300 is a PMOS device and requires +5 volt (V_{SS}) and -12 volt (V_{GG}) power supplies. The analog input can range from -5 to +5 volts.

The ADC 0800 has several shortcomings. First of all, the non-linearity of this device specified as ± 1 LSB at 25°C , and this non-linearity is specified as ± 1 LSB over the full operating temperature range of this device. Thus, although the device is guaranteed to have no missing codes and will obviously always provide eight bits of resolution, it is not guaranteed to provide 3-bit accuracy at 25°C you are only guaranteed 7-bit accuracy; while over the full operating temperature range the device provides only 6-bit accuracy.

The second shortcoming of the ADC 0300 is its power requirement. It requires more power than its counterparts. This is due to the fact that the ADC 0300 is manufactured using PMOS technology, which is much more power hungry than the CMOS process used by most of the other ADC devices.

The eight data output lines from the ADC 0300 are directly connected to the data bus of the system.

The data lines are in high impedance state, except when output enable signal is high. The complement of OE is obtained from Fig.(6.2) as if ADC 0800 were an I/O register. By inverting $\overline{\text{ADCOE}}$ signal we obtain OE signal for ADC0800.

The data output upon completion of conversion is complementary binary coded : the largest positive value is all zeros (0000 0000).

A 0.625 MHz. clock is continuously applied to ADC 0800 during operation. This clock is obtained by dividing the system clock by 4 as shown in Fig.(6.3). A conversion operation initiated by setting START high. While the start signal can be applied asynchronous in relation to the clock input, the duration of start pulse is specified as 1 clock period minimum and 3 1/2 clock periods maximum. If start pulse is less than 1 clock period in duration, the "start conversion" command may be ignored and if the pulse exceeds 3 1/2 clock periods, then conversion errors may be introduced.

When the START signal is first set high, the EOC signal will go low, indicating that a conversion process is in progress. The conversion operation requires 40 clock

periods, i.e. 64 microseconds. At the end of this interval time, the EOC signal will go high to indicate that conversion is presented in the output data latch.

The REF(+) is connected to +5volts and the REF(-) is connected to -5 volts, then the analog input range is ± 5 volts. To change voltages from 0 volts to +10 volts into voltages from -5 to -5 volts a level shifting circuit is used as shown in Fig.(6.3).

6.4.ADDITIONAL HARDWARE FOR DEVELOPING USER PROGRAMS IN THE RAM AREA.

We can add Intel's 8255 PPI based circuitry with a simple keyboard and 7-segment display combination to develop control routines for this digital controller.

The 3255 PPI scans the key matrix while scanning the 7-segment display group. The proposed hardware is shown in Fig.(6.4) and a 500-byte monitor for this circuitry is given in Appendix .

There are 16 keys for hexadecimal numbers, 1 key for choosing address entry mode and 1 key for choosing

7-Segment Display Group

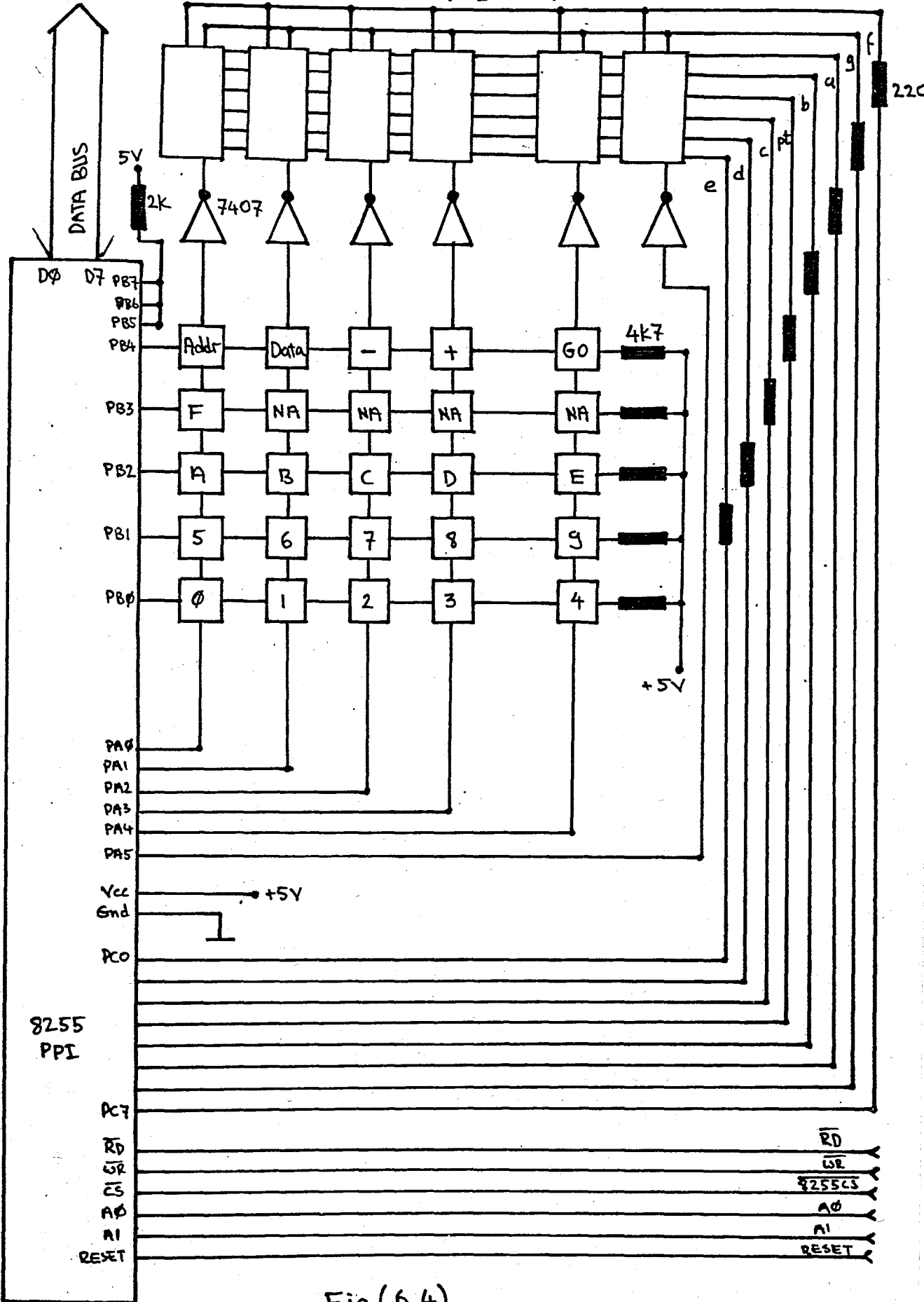


Fig (6.4)

data entry mode of input from keyboard, two keys for incrementing and decrementing the current address pointer of the memory. The other 4 keys are left unassigned for future defining of special function keys. The last key is used to run the program in the memory starting from the current memory location.

7. APPLICATION OF ADAPTIVE POSICAST CONTROL TO A LIGHTLY DAMPED SECOND ORDER SYSTEM.

7.1. INTERFACE CIRCUITS.

The lightly damped second-order system is simulated as explained in chapter 3 with known parameters and it is controlled by a Z80 based digital controller with a single analog input and a single analog output in the range of 0 to 10 volts.

In order to apply Posicast control to the lightly damped second-order system the set-up shown in Fig.(7.1) is constructed. The simulated system can have input and output in the range of -6 to +6 volts. So the amplifiers shown in Fig.(7.1) with coefficients K_A , K_B and K_C represent the interface circuits. The zero-cross detection circuitry has the input of $k_2 \dot{c}(t)$ and has the output of DER. DER is a TTL level signal which is zero when the derivative of the output of the system is zero.

In order to improve the resolution of the digital circuitry, the system is controlled in one direction, i.e. only positive reference voltages will be applied to

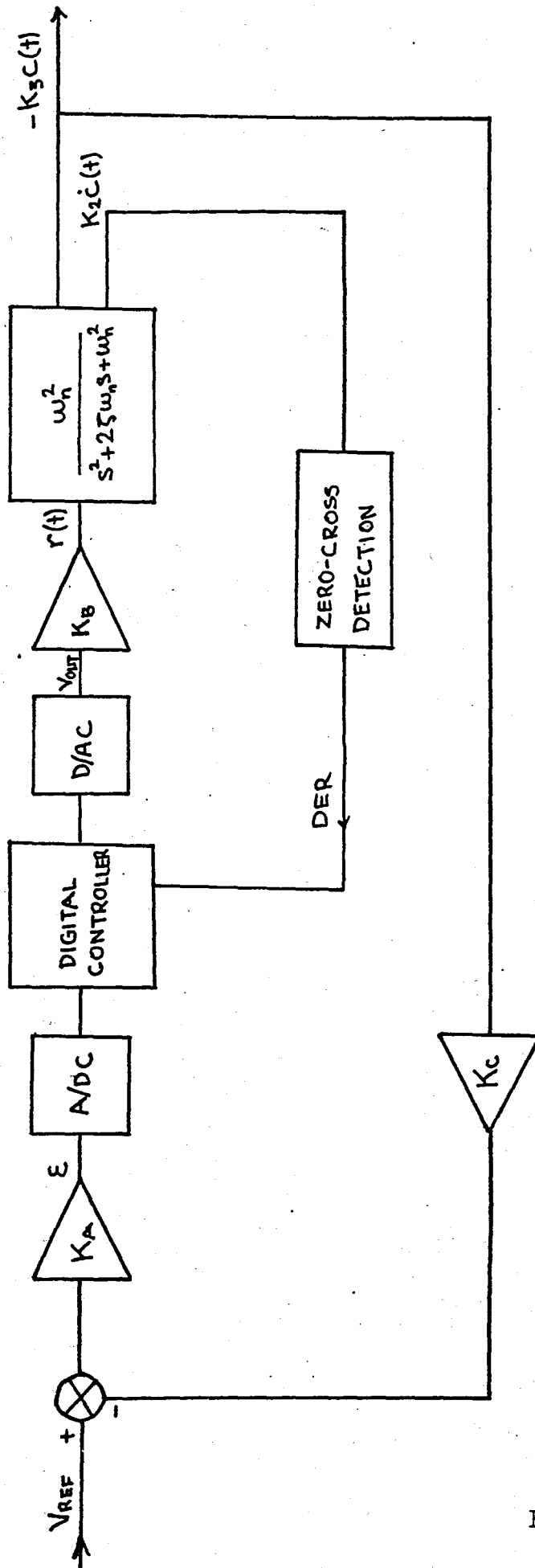


Fig.(7.1)

the system.

To apply the analog output V_{OUT} of the digital controller to the simulated system we must convert the range of this signal into 0 to +6 volts. So the V_{OUT} which is normally +10 volts must be attenuated by a factor of 0.6 to generate $r(t)$ which is the input function of the system. This circuit is shown in Fig.(7.2.a)

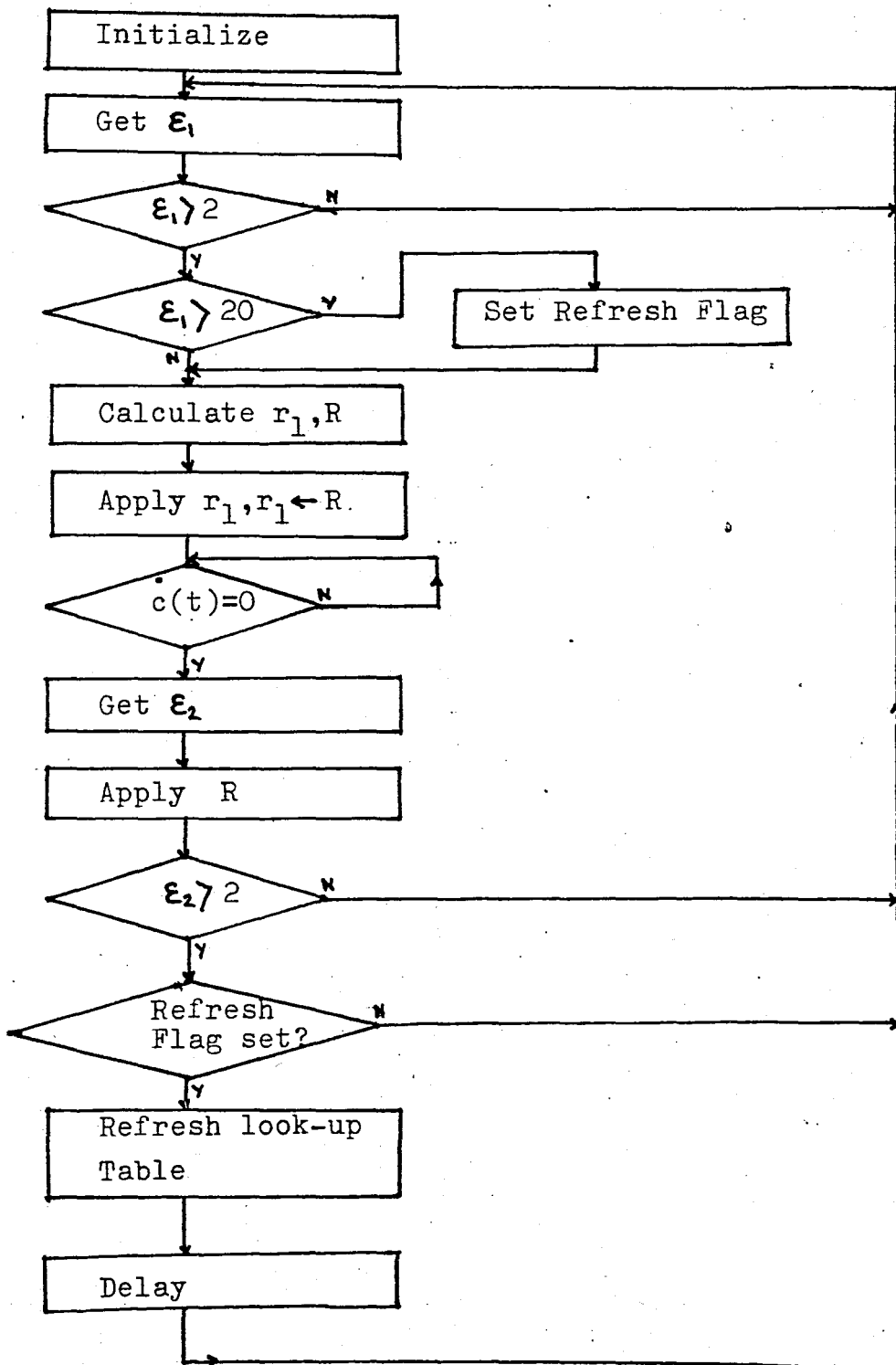
First amplifier in Fig.(7.2.b) makes makes the steady state response unity to a unit step input and inverts the output of the system. By subtracting the inverted V_{REF} signal from the output of the first amplifier by use of op-amp(2) in Fig.(7.2.b) and attenuating this difference signal by a factor of 5/6, we obtain the error signal. Since signal can be any value in the range of -5 to +5 volts we sacrifice from resolution of the A/D converter. By adding +5 volts to this signal we obtain a standard signal in the range of 0 to +10 volts.

The zero-detection circuit has a very simple reasoning in this case. The simulated system derivative

is full wave rectified and then highly amplified and clamped at +5 volts to generate a TTL level DER signal as shown in Fig.(7.2.c.).

7.2.THE FLOWCHART OF ADAPTIVE POSICAST CONTROL.

The adaptive Posicast routine is developed corresponding to the following flowchart.



7.3. THE PROGRAM DEVELOPED FOR THE ADAPTIVE POSICAST CONTROL.

```

INIT   : ;Initialization of the digital controller.

        DI                0500 F3

        ;Set port A as control port (Mode 3).

        LD   A,CF          0501 3E CF
        OUT  (05),A        0503 D3 05

        ;Set all pins of port A as output

        LD   A,00          0505 3E 00
        OUT  (05),A        0507 D3 05

        ;Disable interrupt.

        LD   A,07          0509 3E 07
        OUT  (05),A        050B D3 05

        ;Set port B as control port.

        LD   A,CF          050D 3E CF
        OUT  (07),A        050F D3 07

        ;Set higher 4 bits of port B as output and
        set lower 4 bits of port B as input.

        LD   A,0F          0511 3E 0F
        OUT  (07),A        0513 D3 07

        ;Disable interrupt

        LD   A,07          0515 3E 07
        OUT  (07),A        0517 D3 07

        ;Initialize all flags.

        LD   A,00          0519 3E 00

```

```

LD      (MAG),A          051B  32 00 0F
LD      (SIGN),A        051E  32 01 0F
LD      (CAN),A         0521  32 02 0F

```

```

;Move Look-up table from RAM to ROM

```

```

LD      HL,0700H        0524  21 00 07
LD      DE,0800H        0527  11 00 03
LD      BC,0080H        052A  01 80 00
LDIR                                052D  ED B0
LD      HL,0000H        052F  21 00 00
LD      SP,OFA0H ;      0532  31 A0 0F
LD      D,00            0535  16 00

```

```

START : ;Control loop starts.

```

```

LD      IX,0300         0537  DD 21 00 08

```

```

L1     : ;Start of loop in case of  $\epsilon=0$ 

```

```

CALL   GET              053B  CD C5 05
IN     (A),06           053E  DB 06
AND    02                0540  E6 02
JP     NZ,L1            0542  C2 3B 05
LD     A,B              0545  78
ADD   A,00              0546  06 00
JP     M,L2             0548  FA 4C 05
CPL                                054B  2F

```

```

L2     : SUB 84          054C  D6 84

```

```

JP     C,L1             054E  DA 3B 05

```

```

SUB    20H                0551  D6 20
JP     C,L3              0553  DA 5B 05
;Set refresh flag
LD     A,FFH             0556  3E FF
LD     (CAN),A          0558  32 02 0F
L3    : LD     A,B        055B  78
      ADD    A,00H       055C  C6 00
      JP     P,NEGST     055E  F2 8E 05
;Calculate the values of r1 and R.
SUB    80H                0561  D6 80
LD     E,A               0563  5F
ADD    IX,DE             0564  DD 19
LD     A,(IX 00)        0566  DD 7E 00
ADD    A,L               0569  85
LD     L,A               056A  6F
LD     A,E               056B  7B
SLA    A                 056C  CB 27
ADD    A,H               056E  84
JP     C,POSCOR         056F  DA 73 05
LD     H,A               0572  67
LD     E,00              0573  1E 00
JP     APPL              0575  C3 DA 05
POSCOR: ;Correction routine for overflow in addition
LD     IX,0800H          0578  DD 21 00 08

```

LD	H,FFH	057C	26 FF
LD	E,A	057E	5F
SRL	E	057F	CB 3B
ADD	IX,DE	0581	DD 19
LD	B,(IX 00)	0583	DD 46 00
LD	A,L	0586	7D
SUB	B	0587	90
LD	L,A	0588	6F
LD	E,00	0589	1E 00
JP	APPL	058B	C3 DA 05

;Calculate r_1 and R if ϵ is positive

NEGST :	CPL	058E	2F
	SUB 80H	058F	D6 80
	LD E,A	0591	5F
	ADD IX,DE	0592	DD 19
	LD A,L	0594	7D
	SUB (IX 00)	0595	DD 96 00
	LD L,A	0598	6F
	LD A,H	0599	7C
	SLA E	059A	CB 23
	SUB E	059C	93
	JP C,NEGCOR	059D	DA A6 05
	LD H,A	05A0	67
	LD E,FFH	05A1	1E FF
	JP APPL	05A3	C3 DA 05

NEGCOR : ;Correction routine for overflow in subtraction.

CPL		05A6	2F
INC	A	05A7	3C
SRL	A	05A8	CB 3F
LD	IX,0800H	05AA	DD 21 00 08
LD	E,A	05AE	5F
ADD	IX,DE	05AF	DD 19
LD	A,(IX 00)	05B1	DD 7E 00
ADD	A,L	05B4	85
LD	L,A	05B5	6F
LD	H,00	05B6	26 00
LD	E,FFH	05B8	1E FF
JP	APPL	05BA	C3 DA 05

DEL : ; Delay subroutine

NOP		05BD	00
DEC	HL	05BE	2B
LD	A,H	05BF	7C
OR	L	05C0	B5
JP	NZ,DEL	05C1	C2 BD 05
RET		05C4	C9

GET : ;Analog input routine.

LD	C,06	05C5	0E 06
LD	B,00	05C7	06 00
LD	A,80H	05C9	3E 80
OUT	(06),A	05CB	D3 06

	OUT	(C),B	05CD	ED 41
L4	:	IN	(A),06	05CF DB 06
		AND	01	05D1 E6 01
		JP	Z,L4	05D3 CA CF 05
		IN	(A),08	05D6 DB 08
		LD	B,A	05D8 47
		RET		05D9 C9

APPL : ;Application of steps.

	LD	A,L	05DA	7D
	OUT	(04),A	05DB	D3 04
	EXX		05DD	D9
	LD	HL,0180H	05DE	21 80 01
	CALL	DEL	05E1	CD BD 05
L5	:	IN	(A),06	05E4 DB 06
		AND	02	05E6 E6 02
		JP	NZ,L5	05E8 C2 E4 05
		LD	HL,0050H	05EB 21 50 00
		CALL	DEL	05EE CD BD 05
		EXX		05F1 D9
		CALL	GET	05F2 CD 05 05
		LD	A,H	05F5 7C
		OUT	(04),A	05F6 D3 04
		LD	L,H	05F8 6C
		LD	A,B	05F9 78

	ADD	A,00	05FA	C6	00
	JP	M,L6	05FC	FA	00 06
	CPL		05FF	2F	
L6	:	SUB	83H	0600	D6 83
	JP	C,CLRCAN	0602	DA	D3 06
	LD	A,(CAN)	0605	3A	02 0F
	ADD	A,00	0608	C6	00
	JP	Z,START	060A	CA	37 05
	LD	A,E	060D	7B	
	ADD	A,00	060E	C6	00
	JP	NZ,NEGSTRS	0610	C2	1C 06
	LD	A,B	0613	78	
	ADD	A,00	0614	C6	00
	JP	P,DECR	0616	F2	51 06
	JP	INCR	0619	C3	25 06

NEGSTRS: ;Refresh routine of look up table for negative step

	LD	A,B	061C	78	
	ADD	A,00	061D	C6	00
	JP	P,INCR	061F	F2	25 06
	JP	DECR	0622	C3	51 06
INCR	:	LD	A,(SIGN)	0625	3A 01 0F
	ADD	A,00	0628	C6	00
	JP	NZ,INCSUB	062A	C2	38 06
	LD	A,(MAG)	062D	3A	00 0F
	ADD	A,04	0630	C6	04

	LD	(MAG), A	0632	32	00	0F
	JP	ADDIT	0635	C3	A3	06
INCSUB:	LD	A, (MAG)	0638	3A	00	0F
	SUB	04	063B	D6	04	
	JP	NZ, SUB1	063D	C2	4B	06
	LD	A, 00	0640	3E	00	
	LD	(SIGN), A	0642	32	01	0F
	LD	(MAG), A	0645	32	00	0F
	JP	ADDIT	0648	C3	A3	06
SUB1 :	LD	(MAG), A	064B	32	00	0F
	JP	SUBTR	064E	C3	7C	06
DECR :	LD	A, (SIGN)	0651	3A	01	0F
	ADD	A, 00	0654	C6	00	
	JP	NZ, DECADD	0656	C2	74	06
	LD	A, (MAG)	0659	3A	00	0F
	SUB	04	065C	D6	04	
	JP	NC, ADD1	065E	D2	6E	06
	LD	A, 04	0661	3E	04	
	LD	(MAG), A	0663	32	00	0F
	LD	A, FFH	0666	3E	FF	
	LD	(SIGN), A	0668	32	01	0F
	JP	SUBTR	066B	C3	7C	06
ADD1 :	LD	(MAG), A	066E	32	00	0F
	JP	ADDIT	0671	C3	A3	06
DECADD :	LD	A, (MAG)	0674	3A	00	0F

	ADD	A,04	0677	C6 04
	LD	(MAG),A	0679	32 00 OF
SUBTR	:	LD	A,(MAG)	067C 3A 00 OF
	LD	B,00	067F	06 00
	LD	C,A	0681	4F
	PUSH	HL	0682	E5
	LD	HL,0000	0683	21 00 00
	LD	IX,0800H	0686	DD 21 00 08
	LD	IY,0700H	068A	FD 21 00 07
	LD	D,00	068E	16 80
L7	:	LD	A,(IY 00)	0690 FD 7E 00
	SUB	H	0693	94
	LD	A,(IX 00)	0694	DD 77 00
	ADD	HL,BC	0697	09
	INC	IX	0698	DD 23
	INC	IY	069A	FD 23
	DEC	D	069C	15
	JP	NZ,L7	069D	C2 90 06
	JP	CORRE	06A0	C3 C7 06
ADDIT	:	LD	A,(MAG)	06A3 3A 00 OF
	LD	B,00	06A6	06 00
	LD	C,A	06A8	4F
	PUSH	HL	06A9	E5
	LD	HL,0000	06AA	21 00 00
	LD	IX,0800H	06AD	DD 21 00 08

	LD	IY,0700H	06B1	FD 21 00 07
	LD	D,80	06B5	16 80
L8	:	LD A,(IY 00)	06B7	FD 7E 00
	ADD	A,H	06BA	84
	LD	(IX 00)	06BB	DD 77 00
	ADD	HL,BC	06BE	09
	INC	IX	06BF	DD 23
	INC	IY	06C1	FD 23
	DEC	D	06C3	15
	JP	NZ,L8	06C4	C2 B7 06
CORRE	:	LD HL,3FFFH	06C7	21 FF 3F
	CALL	DEL	06CA	CD BD 05
	POP	HL	06CD	E1
	LD	D,00	06CE	16 00
	JP	START	06D0	C3 37 05
CLRCAN	:	LD A,00	06D3	3E 00
	LD	(CAN),A	06D5	32 02 0F
	JP	START	06D8	C3 37 05

LOOK UP TABLE:

0700	00 01 03 04 06 07 09 0A 0C 0D 0F 10 12 13 15 16
0710	18 19 1B 1C 1E 1F 21 22 24 25 27 28 2A 2B 2D 2F
0720	30 31 33 34 36 37 39 3A 3C 3D 3F 40 42 43 44 46
0730	47 49 4A 4C 4D 4F 50 52 53 55 56 58 59 5B 5C 5E
0740	5F 61 62 64 65 67 68 6A 6B 6D 6E 70 71 73 74 76

0750 77 79 7A 7C 7D 7F 80 82 83 84 86 87 89 8A 8C 8D
0760 8F 90 92 93 95 96 98 9A 9B 9C 9E 9F A1 A2 A4 A5
0770 A7 A8 AA AB AD AE B0 B1 B3 B4 B6 B7 B9 BA BC BD

6. CONCLUSIONS

In this study the problem of compensating a second-order lightly damped linear feedback system by means of a half-cycle Posicast with microprocessor application is examined. The second-order system is simulated by analog computer as shown in Fig.(5.1). In this configuration we can change both the system parameters ζ and ω_n by changing the value of the resistor R_1 or R_5 . So in order to simulate the changes in both parameters of the system at the same time we put a potentiometer to obtain some part of R_5 .

If we run the program developed for Adaptive Posicast Control for the set-up shown in Fig.(7.1), the step response is obtained as shown in Fig.(8.1), where first signal is the output of the simulated second-order system; $-k_3c(t)$, second signal is the control signal generated by the digital controller; v_{OUT} and last signal is the step input ; v_{REF} . In this figure ζ is adjusted to 0.304 and ω_n is adjusted to 164.317 rad/sec

If we change R_5 slowly during the application of a square wave to v_{REF} , both ζ and ω_n change accordingly and no overshoot is observed at the output. However, if we

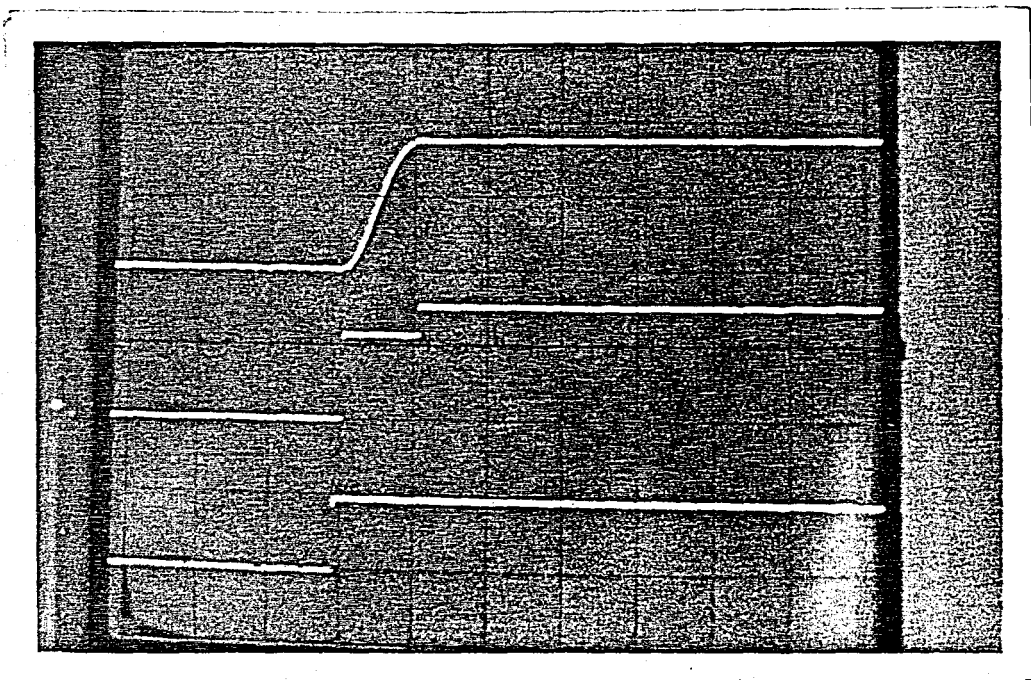


Fig.(8.1). Step response of the second order system with Posicast Control

change R_5 sharply a peak is observed for two or three steps, and the system adaptes itself in course of time so that the transient overshoots disappear.

After observing the practical results the Adaptive Posicast Routine may be thought quite well for the lightly damped second order systems whose parameters change infinitesimally. However since the adaptation is reached by iterative calculations,

for the systems whose parameters change sharply, it takes time to cease the transient overshoots.

For such a system since some degree of intelligence is planned to reach, microprocessors are inevitable to use. The capability of the controller depends on both the hardware and software. In our controller, the microprocessor both scans the inputs of controller and processes the necessary signals to give output as control signal. Since multiplication routine is time consuming for such a controller we use an iterative trial and error method to refresh r_1 table.

If the system is compensated by some other circuitry so that the system is made insensitive to system parameters we can construct a simple hardware to control the system without the usage of microprocessor. However, if adaptivity to parameter changes is concerned the usage of microprocessor is inevitable.

For future application of Posicast Method one must use fast and high resolution A/D and D/A converters. An arithmetic and logic unit (ALU) or a multiplier IC must

also be added for the calculation of r_1 and the application time t_p , so that if the if the system parameters change the r_1 and t_p can be calculated instantaneously instead of calculating them iteratively. We can also increase system clock frequency to decrease the time taken by the control routines. We must use two A/D converters, one for V_{REF} and one for output of the system to be controlled. The one which will be used for output of the system may be a tracking type A/D converter. After these changes we obtain a very powerful configuration and we can develop more efficient routines for Posicast Method.

The routine may be further exploited and more intelligence may be added. For this intelligence we can propose that the machine may be thought so that it will make the corrections in system parameters instantaneously depending only on past knowledge of the deviations without further any calculation, i.e. we may make use of the system's past experience, once some data is calculated there is no reason to calculate it again.

APPENDIX

Appendix

THE MONITOR TO DEVELOP USER PROGRAMS
IN THE RAM AREA OF THE DIGITAL CONTROLLER.

```

INIT : LD A,00 0000 3E 00
      LD (CNTFLA),A 0002 32 FD 0E
      LD A,82H 0005 3E 82
      OUT (03),A 0007 D3 03
      LD SP,OFF0H 0009 31 F0 0F
      LD HL,DSPBUO 000C 21 00 0F
      LD B,06 000F 06 06
      LD A,00 0011 3E 00

L1 :
      LD (HL),A 0013 77
      INC HL 0014 23
      DEC B 0015 05
      JP NZ,L1 0016 02 13 00
      LD HL,RAMSTA 0019 21 00 08

SCAN :
      LD DE,DSPBUF 001C 11 05 0F
      LD A,FEH 001F 3E FE
      LD B,06 0021 06 06

SCAN1 :
      OUT (OOH),A 0023 D3 00
      LD C,A 0025 4F

```

	CALL	DISPL	0026	CD 3D 00
	CALL	DEL20	0029	CD 42 00
	IN	A, (01)	002C	DB 01
	CP	FFH	002E	FE FF
	JP	NZ, NEWCHR	0030	C2 4E 00
RET1	:			
	LD	A, C	0033	79
	RLC	A	0034	CB 07
	DEC	B	0036	05
	JP	NZ, SCAN1	0037	C2 23 00
	JP	SCAN	003A	1C 00
DISPL	:			
	LD	A, (DE)	003D	1A
	OUT	(02), A	003E	D3 02
	DEC	DE	0040	1B
	RET		0041	C9
DEL20	:			
	PUSH	HE	0042	E5
	LD	HL, 0130H	0043	21 30 01
L3	:			
	DEC	HL	0046	2B
	LD	A, H	0047	7C
	OR	L	0048	B5

JP	NZ,L3	0049	C2 46 00
POP	HL	004C	E1
RET		004D	C9

NEWCHR :

CALL	DEL20	004E	CD 42 00
CALL	DEL20	0051	CD 42 00
IN	A,(01)	0054	DB 01
CP	FFH	0056	FE FF
JP	Z,RET1	0058	CA 33 00
LD	(ROWBUF),A	005B	32 FF 0E
LD	A,C	005E	79
LD	(COLBUF),A	005F	32 FE 0E

INIT2 :

LD	A,FEH	0062	3E FE
LD	DE,DSPBUF	0064	11 05 0F
LD	B,06	0067	06 06

SCAN3 :

OUT	(00),A	0069	D3 00
LD	C,A	006B	4F
CALL	DISPL	006C	CD 3D 00
CALL	DEL20	006F	CD 42 00
LD	A,C	0072	79
RLC	A	0073	CB 07
DEC	DE	0075	1B

DEC	B	0076	05
JP	NZ,SCAN3	0077	C2 69 00
LD	A,(COLBUF)	007A	3A FE OE
OUT	(00),A	007D	D3 00
IN	A,(01)	007F	DB 01
LD	C,A	0081	4F
LD	A,(ROWBUF)	0082	3A FF OE
CP	C	0085	B9
JP	NZ,CHRENC	0086	C2 8C 00
JP	INIT2	0089	C3 62 00

CHRENC :

LD	A,(COLBUF)	008C	3A FE OE
CALL	CALC	008F	CD 29 01
PUSH	BC	0092	C5
LD	A,(ROWBUF)	0093	3A FF OE
CALL	CALC	0096	CD 29 01
LD	A,B	0099	78
CP	O	009A	FE 00
JP	Z,REANUM	009C	CA AA 00
LD	B,00	009F	06 00

L4 :

INC	B	00A1	04
INC	B	00A2	04
INC	B	00A3	04

INC	B	00A4	04
INC	B	00A5	04
DEC	A	00A6	3D
JP	NZ,L4	00A7	C2 A1 00

REANUM :

POP	AF	00AA	F1
ADD	A,B	00AB	80
LD	(DATAIN),A	00AC	32 F9 0E
LD	IX,CHRGEN	00AF	DD 21 F1 01
LD	C,A	00B3	4F
LD	B,00	00B4	05 00
ADD	IX,BC	00B6	DD 09
LD	A,(IX 00)	00B3	DD 7E 00
CP	14H	00BB	FE 14
JP	Z,DSPSFT	00BD	CA CE 00
CP	20	00C0	FE 20
JP	NC,DSPSFT	00C2	D2 CE 00
LD	IY,CNTST	00C5	FD 21 D5 01
LD	C,A	00C9	4F
ADD	IY,BC	00CA	FD 09
JP	(IY)	00CC	FD E9
DSPSFT :	PUSH HL	00CE	F5
LD	A,(CNTFLA)	00CF	3A FD 0E
CP	AAH	00D2	FE AA

	JP	Z, ADDR	00D4	CA E1 00
	CP	DDH	00D7	FE DD
	JP	Z, DATA	00D9	CA 02 01
	CP	00	00DC	FE 00
	JP	Z, INIT	00DE	CA 00 00
ADDR	:			
	LD	D, H	00E1	54
	LD	E, L	00E2	5D
	LD	B, 04	00E3	06 04
ROT	:	SLA L	00E5	CB 25
	JP	NC, NEXT1	00E7	D2 EF 00
	RL	H	00EA	CB 14
	JP	TEST	00EC	C3 F1 00
NEXT1	:			
	SLA	H	00EF	CB 24
TEST	:			
	DEC	B	00F1	05
	JP	NZ, ROT	00F2	C2 E5 00
	LD	A, (DATAIN)	00F5	3A F9 0E
	OR	L	00F8	B5
	LD	L, A	00F9	6F
	LD	DE, DSPADR	00FA	11 02 0F
	LD	B, 04	00FD	06 04

	JP	SHIFT	00FF	C3	16	01
DATA :						
	LD	A, (HL)	0102	7E		
	SLA	A	0103	CB	27	
	SLA	A	0105	CB	27	
	SLA	A	0107	CB	27	
	SLA	A	0109	CB	27	
	LD	D, A	010B	57		
	LD	A, (DATAIN)	010C	3A	F9	0E
	OR	L	010F	B2		
	LD	(HL), A	0110	77		
	LD	DE, DSPBUO	0111	11	00	0F
	LD	B, 02	0114	06	02	
SHIFT :						
	LD	C, B	0116	48		
	DEC	C	0117	0D		
L5 :						
	LD	A, (DE)	0118	1A		
	PUSH	AF	0119	F1		
	INC	DE	011A	13		
	DEC	C	011B	0D		
	JP	NZ, L5	011C	C2	18	01
L6 :						
	POP	AF	011F	F1		

LD	(DE),A	0120	12
DEC	DE	0121	1B
DEC	B	0122	05
JP	NZ,L6	0123	C2 1F 01
JP	SCAN	0126	C3 1C 00

CALC :

CPL		0129	2F
LD	B,00	012A	06 00

L7 :

INC	B	012C	04
SRA	A	012D	CB 2F
JP	NZ,L7	012F	C2 2C 01
DEC	B	0132	05
RET		0133	C9

ADRKEY :

LD	A,AAH	0134	3E AA
LD	(CNTFLA)	0136	32 FD 0E
LD	B,08	0139	06 03
LD	DE,DSPADR	013B	11 02 0F

L8 :

LD	A,(DE)	013E	1A
OR	08	013F	F6 08
LD	(DE),A	0141	12
INC	DE	0142	13

DEC	B	0143	05
JP	NZ,L8	0144	C2 3E 01
JP	SCAN	0147	C3 1C 00
LD	A,DDH	014A	3E DD
LD	(CNTFLA),A	014C	32 FD OE
JP	SCAN	014F	C3 1C 00

PLUKEY :

LD	A,DDH	0152	3E DD
LD	(CNTFLA),A	0154	32 FD OE
INC	HL	0157	23
CALL	NEWADR	0158	CD 6A 01
JP	SCAN	015B	C3 1C 00

MINKEY :

LD	A,DDH	015E	3E DD
LD	(CNTFLA),A	0160	32 FD OE
DEC	HL	0163	2B
CALL	NEWADR	0164	CD 6A 01
JP	SCAN	0167	C3 1C 00

NEWADR :

LD	DE,DSPBU0	016A	11 00 OF
LD	B,0	016D	06 00
LD	IX,CHRGEN	016F	DD 21 F1 01
LD	A,(HL)	0173	7E
AND	OFH	0174	E6 OF

LD	C, A	0176	4F
ADD	IX, BC	0177	DD 09
LD	A, (IX 00)	0179	DD 7E 00
LD	(DE), A	017C	12
INC	DE	017D	13
LD	IX, CHRGEN	017E	DD 21 F1 01
LD	A, (HL)	0182	7E
CALL	SRL	0183	CD CC 01
LD	C, A	0186	4F
ADD	IX, BC	0187	DD 09
LD	A, (IX 00)	0139	DD 7E 00
LD	(DE), A	018C	12
INC	DE	018D	13
LD	IX, CHRGEN	018E	DD 21 F1 01
LD	A, L	0192	7D
AND	OFH	0193	E6 0F
LD	C, A	0195	4F
ADD	IX, BC	0196	DD 09
LD	A, (IX 00)	0198	DD 7E 00
LD	(DE), A	019B	12
INC	DE	019C	13
LD	IX, CHRGEN	019D	DD 21 F1 01
LD	A, L	01A1	7D

CALL	SRL	01A2	CD CC 01
LD	C,A	01A5	4F
ADD	IX,BC	01A6	DD 09
LD	A,(IX 00)	01A8	DD 7E 00
LD	(DE),A	01AB	12
INC	DE	01AC	13
LD	IX,CHRGEN	01AD	DD 21 F1 01
LD	A,H	01B1	7C
AND	OFH	01B2	E6 0F
LD	C,A	01B4	4F
ADD	IX,BC	01B5	DD 09
LD	A,(IX 00)	01B7	DD 7E 00
LD	(DE),A	01BA	12
INC	DE	01BB	13
LD	IX,CHRGEN	01BC	DD 21 F1 01
LD	A,H	01C0	7C
CALL	SRL	01C1	CD CC 01
LD	C,A	01C4	4F
ADD	IX,BC	01C5	DD 09
LD	A,(IX 00)	01C7	DD 7E 00
LD	(DE),A	01CA	12
RET		01CB	C9
SRL	:		
SRL	A	01CC	CB 3F

SRL	A	01CE	CB	3F
SRL	A	01D0	CB	3F
SRL	A	01D2	CB	3F
RET		01D4	C9	

CNTST :

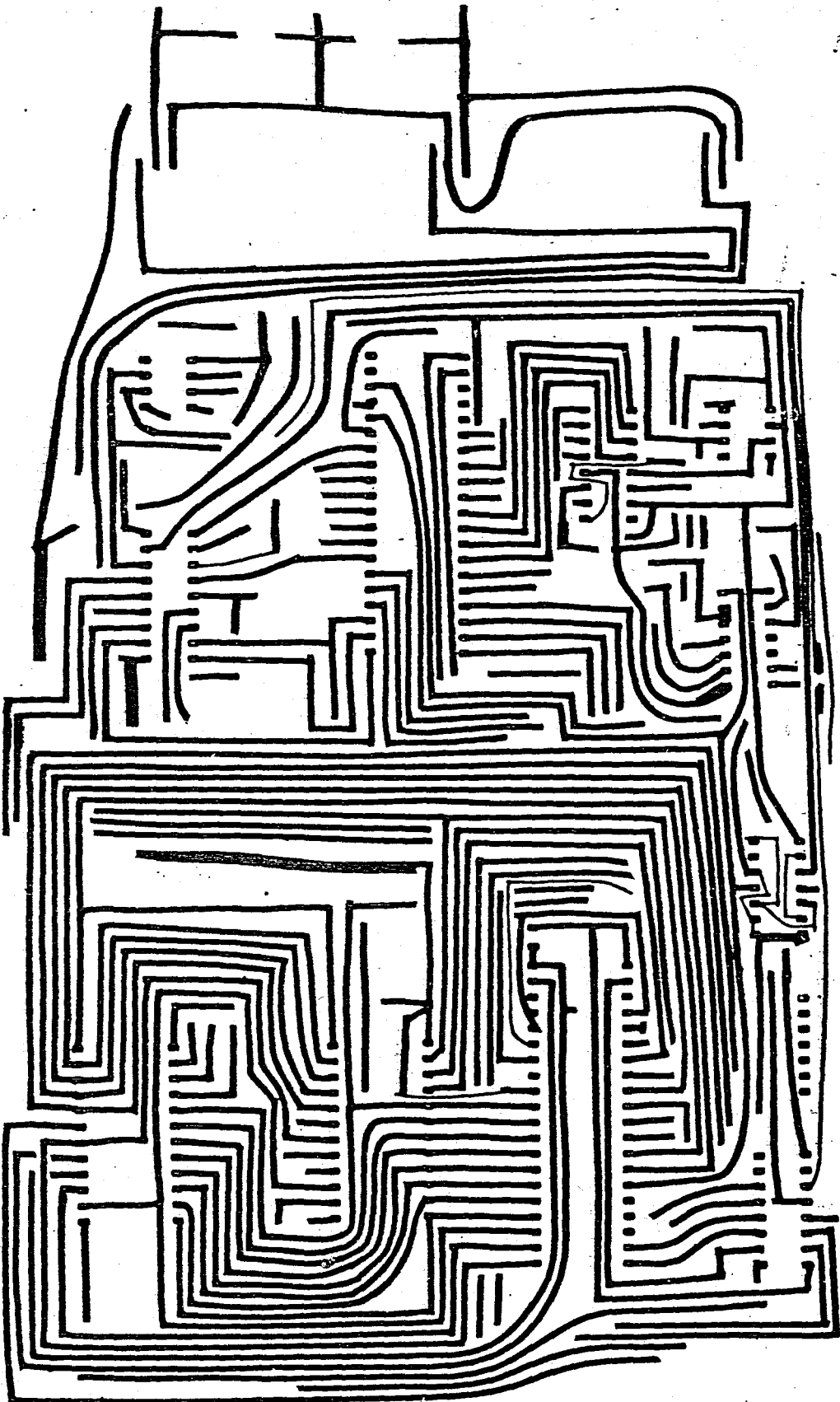
JP	SCAN	01D5	C3	1C	00
JP	SCAN	01D8	C3	1C	00
JP	SCAN	01DB	C3	1C	00
JP	SCAN	01DE	C3	1C	00
JP	ADRKEY	01E1	C3	34	01
JP	DATKEY	01E4	C3	4A	01
JP	MINKEY	01E7	C3	5E	01
JP	PLUKEY	01EA	C3	52	01
JP	GO	01ED	C3	F0	01

GO :

JP	(HL)	01F0	E9	
----	------	------	----	--

CHRGEN:

01F1	B7	14	73	76
	D4	E6	E7	34
	F7	F6	F5	C7
	A3	57	E3	E1
	00	03	06	09
	0C	0F	12	15
	18			



PCB Wire Diagram of the Digital Controller

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