ENERGY HARVESTING WIRELESS OPTICAL MICROSYSTEMS

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ABSTRACT

ENERGY HARVESTING WIRELESS OPTICAL MICROSYSTEMS

This thesis covers a novel approach to photovoltaic energy harvesting and optical data transmission in the context of millimeter-scaled smart autonomous microsystems through the use of a single light emitting diode (LED) to both efficiently harvest optical energy and transmit data to enable wireless, batteryless operation. A proof of concept design for demonstrating the viability of the use of a LED in the proposed manner, harvesting optical energy and transmitting a fixed device ID optically through the same LED using a transmitter based on a continually running charge pump is presented. Next, a low voltage temperature sensor design is integrated into the existing design, to prove by example that the harvested voltage from the LED is high enough that it requires no voltage boosting to power essential analog blocks such as sub-bandgap references, oscillators, and comparators, as opposed to integrated CMOS photovoltaic harvesting. Finally, an alternative, energy efficient optical transmitter architecture and a new ultra low power, ultra low energy temperature sensor are designed and integrated into a single chip. The scalable, inverter based switched capacitor boosting transmitter uses the trickle current from the LED to charge its capacitors directly with minimized losses in efficiency, transmitting data with 1 nJ/bit to a receiver designed and built in-house for up to 10 cm distance. The temperature sensor consumes less than 3 μW, features digital offset correction and an adaptive full-partial conversion algorithm to minimize the conversion time, effectively reducing energy per conversion from 0.6 nJ-3 nJ to 0.15 nJ-0.75 nJ. Total power consumption is in the order of 6 μW, harvested by a 0.1 mm^2 LED, making the system viable for millimeter-scaled outdoor solar harvesting applications. All three designs were fabricated in UMC 0.18 μm CMOS process and tested in-house.

ÖZET

ENERJİ HASAT EDEN KABLOSUZ OPTİK MİKROSİSTEMLER

Bu tez, milimetre ölçekli kablosuz, bataryasız akıllı otonom mikrosistem tasarımı bağlamında verimli enerji toplama ve veri iletimi sorunlarını tek bir ışık saçan diyot (LED) kullanarak çözülmesini kapsamaktadır. Savımızın ispatı olarak, LED ile optik olarak güç toplayan, toplanan güç ile bir yük pompası çalıştırarak sabit bir cihaz kimlik bilgisini optik olarak ileten bir tasarım sunulmaktadır. Bunu takiben, sensör tasarımı için elzem olan temel analog yapı taşlarının, entegre CMOS fotovoltaik hücreler kullanılması halinde olacağın aksine, gerilim yükseltmeye gereksinim duymaksızın doğrudan LED gerilimiyle çalışabileceğini ispatlamak için bir sıcaklık sensör devresi, varolan tasarıma eklenmiştir. Son olarak enerji verimliliği yüksek yeni bir optik veri iletim mimarisi geliştirilmiş, yeni, çok düşük güç ve enerji harcayan bir sıcaklık sensörü ile birleştirilmiştir. Evirici tabanlı, kapasitör anahtarlamalı gerilim yükselten verici, voltaj yükseltici katlar kullanılmasına gereksinim duymadan, doğrudan LED'den gelen akım ile kapasitörlerini doldurmakta, 1 nJ/bit ile laboratuvar imkanlarında yapılmış bir alıcıya 10 cm mesafeden veri aktarabilmektedir. Sıcaklık sensörü 3 μW'tan az güç harcamakta, dijital sapma doğrultumu ve uyarlanabilir tam-kısmi çevrim algoritması ile çevrim başına düşen enerji kullanımını 0.6 nJ-3 nJ aralığından 0.15 nJ-0.75 nJ aralığına indirgemektedir. Sistem toplamda 6 μW güç harcamaktadır ve 0.1 mm^2 alanlı bir LED ile gün ışığı altında çalışmaya uygundur. Bahsi geçen üç tasarım da UMC 0.18 μm CMOS üretim süreci için tasarlanmış ve laboratuvarda test edilmiştir.

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LIST OF SYMBOLS

D_n	Diffusion coefficient of electrons
D_p	Diffusion coefficient of holes
k	Boltzmann constant
L_n	Diffusion length of electrons
L_p	Diffusion length of holes
N_a	Acceptor concentration in n-type side of the junction
N_d	Donor concentration in p-type side of the junction
n_i	Intrinsic carrier concentration
q	Elementary charge
T	Absolute temperature
V_{BE}	Base-emitter voltage
V_d	Diode potential
V_T	Thermal voltage
V_{th}	Threshold voltage
ΔV_{BE}	Difference between two base-emitter voltages
σ	Standard deviation
$\Sigma\Delta$	Sigma-Delta

LIST OF ACRONYMS/ABBREVIATIONS

ADC	Analog to Digital Converter
AlGaAs	Aluminum Gallium Arsenide
ASIC	Application Specific Integrated Circuit
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Complementary To Absolute Temperature
DAC	Digital to Analog Converter
DC	Direct Current
DMM	Digital Multi-meter
DSP	Digital Signal Processing
DTMOS	Dynamic Threshold Metal Oxide Semiconductor
EIRP	Equivalent Isotropically Radiated Power
EMI	Electromagnetic Interference
FoM	Figure of Merit
FPGA	Field Programmable Gate Aray
FSK	Frequency-shift Keying
IC	Integrated Circuit
ID	Identification Data
InGaAsP	Indium Gallium Arsenide Phosphate
InGaN	Indium Gallium Nitride
IoT	Internet of Things
LC	Inductor-Capacitor
LDO	Low Drop-Out (voltage regulator)
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LSB	Least Significant Bit
MEMS	Micro Electromechanical Systems
MIM	Metal Insulator Metal

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRI	Magnetic Resonance Imaging
MSB	Most Significant Bit
NMOS	n-type Metal Oxide Semiconductor
PID	Proportional Integral Derivative
PIN	p-type intrinsic n-type (semiconductor junction)
p-n	p-type n-type (semiconductor junction)
PMOS	p-type Metal Oxide Semiconductor
PNP	p-type n-type p-type (bipolar junction transistor)
PSRR	Power Supply Rejection Ratio
PTAT	Proportional To Absolute Temperature
PVT	Process Voltage Temperature
PZT	Lead Zirconate Titanate
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RFID	Radio Frequency Identification
ROM	Read Only Memory
RTD	Resistance Temperature Detector
SAR	Successive Approximation Register
SCR	Silicon Controlled Rectifier
SMD	Surface Mounted Device
TDC	Time to Digital Converter
TEG	Thermo-electric Generator
UWB	Ultra-wide Band
ULSI	Ultra-large Scale Integration
VLC	Visible Light Communications
VLSI	Very-large Scale Integration

1. INTRODUCTION

An increasing interest in miniaturized, autnomous smart microsystems exists due to potential fields of application in medicine, safety and security, commerce, instrumentation and perhaps entertainment. Internet of Things (IoT) concept foresees smart everyday objects that can sense environmental parameters and/or their own current status and relay data to a user, as well as being able to communicate with other IoT enabled devices. Implantable biomedical sensors can not only render the nuisance of pinprick tests obsolete, but also provide real time feedback to the patient or to an automated system that can optimize the dose of the medication delivered to the patient. Sensory implants can give patients ththeir lost senses (as in the case of retinal implants), and prosthetic limbs can be controlled by smart devices interfaced to nearby, functional tissue. Networks of smart sensors can be distributed to vast spans of land, notifying security and public safety apparatus of a state for natural disasters such as forest fires or border intrusions as well as providing farmers with vital information regarding the status of their fields and crops, such as the humidity and the chemical profile of the soil. Miniaturized smart microsystems are already embedded into the tags of commercial products and credit cards of the people who may purchase them, and are expected to find their way into the nooks and crannies of production processes that cannot be monitored otherwise. They also find their way into biotechnology laboratories, tagging individual specimens as small as ants, and may find use in distributed monitoring of environments that would be hazardous for human beings.

The miniaturization aspect forces certain constraints on the design, mostly on the extent of its usefulness; if a design is required to be millimeter-scaled, so that its intrusiveness is minimized, the number of functions that can be packed inside the specified size envelope is limited due to the fact that it takes silicon real estate to implement those functions. Compounding the problem is the energy requirements of the system to operate on; even the smallest batteries can push the overall system size from millimeter-scale to centimeter-scale. In addition, once the battery runs out, the system becomes effectively useless, and it has to be extracted from the environment

it was introduced to in order to have its battery replaced, which reduces the attractiveness of the solution. Therefore these systems have to gather the energy necessary for operation from their ambient environment, so that their operation is "perpetual", that is, as long as enough ambient energy exists. This thesis focuses on solving a particular set of problems in optical energy harvesting in the context of smart miniaturized microsystems, increasing harvesting efficiency while providing an alternative data transmission scheme using an unconventional approach. It is the aim of this work to demonstrate an alternative path to the commonly followed approaches in designing smart microsystems that harvest photovoltaic energy, with the hopes to provide a small step towards realizing a world of ubiquitous connectivity, sensing and computation.

The challenges in the design of smart, autonomous energy harvesting microsystems can be broken down into sub-problems of energy harvesting, power management and energy storage, on-chip sensing and data transmission (Figure 1.1). We will begin our discussion with case studies on published designs, drawing commonalities and dissimilarities in implementation.

1.1. Case Studies

A review of prominent wireless batteryless smart sensors is instructive in highlighting key design challenges. Such microsystems are primarily encountered in the field of biomedical implants. The total volume is in the order of millimeter-cubes to tens of millimeter-cubes in such designs, usually operating in the range of 10-100 μW, being powered externally by RF radiation or optically with storage capacitors and/or thin-film batteries, capable of measuring environmental variables using on-chip sensors and transmitting recorded data wirelessly.

- A wireless fluorimeter designed for long term implantable blood glucose monitoring, powered inductively via a standard 13.56 MHz link to an external ferrite antenna with on-chip photodiodes for sensing the fluorescent indicators excited by flip-chip mounted LEDs have been proposed [1]. An 11-bit charge balancing ADC digitizes the transimpedance amplifiers that measure the photodiode

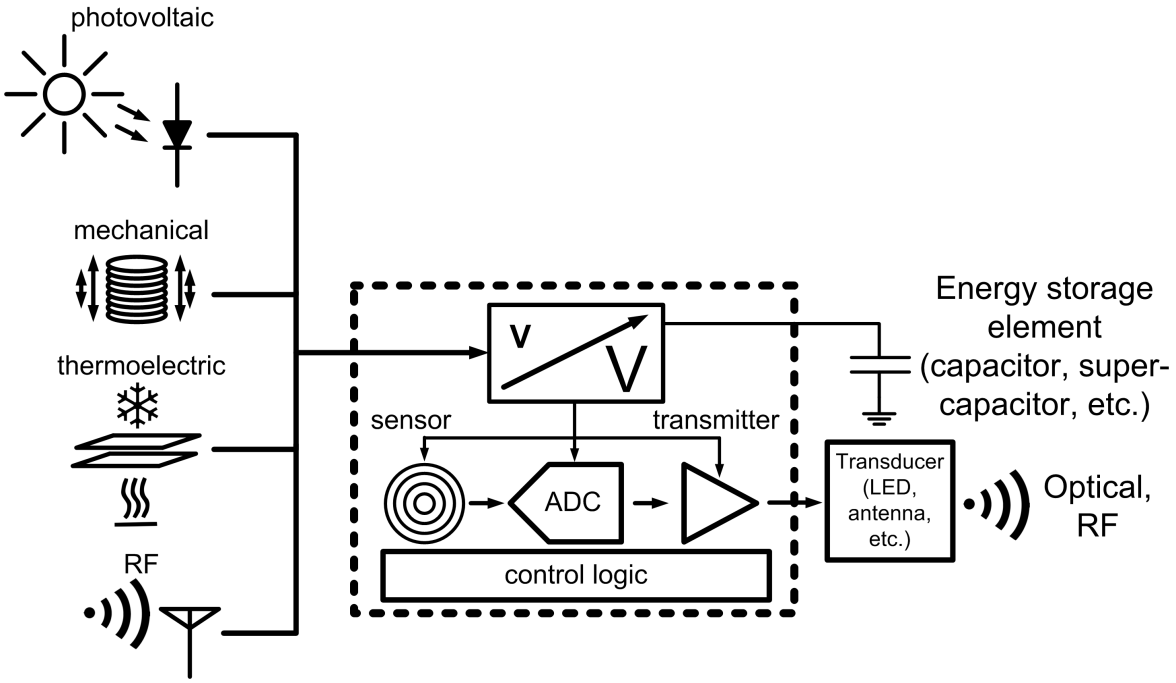

Figure 1.1. A generalized illustration of smart wireless batteryless energy sensors depicting major components

current, as well as the temperature sensor output that is used to compensate the measurements for temperature effects. 1 μJ per measurement is achieved, consuming 250 μW at a sample rate of 7 kHz. The chip is realized in 0.6 μm technology, the die size is 10 mm^2, and the typical operating voltage is around 3.0 V. The design demonstrates the use of a flip-chip LED die, along with smart temperature sensing capabilities, which provides an interesting data point in the context of this thesis.

- The low power smart system features an unconventional optical communication scheme, reflecting directed laser beams on and off using a MEMS corner cube retroreflector [2]. The observation the authors make is that efficient RF communications within die sizes that are orders of magnitude smaller than the wavelength of the RF link is difficult, therefore optical communications that allow structures smaller than millimeter-square sizes as an efficient alternative to RF links are proposed. Retroreflectors, as featured in this publication, are complex and fragile MEMS structures that support extremely low data rates (32 bps), but

consume very low power and support long communication distances as long as the external laser is aligned successfully. The design features a triple well CMOS photodiode that is essentially an N-well and a P-well photodiode connected in series, providing 3.8 μA at 0.8 V with an optical to electrical conversion efficiency of 5.7%, in itself summarizing a major problem with on-chip silicon photovoltaic harvesting. The photodiodes occupy an area of 1.5 mm^2, and the total die size is 25 mm^2. The load is purely capacitive, which offsets the low energy harvesting efficiency; 16 pJ/bit is enough for communicating data. There is no sensing capability and the system transmits a fixed device ID, but it is a very interesting body of work in the context of wireless batteryless smart microsystems.

- In [3], a collection of building blocks, implemented as two CMOS chips, a thin-film battery and a capacitive MEMS pressure sensor stacked vertically to an overall volume of 1.5 mm^3, that is assembled and wirebonded together to form a smart pressure sensing energy harvesting, battery powered microsystem that is designed to provide real time measurements of the inner pressure of the eye of a patient are presented. 80 nW is harvested from 1mW/mm^2 illumination by a switched capacitor voltage booster, recharging a 1 μA·h thin film battery in 1.5 hours under sunlight. A 14-bit 7 μW current source based $\Sigma\Delta$ capacitance to digital converter digitizes the intraocular pressure at a resolution of 0.5 mmHg, and 4.7 nJ/bit RF transmission of the recorded data up to 10 cm is possible at a rate of 7.5 kbps, implemented as a separate chip. A measurement is transmitted every 1.5 hours due to the scarcity of energy.
- The relatively high power consumption of $\Sigma\Delta$ and zoom-ADCs for energy harvesting applications is addressed in [4], where a power consumption of 10 μW is too large for a batteryless, RF powered design. A counter based 8-bit temperature sensor is presented, with a rate of 25 samples/sec and a total consumption of 2.4 μW at 1.2 V supply voltage. The time based temperature sensing approach is similar to the work that will be presented in the following chapters. The system relies on an external 4.5 $\times$ 4.5 mm antenna, but the problems the design tackles are in line with the focus of this thesis.
- Indoor solar harvesting and thermoelectric generators are employed as comple-

mentary energy harvesting techniques in [5]. The system tracks patient temperature, heart rate and motion with the assistance of a commercial of the shelf accelerometer, can perform DSP functions on recorded data and communicate asymmetric UWB radio links. The system can continuously transmit motion data consuming 6.5 μW at 1.4 V supply voltage, with a total die area of 13.5 mm^2, implemented in 0.13 μm technology. The photovoltaic harvester is a commercially available device that can supply a maximum of 80 μW at 1.2 V under indoor lighting conditions, which implies at least 1 cm^2 cell area considering 8% conversion efficiency in commercial silicon photovoltaic cells and 10 μW/mm^2 indoor illumination intensity [6]. The extent of integration featured in this design is a step towards the realization of Wireless Body Sensor Network (WBSN) concept.

- Wireless neural probes that can be implanted within the vicinity of a prosthetic limb, transmitting a patient's neural activity to a base station within the prosthetic limb as commands for movement are featured in [7]. 915 MHz RF energy is collected by an external antenna, upconverted by boost converter, and stored in a 100 mF carbon nanotube supercapacitor. Neural stimuli are amplified by an LNA, digitized by a 10-bit SAR ADC at 40 kS/s consuming 300 nW. Transmission is achieved at 457.5 MHz consuming 5.4 μW with a data rate of 1 Mbps. The average power consumption of the design is 24 μW, reaching 140 μW at its peak. The die area is 1.4 $\times$ 1.5 mm^2, implemented in 0.18 μm technology.
- Active Pixel Sensor (APS) arrays that can both harvest optical energy and capture images at a resolution of 54 $\times$ 50 pixels and 7.4 frames per second were implemented in 0.5 μm CMOS technology [8]. 14 μW is consumed from a 1.2 V supply, which is used to digitize the outputs of the pixels with a 10-bit SAR ADC, while the pixels are capable of harvesting 0.4 V at a power output of 3.4 μW. Off-chip capacitors store charge-pump elevated voltage, and imager is operated as enough energy is collected.
- In [9] a 8.7 μVRMS neural recorder with a sampling rate of 20 kHz realized in 0.18 μm technology that consumes 3.9 μW from a 1 V supplied by RF radiation harvested from a loop antenna that transmits the 8-bit data via a LED is

described.

- A commercialized, 500 μm $\times$ 500 μm smart ID tag harvests optical energy and transmits device ID via an on-chip antenna to an RF receiver at contact distances, enabling tagging of individual ants [10] and integration into MEMS microgrippers [11] due to its small size and light weight.

The above examples share certain commonalities. Minimal invasiveness is a key point in implantable designs and other miniaturized smart microsystems. 0.18 μm process nodes are commonly used due to the low standby leakage, high enough supply voltage ranges. The relatively low complexity of digital circuitry in these systems does not validate moving to more advanced ultra-deep submicron nodes such as the 65 nm process, as smaller feature sized technologies complicate analog design more than the benefit they can provide in terms of digital processing [12]. The high resolution and low sample rate integrating and $\Sigma\Delta$ ADCs tend to be on the high side in terms of energy consumption, as integrating ADCs complete a conversion once in every 2^{n+1} clock cycles while a first order $\Sigma\Delta$ ADC does so once in every f clock cycles (where f is the oversampling ratio) for n bits of resolution. In contrast SAR ADCs are energy efficient topologies with moderate resolution, taking n cycles to perform a 2^n bit conversion. Incremental zoom-ADCs are hybrids in between, quantizing the signal of interest using a coarse SAR ADC and a fine $\Sigma\Delta$ ADC to achieve excellent resolution and energy efficiency [13], but the absolute power and energy consumption might be so high that the harvested energy may not be able to sustain continued operation.

The power consumption coupled with long conversion times increase energy consumption, which can also impose a limitation as some form of energy storage element becomes necessary to supply the immediate current requirements, such as storage capacitors, supercapacitors or thin-film batteries. If RF power transfer is used, on-chip antennas become problematic especially in terms of energy harvesting, whereas on-chip photovoltaic harvesting requires wide area photodiodes that consume the already expensive silicon real-estate with structures that can only be used for one purpose aside from reduced conversion efficiencies. External antennas extend the readout range dramatically to 10 cm - 1 m range, but push the overall volume beyond the millimeter-

cube constraint; on chip antennas that remain inside this limit allow read ranges in the vicinity of 1 mm - 1 cm. The various approaches to energy harvesting, power management (including energy storage), sensing (with an emphasis on temperature sensing as featured in this thesis) and data transmission along with their advantages and disadvantages are broken down into respective subsections.

1.2. Energy Harvesting in Microsystems

The energy requirements of the wireless batteryless smart microsystem define its capabilities and applicability in a practical sense; the energy available to the system imposes a limit to what can be achieved by the microsystem and the speed thereof. The problem of energy management can be decomposed down into two further sub-problems, the first being the efficient harvesting of available ambient energy along with the necessary power management that can provide a useful voltage and current output to the microsystem and second being the efficient use of the energy provided by the solution of the first part of the problem by the functional blocks such as sensors, ADCs. Even though the usefulness of a smart microsystem will be judged by the functionality that it provides, the said functionality hinges upon the ability to operate within the imposed energy limitations; else the microsystem will become impractical for a set of applications. As an example, a commercialized optically powered smart RFID microsystem has found applications in identifying small biological samples such as tagging individual ants [10]; the optical powering and interrogation of the tag occurs in a small time window requiring a small amount of energy that can be delivered to an on-chip photodiode, which is achieved within a small size envelope (0.5 mm x 0.5 mm) and light weight. While the added capability of real time tracking and transmitting of the motion of each tagged specimen might have been desirable, the added weight, volume and cost of including a battery to achieve these goals would render the design useless in this context. Therefore it can be demonstrated that the bottleneck to miniaturizing a smart microsystem is limited by the means of energy harvesting, as exemplified in designs that will be discussed in further chapters where energy harvesting facilities take up a considerable portion of the already expensive

silicon real-estate.

1.2.1. Photovoltaic Energy Harvesting

Photovoltaic energy harvesting involves the conversion of light to electricity. The physics behind photovoltaic conversion can be understood by examining the semiconductor p-n junction. The photovoltaic converter is in principle a diode optically exposed to the outside world, where the injection of carriers is performed optically as opposed to electrical injection in the regular use of diodes. Upon bringing together a p-doped region and an n-doped region, an exchange of positive and negative charges occur and a depletion region with a neutral net charge forms. At the opposite sides of the p-n junction there exists excess positive and negative carriers respectively, forming a built in potential across the depletion region. When electrons are injected into the depletion region, either electrically or by optical excitation, the generated electron-hole pairs are swept away to the opposite sides of the depletion region, causing a net current flow. The engineering of the junction is of vital importance in the performance of the photovoltaic cell, and in the context of CMOS implementations of photodiodes, is typically insufficient due to shallow junction depths and doping profiles optimized for MOSFET operation and not for substrate diodes. PIN diodes have wider neutral or quasi-neutral regions that effectively add up to the depletion region, allowing a higher probability of optical excitation within that region.

Another consideration is the bandgap of the semiconductor being used within the junction of the material. The open circuit voltage of the p-n junction, referring to the conditions where zero net current flows into the junction under a given level of optical excitation, is a direct function of bandgap energy. By the same token, the current generated by the p-n junction is reduced as the bandgap energy increases [14]. The responsivity of the material to a given wavelength of light becomes zero when the energy of the photons is lower than the bandgap energy at the junction. While theoretically there is no upper bound for the absorption of photons above the bandgap energy of the semiconductor, the surface states that occur during the fabrication of the device capture the higher energy photons so that they contribute very little to the

net photocurrent [15]. The current-voltage characteristics of the p-n junction under optical injection can be expressed as:

$$\begin{aligned} I &= I_d - I_{opt} \\ &= I_{\mathrm{o}} \cdot \left(e^{\frac{V_d}{V_T}} - 1 \right) - I_{opt} \end{aligned} \tag{1.1}$$

Where V_{d} is the potential across the p-n junction and V_{T} is the thermal voltage $k \cdot T/q$. For photovoltaic harvesting conditions, this expression can be simplified as:

$$I \approx I_{\mathrm{o}} \cdot \left(e^{\frac{V_d}{V_T}} \right) - I_{opt} \tag{1.2}$$

For $V_{\mathrm{d}} < 0$, i.e. within the third quadrant of its operating regime, the p-n junction under illumination acts like an ideal current source, given that the effective parasitic series and parallel resistances are negligible. As the forward bias exceeds zero and increases further, the current injected by the forward biasing increases exponentially to neutralize the optically generated current, until the open-circuit voltage is reached where no net current flows into and out of the junction. Before the open-circuit voltage is reached, the p-n junction under illumination supplies current to the load, and when the open-circuit voltage is exceeded the p-n junction draws current from the load. This dynamic is exploited in the designs that are covered in this body of work as discussed further in the proceeding chapters. Note that the open-circuit voltage is pushed forward logarithmically as the optically injected current increases. On the current-voltage curve of the p-n junction, there is a maximum power point where the power extracted from the photovoltaic cell is maximized. A fill-factor can be defined as a ratio of maximum power point to the product of open circuit voltage and short circuit current as a figure of merit;

$$f = \frac{P_{max}}{V_{OC} \cdot I_{SC}} \tag{1.3}$$

The fill-factor defines how much power can be extracted with respect to the open circuit voltage and short circuit currents under given conditions of illumination and temperature. A low fill factor identifies the parallel and series parasitic resistances within the photovoltaic cell, revealing inefficiencies [15]. Maximum power point tracking can be employed, matching the impedance at the maximum power point by adjusting the clocking frequency of a boosting power management unit, so that harvested energy is utilized maximally [16]. However, the problem is complex and requires tracking of the voltage and/or the current harvested which adds to the power budget in addition to the silicon overhead necessary for the control circuit. The photovoltaic conversion efficiency for p-n junctions is bound by the Shockley-Queisser limit, which was first calculated with the solar spectrum in mind, to about 30% for single junction photovoltaic cells, while in reality the efficiency ranges from below 10% to 20% [15]. With a power density of 1 mW/mm^2 outdoors and 1-10 μW/mm^2 indoors [17], photovoltaic harvesting can supply adequate levels of power that can support the operation of functional blocks within the microsystem such as sensors and/or voltage boosters that can store energy in storage elements such as capacitors so that the energy storage element can be used as a power source intermittently if the required power output is greater than that can be supplied by the photovoltaic cell. The relatively small area compared to competing approaches and the availability of high intensity optical sources, such as the sun, halogen spotlights, or laser beams, optical energy harvesting becomes a very attractive choice for miniaturizing smart sensors to dimensions in the order of millimeter-cubes.

1.2.2. Mechanical Energy Harvesting

Mechanical means of energy harvesting can be divided into three sub-categories; piezoelectric, electromagnetic and electrostatic [15]. Piezoelectric harvesting exploits

the lattice properties of certain materials where the mechanical strain of the lattice causes the dipoles within the material to polarize, creating an electric field. Electromagnetic harvesting makes use of a permanent magnet being accelerated within a coil, creating a change in magnetic flux to induce a voltage. Finally, electrostatic harvesting relies on capacitive MEMS structures with gaps that can be varied by acceleration along their movement axis. The capacitor is held at a constant voltage and as the gap widens due to mechanical acceleration, the fall in capacitance produce a net flow of charge out of the MEMS structure. Alternatively, charge can be injected and voltage may be boosted due to movement. Incidentally, the parametric amplification of electrical quantities is in principle similar to the transmitter design demonstrated in the final chapters of this work. An interesting application features the combination of radioactive, electrostatic and piezoelectric domains, where a beta emitting radioactive specimen is deposited near a MEMS cantilever made out of a piezoelectric material. As negative charge builds up in the cantilever, it becomes attracted to a metal plate and bends until it touches the metal plate, discharging the accumulated charge and snapping back as the electrostatic neutrality is now achieved. The snapping back of the cantilever induces a sudden stress on the lattice, producing a sudden rise in electric field, which can be harvested by a full wave rectifier [18].

Despite the ingenuity of the schemes employed in harvesting mechanical energy, there are multiple problems to be tackled [15]. In general, air damping of the movement of the parts involved reduces the harvesting efficiency. In addition, the resonant frequency of the structures are increased as the physical dimensions are diminished, which places the peak efficiency further away from vibrations generated by some sources; as an example the acceleratory movement generated by the human body is in the order of 1-10 Hz, while industrial vibration sources such as motors are around 100 Hz, whereas CMOS integrated designs resonate at as low as 1-10 kHz. Electrostatic or electromagnetic tuning of the MEMS structures is a possibility in this regard. In the case of piezoelectric harvesting, silicon itself is not enough to generate useful levels of power, and deposition of efficient piezoelectric materials such as PZT on the MEMS structures is necessary, which drives up costs due to additional needs for fabrication

steps, materials and material deposition equipment. As a result, the reduction in yield and the increased number of process steps increase the cost. Electromagnetic harvesting requires a high number of tightly wound loops with a low resistance and suffers from electromagnetic damping. Around 1 μW/mm^2 can be expected from CMOS compatible, millimeter-cube sized implementations operating at resonant frequencies.

1.2.3. Thermal Energy Harvesting

Thermal energy harvesting enables the energy released by sources such as engines, water pipes or even human body in the form of heat to be recycled into electrical energy [15]. Thermoelectric generation is observed in junctions built out of two dissimilar metals or between p-n semiconductor junctions. Semiconductor junctions exhibit two orders of magnitude greater voltage per degrees Kelvin, and therefore are used more commonly. Greater thermal gradients across the junction result in higher conversion efficiencies, and thermal conductivity between the sides of the junctions poses a problem in maximizing efficiency. Power per area is about 200-500 nW/mm^2 for thermoelectric generators running on 5-10 K differential, and as maximum power extracted from the thermoelectric stack depends on the square of the temperature difference, heat removal from the cold side involving heat sinks becomes a design priority, increasing the overall volume of the system.

1.2.4. Radio Frequency Energy Harvesting

Aside from the discussed energy domains that can be harvested for microsystem operation, RF radiation can also be used to deliver power to the device when ambient energy sources are not enough to run the microsystem [17]. Usually, the readily available RF radiation is inadequate in powering the microsystem by itself, so a dedicated transceiver has to deliver power as well as sending and receiving data. As discussed in prior literature, the harvesting efficiency of RF radiation is high, but the ambient energy available is inadequate [19]. In addition, the antenna sizes that can be realized within millimeter-cube sized packages is likely to be much smaller than the wavelength of the carrier signal, coupled with relatively low quality factor metallized layers

on sub-optimal substrates, this poses a major problem in realizing efficient RF power harvesting. As a result, on-chip or flip-chip antennas that can fit within millimeter-square areas require about 1 W EIRP and can communicate within 1 mm – 10 mm typically, as will be discussed in the transmission section below. Within ranges much less than the wavelength of the signal, the RF emissions can be considered as near-field emissions, with field strength diminishing by d^{-3} as opposed to far-field emissions where strength is attenuated by d^{-1} where d is the distance between the tag antenna and the reader antenna [17].

Considering competing and complementary technologies in energy harvesting, photovoltaic technologies deliver the greatest amount of power in the smallest volume [20] [21]. A photovoltaic cell is much easier to design compared to complex MEMS structures necessary for the scavenging of mechanical energy. In terms of integration with integrated circuits, photovoltaic energy harvesting methods are mature, scalable, and reliable, with the disadvantage of taking up expensive on-chip area. Piezoelectric, electrostatic and magnetic methods of energy harvesting convert mechanical motion into electrical energy. This involves MEMS design with moving parts, which requires additional design efforts and larger areas. Integration of piezoelectric or magnetic materials to the microsystem is another challenge along with the additional need for power conditioning circuitry. Thermoelectric generators are also scalable and reliable alternatives, having no moving parts, but as the amount of power produced by the device requires a temperature gradient, a small sized thermoelectric generator may produce modest amounts of power [15].

1.3. Power Management and Energy Storage

Power management in energy harvesting schemes is usually inevitable. The voltage output of the harvester is usually too low to be used for operating regimes outside of subthreshold. Therefore, voltage boosting schemes are employed to up-convert the harvested voltage, at the cost of reduced current drive at the output of the booster, to attain supply voltages useful enough for the operation of the chip (Figure 1.2). Since power conversion efficiencies are below 100%, the necessity of boost conversion

subtracts from the end-to-end efficiency of the energy harvesting block. The output impedance of the booster tends to be relatively high, so decoupling capacitors find use in supplying peaks in current demand, as well as filtering the voltage ripple at the supply line. As the smart microsystem may draw relatively high current values for short intervals with long standby times in between, charging up a large storage capacitor is a useful strategy; this way the instant current demand is met by the storage capacitor. This is applicable for thin-film battery or supercapacitor based energy storage schemes as well, as their current outputs tend to be low as well. The contrast between power and energy requirements in energy limited systems such as miniaturized smart sensors becomes clearer once we consider that using half the energy of a storage capacitor reduces the voltage across the capacitor to one 70% of its original value. Therefore, the duration of the power consuming operation is as important as the power it consumes. In [22], specific power (W/kg) and specific energy (W· h/kg) for various energy storage technologies is presented whereby we can treat the kilogram figure as a proxy for volume in the context of miniaturized smart microsystems. Capacitors tend to have the lowest volume and highest specific power, but the specific energy is very low, and the situation is diametrically opposite for batteries, with supercapacitors somewhere in between. Barring the use of batteries and resorting to the use of SMD capacitors for energy storage elements to minimize the volume, the smart microsystem has to be designed to drain low amounts of current and perform the operation quickly enough before the voltage across the capacitor falls to levels not useable by the system. If the energy harvester replaces the used current at the same rate, the system can run perpetually, that is as long as the external source of energy keeps supplying the system.

Boosting the harvested voltage can be achieved by two major alternative approaches; charge pumps that rely mostly on on-chip capacitors integrated on the die, or boost converters that require an inductor (Figure 1.2). The on chip inductors cannot have high enough values, therefore an external inductor becomes necessary. External inductors are relatively expensive and large elements, but the use of a boost converter yields higher conversion efficiencies compared to charge pumps, ranging between 70-80% [16]. Flyback topologies can be included in the discussion of the LC

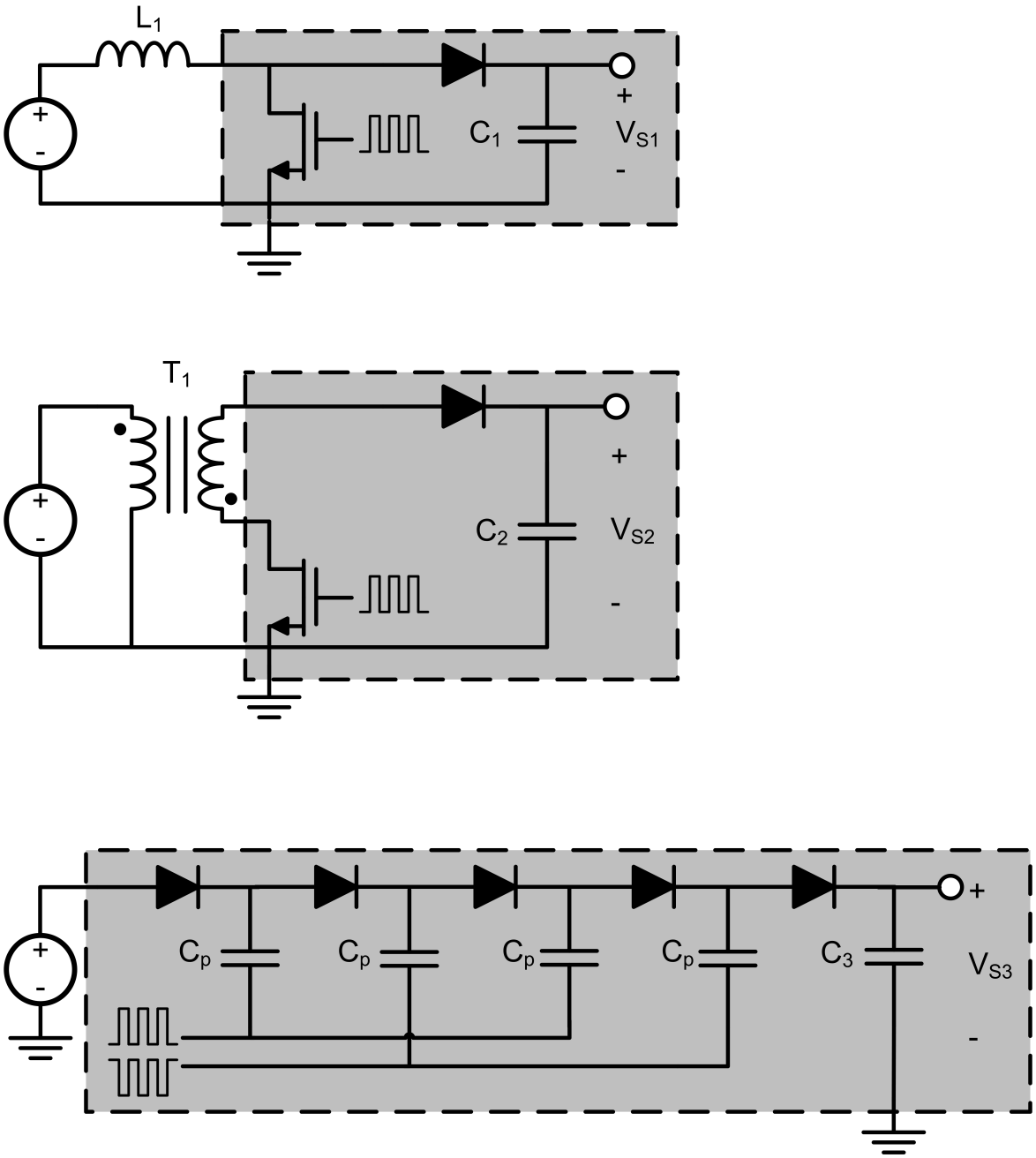

Figure 1.2. Simplified diagrams for boost converter (top), flyback converter (middle), and charge pump (bottom) circuits, with dashed boxes marking the components that can be implemented on-chip

boosting converters, and successfully commercialized microwatt range energy harvesting ICs exist [23, 24]. Flyback topologies are particularly interesting in the context of energy harvesting, as startup voltages as low as 40 mV are enough to self-start operation, and end-to-end conversion efficiencies up to 60% are achievable. The transformer involved is bulkier and more expensive than an inductor, which increases size and cost. In contrast with boost and flyback converters, charge pumps are compatible with standard CMOS integration but tend to suffer from lower conversion efficiency. The low harvested voltages reduce the efficiency of the charge pump dramatically, as switches cannot be driven well into linear regime. Various designs aim to circumvent these problems, such as locally boosting the control voltages of the gates of the switch transistors. The low supply voltage problem is illustrated in [25]; the >75% efficiency of the charge pump presented in the mentioned work drops down to <40% when the supply voltage drops from 1.2 V, applied from a bench source, down to 350 mV, the harvested voltage from an on-chip photodiode. In this example, the output power of the switched capacitor booster is not high enough to run the circuitry directly, but to charge a thin-film battery so that the system can wake up every 3 minutes and transmit data. The referred work is also a clear example of the inefficiency of silicon photodiode based harvesting for miniaturized smart systems; even if voltage boosting is necessary for the operation of the design, it is better to start from a harvested voltage higher than that can be supplied by a silicon photodiode array in order to make the design more efficient, and as evidenced by the recent move to AlGaAs photodiodes for indoor photovoltaic harvesting by the same research group [20], the idea of using higher bandgap semiconductors for miniaturized smart microsystems is gaining traction.

1.4. Sensor Interfaces

Temperature sensing schemes rely on comparing a quantity of positive or negative temperature coefficient to a reference quantity of zero temperature coefficient, mapping the difference between the two quantities to a change in temperature. Tradeoffs between accuracy, power, conversion speed, complexity and area must be taken into

account in choosing between different approaches to be implemented into the smart microsystem. A useful metric for comparing designs of various approaches is the $\mathrm{J{\cdot}K^2}$ figure of merit (FoM) proposed by Kofi Makinwa [26]. It must be noted that it does not take area into account and favors resolution more, but it is still a good measure for comparison purposes. In the context of miniaturized energy harvesting sensors, primary concerns should be meeting the power and energy requirements, including low voltage operation capabilities. Resolution and accuracy requirements increase the power and area costs, so a trade-off suitable for the application field of the smart microsystem must be made. In the context of smart temperature sensors, the signal bandwidth is in the order of 10 Hz, therefore sampling rate can be kept on the low side to achieve greater resolutions [27]. Various approaches to temperature sensing techniques will be discussed in the following subsections.

1.4.1. ΔV_{BE} based temperature sensing

The gold standard in accurate and linear temperature measurement is the ΔV_{BE} technique. Starting from the ideal diode equation is as follows

$$I_D = I_\mathrm{o} \cdot \left(e^{\frac{V_d}{V_T}} - 1 \right) \tag{1.4}$$

where

$$I_0 = q \cdot A \cdot n_i^2 \cdot \left(\frac{D_n}{L_n \cdot N_a} - \frac{D_p}{L_p \cdot N_d} \right) \tag{1.5}$$

To generalize, the above relations will be rewritten in terms of current densities, by substituting $I_0 = J_0 \cdot A$, as follows:

$$J_D = J_\mathrm{o} \cdot \left(e^{\frac{V_d}{V_T}} - 1 \right) \tag{1.6}$$

If diode potential V_d is much greater than the thermal voltage $k \cdot T/q$,

$$V_d \approx \frac{k \cdot T}{q} \ln\left(\frac{J_d}{J_o}\right) \tag{1.7}$$

The potential difference between two p-n junctions biased at two different current densities becomes;

$$\begin{aligned} V_2 - V_1 &= \frac{k \cdot T}{q} \ln\left(\frac{J_2}{J_0}\right) - \frac{k \cdot T}{q} \ln\left(\frac{J_1}{J_0}\right) \\ &= \frac{k \cdot T}{q} \ln\left(\frac{J_2}{J_1}\right) \end{aligned} \tag{1.8}$$

The difference between the two junction potentials is independent of J_0 as opposed to the potential of a single junction. As a result, doping profile and concentration related fabrication variations are cancelled out, leaving a logarithmic dependence on user defined parameters and a linear dependence on absolute temperature, at least in ideal case. Therefore the untrimmed accuracy for this technique is high (in the order of ± 3 °C for classic implementations), and ± 0.1 °C 3σ accuracy is achievable when dynamic element matching in bias circuitry and chopping is employed in more advanced designs [27]. The implementation usually involves diode connected substrate PNP bipolar transistors and the difference between two base-emitter junction potentials is of interest in this scheme, hence the expression ΔV_{BE}. Note that a single p-n junction could be biased at one current and have its junction potential digitized, and then switched to a multiple of the initial current level and measured again so that subtracting the two measurements digitally would yield a ΔV_{BE} measurement, and given that the measurements are made fast enough that the die temperature does not change, this approach could save area and power. Advanced implementations [28] achieve 0.003 °C resolution and ± 0.15 °C 3σ trimmed accuracy with a conversion time of 2.2 ms consuming 55 μA at a minimum supply voltage of 2.9 V; yielding a FoM of 3.6 pJ·K^2, and an area of 0.8 mm^2 in 0.7 μm process. Here, we see that despite the stellar resolution, accuracy and FoM, the power consumption is too much for har-

vested power within 1-10 μW range along with whole chip implementation that leaves no space for transmitter, state control logic, etc. A better suited implementation uses 5 μW at 1.5 V with a resolution FoM of 11 pJ·K^2 using a SAR ADC to "focus" into the measurement voltage range as a part of 2nd order zoom-ADC to speed up the conversion and relax gain requirements of the integrator amplifiers [29]. The first integrator stage features a fully differential telescopic cascode draining 600 nA, while the inverter based second stage consumes 140 nA. Bias currents are in the range of 100 nA, which is much lower than what is prescribed in [27]. The 0.16 μm implementation occupies 400 μm $\times$ 200 μm on-chip area, but decimation filter and digital backend is implemented off-chip, which tend to consume both major area and power depending on the implementation.

The ΔV_{BE} technique can be adapted to diode connected DTMOS transistors, biased at current levels in the order of 100 nA to achieve lower power consumption and more compact design that is more suitable for miniaturized energy harvesting smart microsystems [30]. Power consumption is 600 nW, area is 0.085 mm^2 in 0.16 μm, resolution is 0.6 °C with a conversion time of 6 ms; yielding a FoM of 14.1pJ·K^2. The design features inverter based integrators and comparators to realize a zoom-ADC to fit the ultra-low power and low voltage requirements. It may be worth noting that the use of DTMOS diodes in ultra-deep submicron technologies such as 65 nm may be problematic as gate leakage is very high compared to process nodes such as 180 nm; input impedance appears to be resistive below 0.1 Hz for 180 nm as opposed to 1 MHz in 65 nm [12]. One drawback with the $\Sigma\Delta$ based converters that are presented above is that decimation filters and digital back-ends are located off-chip; in a full implementation the additional power and area demands imposed by the additional circuitry may be detrimental for the energy harvesting smart microsystem.

1.4.2. Resistance based temperature sensing

Resistor string based SAR ADCs have been proposed for temperature sensing without resorting to bandgap references [31]. A supply insensitive current source biases a reference resistor with a negative overall temperature coefficient and the pos-

itive temperature coefficient resistive DAC. Using a unique successive approximation scheme, the reference resistor is approximated coarsely, then further adjustments made by switching in smaller resistances until the reference resistor voltage is approached. Consuming 20 μA at 1.2 V with a resolution of 0.25 °C at a conversion time of 12.5 μs, the FoM for this implementation is 15.6 pJ·K^2, and while the power consumption is high, the energy consumed for one measurement is 0.3 nJ, which may make this a suitable, simple implementation for energy harvesting microsystems if the sensor is shut down while not in use and the instantaneous current demand is met by a backup energy storage scheme.

1.4.3. Time domain temperature sensing

Time based conversion schemes leverage either temperature dependent mobility or convert ΔV_{BE} quantities into time domain through voltage or current controlled oscillators. A relatively conventional implementation features a relaxation oscillator with a 14-bit current mode SAR DAC adjusting the charge and discharge currents, controlling the frequency [32]. A time to digital converter (TDC) digitizes the output frequency of the oscillator and providing feedback to SAR ADC if the TDC overflows. Reference input of the oscillator is multiplexed between PTAT and CTAT voltages, in effect forming a $\Sigma\Delta$ ADC. The sensor is calibrated by an on-chip voltage sensor without needing to set the temperature to a calibration value, which makes the design more practical. Under 1.8 V the sensor draws 260 μW, measuring at a resolution of 0.25 °C with 480 kS/s. As a result, conversion takes approximately 0.5 nJ, resolution FoM becomes 32.5 pJ·K^2. Built in 0.18 μm technology node, the total area is 0.122 mm^2.

The change in carrier mobility can also be exploited to detect temperature changes in an interesting pulse shrinking scheme [33]. The circuit consists of a delay line made out of inverters with identically sizing and one pulse shrinking stage that has disproportionate PMOS and NMOS strengths so that the rising edge is faster than the falling edge. When this pulse is fed to the delay stage again, the result is a slightly shortened pulse, which arrives at the pulse shrinking stage again for cycles

until the pulse disappears altogether. The amount of pulse shortening depends more or less linearly on temperature, and the longer it takes for the pulse to disappear through the oscillator the lower the temperature is. Total area is 0.025 mm^2 in 0.35 μm process, power consumption is 1.5 μW under 3 V supply, measuring temperature with a resolution of 0.2°C with a rate of 10 S/s. The energy per conversion is 150 nJ, but power consumption is low enough that the energy harvester source such as a photodiode can continuously supply the necessary power if the design were adapted to a smaller technology node that would allow 1 V operation.

Temperature dependence of drain current in the subthreshold regime can be used in a ratiometric manner to minimize process dependencies, counting the time it takes to discharge a reference capacitor while counting the output of an oscillator to create a very energy efficient sensor [34]. In this example, instead of attempting to transform the exponential dependence of drain current to temperature into a linear relation in analog domain, a logarithmic counter is implemented to perform that transformation in digital domain. The 65 nm design takes 26 μm $\times$ 60 μm in total, with the sensor occupying 7.4 μm $\times$ 60 μm, consuming between 3.16 to 0.24 nW and 630 to 48 pJ with a 0.28 °C resolution and a 3σ inaccuracy of $\pm$1.2 °C. This design is intended for dynamic thermal management purposes in the context of VLSI-ULSI applications such as DRAMs, using a minimalistic approach to implement the sensor in time domain. The sensor output can be processed and corrected digitally, leveraging the gate size advantage of the ultra-deep submicron process nodes, and can be put to sleep mode when not in use to minimize power consumption. This aspect of the sensor described in [34] can also be adapted to an energy harvesting design, where minimized use of analog blocks and the ability to power down sections not in use are advantageous design features in a setting of limited energy.

1.4.4. Thermal diffusion based temperature sensing

Finally, the thermal diffusivity of bulk silicon can be leveraged to implement a thermal integrator based $\Sigma\Delta$ temperature sensor, using on-chip heaters and detecting the change in temperature in a separate location by means of a thermopile. Heater

and thermopile are implemented as diffusion resistors, an autozero amplifier senses the thermopile voltage and drives a comparator, and the output of the comparator drives the current sources that bias the heater resistor; thus closing the $\Sigma\Delta$ loop. Analogous to the electrical integrator, the heat mass of the silicon die performs as a low-pass filter in thermal domain. The thermal diffusivity of silicon is a strongly temperature dependent variable ($T^{-1.8}$), which ensures high accuracies even without trimming the device for errors. As the design measures the delay between the turn-on of the heater and the detection of the heat change in the thermopile, it is an inherently time-domain based ΔV_{BE} architecture and as such, increased speed in more advanced process nodes can be leveraged fully. In addition, as the feature sizes become smaller, the accuracy of this family of sensors improves [35]. The sensors can be made very small, which allows multiple temperature sensors on multi core chips, or more interesting applications such as solid-state wind flow and direction sensors. The power consumption is impractically high for the context of energy harvesting microsystems, though, in the order of milliwatts to tens of milliwatts.

System level decisions are to be made in order to reduce area and power and/or reduce conversion time in order to fit the requirements of millimeter-cube sized smart microsystem that includes not only a sensor, but also transmitter, control logic, possibly other sensors, etc. If the sensor is to operate for long time intervals with low power consumption, continuous harvesting of energy needs to be guaranteed, whereas if the system is to store energy and perform the conversion with relatively high power in a short amount of time, the power output capabilities of the energy storage element as well as the voltage drop that will happen must be accounted for. Indeed, the best approach would be to aim for an optimally low power and low energy combination, enabling sustained operation while ambient energy is enough by itself or if there is a reduction in the available energy, the microsystem would rely on its backup energy storages.

1.5. Data Transmission in Smart Microsystems

Two physical domains are particularly conducive for free space data transmission in the context of wireless batteryless microsystems; optical and RF. Alternative technologies such as magnetic or acoustic coupling can also be adapted for data transmission. The data transmission scheme must be selected with the following criteria in mind:

- Energy requirements: Under the constraint of wireless, batteryless operation, the energy must be harvested from an outside source, and as discussed in the previous chapter it can be scarce. The transmission process must consume low enough energy that the harvested and stored energy allows sustained operation. On the other hand, the power usage during transmission can be high if transmission is kept brief, staying within the energy limitations discussed above. If the energy must be actively applied from an outside source, as in RFID tag designs, that becomes a factor as well for determining the practicality of the design.
- Read range, readout circuitry cost: The range from which the sensor data can be read determines how practical the design can be. Perhaps more important is the cost of the readout circuitry necessary for receiving the said transmissions; a very sensitive piece of equipment with a low noise floor may be able to extract the data from quite a distance, but if the unit cost is too high the applicability of the design becomes limited by the availability of the said equipment.
- External elements necessary for transmission: When off-chip elements are being resorted to, the cost of these additional elements as well as their contribution to the overall size envelope of the microsystem must be taken into consideration. Specifically, this includes off-chip antennas, LEDs, laser diodes as well as necessary energy storage elements such as SMD capacitors. The cost is more of a question of volume. Depending on the number of units to be fielded,the cost of the external elements may not be a primary concern; this can apply to cases of very few devices, where the total absolute cost is low enough, or very high volume applications where acquiring the necessary external elements in bulk provides an

economical advantage. Clearly, off the shelf products that can be obtained from various suppliers and/or from alternative manufacturers would lower the costs and help avoid bottlenecks in production.

- Data rate: In the context of smart microsensors the bandwidth for data transmission is expected to be low, especially if slow changing environmental variables are being measured. Data rate is more or less a question of available energy storage options.

The use of LEDs as a means for free space visible light communications (VLC) is gathering interest as the frequency bands available for unlicensed use becomes more and more crowded. Several hundred THz of unlicensed spectrum, immunity to electromagnetic interference with RF systems and additional security due to line of sight nature of the link are the prominent advantages, as described in the recent IEEE 802.15.7 Strandard for Local and Metropolitan Area Networks [36]. The line of sight nature of communication of the LED may be leveraged to reduce interference with neighboring LED based communication systems in environments with large numbers of coexisting smart microsystems, as envisioned by the Internet-of-Things (IoT) concept. The advantages of optical communications include low power consumption, no need for license (as of the writing of this work), wide bandwidth, unregulated spectrum, and the use of low power, low cost, well-established optoelectronics technology [37]. Like a radio antenna, the LED can be used as a receiver just as it is a tranmsitter, and discrete designs built out of off the shelf components supporting 50 Mb/s at 5 cm and 100 Mb/s at 1 cm, consuming an estimated 20 mW of power without focusing optics [38]. The use of LED as a wavelength selective photodetector reduces interference of ambient light sources as well as reducing the cost, as PIN diodes used for photodetection are expensive, and combines transmitter and receiver device into one, reducing complexity. Using micro-LEDs of 50 μm diameter, 3 Gb/s data links for distances over 5 cm has been demonstrated [39] with a power consumption estimated at 20 mW, without lenses as above. The high data rate and high power consumption may leave these implementations outside the scope of energy harvesting smart microsystems, but they provide good examples for demonstrating the capabilities of a

low cost LED in establishing short range optical data links. A fully integrated LED transmitter for IEEE 802.15.7 VLC standard has been recently published, transmitting at 5 nJ/bit to 2 m without lens and 20 m with lens, demonstrating the increasing viability of the LED based optical communications for the near future [40]. VLC is foreseen as a supplementary addition to 5G communications, and schemes to achieve compatibility with readily existing CMOS cameras on ubiquitous mobile phones has been proposed [41]. LED based communications also find use in subdermal implants transmitting neural recordings to the end user [9]. Compared to LED based VLC, RF methods are more prevalent in establishing a wireless link, especially for energy harvesting smart microsystems. In the context of energy harvesting microsystems, back-scattering technique is employed for very low power RF communications. Back-scattering involves modulating the terminating impedance of an antenna to change its reflectivity to the incoming radio waves, using very little power, in contrast with active transmission schemes. The power is delivered by the interrogating RF field and the response from the tag comes as strong and weak reflections depending on the data being transmitted. While a direct comparison is not possible as the commonly used back-scattering technique does not have a one-to-one correspondence in optic domain, the power and energy requirements in such systems is instructive in determining the requirements for an energy harvesting design that uses such technology. In back-scattering, the externally applied power is a determining factor for read-range and therefore must be taken into consideration in evaluating the practicality of the overall system. Considering millimeter-cube sized energy harvesting systems, the antenna area is limited to few millimeter-squares, which means that the antenna length will be much shorter than the wavelength of the transmission frequency, and just as in the case of RF energy harvesting the data transmission will be suboptimal.

In [42], an RF based design built in 0.18 μm harvests energy at 5.8 GHz and transmits via a UWB data link via two separate antennas taking up a total of 4.5 mm^2. Received RF signal is rectified and stored in a capacitor and while powered at an EIRP of 4 W, the chip consumes a total of 16 μW, transmitting up to 7 cm using 12 μW of the total power. In contrast, the 0.13 μm design presented in [43] features a

0.5 mm^2 coiled antenna, operating at 2.45 GHz, consuming 0.75 μW to transmit data by back-scattering with a read range of 0.5 mm. The power delivered to the device is 0.5 W, and the device consumes 9 μW for reading from a non-volatile memory and 56 μW for writing. In other words, more than enough power can be delivered to the on-chip antenna, but the read distance is very short due to back-scattering technique. A multi-standard 0.13 μm temperature sensing tag operates on 13 MHz, 2.4 GHz and 5 GHz bands, back-scattering to transmit on-chip temperature sensor or off-chip sensor data picked up by its sensor interface, digitized by a 10-bit SAR ADC with a sample rate of 36 kS/s [44]. Total power drawn is 8 μW, and the tests were conducted from contact distance. Pulse based UWB transmission schemes in RF domain is shown to be the most energy efficient way to transmit and receive data, consuming 5 nJ/bit for transmission and using low complexity, energy detection based efficient receiver topologies [45]. Optical implementations of pulse based transmission schemes are perhaps even simpler in that pulse shaping is not needed as opposed to RF domain implementations; forward biasing the LED for a brief period of time suffices in creating the pulse.

1.6. Conclusion

Designing a millimeter-scale smart sensor design requires a careful balance of features, making optimal use of the energy available to the system constrained by the small volume of the energy harvester. 1-10 μW/mm^2 can be expected from such size limits if photovoltaic harvesting is used, less if alternative means are employed. Harvesting efficiency has to be maximized as the harvester is already size limited, and additional costs to improve harvesting efficiency by using a more appropriate technology may be well worth the effort and cost. The harvester usually supplies voltage levels too low to be useful for sensor design and/or analog interfaces, so the high voltage is very commonly supplied by a voltage boosting scheme. The conversion inefficiencies detract from the already low energy harvesting efficiencies. Circumventing the need for intermediary conversion stages might be necessary for lowering the minimum energy floor for the design to operate. Designs with high power demands require an

energy storage scheme to support short bursts of instant current demands, in contrast to low power designs which can operate directly from the power supplied by the energy harvesting device. As the smart microsystem is expected to interface with the outside world in order to perform a useful operation, sensors and interfaces are important to pay attention to. Temperature sensors are usually included in published energy harvesting millimeter-scale sensors as a functional block to prove that the design can support the integration of analog sensor interfaces. System level innovations have been applied to the well known problem of temperature sensing, reducing energy per conversion and increasing sensor figure of merit. These innovations can be applied to other sensor interface problems that can be faced in energy-harvesting millimeter-scale designs. Cutting edge temperature sensor designs perform at a resolution FoM of 5-50 pJ/K^2, however some designs feature too much continuous power use to be suitable for energy harvesting designs. Generally, $\sim$1 μW power use, $\sim$1 nJ/conversion are goals for the sensors in autonomous smart microsensor applications; very high resolutions increase power consumption and conversion time too much that their operation cannot be sustained by the energy harvesting device. Finally, the recorded sensor data is to be transmitted to the end-user. Prominent wireless techniques feature RF and optical communications of some sort, and the efficiency of the transmission is again limited by the scale constraints. Not only the energy and power is limited, but also the size limitations require reduced antenna or LED dimensions. The reduction in antenna size reduces the transmission efficiency, a disadvantage the LED suffers to a smaller extent. 100 pJ/bit – 1 nJ/bit can be expected, and transmission in millimeter-scaled energy harvesting designs tends to have ranges of 1 mm – 10 cm.

An optimal combination of the discussed alternatives along with system level innovations will help designers create smaller smart systems operating at lower energies. In order for these devices to become real, practical commodities that enhance the life quality of people around the world as opposed to being limited to laboratory prototypes, certain aspects to them have to change.The following chapters seek to provide some solutions to make an incremental contribution to this rapidly expanding field, discussing LED based energy harvesting and data transmission in the context of

energy harvesting smart microsensors and the evolution of the implemented designs throughout the progress of this thesis.

Chapter 2 details the basis of the approach proposed by this thesis to miniaturized photovoltaic harvesting, discussing the use of a light emitting diode (LED) as an efficient energy harvester aside from its data transmission capabilities.

Chapter 3 details a proof of concept design that harvests optical energy and transmits a fixed device ID optically using single LED, and a smart temperature sensor that runs directly from the harvested voltage.

Chapter 4 discusses the experimental results for the first and second generation designs described in *Chapter 3*.

Chapter 5 proposes an ultra low power, ultra low energy smart microsystem that uses a more efficient transmitter architecture as well as a more energy efficient smart temperature sensor. The details regarding the design of the transmitter and the sensor featured in this third generation design are further discussed in *Appendices A* and *B* respectively.

Chapter 6 discusses the measurement results for the design described *Chapter 5*. Details on the experimental setup are discussed in *Appendix C*.

Chapter 7 concludes this work, summarizing the work done and the end results.

2. DESIGN CONCEPT

2.1. Introduction

The smart-dust concept aims to realize a smart microsystem that can fit inside a volume of few millimeter-cubes and harvest the energy necessary for performing useful functions, such as sensing and transmitting environmental data. The inclusion of batteries, even at the button cell level, causes a dramatic increase in the overall size of the microsystem, pushing the volume from a few millimeter-cubes to hundreds of millimeter-cubes or centimeter-cubes. In addition, the unit cost will increase and be heavily determined by the cost of the battery. The inclusion of thin film and thick film batteries as energy reservoirs that can be charged up slowly and used to charge storage capacitors for more instantaneous current demands have been demonstrated [3], again at economical costs as well as the increased size. Following the previous discussion on miniaturized energy harvesting designs, the use of photovoltaic energy harvesting in this context is a logical first choice, as the power delivered per millimeter-cube is the highest in photovoltaic harvesting, especially for outdoor lighting conditions [21].

The short history of smart energy harvesting microsystems is also an indication of the success and popularity of photovoltaic energy harvesting. Identification chips designed for subdermal implantation have been fabricated for commercial purposes, powered optically by means of an external laser and transmitting data through a minimal size antenna, which has found use in tagging individual ants in studying ant behavior [10] and in tags bonded on MEMS microgrippers [11]. The size limitation of the radio frequency integrated chip (RFIC), 500 μm x 500 μm in this application, limits the size of the antenna to a dimension that is infeasible for the harvesting of RF energy from practical distances, allowing only data transmission within distances of a few millimeters. Thus, optical power delivery using an on-chip photocell has been used in these examples [10], as well as in wearable biomedical sensors [46], implants [47], retinal and other prostheses [48], individually addressable neurostimulators [49], and in biomedical applications such as interventional magnetic resonance imaging (MRI) [50].

In wireless power and data transmission, optoelectronic systems can be smaller than the alternatives since they can deliver higher power densities simply using lasers or other light sources. RF tags that has on-chip silicon photodiodes has been powered using laser beams, which fit to an area of 500 μm x 500 μm [11]. However, these small RF tags communicated with RF signals using small on-chip antennas, limiting their working distance to around 5 mm. A 1.5 mm^3 wireless intraocular pressure monitoring system has been achieved using an integrated 0.07 mm^2 solar cell, implemented as p-n junctions on CMOS layers. This solar cell can generate a maximum power of 80 nW under atmospheric solar spectrum (100 mW/cm^2). It also utilizes a 4.7 nJ/bit FSK modulating RF transmission over a distance of 10 cm [3]. A millimeter scale wireless imaging system is also implemented by optical powering, optical data reception and RF data transmission. The system can generate 456 nW electrical power under 10 klux light [51]. A common theme with the above implementations is that each example features a wireless link to transmit data to the user, which is achieved by an on-chip radio with on-chip antennas, limiting the transmission range to a few millimeters due to size limitations imposed by the system envelope on the antenna size. The short history of smart energy harvesting microsystems is also an indication of the success and popularity of photovoltaic energy harvesting, however there are problems to be circumvented in order to realize successful implementations.The following sections will first review the shortcomings in miniaturized photovoltaic energy harvesting, then propose a solution that will not only result in increased photovoltaic harvesting efficiencies, but also will bear the added benefit of data transmission that must be handled separately in conventional design approaches

2.1.1. Problems with on-chip photovoltaic harvesting

A major problem of silicon p-n junctions in standard CMOS miniaturized smart systems is that while the silicon photodiode can provide adequate current output, the open circuit voltage is limited by its relatively low bandgap energy [52]. Around 0.5 V, the open circuit voltage of the silicon CMOS photodiode is already severely limiting especially analog design; indoor illumination levels can result in generated voltages of

around 0.3 V [53]. Cascading multiple p-n junctions to create two serially connected photodiodes yields highly reduced efficiencies at 3.5%, in contrast to a single p-well on deep n-well photodiode efficiency of 7.5%, due to a lack of bulk isolation [54]. Although SOI processes can provide such isolation that enables successful implementations [55], they are more expensive than standard CMOS processes. Furthermore, the area consumed by the on-chip photodiode can take up the majority of the chip area [55, 56], reducing the already expensive available die area that could otherwise be used for more functionality and depending on the energy harvesting necessities, dedicated, separate dies covered entirely with photodiodes become necessary [25]. Even more problematic than these issues are the inevitable illumination of silicon regions around the clear photodiode region when optical powering is directed on the silicon die. Strong light around this region generates high leakage currents on the silicon die, deteriorating low-power circuit implementation and causing reliability problems. In fact, directed laser beams have been proposed as a method for testing the proneness of a chip for latch-up at its various sites [57]. Hence, it is more advantageous to have dedicated dies for the photovoltaic cells stacked on the IC that has all the functional digital and analog blocks, and having the latter covered with dark epoxy to block light. As it will be discussed later on, the approach proposed in this thesis takes this idea one step further, demonstrating the use of an external photovoltaic cell for more than just energy harvesting. The problem of low harvested voltage can be illustrated by examining the minimum needs for major functional blocks. For example, the minimum supply voltage, $V_{DD,min}$, to allow linear rail to rail input for a CMOS differential pair is calculated as [58]:

$$V_{DD,min} = 2 \cdot V_{GS} + 2 \cdot V_{DS,sat} \tag{2.1}$$

In Eq.(2.1) V_{GS} is the gate-source voltage and $V_{DS,sat}$ is the drain-source saturation voltage of a transistor. Substituting for V_{GS} necessary to keep the transistors in saturation region with $(V_{GS} = V_{th} + V_{DS,sat})$, equation (3.1) becomes

$$V_{DD,min} = V_{th,n} + |V_{th,p}| + 4 \cdot V_{DS,sat} \tag{2.2}$$

where $V_{th,n}$ and $V_{th,p}$ are the threshold voltage levels of NMOS and PMOS transistors, respectively. Assuming an average threshold voltage of 0.4 V for contemporary submicron CMOS technologies, and minimum 0.1 V overdrive voltage, the minimum supply voltage can be 1.2 V and above for analog design. Lower voltages than this can be used if the transistors are to be operated in the subthreshold regime, but matching and bandwidth are two major obstacles with this approach [21]. To solve the low voltage problem, voltage boosting solutions have been applied to step up the harvested voltages to the operational voltage level of the sensor node. The low supply voltages, however, reduce the efficiency of voltage boosting architectures such as charge pumps as illustrated in the context of both generalized applications [59] and photovoltaic energy harvesting millimeter sized designs [53, 55, 56, 60]. The current drawn by the charge pump loads the photodiode and moves the operating point further below the already low open circuit voltage, further reducing the efficiency. To alleviate this, maximum power point tracking can modulate the current drawn by the step-up converter to keep the photodiode bias at the optimal current-voltage point, but this takes relatively complex algorithms that require voltage and current sensing, along with the additional power consumption and area requirement.

2.1.2. LED-based Photovoltaic Harvesting

Following from the successful implementations with off-chip CMOS photodiode dies, designs featuring external, off the shelf optoelectronics made out of compound semiconductors, such as LEDs, for more efficient photovoltaic harvesting are a rational choice. The LEDs are off the shelf components available in large volumes, fabricated and marketed by multiple manufacturers and vendors, which drives the unit costs of these devices lower. In this case, the CMOS portion of the smart microsystem will likely impose the economical bottleneck, depending on the production volume. The gains in energy harvesting efficiency increase the capabilities of the smart microsystem, raising its potential for viable applications. An AlGaAs photovoltaic cell can be optimized for the wavelength spectrum of indoor or outdoor illumination by engineering the composition of the heterojunction to achieve the appropriate bandgap energy,

making it a much more efficient photovoltaic harvester than a silicon one [20, 61]. Different voltage levels, for example from around 0.5 V (1300 nm infrared InGaAsP LED) to around 3 V (450 nm blue InGaN LED) can be generated by selecting a proper commercially available LED with the right bandgap energy satisfying different voltage requirements of ICs. They can be produced in bulk, and be readily integrated to a standard CMOS design by any typical packaging method [1,62]. Being direct bandgap materials, LEDs are more efficient photovoltaic cells for their narrow wavelength range, and capable of optical transmission. In fact, efficient LEDs and heterojunction photovoltaic cells have overlapping aspects in terms of physical structure and design [63]. The reciprocal optical to electrical input-output relationship of a solar cell and a LED can be expressed as a single expression [64]:

$$\phi_{\mathrm{em}}^{\mathrm{norm}}(E_\gamma) = EQE_{PV}\left(E_\gamma\right) \cdot \phi_{bb}\left(E_\gamma\right) \cdot \left[\exp\left(\tfrac{qV}{kT}\right) - 1\right] \tag{2.3}$$

Where $\phi_{\mathrm{em}}^{\mathrm{norm}}\left(E_\gamma\right)$ is the luminescence emission, $\phi_{bb}\left(E_\gamma\right)$ is the blackbody emission, and $EQE_{PV}\left(E_\gamma\right)$ is the external photovoltaic quantum efficiency at photon energy E_γ. In addition, there exists a logarithmic relation between the open-circuit voltage and emissive external quantum efficiency;

$$\ln\left(EQE_{LED}\right) = \frac{q \cdot V_{OC}}{k \cdot T} + \ln\left(\frac{J_{em,0}}{J_{SC}}\right) \tag{2.4}$$

With J_{SC} and $J_{em,0}$ being short circuit and emissive current densities, respectively. Thus, using a direct bandgap LED to harvest photovoltaic energy, does not only provide higher generated voltages, good energy conversion efficiencies but also an optical communication medium for both receiving and transmitting sensor data. Leveraging these two advantages constitute the motivation behind this thesis. The benefits of this approach can be listed as follows:

- By choosing a LED having a higher bandgap energy compared to that of silicon, a higher open circuit voltage can be achieved (1.2 V for near infrared, 1.6 V for red, 1.7 V for green, etc. as opposed to 0.5 V supplied by silicon photodiodes). Circuitry can be run directly from this higher voltage without the need for a step-up converter.
- The commercially available dies of these LEDs have dimensions of around 350 μm x 350 μm, realizing the goal of having a very small wireless and batteryless microsystem. Absorption in indirect bandgap materials require energies in excess of bandgap energy to account for the change of momentum necessary for the transition of the electron from the valence band to conduction band; band to band transition in indirect bandgap semiconductors depends on the availability of phonon states [14]. In contrast, phonon availability is not a requirement in band to band transition with direct bandgap semiconductors. The probability of absorption is higher and therefore photon absorption is more efficient in direct bandgap materials. Furthermore, maximizing the extraction efficiency of photons for solar cells has been demonstrated to maximize device efficiency as well as increasing the maximum voltage supplied by the solar cell. External luminescence is a key parameter in solar cell design as it is in LED device design, and the maximization of this parameter has yielded record efficiency improvements in GaAs solar cells [63]. Using a commercial LED device optimized for efficient external luminescence is doubly useful as it is also an efficient photovoltaic cell for a short range of wavelengths that are about 20-30 nm shorter than peak emission wavelength.
- Placing the photodiode outside of the die saves expensive on-chip area and may be more advantageous especially if numerous functional blocks are to be included in the design. It is also a more robust approach as the die can now be optically isolated, as opposed to the die being illuminated by a high intensity beam of laser. The photons that are not absorbed at the photodiode junction could cause latch-up and substrate noise problems if the photodiode was to be left on-chip.

2.1.3. Optical Data Transmission

As it is desired to minimize the size, weight and cost of the sensor node, using the LED as a means for data transmission and as energy harvester maximizes its utility, increasing its cost-effectiveness. Optoelectronic systems can be smaller than the alternatives, including RFID systems with their coils or antennas, since the sizes of the possible components in these systems such as photodiodes, light emitting diodes or laser diodes are in the order of hundreds of micrometers. The line-of-sight nature of optical wireless communications makes it more secure as opposed to RF communications, since the beam must be intercepted in order to eavesdrop on the communications as opposed to RF communications which is easier to eavesdrop on due to the radiating nature of the RF emissions. Short range optical identification is evaluated to be more secure compared to RFID in security sensitive applications [65]. As the receiver for the optical transmissions is designed to respond to a desired narrow wavelength window, interfering signals are less likely to hinder communication; whereas the ubiquitous RF radiation spanning a vast range of wavelengths can prove problematic in RF communications, especially when the microsystem is operating on a tight energy budget and the signal levels that it can produce are comparable to the background noise.

Design and tuning of an antenna sensitive to the transmission wavelengths are mostly avoided in an optical communication scheme as a photodiode selective to the desired wavelength can be chosen in the design of the photodiode amplifier with no further need for tuning. High electromagnetic interference (EMI) environments would bar the use of RF communications, leaving optical communications as the sole option. One such field of application involves smart catheters for interventional magnetic resonance (MR) imaging use. The high power electromagnetic fields inside MR equipment prevent long metallic wires from being inserted into a patient's body as the said wires would heat up quickly, injuring or causing discomfort to the patient. For this case, delivering power to and communicating with a microsystem through an optical fiber has been proposed and a practical solution is demonstrated, where an on-chip photovoltaic cell is used for powering and a separate laser diode for communication [56]. Since the microsystem is designed to transmit data optically, an external optoelectronic

element becomes necessary, as the contemporary silicon CMOS processes are practically incapable of efficient photon emission. Considering that the use of an external optoelectronic device is unavoidable in these classes of microsystems, maximizing the utility of the said external element for additional benefits would enhance such a design. Integration of optoelectronic elements in similar microsystems has been demonstrated before, placing the external elements in close proximity to the silicon die with the entire system being bonded on the same surface [53, 56, 60]. LED's have been used as photodetectors in sun photometry due to their sensitivity to desired wavelength ranges [61], in bi-directional fiber optics applications where a single LED is used to transmit and receive data [66] and in a matrix format as tactile sensors [62].

2.2. System Concept

Leveraging the ability of the AlGaAs LED for its abilities in efficient photovoltaic harvesting and optical transmission, the evolution of microsystem architecture covered in this thesis aims to provide a framework that is flexible and adaptable for various applications. The harvested voltage will be high enough that no intermediary step-up conversion schemes be necessary to support the operation of analog blocks such as bandgap references, comparators and amplifiers. For demonstrative purposes temperature sensing capabilities are integrated into the described framework, as a comprehensive design example for the illustrating the capabilities of the proposed approach as well as overcoming the challenges faced in miniaturized energy harvesting designs. During transmission the open circuit voltage of the LED must be exceeded to forward bias it; as the open-circuit voltage is the maximum harvested voltage that can be provided by the LED, a boosting scheme optimized for the transmission cycle is necessary. The harvested voltages are to be stored in external capacitors and data is to be transmitted bit by bit as enough energy becomes available for each bit; as the optical reception of the microsystem is expected to vary, the charge-up time for the capacitor and the delay between transmitted symbols will vary as well. Therefore the transmission scheme must tolerate the availability of the ambient energy in the environment. The overall system combines transmitter and sensor blocks to achieve

an autonomous energy harvesting design that can be minimized to millimeter-cube size limits, as illustrated in Figure 2.1.

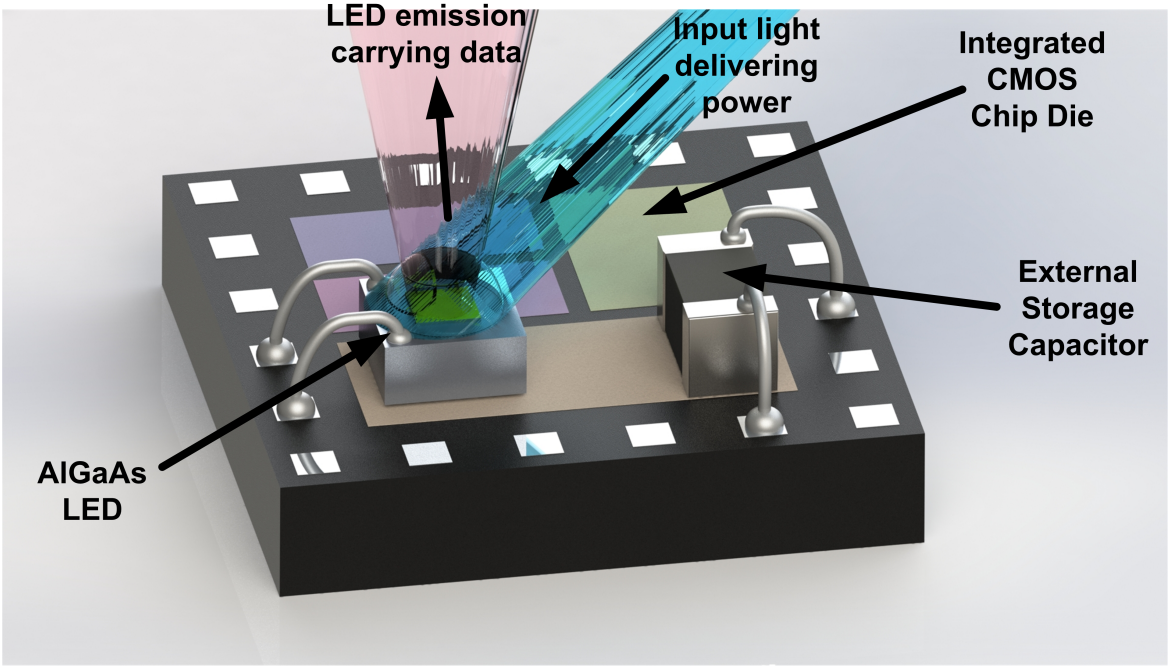

Figure 2.1. Conceptual representation of the proposed microsystem

2.3. Conclusion

The structural properties and the solid-state physics of the LED make it not only an efficient emitter of photons, but also an efficient harvester of photons as well, giving high optoelectronic conversion efficiencies as opposed to photovoltaic cells that can be realized on standard CMOS processes. In addition, the high bandgap energy of the selected LED allows the harvested voltage to be high enough that it can be used without needing voltage boosting for powering analog circuitry, and if necessary, voltage boosters will operate with higher efficiency with the higher voltage supplied by the LED. Removing the intermediary stages that result in inevitable losses in power conversion efficiency, the designer can reduce the absolute minimum necessary energy that allows the microsystem to operate. LED based transmission allows simple, low energy communication schemes that are immune to EMI, and the small size of the

LED die enables millimeter-scale integration; as opposed to RF domain transmission schemes where millimeter-scaled antenna sizes severely reduce transmission efficiencies for practical frequency ranges in use.

3. FIRST AND SECOND GENERATION DESIGNS

3.1. Introduction

Following from the previous chapter, the capability of the LED to harvest optical energy and transmit optical data requires demonstration, which is the aim of the first generation design. While the harvested voltage is high enough to power analog circuitry with, the maximum voltage that can be extracted from the LED is the open-circuit voltage, as discussed in Chapter 1, which has to be exceeded in order to forward bias the LED in order to emit photons. Therefore, a voltage elevation scheme becomes necessary, and the first generation design features a charge pump to achieve this. The second generation design integrates a time-based smart temperature sensor into the existing energy management framework to demonstrate that vital analog design blocks such as amplifiers, bandgap references, oscillators, etc. can be operated directly form the harvested LED voltage.

3.2. System Description

The first generation microsystem consists of a LED die, a storage capacitor and an ASIC die. Its block diagram is shown in Figure (3.1). The ASIC is implemented in UMC 0.18 μm CMOS technology to exploit its low threshold voltage values, which still has lower static leakage compared to smaller processes such as 0.13 μm or smaller feature sized process nodes [12]. Other reasons are its wide availability and low cost. The system operates in energy harvesting and data transmission modes. These modes are controlled by the ASIC. Initially, ASIC puts the LED in energy harvesting mode, converting the optical energy to electrical energy. Electrical energy is stored on a storage capacitor. Once the voltage over the capacitor exceeds a certain value, ASIC puts the LED in data transmission mode. These are achieved by the supply control switch, output switch and Schmitt trigger blocks of the ASIC. The ASIC drives the LED with pulses to generate double light pulses for logic 0 and single pulse for logic one. Charge pump, pulse generator and a 16-bit read only memory (ROM) blocks are

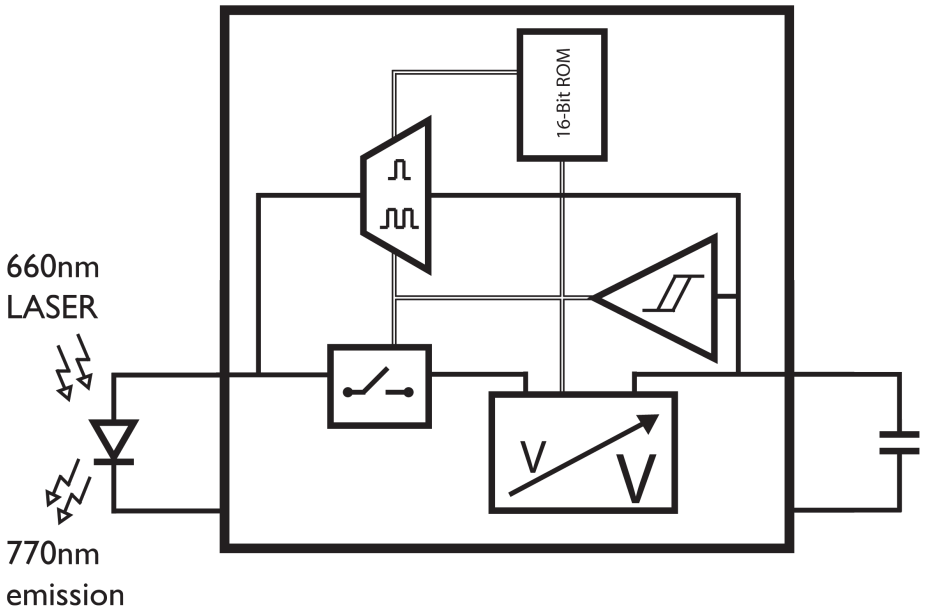

Figure 3.1. Block diagram of the first generation design

used for this purpose. The hardwired ROM data is transmitted repeatedly as long as there is enough stored energy. Transmission rate depends on the power of illumination. The LED must be forward biased adequately such that enough current can be injected to achieve practically detectable levels of photon emission. The photovoltaic voltage induced by the absorbed photons in the LED is lower than the turn-on voltage of the LED for light emission. Therefore, the generated voltage supplied by the LED must be elevated and stored in a capacitor to intermittently forward bias the LED and generate the desired optical transmission. The optical power output generated by the LED is linearly dependent on the current injected to the LED [14], and a minimum of 1 mA current is aimed to be discharged over the LED during a transmission event. To achieve these minimum current levels, about twice the open circuit voltage of the LED is generated by means of a charge pump, storing the elevated voltage at a storage capacitor for future use. The charge pump operates at supply voltages lower than the nominal supply voltage for the 0.18 μm CMOS technology (at or below 1.2 V as opposed to 1.8 V), therefore the design must tolerate suboptimal supply voltages and provide high enough output DC levels at the expected low supply voltages. The load of the charge pump is mostly capacitive, and the charge up time is not critical

but determines the time interval between the transmission of two bits and therefore the data rate. The design constraints for the charge pump in terms of its output current drive capabilities can be more relaxed, as the charge pump does not need to drive a constant current load. In the case of a charge pump driving a constant current drain, the charge pump has to be able to support the current drawn from its output, otherwise, its output voltage drops. The charge pump can supply higher output currents if larger capacitors and faster clocks are used. This reduces power efficiency since it causes large clock buffers drive large capacitive loads.

By using a wide bandgap optoelectronic element, voltage levels in the range of 1.2 V can be reached without suffering the area and efficiency penalties that would result from an on-chip photodiode coupled with a charge pump operating at a low voltage. Digital and carefully designed analog blocks can be operated directly from the voltage supplied by the LED. Additionally, a charge pump running with lower supply voltages is less efficient as the threshold voltage drops become comparable to the supply voltage, requiring more numerous stages to achieve the same levels of output voltage. The elevated voltage stored at the capacitor is discharged over the LED when it reaches a set level and the recharging of the storage capacitor commences as the stored voltage drops below a minimum value. The current through the LED decreases exponentially during discharge as the storage capacitor voltage approaches the open circuit voltage of the LED after which it becomes the saturation current of the LED and photon emission practically ceases. The discharge cycle must be stopped before reaching the open circuit voltage. Otherwise, the system gets stuck at this operating point. When the charge pump starts to charge up the storage capacitor again, its output reaches the desired high voltage level after a certain time. This ends the charging cycle. Before the discharge cycle starts, the remaining of the circuitry is disconnected from the LED to protect them from damage due to over voltage and also to maintain a more stable power supply, which ensures the stability of the memory elements. To retain the state of the memory elements, an on-chip capacitor acts as a backup power supply as the blocks are disconnected from their main power source, the LED. When the voltage at the storage capacitor reaches the set upper limit, the digital

blocks are isolated from the power supply (LED), and the shift register pushes the bit to be transmitted. A single pulse or two pulses in quick succession is generated within a single discharge cycle according to the output of the shift register, signifying logical 0 and 1 values, transmitting a single bit at a time. When the stored voltage drops below the minimum set point the next charge up cycle is initiated for the transmission of the following bit, reconnecting the digital blocks back to the LED power supply, disconnecting the storage capacitor from the LED, and commencing charge pump operation.

To test the capabilities of LED as a photovoltaic cell, a commercially available 770 nm AlGaAs LED was exposed to 660 nm laser beam of varying intensities. Optical power of the laser beam was measured using a ThorLabs power meter with S121C sensor. For comparison purposes, a commercially available silicon photodiode (Hamamatsu S2387) and a PIN silicon photodiode (Hamamatsu S5973), which have better conversion efficiencies than CMOS on-chip photodiodes, are also tested. To make a fair comparison, current density values of the devices are calculated by dividing the measured current values by effective areas of each diode and plotted against obtained voltages as shown in Figure 3.2. The effective device area values are 1.2 mm^2 for s2386, 0.12 mm^2 for s5973 and 0.1 mm^2 for the 770 nm LED. Tests are conducted with 120 mW laser power delivered with a spot size of 1.5 mm diameter, giving a power density of 68 mW/mm^2. PIN diodes are expected to have better photovoltaic properties than the regular photodiodes. This can be seen in Figure 3.2 with a maximum obtained power density of 12.5 mA/mm^2 compared to 2.5 mA/mm^2 for silicon photodiode at an optical power density of 68 mW/mm^2. This is 15.3 mA/mm^2 for the LED showing that for laser illumination of 660 nm wavelength, AlGaAs LED performs better than silicon PIN photodiodes with a power conversion efficiency of 22%. It also gives twice the open-circuit voltage of silicon diodes, which can be used to directly supply the circuitry without needing intermediary voltage boosting stages that would reduce end-to-end efficiency.

A similar microsystem has been realized using an on chip CMOS photodiode before [56]. Under a 660 nm laser illumination this photodiode powers a charge pump,

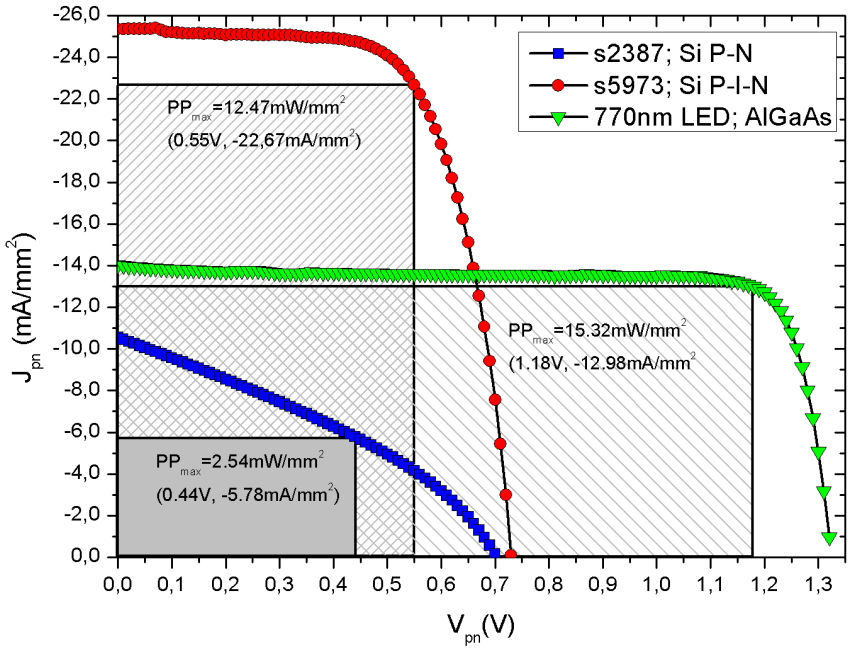

Figure 3.2. Current density vs voltage plots for commercial silicon PIN diode, 770 nm LED, and silicon photodiode under 68 mW/mm^2 660 nm laser illumination.

which then elevates the photovoltaic voltage to 1.2 V to power the analog blocks on the chip. This on-chip CMOS photodiode has a maximum power density of around 2.2 mW/mm^2 and around 0.55 V open-circuit voltage under 68 mW/mm^2 laser illumination [56]. The said photodiode occupies 600 μm x 600 μm on chip area, with additional space taken up by the charge pump. The efficiency of the charge-pump circuit in the related work for this optical power level is around 25%, reducing the available power density for the circuitry to 0.6 mW/mm^2 . Using the off-chip LED as a means of power delivery to the system, our approach enables 1.2 V to be obtained at a 15.3 mW/mm^2 level, without using a charge pump. Compared to this approach, powering the microsystem through an external LED allows an increase by a factor of 25 in the power density delivered to the circuitry without suffering from major area penalties, as well as serving as an optical data transmitter.

The absorption spectrum of the 770 nm LED is measured to determine the optimal wavelength for power delivery as shown in Figure 3.3. It shows absorption

sensitivity from 620 nm to 760 nm and has the highest absorption from 720 nm to 760 nm. The LED shows a distinct shift of about 20 nm between absorption and emission peaks. Similar shifts in emission and absorption spectrum can be observed in previous works with distinct deviations from Gaussian profile with varying lattice materials [61]. The observed shift between absorption and emission spectrum is called the Stokes/Frank-Condon shift, which is well documented in optical devices [14]. This phenomenon is exploited in our design; by delivering the power to the device in a wavelength that is far away enough from its emission center-wavelength such that a commercially available external photodiode can be selected to receive the emissions from the LED while remaining less responsive to the high intensity light reflecting off the surface of the device.The photovoltaic potential generated by the LED under illumination with a monochromatic light source (i.e. 660 nm laser beam) shows logarithmic dependence on the power of the incoming light as shown in Figure 3.4, which in effect desensitizes the microsystem to changes and fluctuations in the intensity of the optical power signal.

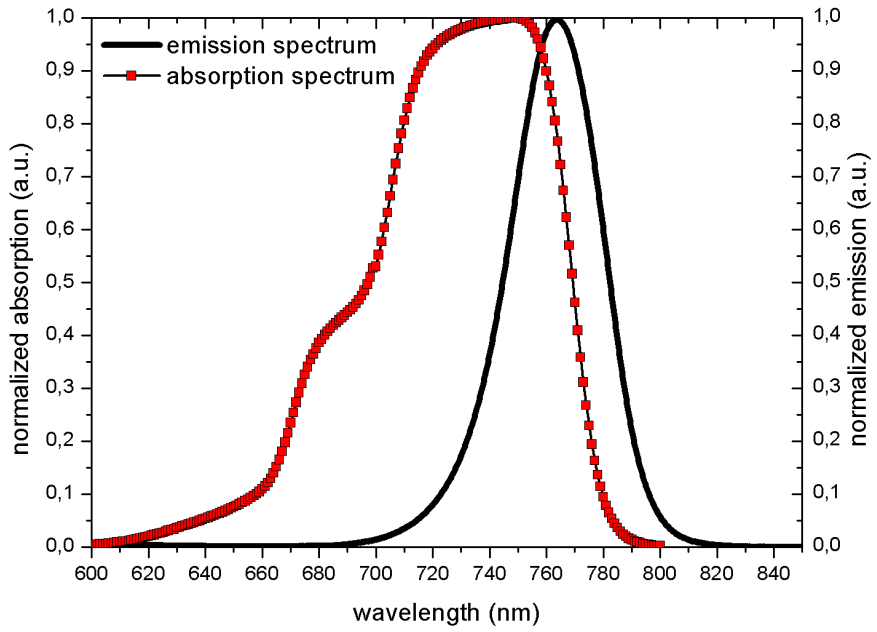

Figure 3.3. Normalized absorption and emission spectra of the 770 nm LED

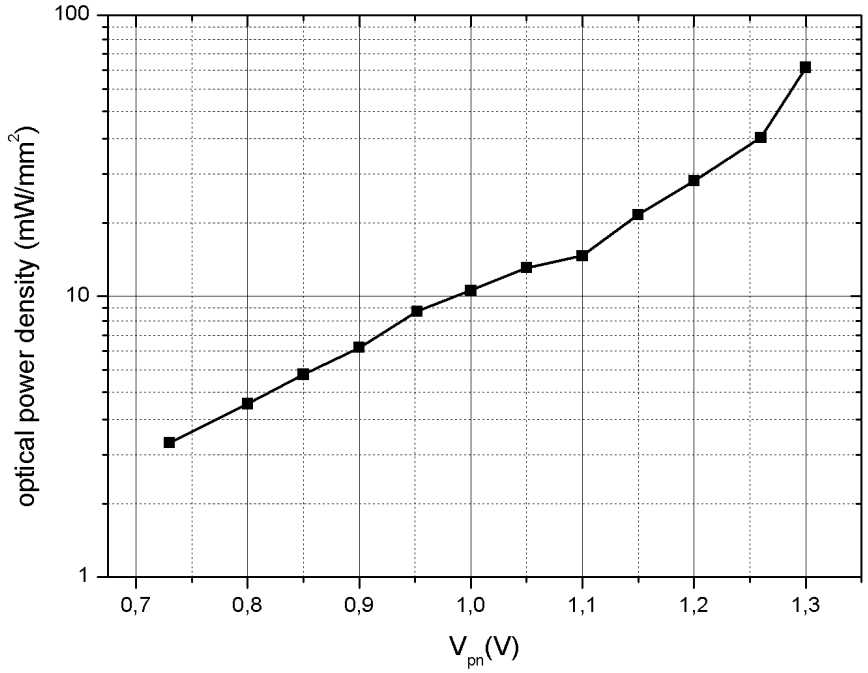

Figure 3.4. Power density of the laser vs on-chip supply rail voltage plot showing the logarithmic trend of the supply voltage with the power of the laser beam.

3.3. Transmitter System Design

The ASIC part of the system consists of supply control switch, charge pump, Schmitt trigger, pulse generation, output switch and ROM memory blocks (Figure 3.1). The details of these blocks are explained below.

3.3.1. Supply Control Switch

To avoid reliability problems with the low voltage transistors which compose the majority of the devices within the design as well as latch-up problems and stability problems with memory elements, the remaining of the circuit is isolated from the supply and put on standby, holding their states while being supplied by a smaller on-chip capacitor. The connection between the LED and the power supply of the digital blocks is realized using a single PMOS pass transistor instead of a transmission gate. A well-known problem with the inverter driven transmission gate, used as an analog

switch, is that it is prone to latch-up problems with its output exposed to the outside environment through a pad [67]. The output switch is inevitably connected to an output pad to drive the LED, therefore resistance to latchup is necessary. The close proximity of NMOS and PMOS transistors in the transmission gate and the inverter form parasitic BJTs connected in positive feedback configuration through substrate, resulting in a structure similar to silicon controlled rectifier (SCR) switches. Sudden spikes in the output pads may inject enough current into this parasitic SCR structure to switch it on. When switched on, these structures are hard to turn off due to the inherent positive feedback, which may require power to be completely turned off to exit this state. Latch-up events can become destructive where the low resistance path from the supply rail to the ground rail induces heating of the die, enhancing current flow in a positive feedback until catastrophic failure of the chip occurs due to the excessive heat generated. Removing the NMOS from the transmission gate helps avoiding one of the two parasitic BJTs in the said unwanted configuration, thereby removing the positive feedback from this configuration and diminishing the probability of a latch-up. Using a pass transistor instead of a transmission gate (Figure 3.5) comes at the cost of varying channel resistance in driving the LED, which would cause nonlinearities, but as the system is designed to operate on an on-off keying scheme, transmission of data is not sensitive to such nonlinearities as long as a minimum level of designed current is passed through the LED to enable peak detection. Assuming zero stored voltage within the inner capacitances of the microsystem, upon receiving laser illumination the LED produces a voltage at the source terminal of the PMOS pass transistor while the gate is held at ground level. As long as the source potential is greater than the threshold voltage of the low voltage pass transistor, the pass transistor turns on and the remaining portions of the system receive the power coming in from the LED. To disconnect the system from the LED, the control logic pulls the PMOS gate voltage to the supply level, which is provided by the small on-chip backup capacitor, turning it off. As long as there is voltage remaining on the backup capacitor, the pass transistor remains in cut-off, until it is switched back on by the control logic.

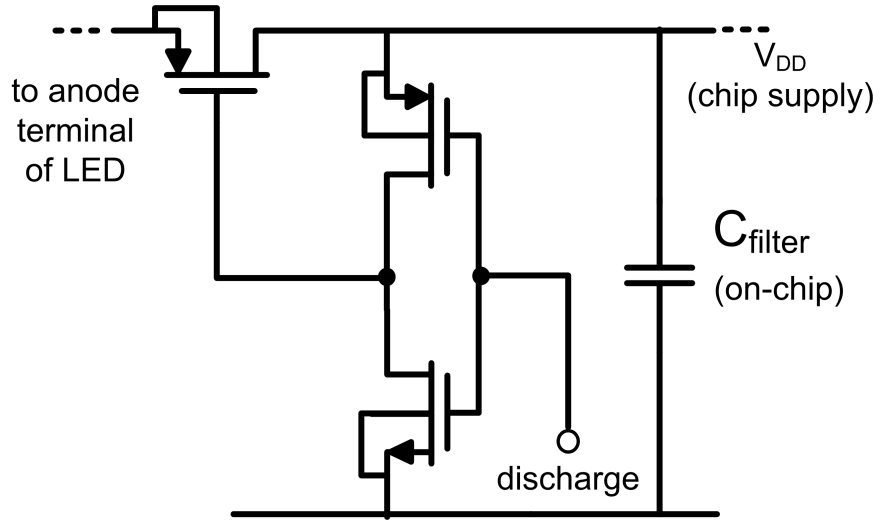

Figure 3.5. Supply control switch implemented to disconnect the LED from the chip supply during pulse transmission and reconnect it during the charge-up phase.

3.3.2. Charge Pump

Dickson charge pump efficiency suffers greatly along with the maximum output voltage available. The output voltage of a charge pump has a linear dependence on the difference between the clock signal amplitude and the turn-on voltage of the stages [59]:

$$V_{out} = V_{DD} - V_{th} + n \cdot \left[\frac{C_{pump}}{C_{pump} + C_{stray}} \cdot V_{clk} - V_{th} - \frac{I_{out}}{(C_{pump} + C_{stray}) \cdot f_{clk}} \right] \quad (3.1)$$

The amplitude of clock signal V_{clk} that has a frequency of f_{clk} is normally determined by the supply voltage V_{DD} of the system, whereas the turn-on voltage is due to the threshold voltages V_{th} of the MOSFET switches. The amount of charge delivered to following stages depends on the ratio of the pump capacitors C_{pump} to the total of the stray capacitances C_{stray} and pump capacitance at a given node. A static current load I_{load} decreases the output voltage by subtracting charge from the output capac-

itor whereas a purely capacitive load poses no such problem. As the supply voltages become comparable to threshold voltages of the MOSFETs, the output voltage of the charge pump diminishes, along with the power efficiency of the charge pump. Another important matter is that the voltage at the intermediary nodes becomes higher as the number of stages n grows, introducing body effect, raising the threshold voltage at the node and further reducing the voltage gain per stage [59]. There are common measures that can be taken to counter these shortcomings. Biasing the MOSFET switches at a gate voltage higher than their respective drain voltages by means of bootstrapping capacitors is one of them. However, this introduces a relatively complex 4-phase clocking scheme as opposed to the original 2-phase clock. Charge transfer switches based on transmission gates driven by locally generated high amplitude 2-phase clock signals is also a solution [68]. Alternatively, cross coupled dual charge pumps [68, 69], also known as latched charge pumps or voltage doublers, can be used.

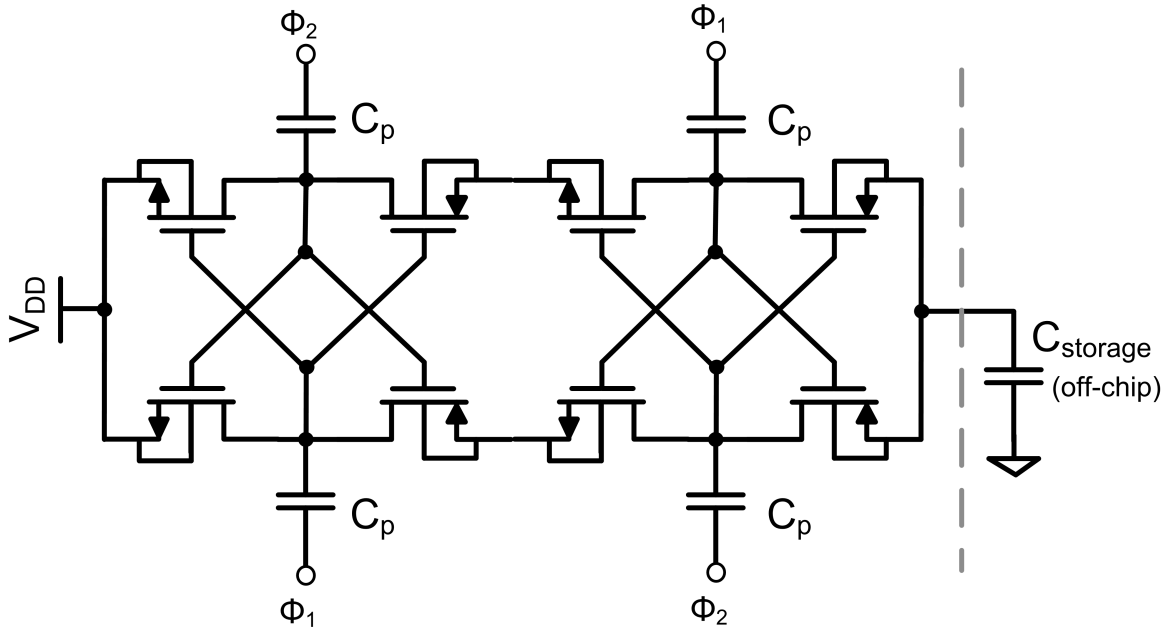

Figure 3.6. Two stage cross coupled voltage doubler, operating on two antiphase clock signals, charges up an external storage capacitor.

In the first and second generation designs, a latched charge pump with cross coupled stages is used (Figure 3.6.). Cross coupled voltage doubler schemes in 0.18 μm CMOS process have been demonstrated to be more efficient compared to classical

Dickson or bootstrapped charge pump architectures [69], and they impose lower bias stress on the oxide compared to charge transfer switch architectures [68]. A single stage of this charge pump can be viewed as two inverters cross coupled in positive feedback configuration, meaning that an intermediate voltage would be restored to either positive or negative rail of each stage. This minimizes the voltage drops per each stage that would be encountered in a Dickson charge pump while avoiding the additional bootstrap circuitry necessary to bias the gate of a stage to a voltage higher than its drain terminal along with the four phase non-overlapping clocking scheme that complicates design further and drains additional power. The cross coupled charge pump is also advantageous in terms of device reliability since the voltage drop over the gate to source drain or bulk does not exceed supply voltage levels [68], which is critical for deep submicron process implementations since overvoltage requirements are more stringent for these technology nodes. As larger buffers driving the pump capacitors create great supply noise, buffers are made deliberately weak to reduce the supply noise and ensure that the flip-flops retain their states without problem. The operation of the charge pump is halted when the stored voltage is being discharged over the LED to prevent noise, which ensures a clean optical signal to be transmitted. Triple well NMOS devices available with the process have been used to further diminish threshold voltage drops.

3.3.3. Schmitt Trigger

According to the operational requirements of the design, the charge pump must run until a set maximum point is reached, and then the storage capacitor must be discharged over the LED until the capacitor voltage reaches a minimum set point, after which the cycle repeats. This implies a need for a hysteresis window, which was implemented by a Schmitt trigger based on inverters and a pull-down network driven by the output of the Schmitt trigger (Figure 3.7.) [70]. Hysteresis in the transfer characteristic of the Schmitt trigger also provides immunity to noise in the charge pump output. To achieve low current consumption in the transition state, the transistors are chosen to be very long. Charge pump output is sampled through a voltage divider.

High resistance poly is used in the divider for its simplicity. Capacitive dividers could also have been used, but the internal node has to be discharged regularly to avoid charge accumulation, complicating the design. Although the resistive divider imposes a current load to the charge pump, it is quite small and does not lower the output voltage of the charge pump. The Schmitt trigger output acts as a control signal, initiating charge-up and transmission cycles. The amount of optical energy available to the microsystem determines the time it takes to charge up the storage capacitor, therefore the design is self-timed without a need for a global clock signal.

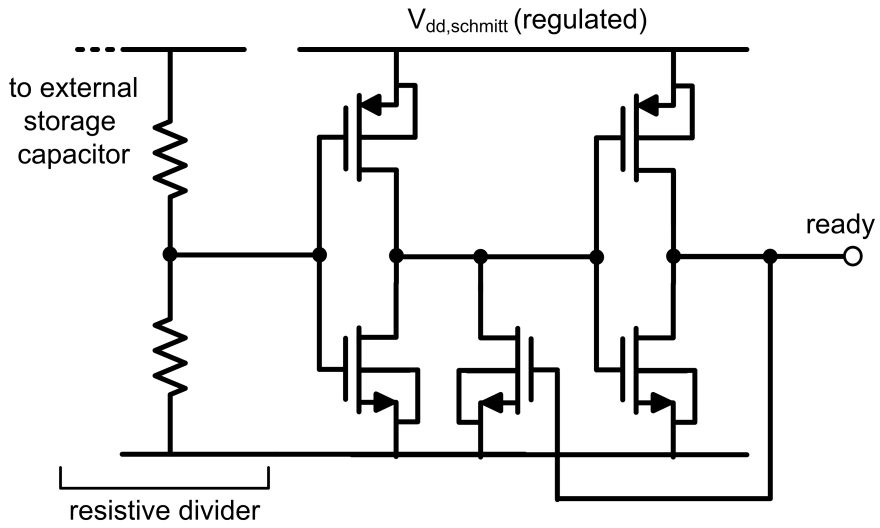

Figure 3.7. Schmitt trigger circuit used in this design features long transistors to minimize current consumption during ramp-up of the charge pump output voltage.

3.3.4. Transmitter

To keep the necessary circuitry simple and compact, the stored charge is discharged over the LED in single and double pulses to represent logic 0 and 1 values, transmitting a single bit per every charge-up cycle. The double pulses transmitted in quick succession require a small state machine, driven by a slow ring oscillator and a counter (Figure 3.8). The charge pump is restarted again in between the two pulses in transmitting a double pulse to accumulate some more charge. The switch that forms the bridge between the external LED and the charge pump is required to withstand

voltage levels greater than the recommended supply voltage for the standard 0.18 μm transistors, which is limited to 1.8 V. To avoid breakdown of the gate oxide as well as drain to source punchthrough, 3.3 V transistors available to the used technology node were employed in a pass transistor configuration. The output transistors isolate the storage capacitor and the output of the charge pump from the LED until a bit of data is to be transmitted, and are switched by the control circuitry according to the stored data to produce the aforementioned single pulse or the two pulses in quick succession.

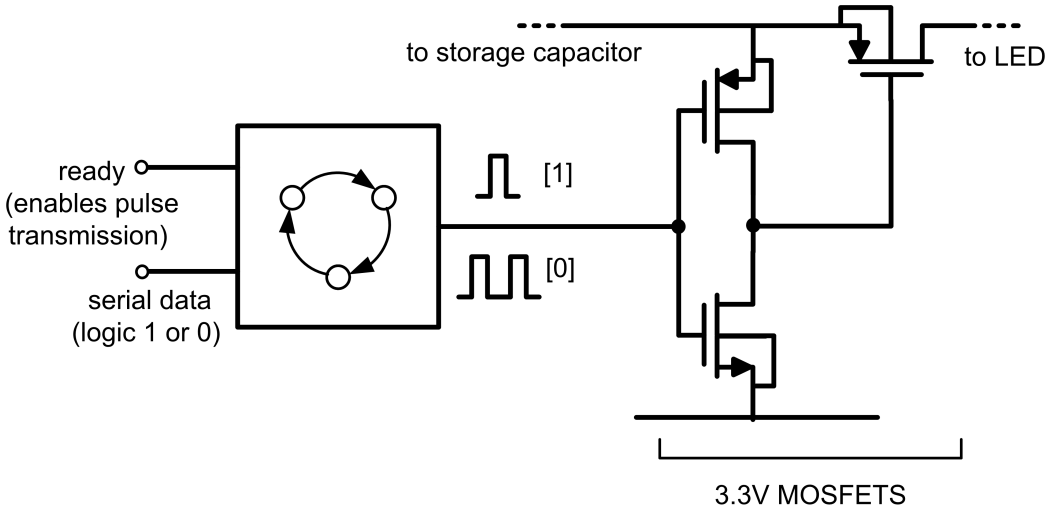

Figure 3.8. Representation of the pulse generation scheme used to discharge the storage capacitance across the LED, featuring a finite state machine and 3.3 V high voltage compatible transistors.

The described energy management and data transmission unit requires large MIM capacitors for use in charge pump, and its profile can be minimized by locating the remaining circuitry beneath the pump capacitors. The presented implementation fits inside a 230 μm x 210 μm area as shown in Figure 3.9. The circuitry is packed under MIM capacitors to minimize the total silicon area taken up by the design.

The micrograph of the entire microsystem is displayed in Figure 3.10, realized by hybrid integration of the ASIC die, LED die and a surface mount packaged storage capacitor. The ASIC is fabricated in UMC 0.18 μm CMOS process, with a total die

size of 1500 μm $\times$ 1500 μm. The described power management circuit takes up a small fraction of the total area, leaving ample space for various functional blocks such as sensors, interfaces, memory blocks to be integrated into the system. The storage capacitor is a 10 nF SMD capacitor with dimensions of 1000 μm $\times$ 500 μm. The bare LED die is extracted from its resin casing and has a size of 350 μm $\times$ 350 μm. Stacking the devices on top of one another yields approximately 1 mm^3 volume, meeting our miniaturization goal.

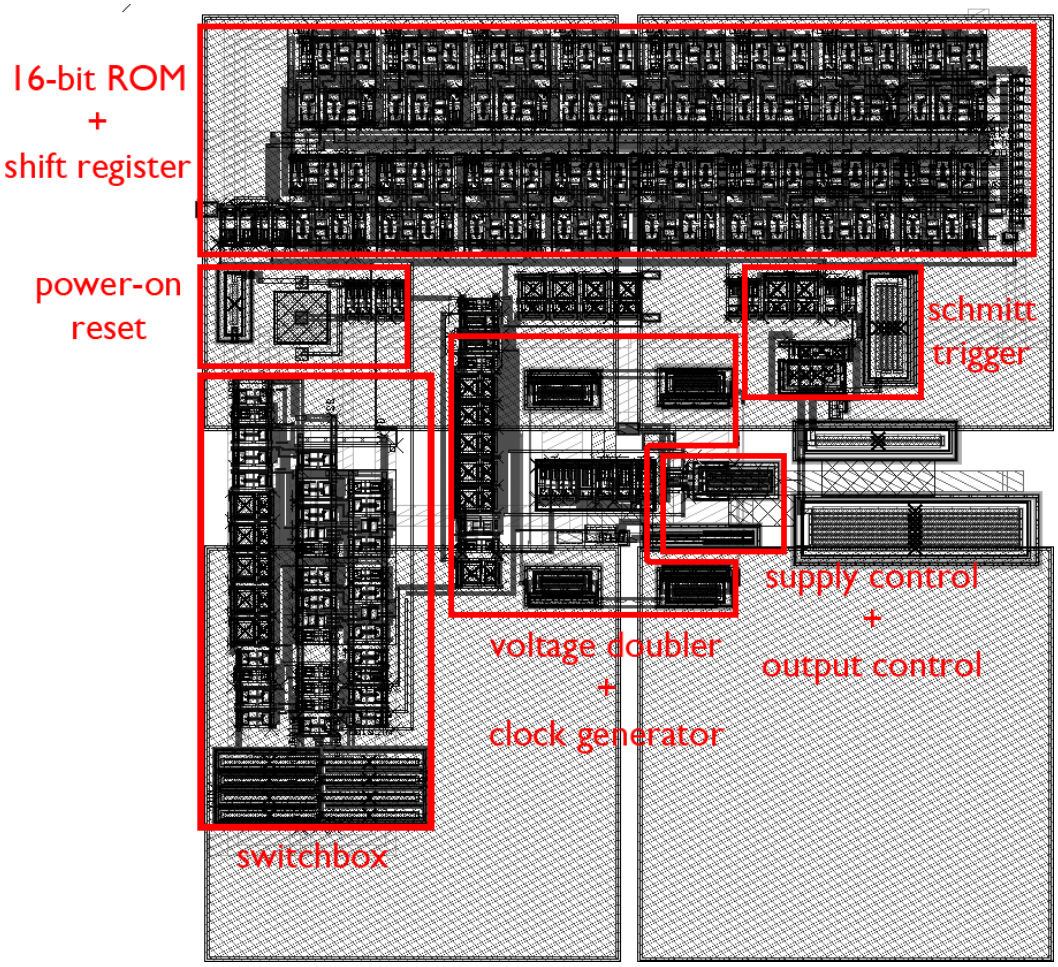

Figure 3.9. Layout of the proposed design fits into a 230 μm x 210 μm box, designed and farbicated in a 0.18 μm CMOS process.

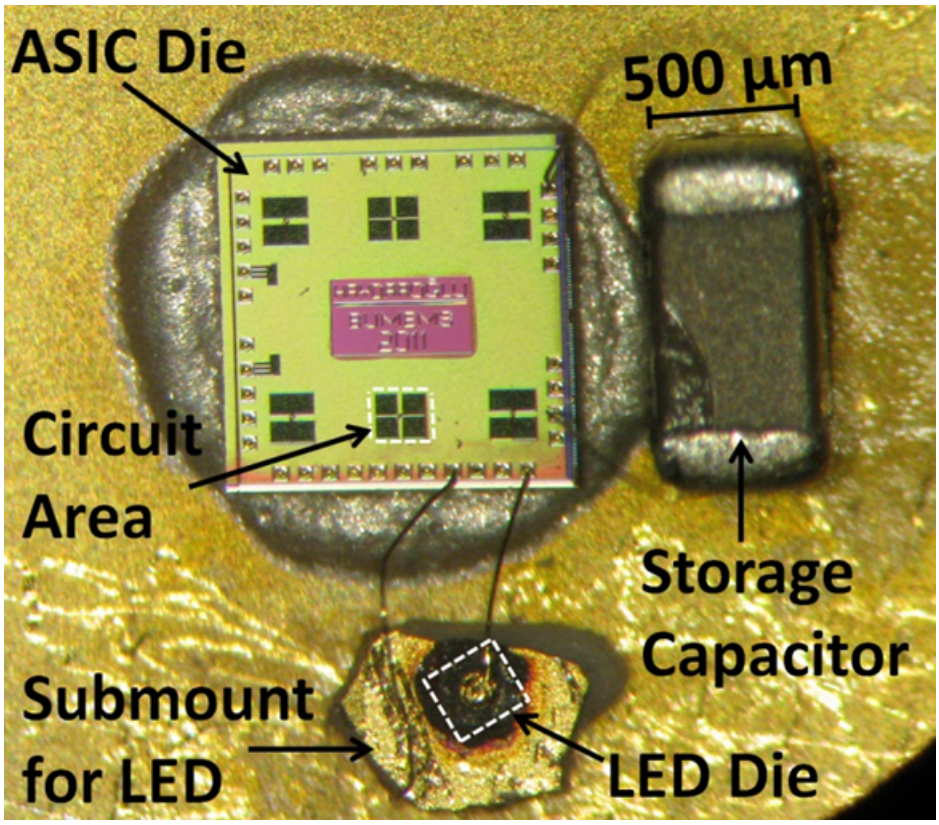

Figure 3.10. The proposed microsystem realized by wirebonding the external storage capacitor and the LED die to the ASIC die.

3.4. Time-Based Temperature Sensor Design

The second generation design features a temperature sensor, capable of operating under the voltage supplied by the LED. The temperature sensor design is based on generating a ΔV_{BE} voltage, as detailed in the previous chapter, and mapping it to a time window for high resolution quantization, leveraging the low gate delay of deep submicron CMOS technologies (Figure 3.12.).

The implemented design achieves this by charging up an initially discharged reference capacitor with a temperature compensated current source, starting a temperature compensated reference oscillator when the capacitor voltage reaches V_{BE1}, and stopping the oscillator when V_{BE2} is reached, as shown in Figure 3.13. The time interval

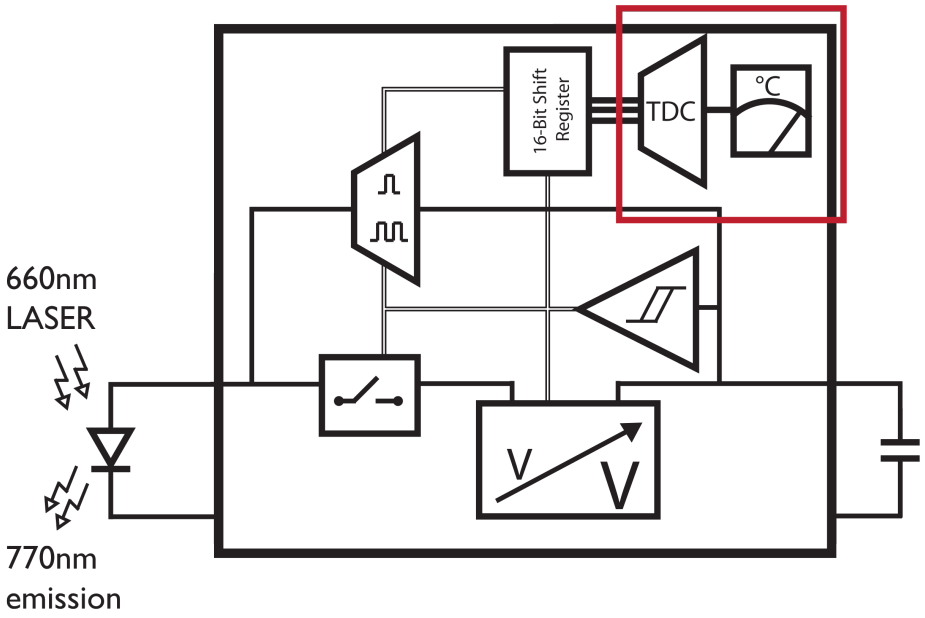

Figure 3.11. Block diagram of second generation design, featuring the time to digital converter based temperature sensor integrated into the existing energy management and transmitter design

between the two events is digitized by a counter, counting the number of cycles the reference oscillator completes within that time interval. Similar pulse position modulation techniques have been proposed for low power, minimalist conversion schemes, employing only a comparator and current source as analog components, quantizing time intervals using coarse and fine blocks, employing counter for the former and a Vernier delay line for the latter [71]. Dual comparators with chopped inputs generating a time window have also been implemented, using a simple counter for one-stage time domain quantization as opposed to a coarse-fine conversion architecture [72]. The digital output can be mapped to a V_{BE} quantity that is linear with temperature and ideally technology and process independent, as discussed in previous chapters.

The design parameters are as follows: The junction ratio is 1:8 realized with substrate diodes as opposed to substrate PNPs; V_{BE} is expected to have a temperature dependence of 200 μV/K, as displayed in Figure 3.14. A MIM layer reference capacitor of 50 pF is charged up with 40 nA, yielding a reference voltage ramp rise time of

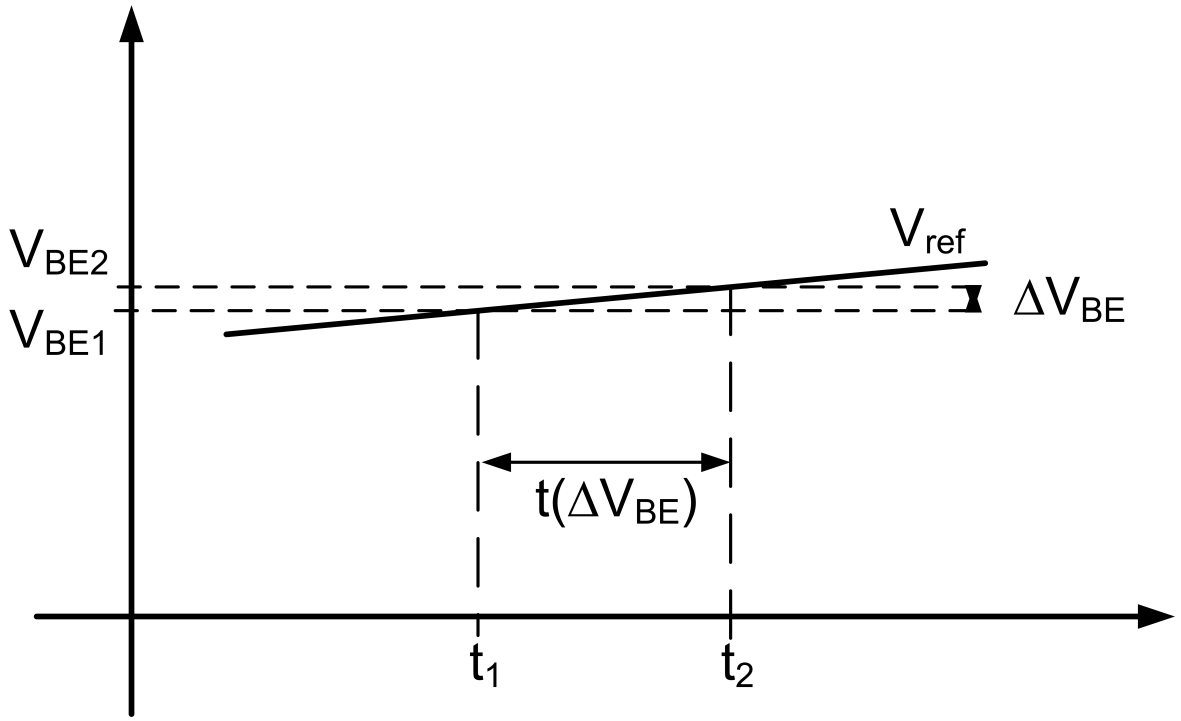

Figure 3.12. Principal of operation for the described temperature sensing scheme, mapping the small difference between two voltage domain quantities into a time interval.

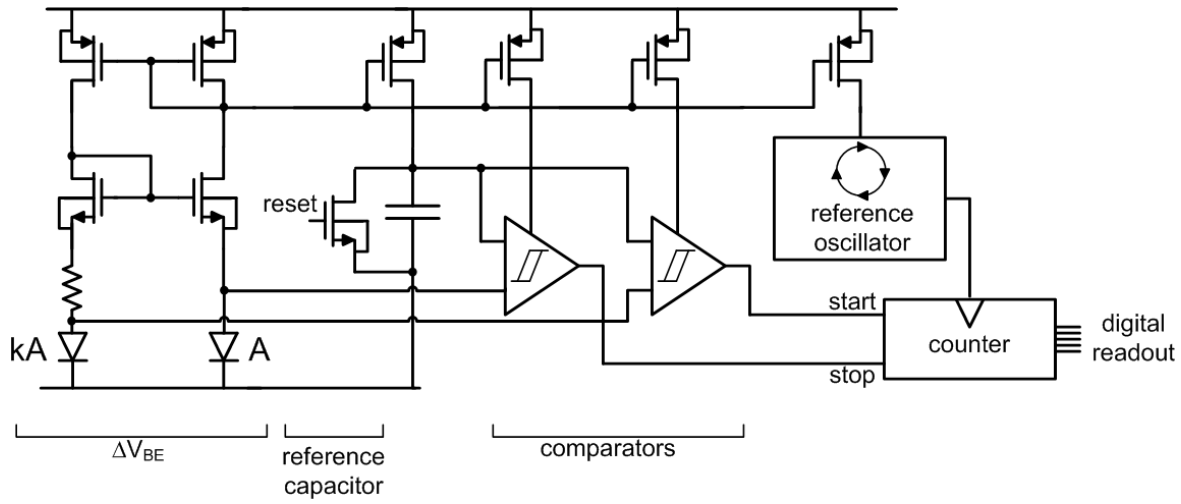

Figure 3.13. Simplified schematic of the time-domain temperature sensor.

800 V/s. Therefore, 250 ns is necessary for resolving 1 °C. A 40 MHz temperature compensated oscillator therefore yields approximately 0.1 °C resolution. The reference oscillator consists of current steering differential inverters, preferred due to their low supply noise. To avoid kickback noise from deteriorating the reference capacitor charge, two continuous time comparators were used instead of multiplexing a single latched comparator. Conversion time ranges from 70 μs to 90 μs between the range of 0 °C to 100 °C, standby current consumption is 12 μA to 55 μA, and total current consumption when oscillator is running is 80 μA to 150 μA. The temperature related time window, the oscillator frequency and the resulting digital output are displayed in Figure 3.15. Oscillator draws 70 μA to 100 μA as a result, and at 1.2 V supply voltage, consumes 5.88 nJ to 10.8 nJ at the temperature range in question. As bandgap reference consumes around 2-5 μA, continuous time comparators consume around 5-25 μA each. Total conversion energy as a result becomes 6.7 nJ to 16.2 nJ in the 0 °C to 100 °C range. The design is realized using low threshold voltage transistors in UMC triple well 0.18 μm CMOS process.

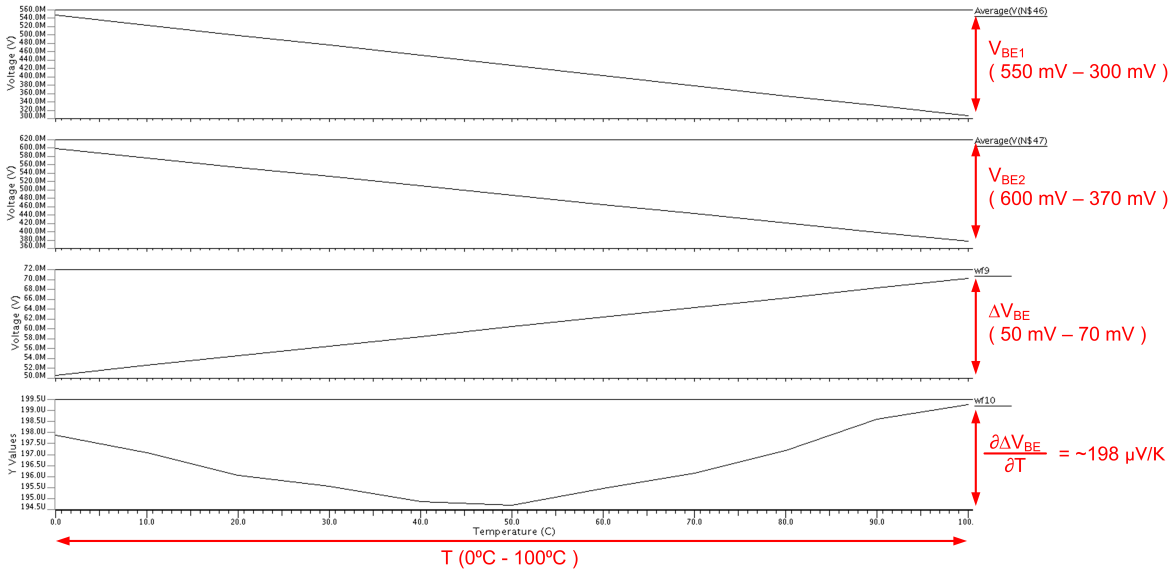

Figure 3.14. V_{BE2}, V_{BE1}, ΔV_{BE} and temperature coefficient of ΔV_{BE} for the temperature sensor, plotted from 0 °C to 100 °C

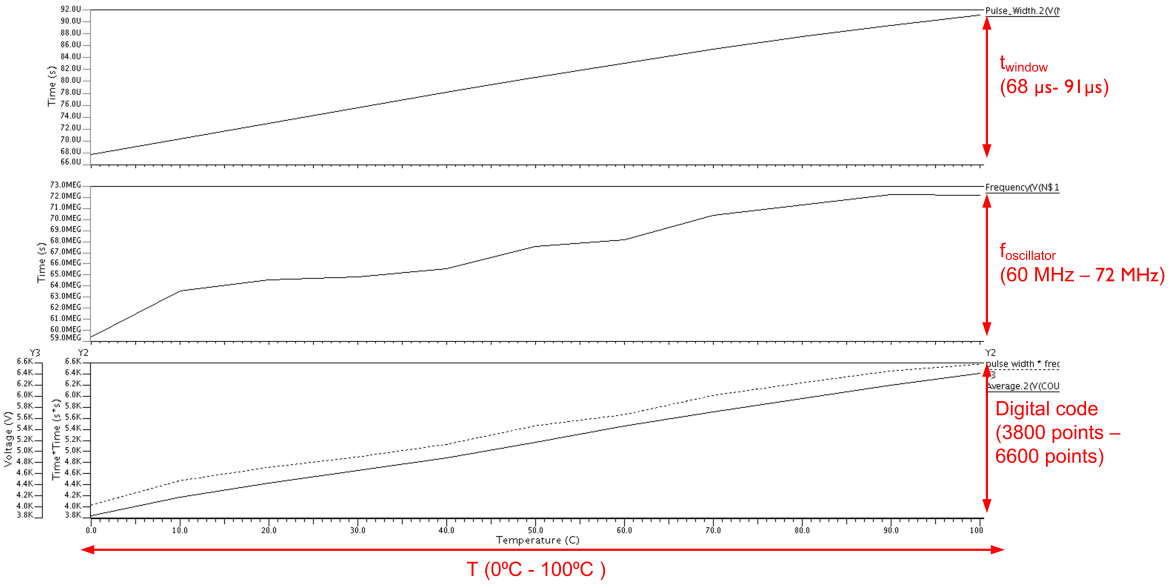

Figure 3.15. Variation of V_{BE} time interval, oscillator frequency, and digital output with respect to temperature, plotted from 0 °C to 100 °C. Multiplication of pulse width and frequency is provided as a dashed line, which tracks the digital output by a fixed offset of 200 counts.

The slow rising voltage is expected to cause the most problems in terms of starting and stopping the oscillator. Hysteresis is implemented into the comparator to avoid rapid fluctuations in comparator output near the transition voltage. Noise simulations at 300 K reveal ±120 ns 1σ deviation, which maps to a ±0.5 °C uncertainty, resulting in 1 °C sized bins. The slope of the charging current is on average 800 V/s and varies by 0.43 V/s between within a range of 100 mV, yielding approximately 11-bit linearity. Since V_{BE} values are expected to be smaller, the nonlinearity errors introduced by the reference current variations are much smaller in contrast with noise related time domain errors in the comparator. The sub-bandgap reference circuit generates a temperature compensated reference current that supplies the comparators, the reference oscillator, and a charging current for the reference capacitor, as well as providing robustness against PVT variations. The layout of the smart temperature sensor integrated with the charge pump based transmitter block is shown in Figure

3.16. In addition, a BJT based bandgap reference and analog temperature sensor was included into the design, which uses up smaller space but was not ascertained to function properly due to the existing simulation models for the BJT devices within the design kit supplied by the manufacturer.

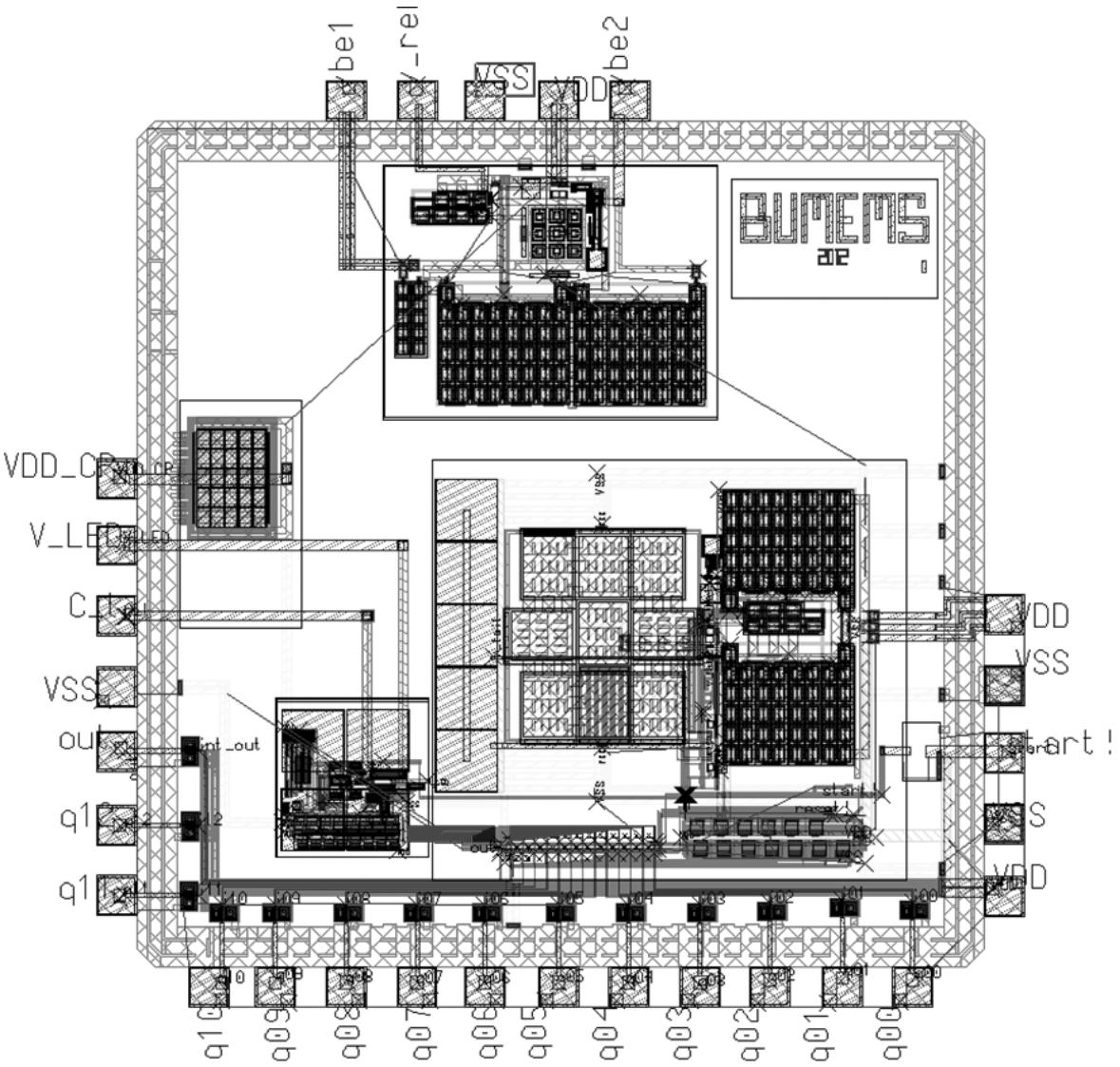

Figure 3.16. Layout of the microsystem takes 1500 μm $\times$ 1500 μm including the pad frame; the charge pump based energy management and transmitter takes up about 250 μm $\times$ 250 μm while the smart temperature sensor occupies 600 μm $\times$ 600 μm in 0.18 μm CMOS technology node.

3.5. Conclusions

The presented work defines an energy management and data transmission framework for the use of optically powered, optically communicating microsystems. Wireless delivery of optical power to the microsystem and optical data transmission can be achieved using a single LED. Optical microsystems based on standard silicon processes can be designed to harvest optical energy but transmission of optical data inevitably requires an external, dedicated optoelectronic device in the form of a LED or a laser diode. The presented approach combines the energy harvesting capabilities of the LED with its well-known and well used data transmission capabilities to obtain higher supply voltages than that could be obtained with silicon photodiodes, saving expensive on-chip area and generating higher supply voltages. A design to intermittently transmit data through the energy harvesting LED is presented to demonstrate the concept that is being proposed, which occupies small amount of area, facilitating the placement of additional functional blocks to the wireless microsystem. A field of application would involve wireless sensors and optically powered sensors, where the immediate delivery of higher voltages in comparison with silicon photodiodes can help to avoid the elevation of the supplied voltage, simplifying design, increasing efficiency and saving further on-chip area, thus potentially reducing unit cost. A low voltage, low energy smart temperature sensor is presented, aiming to solve the low voltage problem by leveraging the time domain resolution that can be achieved in deep submicron technologies. The analog parts consist of a subbandgap reference, continuous time comparator and a reference current source, and the sensor takes up 600 μm $\times$ 600 μm with the bandgap reference taking up around 500 μm $\times$ 500 μm.

4. EXPERIMENTAL RESULTS FOR FIRST and SECOND GENERATION DESIGNS

4.1. Transmitter Results

The two stage voltage doubler charge pump circuit of the ASIC was first characterized for a range of supply voltage values as shown in Figure 4.1. V_{DD} was applied electrically through the pads of the chip during this phase of tests. A design requirement to bias the LED at a peak current of approximately 1 mA was set to produce detectable photon emissions. In order to conduct 1 mA current through the LED, 1.4 V or higher voltage is necessary; thus the output of the charge pump must be at least 1.4 V to achieve the necessary levels of photon emission. This 1.4 V minimum voltage level can be produced with an input voltage level of 0.8 V that can be generated by the LED at relatively low illumination levels (below 5 mW/mm^2 power density). Below this minimum voltage, the Schmitt trigger stops functioning, halting the operation of the system. The elevated voltage at the output of the charge pump is lower than ideal due to losses caused by the deliberately weakened clock drivers, which serves to reduce the supply noise and the instantaneous current demands on the LED.

As a preliminary verification step, the LED is connected to the supply rail of the chip along with an external DC electrical supply of 1.1 V. This electrical supply powers the system and gives an opportunity to test the system. A 1 nF external capacitance is used as a storage capacitor. Acquired data reveal that the same 16-bit word is transmitted repeatedly (Figure 4.2). Double and single pulses can be identified in the figure. The received data is the same as the stored data in the ROM of the ASIC. The next step is to test the prototype as intended, with the power being delivered to the LED optically and detecting transmissions of the LED with an external photodetector. In this all optical test setup, the microsysytem has no electrical connection to the outside world, including the measurement equipment. Similar to previous setups, optical power is delivered using a 660 nm laser beam. The

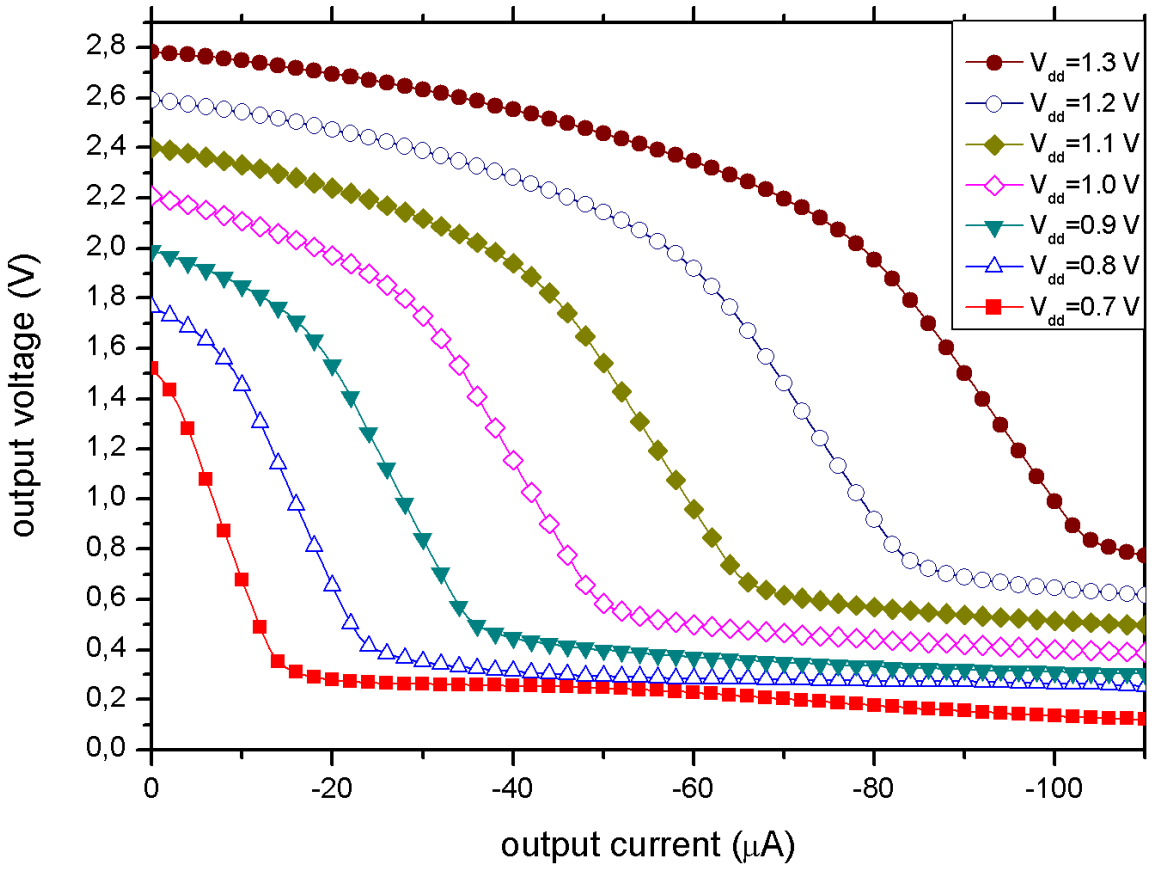

Figure 4.1. Two stage voltage doubler charge pump current-voltage characteristics under varying supply voltages

results of a successfully operating microsystem can be seen in Figure 4.3. Double and single pulses acquired by probing the pads of the LED (Figure 4.3, left column) and by the external photodetector and its circuitry (Figure 4.3, right column) prove that the microsystem works as designed. Putting an opaque but RF transparent obstacle between the LED and the photodetector ends the reception of the signals received by the photodetector amplifier, while removing the obstacle resumes the reception of the optical signals, demonstrating that the LED is transmitting data optically and not by means of stray RF signals.

From the lower row in Figure 4.3. it can be seen that the second peak detected by the photodetector amplifier is much lower in intensity compared to the first peak. A linear decline in junction bias voltage reflects an exponential drop in LED's forward

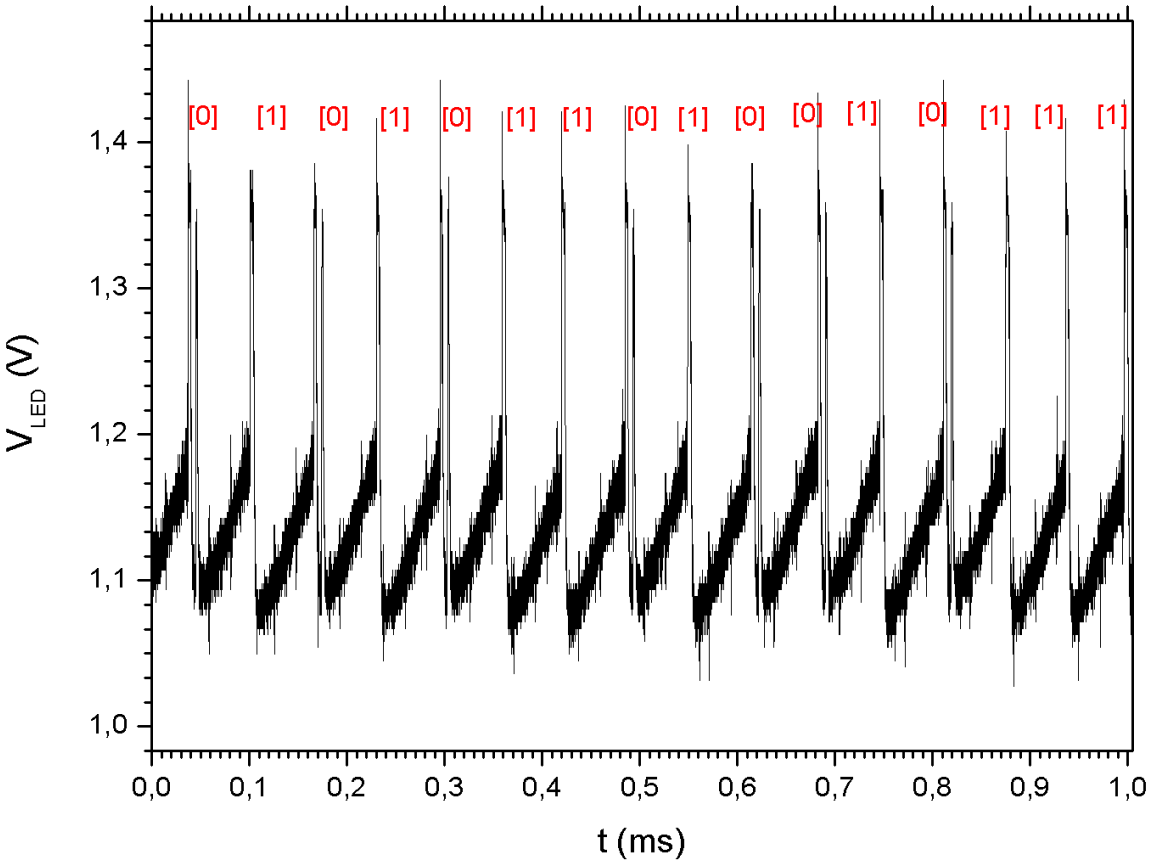

Figure 4.2. Microsystem output when connected to an external electrical supply. The double and single pulses are labeled to reflect the logical values they represent.

current, and since the number of emitted photons is proportional to the forward current passed through the LED, the generated optical signal rapidly drops in intensity as the storage capacitor is discharged. Increasing the storage capacitance makes the second peak more discernible in this scheme of data transmission, at the cost of increasing overall size. The time intervals between the transmission of consecutive bits change with varying illumination levels. This self-timed nature of the microsystem also provides a feedback to the user regarding the amount of power delivered to the LED, which may help in identifying losses in power delivery, due to transient variations in the intensity of the projected laser beam or interferences within the transmission media, letting the user know whether adequate power is supplied to the microsystem or not. In the sample measurements in Figure 4.4, the chip is able to operate at a

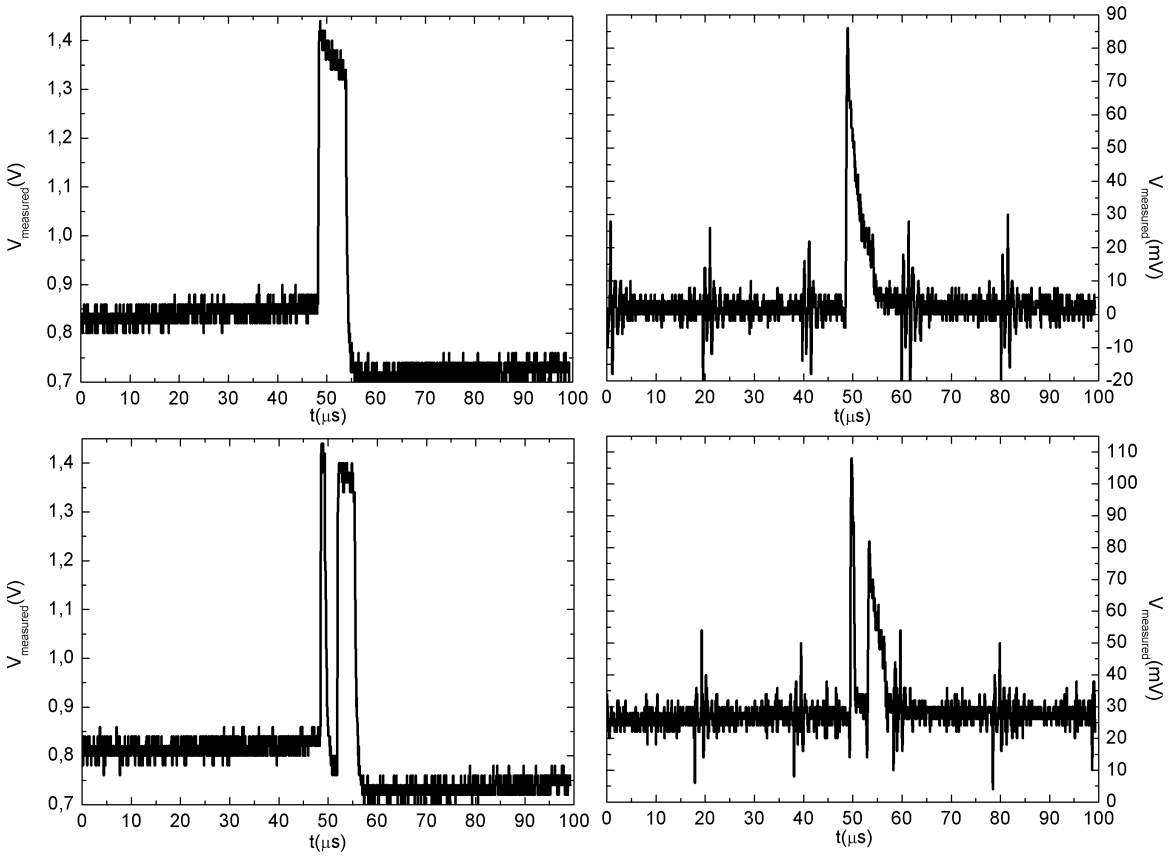

Figure 4.3. Single and double pulses detected from the positive terminal of the LED (left column) and by the remote photodetector amplifier (right column)

minimum supply voltage of 0.78 V at 4 mW/mm^2 laser power density, producing discernible single and double pulses at a data rate of 4 Kb/s. This increases to 26 Kb/s at 70 mW/mm^2 incident power. The data transmission rate follows a linear trend with respect to chip supply voltage, making it possible for the operator to deduce the actual chip supply voltage based on the rate of arrival of bits. This feature provides valuable information to the operator in case of systems that require certain voltage levels for proper operation. Analog voltage references and/or integrated sensors may perform inaccurately below a minimum supply voltage, producing unreliable results.

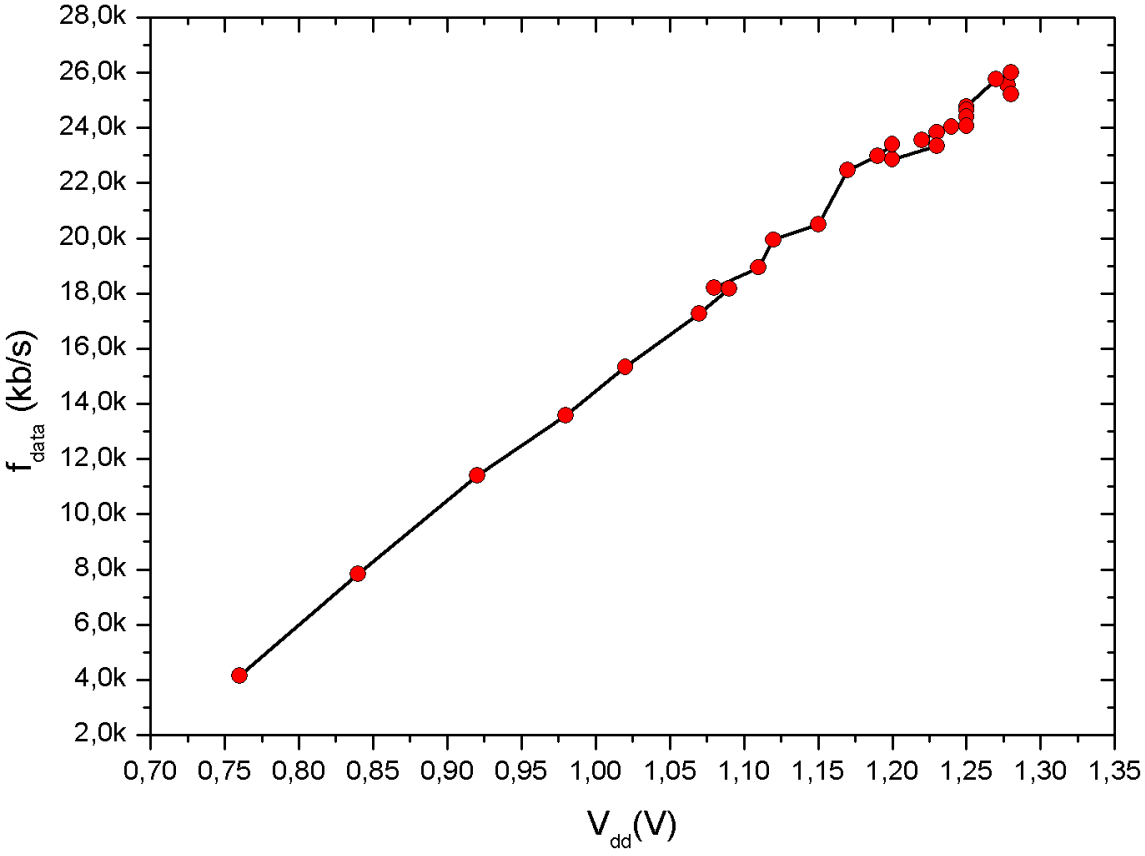

Figure 4.4. Data rate follows a linear trend with respect to chip supply.

4.2. Temperature Sensor Results

The temperature sensor included in the second generation chip was tested by thermally coupling the ceramic chip package to the hotplate (model: Thermo Scientific Super-Nuova), triggering a measurement via an external signal, and reading out the digital output in parallel. The hotplate has a resolution of 1 °C and a temperature stability of ±0.5 °C within 5 cm of the center spot of the hotplate. The supply voltage necessary for operation is supplied by benchtop DC supplies (Figure 4.5).

The functional samples outputted lower than expected effective resolution with approximately 1 point / 2.5 °C (Figure 4.6). This is attributed to ambiguities faced during the design stage where drastic variations between schematic level simulations and post-layout simulations existed. The final sizing of the oscillator transistors had

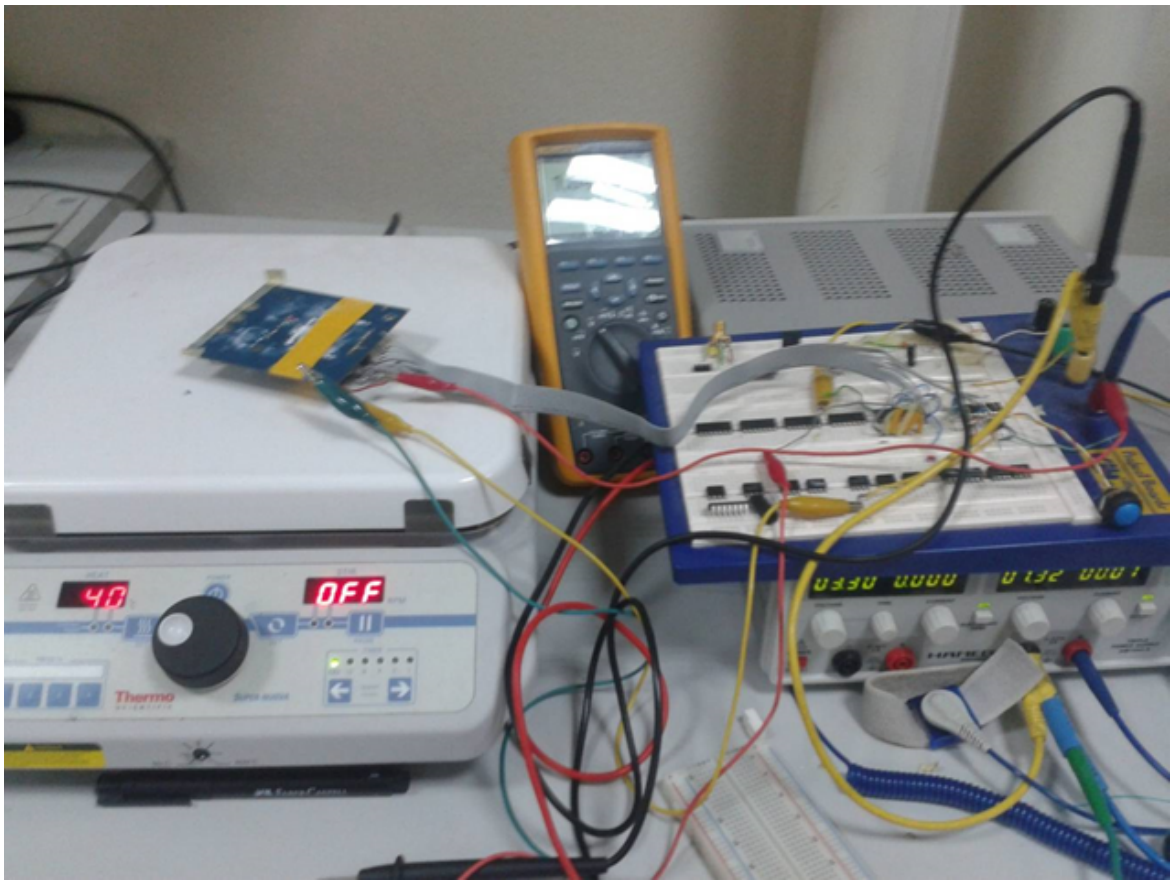

Figure 4.5. Temperature sensor test setup

to be tweaked multiple times to obtain the desired frequency of operation during the post-layout simulation stage of the design process. Coupled with the lack of Monte-Carlo simulations and corner analyses, the use of low threshold voltage transistors are assumed to have caused unforeseen drifts from original design parameters. The PNP based bandgap reference produced reasonably stable reference voltages when heated with a hot air gun. Overall, both the smart sensor and the analog output PNP based sensor were functional and performed suitably enough for general purpose temperature sensing, albeit at lower than expected performances.

4.3. Conclusions

The transmitter was determined to operate under optical illumination and transmit optical data at the same time, capable of operating under supply voltages as low

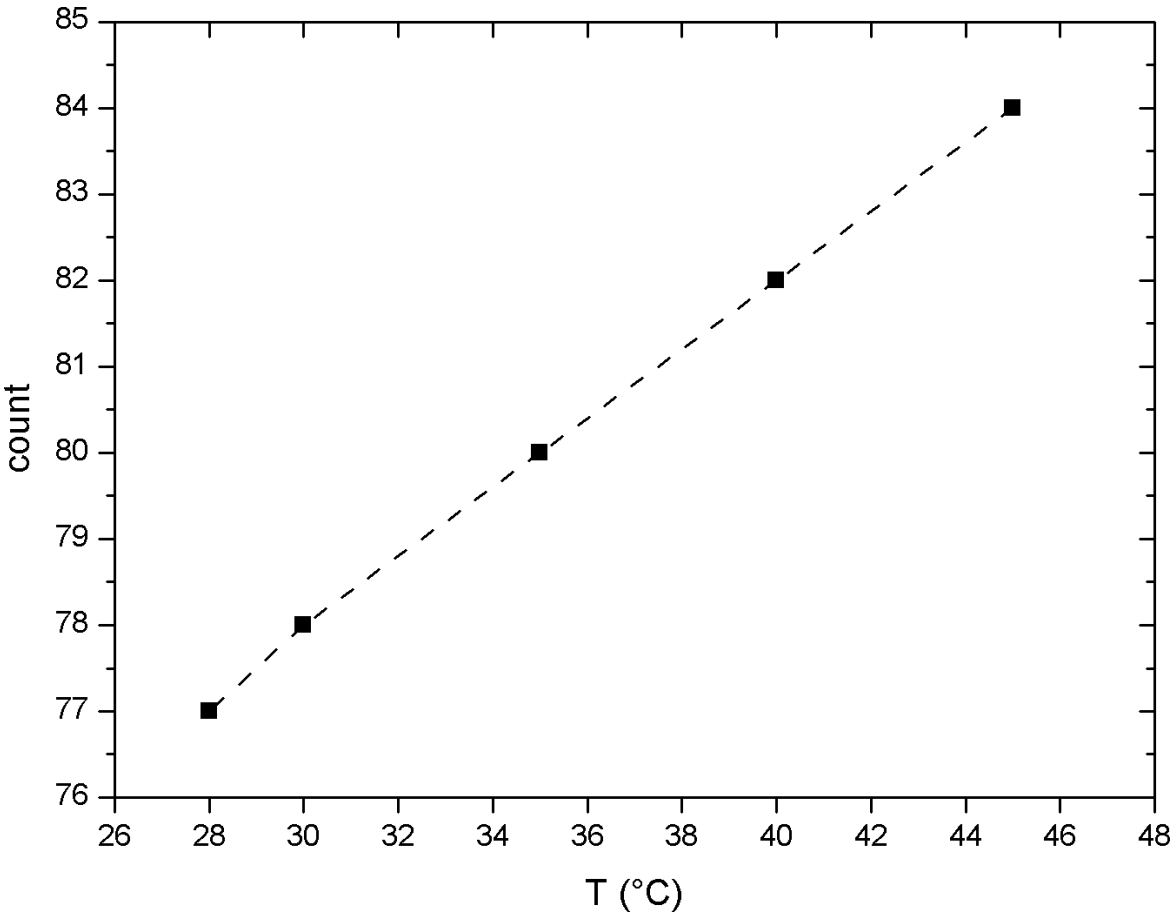

Figure 4.6. Temperature sensor readout for one of the functional samples at a supply voltage of 1.2 V

as 0.75 V, attained at 3.5 mW/mm^2, which translates to a received power of 200 μW assuming 1.5 mm laser spot diameter projected on the 0.1 mm^2 LED. The energy adaptive asynchronous transmission scheme means that data rate is a linear function of supply voltage. The smart temperature sensor is functional, but shows lower resolutions than expected from post-layout simulations with added parasitic capacitances, which is attributed to process variations.

5. THIRD GENERATION DESIGN

5.1. Introduction

The prominent sources of inefficiencies in the design covered in the previous chapter are the buffers driving relatively large on-chip capacitors at charge-pump operation frequencies, and the losses within the switch that connects the storage capacitor to the LED. The focus of this chapter is on an efficient switched capacitor boosting transmitter that allows the capacitors to be charged up directly by the current trickling from the LED to source the sensor node and delivering an elevated voltage to the LED on demand for transmission. While the buffer and discharge switch inefficiencies will remain, the buffer will be switched only at the instant of transmission, as opposed to hundreds or thousands of cycles it takes to charge up a storage capacitor in a classical charge pump implementation. The work being presented demonstrates a miniaturized smart temperature sensor that uses the same LED to scavenge energy and transmit the obtained data without needing to use a boosting power management. While the system is designed for free space optical power and data delivery, it can also be adapted for use on the tips of optical fibers integrated into biomedical catheters to make them magnetic resonance imaging (MRI) compatible. Since the LED is responsible for both harvesting energy and transmitting data, coupling a single fiber is enough, instead of having to align separate fibers for the photodiode array and transmitting LED/laser diode, which complicates fabrication and increases costs [56].

5.2. System Description

Figure 5.1 shows the overall system architecture of the design that is fabricated in a standard 0.18 μm CMOS process. The system uses an external 0.09 mm^2 770 nm wavelength AlGaAs LED for energy harvesting and optical data transmission. The temperature sensor block consisting of sub-bandgap reference generator, digitally programmable oscillator and bias generator, along with the auxiliary circuits, measures junction temperature based on V_{BE} technique and outputs the digital temperature data

after some correction processes. Stored temperature data is transmitted through the LED by using a switched capacitor boosting driver (pulser) that is pulsed with a faster, digitally adjustable oscillator. The system is capable of working at a supply voltage as low as 1.0 V, which is nearly half of the nominal supply voltage of the technology node.

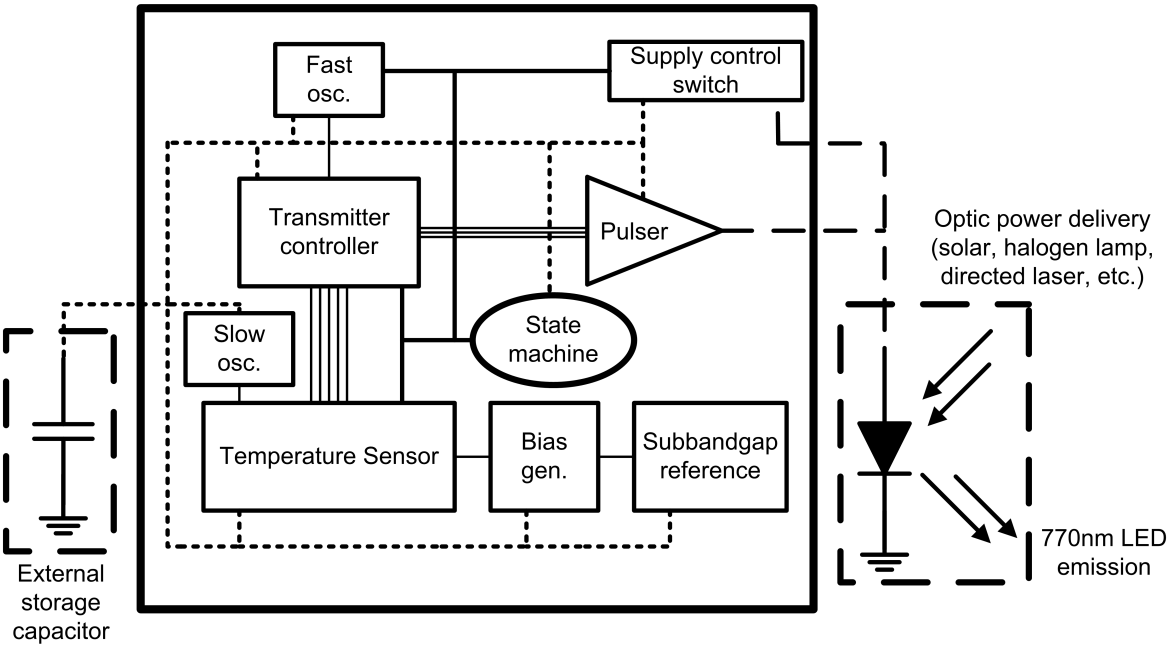

Figure 5.1. Block diagram of the third generation design

5.2.1. Switched Capacitor Boosting Transmitter

As mentioned at the beginning, a wide bandgap LED can provide enough voltage to run a submicron CMOS sensor design without resorting to voltage boosting that would inevitably reduce overall efficiency. However, the system still needs higher voltage than the harvested voltage to drive the optically excited LED into forward bias region and emit photons for data transmission. This can be seen from the DC current-voltage measurements of the LED under different lighting conditions (Figure 5.2), which are captured by using Keithley 4200 Semiconductor Parameter Analyzer. A laser with a labelled peak emission of 650 nm wavelength, which stabilizes to 680 nm as the laser heats and stays at its final temperature, is used in the measurements

to generate optical power densities from 1.3 mW/mm^2 to 20 mW/mm^2.

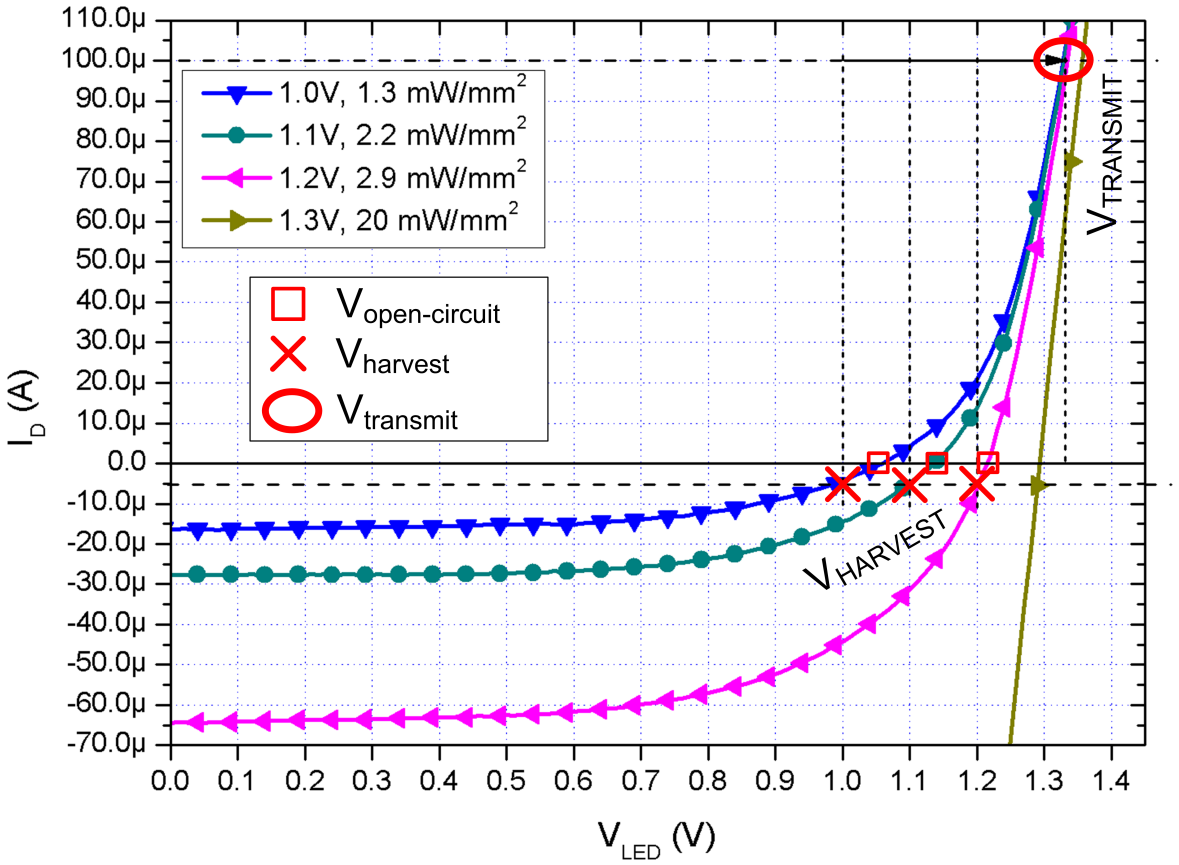

Figure 5.2. DC current-voltage measurements of the 770 nm LED under 680 nm laser illumination with different optical power densities. Harvested voltages for 5 μA current consumption are illustrated.

In Figure 5.2, three different voltage values, $V_{open-circuit}$, $V_{harvest}$ and $V_{transmit}$ and two current values, -5 μA and +100 μA, for harvesting mode and transmission mode currents respectively, are marked. If no current is extracted from the LED, its voltage would sit at its $V_{open-circuit}$ value, which is around 1.05 V for 1.3 mW/mm^2 laser optical power density. This can wake-up the IC as it is designed to extract around 5 μA current, the LED's voltage will move to $V_{harvest}$ value, which is around 1.0 V for the mentioned laser illumination and current extraction. The IC can work with this generated $V_{harvest}$ voltage. However, LED cannot generate light at this voltage. It must be forward-biased to a voltage value, which corresponds to a specific

forward current value. This specific current value is chosen so that the generated light intensity can be detected externally. The generated light intensity is proportional to the forward LED current. For instance, assuming +100 μA forward current is enough for external detection, the LED must be forward-biased to $V_{transmit}$ of 1.33 V as shown in Figure 5.2. Therefore, 1.05 V must be boosted to 1.33 V under laser illumination of 1.3 mW/mm^2. Similar cases are valid for the other illumination levels. A switched capacitor boosting technique is used in the transmitter to create the needed higher voltage for the transmit operation. During the charging phase the internal boosting capacitor is connected in parallel with the external storage capacitor so that the capacitors can be charged up directly by the current trickling from the LED. A programmable fraction of the voltage across the storage capacitor is compared to a reference voltage by a clocked comparator to determine whether enough energy is available for transmission. To transmit one pulse, the ground terminal of the boosting capacitor and the supply terminal of the storage capacitor are disconnected from their original nodes and instead connected together so that the already charged up capacitors are now in series configuration, which momentarily creates higher voltage and provides required energy to emit photons. The operation principle of the transmitter is shown in Figure 5.3.

The proposed transmitter can be implemented using inverter based circuits, using MOS and MIM capacitors in parallel as internal capacitors (Figure 5.4). During charge-up, the switch between the external capacitor and the LED is closed, and the input of the inverter is low so that the two capacitors can be charged in parallel. Supply switch disconnects the LED from the supply rail before transmit operation begins, and then a logic high pulse is sent to the input of the inverter, switching the two capacitors to series. Each pulser is triggered to transmit one pulse from a train of pulses. This design choice ensures that the charge necessary for a train of pulses is already stored so that the system will not wait for the internal capacitors to recharge when sending out a quick succession of pulses. The outputs of multiple pulsers are simply wired together to sum the output signals in current mode and feed it to the LED. Further details on the design of the pulsers can be found in Appendix A.

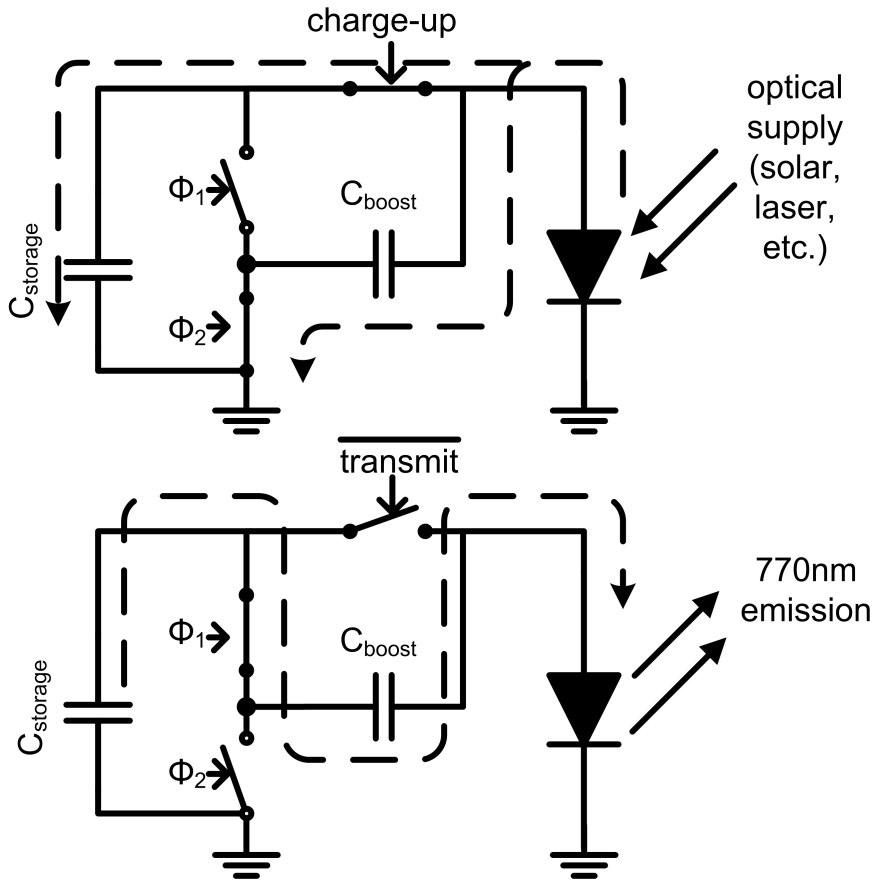

Figure 5.3. Operation principle of switched capacitor boosting transmitter

Figure 5.5 shows the overall transmitter architecture, with three clusters of three pulsers each. This allows adjustable signal strength, presenting the user with programmable options on transmission range vs. energy consumption tradeoff. A comparator flags that enough energy is available when the capacitors are charged up to a high enough voltage, which initiates a transmit cycle. In a transmit cycle, three, two or one pulse is transmitted, and then the storage capacitors are allowed to charge. These consecutive pulses constitute three different symbols; three pulses (preamble), two pulses (logic 0) and single pulse (logic 1). The time delay between the successive pulses during the transmission of a single symbol is programmable through an internal oscillator to provide flexibility for system optimization depending on the available energy in the system. The transmitter oscillator consumes less than 850 nW average power with digitally programmable frequency (0.6 to 1.5 MHz). The time delay

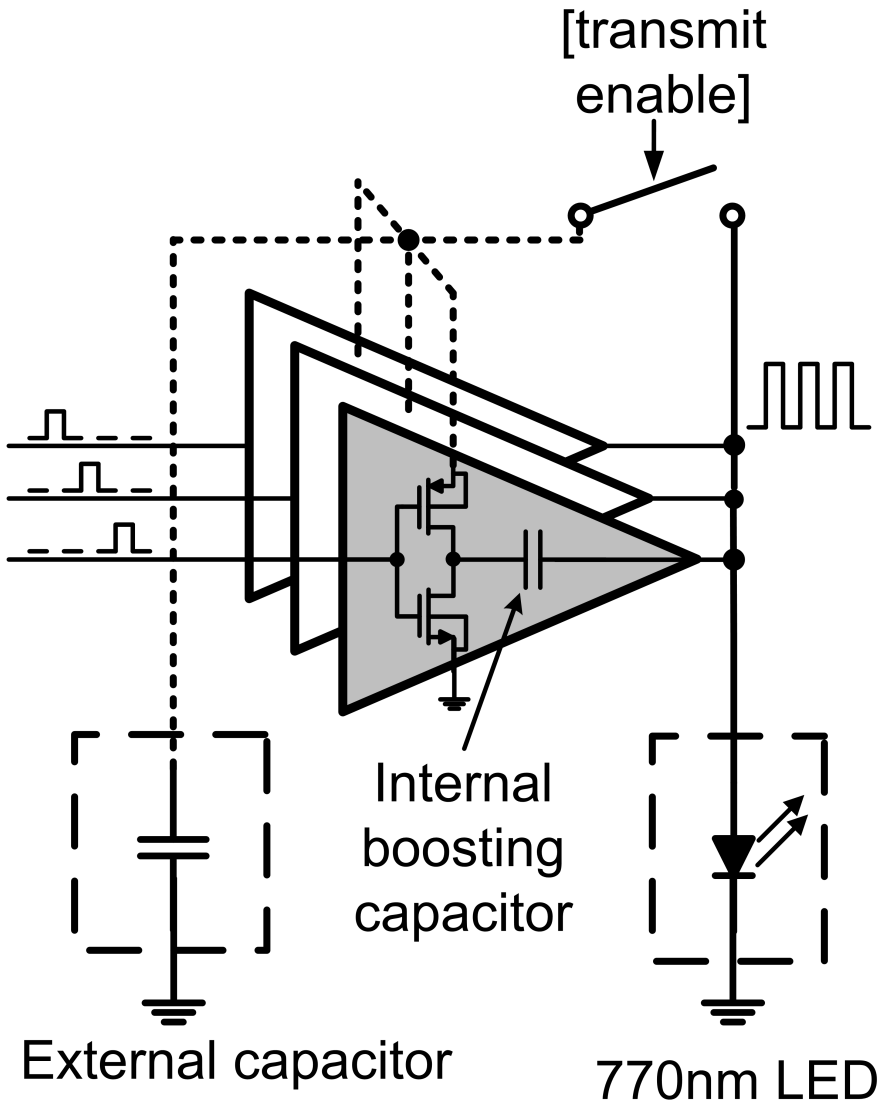

Figure 5.4. Internal view of the pulser unit

between the symbols on the other hand is energy dependent; the symbol rate is determined by the charge up time of the capacitors. At higher illumination levels where the LED current can charge up the storage and boosting capacitors quickly, the clock frequency of the clocked comparator that samples the storage capacitor voltage determines the rate of transmission, which imposes a built-in upper limit to the data rate that differentiates between two consecutive symbols. On the receiver side, which is built in house to characterize the transmitter, a positive-edge triggered countdown timer is used to differentiate between pulses within the same symbol and the pulses

of the following symbol. A sample algorithm used on the receiver side to decode the incoming pulse trains into symbols is shown in Figure 5.6.

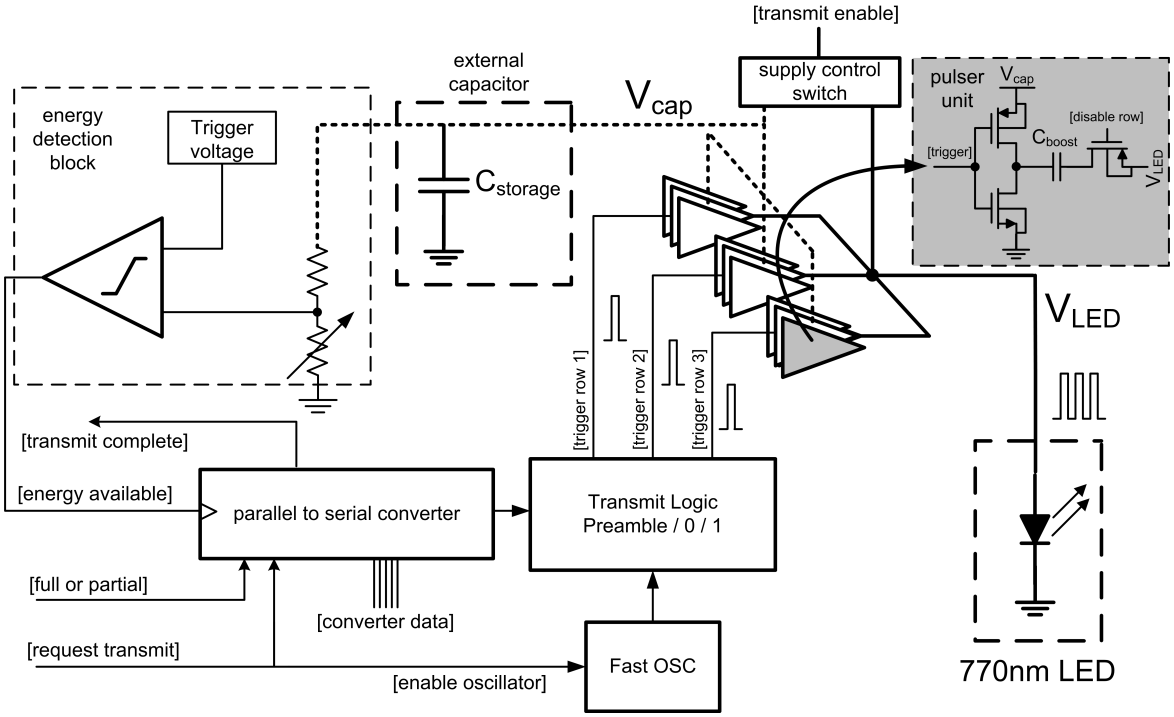

Figure 5.5. Transmitter block diagram; transmitter control circuitry, supply control switch, pulser units and digitally programmed oscillator

As the LED trickle current charges up the storage and boosting capacitors, a final voltage $V_{harvest}$ will be reached where the LED ceases to perform as a current source. At this point, the energy of the system is

$$\begin{aligned} E_{harvest} &= \frac{1}{2} \cdot C_{harvest} \cdot V_{harvest}^2 \\ C_{harvest} &= C_{storage} + C_{boost} \end{aligned} \tag{5.1}$$

When a discharge event is triggered, switching the capacitors to series configuration reduces the total capacitance to a fraction p of the original capacitance.

```
while (1)
if  posedge receiver then
   restart timer(t);
   increment(pulseCount);
end if
if  timer = 0 then
   currentSymbol=pulseCount;
   if  currentSymbol=3 then
      preambleFlag=1;
      receivedWord=currentWord;
      initalize(currentWord);
      initialize(fullFlag); initailize(partialFlag); reset(receiveIndex);
      else
      preambleFlag=0;
      currentWord[receiveIndex]=currentSymbol;
   end if
end if
if length(receivedWord)=fullLength then
   fullFlag=1;
   report(receivedWord);
   report(fullFlag);
   elseif length(receivedWord)=partialLength
   partialFlag=1;
   report(receivedWord);
   report(partiallFlag);
   else
   discard();
end if
end while
```

Figure 5.6. Sample algorithm for pulse receiver

$$p = \frac{C_{storage} \cdot C_{boost}}{(C_{storage} + C_{boost})^2} \tag{5.2}$$

As the total charge is conserved, at the instance of switching the voltage of the system becomes

$$V_{transmit} = \frac{Q_{harvest}}{p \cdot C_{harvest}} = \frac{V_{harvest}}{p} \tag{5.3}$$

While this expression gives an idea about the voltage boosting process, the current load being driven by the transmitter (the LED) exhibits exponential current-voltage characteristics, acting like a snubber diode that prevents overvoltage. The current drawn from the capacitors reduces the stored voltage, therefore the maximum voltage is limited by the current load. A more detailed treatment of the transmitter equations can be found in Appendix A.

5.2.2. Temperature Sensor

Figure 5.7. shows the architecture of the temperature sensor and current consumption of the major blocks. A BJT based V_{BE} temperature sensing method is implemented with a bias current of 750 nA at each junction. The minimum bias currents are desired to be in the order of 1 μA to minimize base resistance related voltage drops [27]. Two columns with equal bias currents are present in this scheme; a narrow junction that generates V_{BE2}, and a reference resistor in series with the wide junction generating $V_{BE1} + V_{DAC}$. The current flowing through the DAC is steered to adjust V_{DAC}, whereas the total current flowing into the wide junction is constant and is equal to the current going into the narrow junction. The steering current DAC is a segmented 14-bit design, a combination of 4 bit (MSB) thermometer coded current

steering and 10 bit (LSB) R-2R DAC. The current flowing into the reference resistor is steered by successive approximation until $V_{BE1} + V_{DAC} = V_{BE2}$, so that V_{DAC} equals ΔV_{BE} at the end of one conversion cycle.

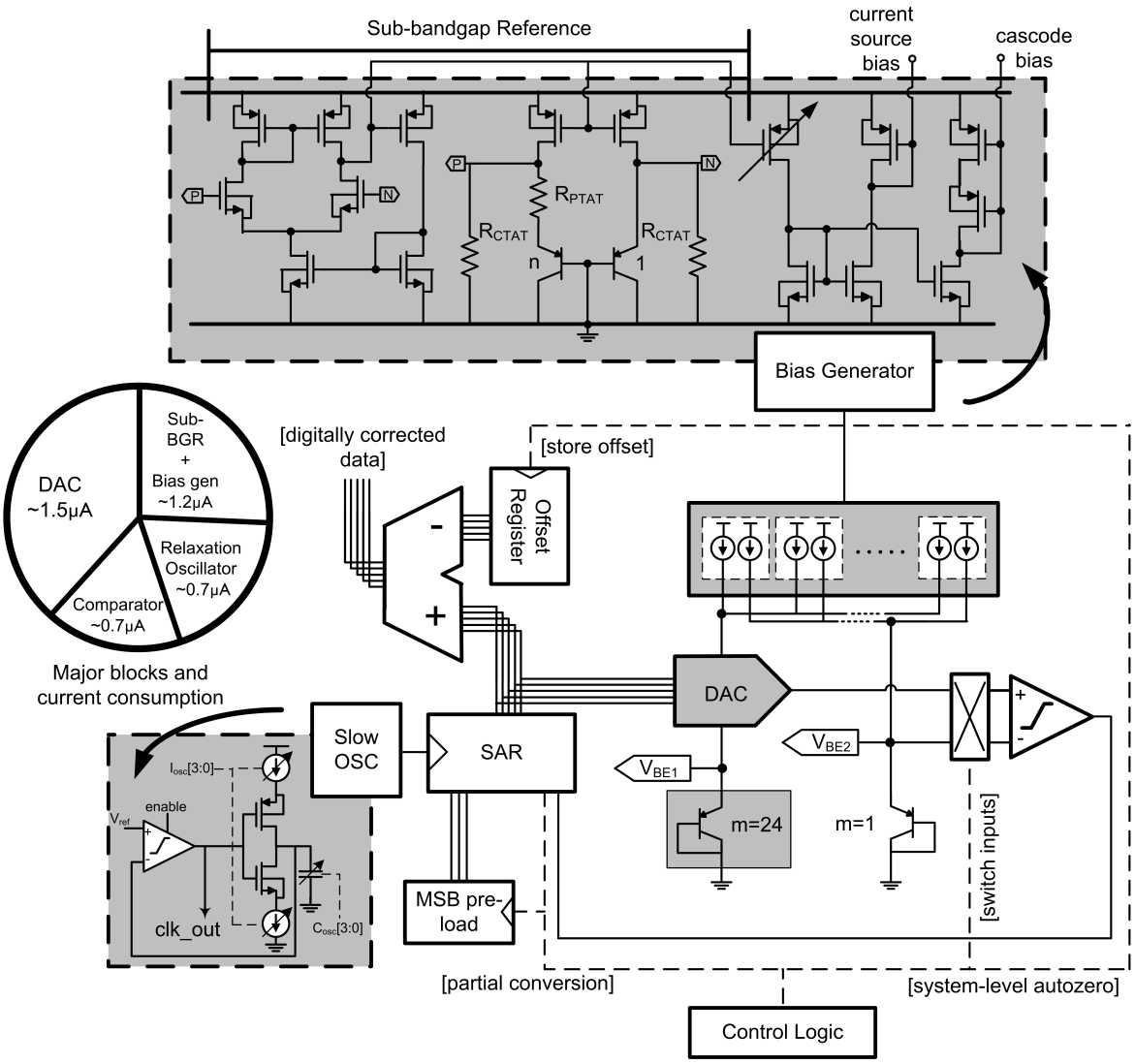

Figure 5.7. Block diagram of temperature sensor architecture

V_{DAC} is a function of the generated bias current and the value of the reference resistor; since the reference resistor and the resistors used within the sub-bandgap generator are of the same type, V_{DAC} is ideally process independent. ΔV_{BE} depends on the logarithm of the ratio between the current densities of the two p-n junctions, and should also be unaffected by small variations in the absolute bias current. Dynamic range vs. resolution trade-off is another consideration, where in a conventional ap-

proach V_{BE2} and V_{BE1} have to be quantized with respect to a fixed reference voltage, whereas in the presented approach the difference between the two voltages is measured as a multiple of the unit step generated by the DAC. As an example, for the range of 20 °C to 50 °C the junction potentials range between 500 mV to 660 mV whereas the difference between the two junction potentials ranges from 85 mV to 93 mV Measuring the two junction potentials separately with the same absolute resolution requires more bits in comparison to measuring the ΔV_{BE} directly (Figure 5.8). Circuit level implementation details and key performance parameters of the temperature sensor are discussed in Appendix B.

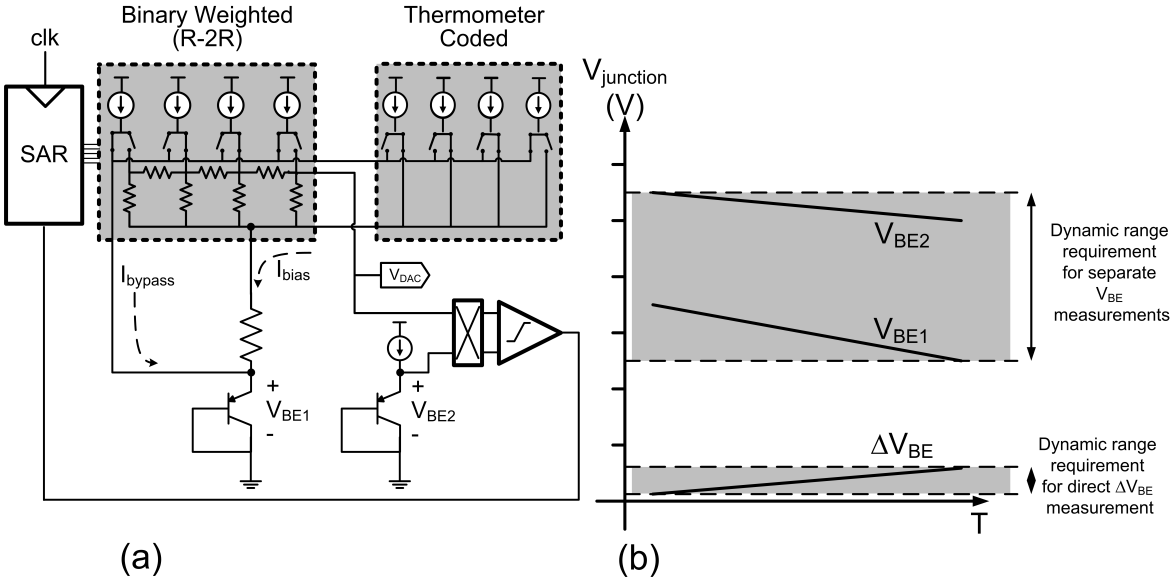

Figure 5.8. Simplified diagram of temperature sensor (a) and dynamic range requirements for direct V_{BE} measurement and separate measurement of V_{BE2} and V_{BE1} (b)

Since the ΔV_{BE} value can be comparable to or even smaller than the offset of the comparator, an offset compensation scheme is necessary. The offset is determined by measuring ΔV_{BE} with positive terminal of the comparator connected to V_{BE2} and the negative terminal connected to V_{BE1} + V_{DAC}, yielding a digital code equal to $V_{meas,1} = V_{BE1} + V_{DAC} + V_{offset}$, then swapping the terminals and measuring again, which gives $V_{meas,2} = V_{BE1} + V_{DAC}$ - V_{offset} where V_{offset} is the offset voltage of the

comparator. Subtracting the second measurement from the first gives twice the offset value, $2 \cdot V_{offset}$, dropping the LSB to approximate a divide-by-2 operation gives the offset code. The calculated offset code is stored and subtracted digitally from the following measurements, without having to swap the inputs at each measurement cycle. This process is analogous to classical auto-zero offset compensation on a system level, where the analog offset voltage is stored in a capacitor and subtracted from the subsequently sampled voltage. Another improvement on conversion energy efficiency stems from the observation that the die temperature is expected to vary slowly due to the low power operation of the sensor node; changes in ambient temperature will reflect to the die temperature with a delay at a bandwidth in the order of 10-100 Hz [27]; therefore, with a measurement rate in the order of 1-10 kS/s only a few LSBs of the 14-bit code will change between measurements and going through the conversion steps for the MSBs will be unnecessary. In order to reduce the number of conversion steps and increase the energy efficiency of the system, a modified SAR algorithm similar to the on in [73] is employed in this design. After one full measurement is made, only 7 LSBs (corresponding to ± 1.6 °C change) are re-measured for 15 consecutive cycles. If a partial measurement code overflows 7 LSB range, the process will be reset and a full measurement will be made in the next cycle (Figure 5.9). An algorithmic description of the modified SAR algorithm is provided in Figure 5.10. Each full measurement refreshes the stored offset as well, cancelling out temperature and aging related offsets as well as very low frequency noise components. A slow, programmable oscillator provides the clock for the converter and the assisting digital circuitry that has a frequency range of 30 to 150 kHz and consumes 800 nW. By varying the frequency of the clock, energy consumption can be reduced at the cost of slower conversion rate. The circuitry in the sensor node consumes less than 3 μW from 1.0 V supply, and 6 μW from the nominal 1.2 V supply during continuous operation, except for the LED driver during transmission operation where a few milliwatts is expended within a microsecond.

The third generation design was fabricated in UMC 0.18 μm triple well CMOS process, as in the previous designs. About half the silicon real estate is taken up by the transmitter; optimizing the transmitted pulse energy versus the area taken up by

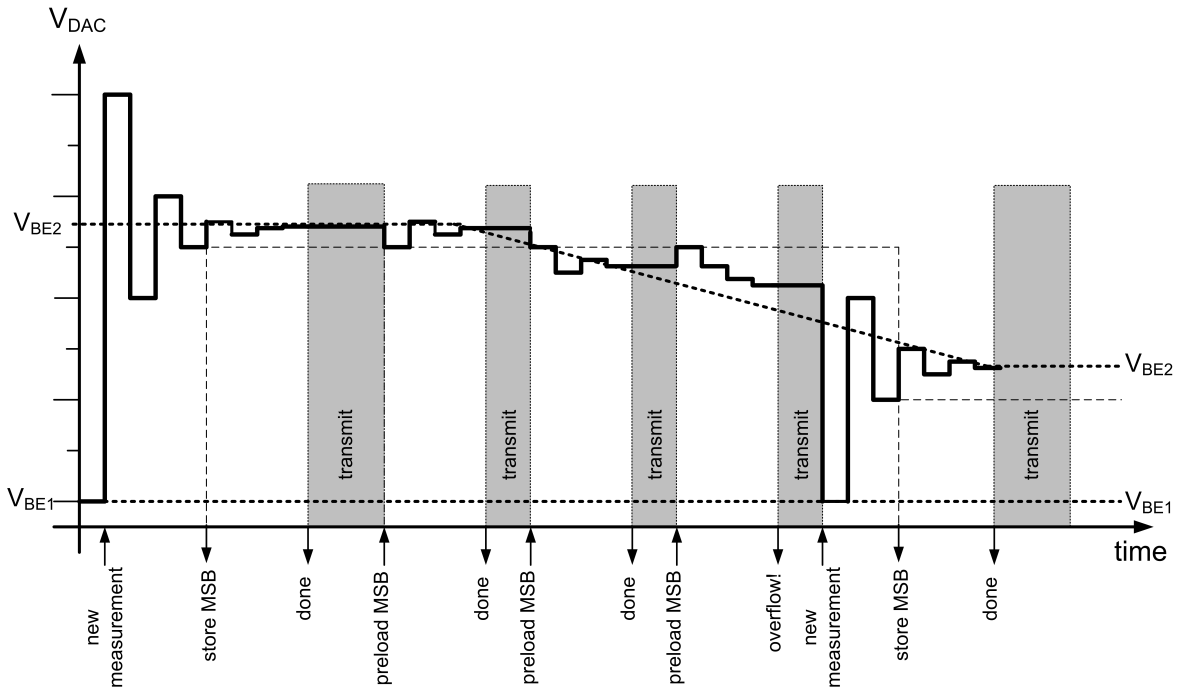

Figure 5.9. The execution of the modified SAR algorithm for full and partial measurements

the necessary physical implementation has to be optimized if additional features are to be integrated into the design. The design fits into a die of 1500 μm $\times$ 1500 μm, with major building blocks highlighted in the micrograph in Figure 5.11.

5.3. Conclusions

The improved LED transmitter removes the intermediary voltage boosting stage to reduce the efficiency loss. The classical charge pump that operates for hundreds to thousands of cycles is replaced with a switched capacitor design that instantaneously boosts the harvested voltage for transmission. The transmitter can recharge its capacitors dirctly from the harvested LED current without needing an intermediary stage, which increases efficiency. The temperature sensor presented in this chapter measures the ΔV_{BE} quantity to save time, employs digital offset correction that also corrects for temperature and aging related drift, and a partial measurement update algorithm that cuts down on the time needed to digitize a slow changing analog signal, improving

```
if reset then
  fullFlag=1;
end if
if fullFlag=1 then
  startIndex=0; //start from MSB for full conversion
  reg = FF;
  else
  startIndex=N/2; //start from half for partial conversion
  reg[0:N/2]=MSB;
end if
for i = startIndex to N do
  reg[i]=comparatorOutput!; //SAR
end for
if fullFlag=1 then
  MSB=reg[0:N/2] //store MSB
end if
if fullFlag=0 then
  if reg[N/2:N]=F ∨ reg[N/2:N]=0 then
    fullFlag=1;
    discard();
  end if
end if
```

Figure 5.10. Modified SAR algorithm example

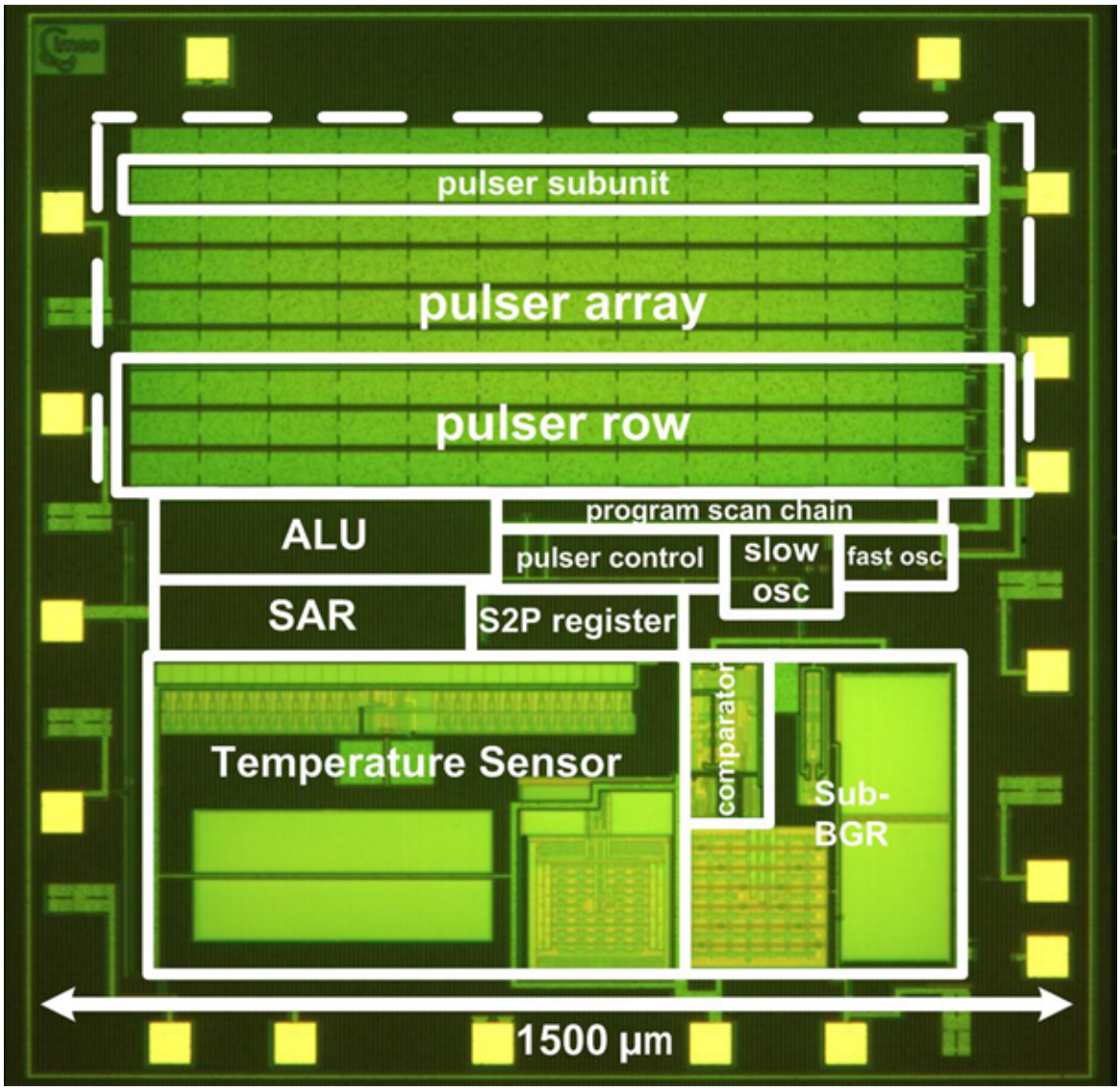

Figure 5.11. Die photo of the design, fabricated in UMC 0.18 μm triple well CMOS process

energy efficiency by reducing conversion time. The ADC and the necessary bias current for the bipolar core are shared, which also saves power by merging two sources of power use into one. Further details regarding the design of the transmitter and sensor blocks, along with energy and figure of merit calculations, can be found in Appendices A. and B., respectively.

6. EXPERIMENTAL RESULTS FOR THIRD GENERATION DESIGN

The testing procedures of the fabricated designs involve the separate characterization of the temperature sensor and the transmitter sections, along with full functionality tests where the microsystem is powered optically and data is received optically.

The characterization of the temperature sensor inside the microsystem is discussed first. The sensor section has multiple adjustable parameters to ensure correct operation and optimize for speed-power tradeoffs. The biasing current that is used within the temperature sensors can be adjusted by the operator or determined by a feedback loop within the microsystem. The resolution and sensitivity of the sensor vary with these settings. Another factor that is expected to affect the performance of the sensor is the conversion speed; slower clock rates allow more time for the DAC to settle to its final value reducing dynamic error, at the cost of increased energy per conversion. Since the DAC dissipates a constant power during operation, the faster a measurement is made the more energy efficient it effectively becomes. A combination of settings is therefore expected to exist where energy per conversion and accuracy is optimized. A primary necessity to determine the said optimal point is to have a consistent, reliable temperature control scheme. In order to verify the microsystem is capable of the designed resolution, sensitivity and accuracy, the temperature control scheme is desired to be at least an order of magnitude finer than that expected from the microsystem [27].

6.1. System Level Verification

Prior to the characterization of the temperature sensors of each fabricated device, functionality tests were conducted to determine which units worked or not. A program word was entered into the settings register (C000 0000), determining the DAC

current by self-biasing feedback mode and setting the oscillator to slowest setting. Of the 20 devices, 4 devices drew substantially large currents, implying failures in self-biasing mode. Remaining devices all drew currents within $\pm 2\sigma$ ($\pm$200 nA) from the mean (5.3 μA) (Figure 6.1). The current consumption for the intended supply voltage range was predicted reliably by the simulation models especially for the intended low voltage range, as seen in Figure 6.2. The closest model to the mean was fast-fast corner, implying lower than expected threshold voltages. In contrast, the digitally programmable current levels are systematically higher than predicted by Monte Carlo and corner simulations (Figure 6.3).

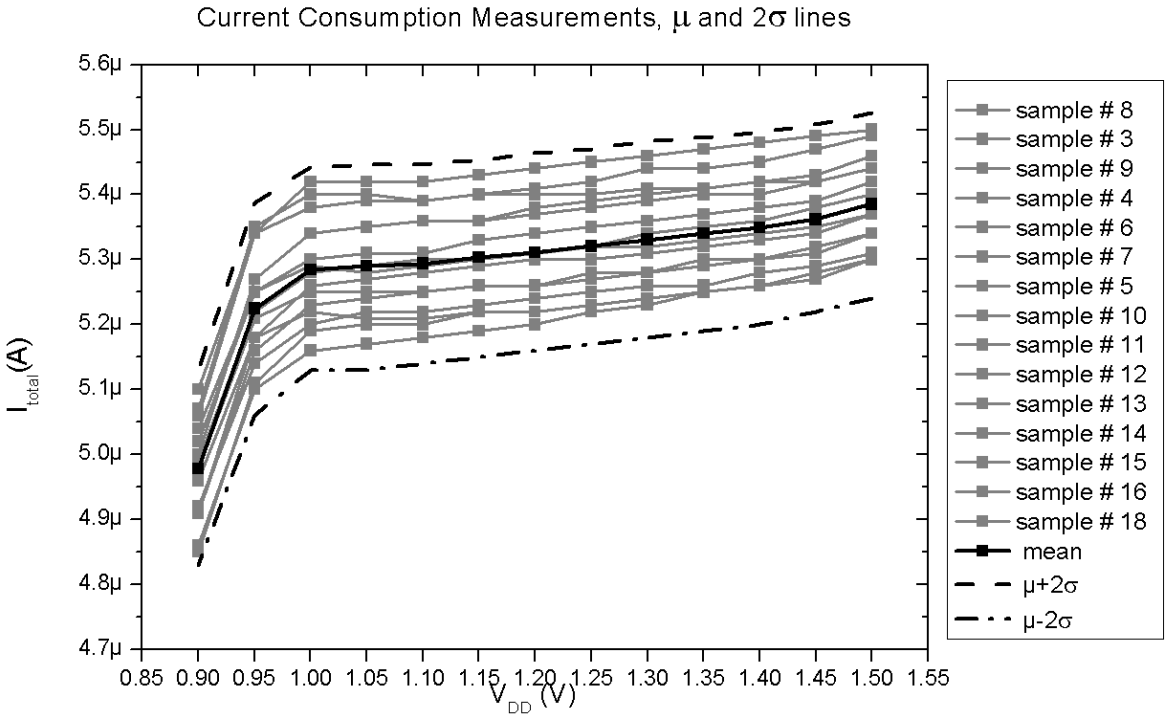

Figure 6.1. Total current consumption plots for tested and functional samples, along with mean and $\pm 2\sigma$ plots

Pulser oscillator was characterized next, as it provides a direct means of measuring the effects of the program word entered into the settings register. Program word was varied so that the loading capacitors of the oscillator are increased with each step, increasing the delay (Figure 6.4).

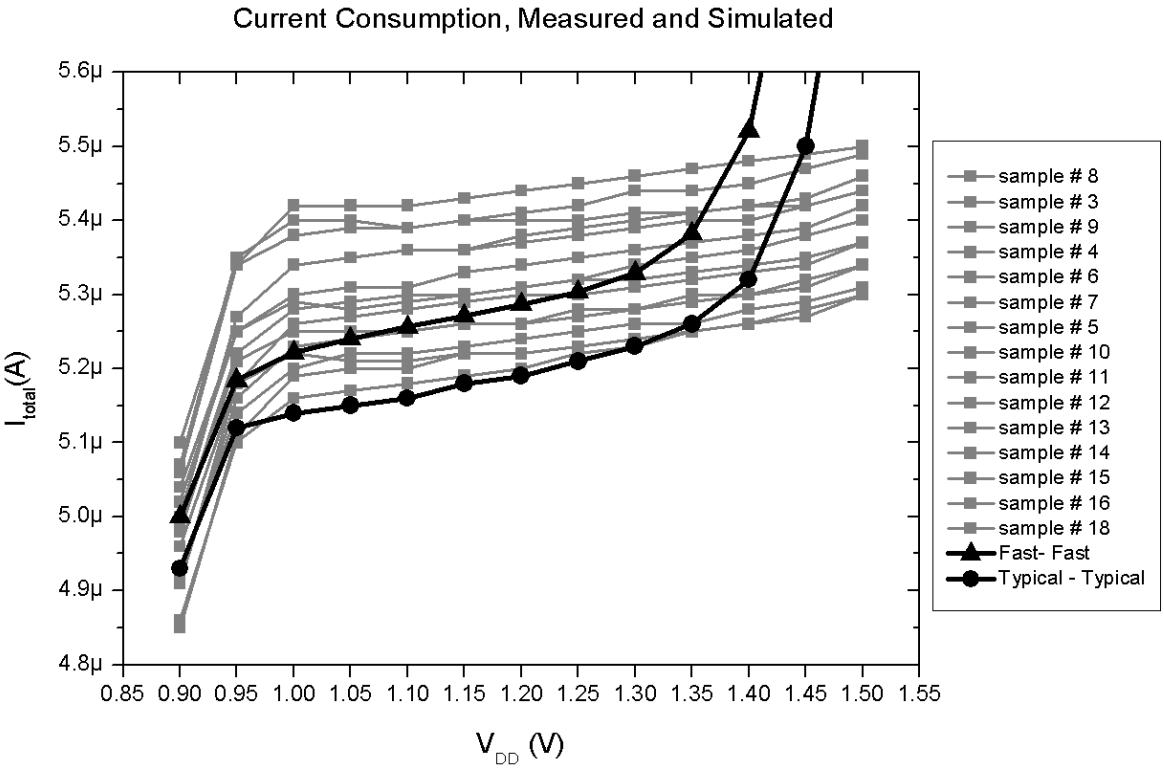

Figure 6.2. Measured current consumption vs simulated typical-typical and fast-fast corners

6.2. Transmitter Characterization

The pulser was characterized in two phases. The first phase involves the determination of the electrical output characteristics of the pulser; i.e. peak LED voltage and current levels that it can provide. Following that, optical measurements were performed to prove that the pulser is indeed capable of optical transmission. To measure the current profile through the LED during transmission, a high speed instrumentation amplifier is required, where noise, linearity and offset are not of primary importance as opposed to amplifier bandwidth. A high speed quad op-amp (Analog Devices ADA 4891-4) was used to construct a classical three op-amp instrumentation amplifier configuration, using matched resistor arrays to minimize gain errors and the offset was trimmed out by a potentiometer. A 1 Ω sense resistor is connected between the two terminals of the makeshift instrumentation amplifier to serve as a bridge between the LED and the chip and also to convert the flowing current into a voltage that can

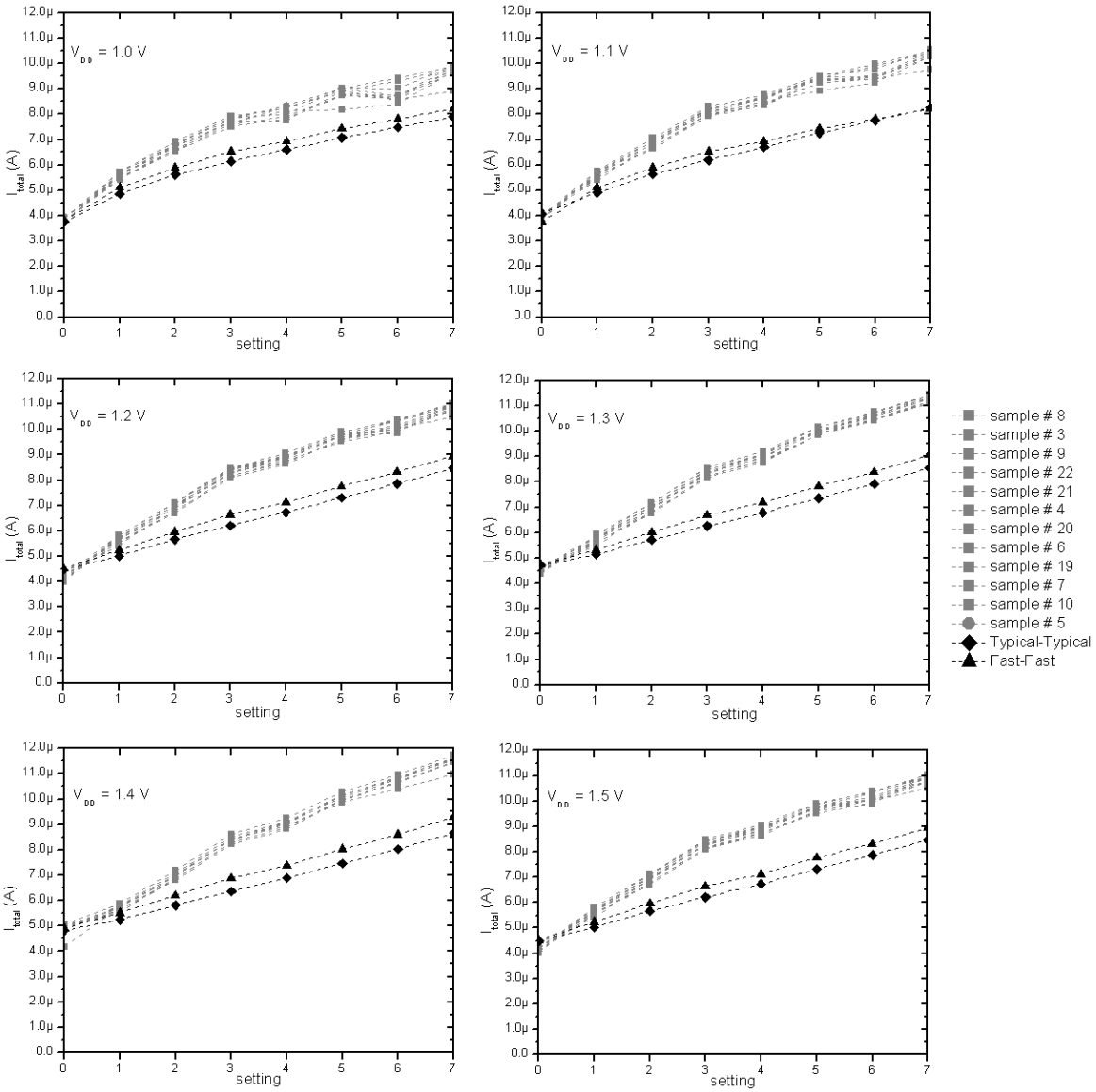

Figure 6.3. Programmable current settings and corresponding total current consumptions for supply voltages from 1.0 V to 1.5 V

be measured by a regular oscilloscope probe. The current to voltage conversion gain was calibrated with the help of an HP 34410 DMM, mapping approximately 1.38 mA to 1 V. A second probe directly measures LED voltage profile, making it possible to measure the power dissipated by the LED during transmission.

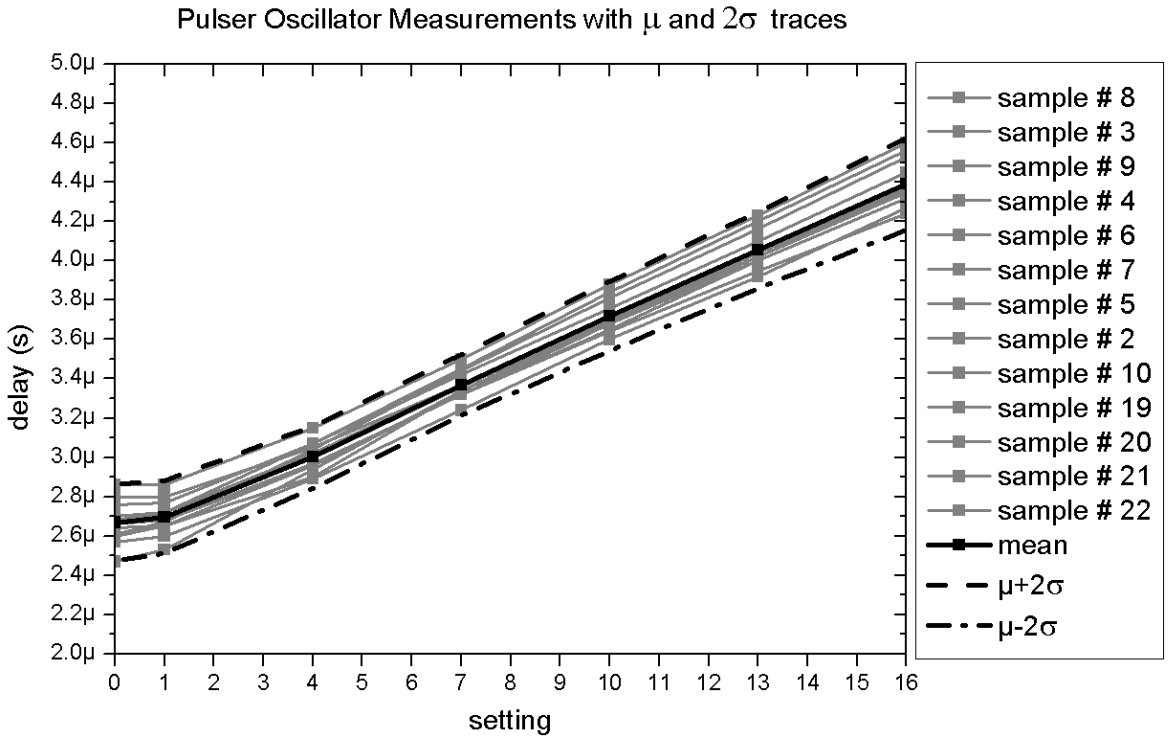

Figure 6.4. Measured delay between consecutive pulses for functional samples, along with mean and $\pm 2\sigma$ plots

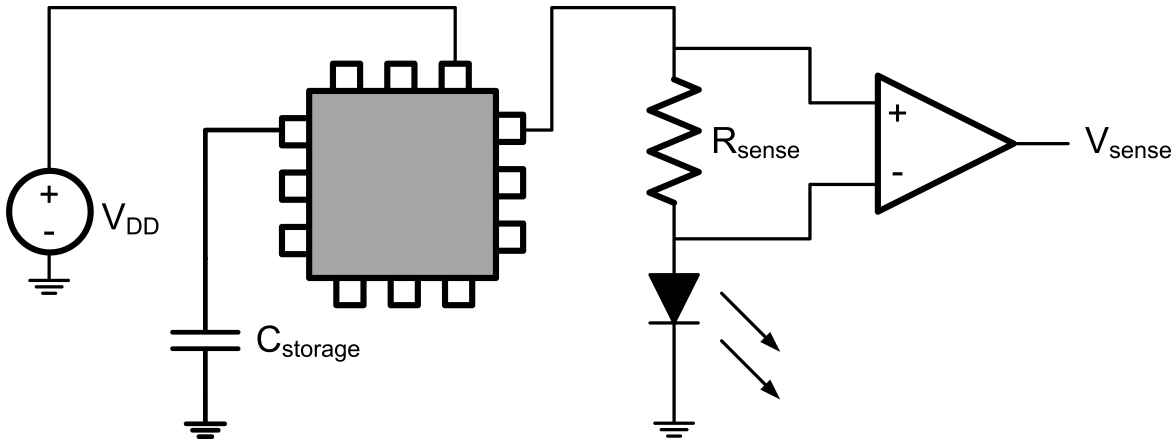

Figure 6.5. Setup for electrical characterization of the LED current during transmission

The current and voltage profiles of the LED were measured for a range of external storage capacitor values in order to determine the level of energy required to make

transmissions. As a transmission is made, both the external storage capacitor and the internal bosting capacitor spend charge, resulting in a voltage drop in each element. As the voltage on the external capacitor drops, the pulser cannot boost the LED voltage high enough to forward bias the LED as strongly, resulting in reduced current flow through the LED. It is necessary to optimize the size of the external storage capacitor, as an undersized storage capacitor will not provide enough energy for consecutive pulses in a single bit to be detectable, whereas an excessively large storage capacitor would increase the total volume of the microsystem unnecessarily. The decline in peak pulse current and voltage levels between three consecutive pulses in a preamble symbol, is displayed in Figure 6.6, showing the I-V characteristics of the LED during the transmission of a preamble symbol that is conductively captured across the LED for 4.7 nF and 100 nF as storage capacitor values. When the transmitter switches back to parallel from series, the LED voltage is expected to drop, but in order to change the LEDs junction potential the space charge has to be depleted first [74]. Current spikes flowing into the IC after the completion of the transmission of a pulse are marked as dashed circles in Figure 6.6.

As the third pulse of the preamble signal is what differentiates the preamble from logic 0 in our transmission scheme, the size of the storage capacitor must be chosen in consideration. Figure 6.7 shows the peak power decline in consecutive pulses for varying storage capacitor and supply voltage values more comprehensively. Sufficient storage capacitor size ensures that the peak power for subsequent pulses carry enough power to be discerned as separate pulses so that symbols do not get confused with one another, at the cost of slower charge-up times. The delivered energy to the LED is experimentally determined to be proportional to the pulse duration and the harvested voltage as seen in Figure 6.8. As the storage capacitor becomes much greater than the boosting capacitor, the delivered energy becomes independent of the capacitor size and predominantly dependent on illumination received by the LED; the size of the storage capacitor should be optimized for pulse to pulse consistency versus the physical dimensions of the storage capacitor. Since the storage capacitor provides energy for the whole system, the pulse duration is kept short enough to support the

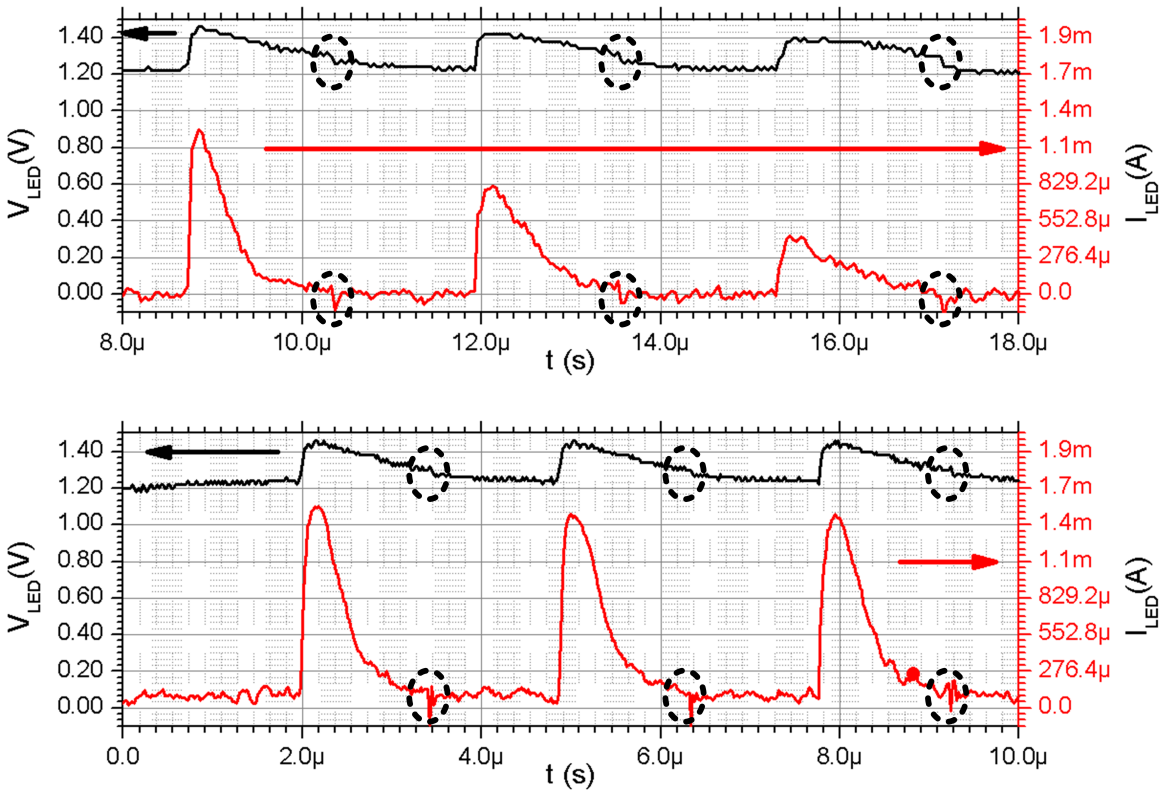

Figure 6.6. Transient LED current and voltage profiles during transmission of consecutive pulses of a preamble signal for different storage capacitor values; 4.7 nF (top) and 100 nF (bottom). The current dips below zero as LED charges up small capacitances (marked as dashed circles).

continuous operation of remaining circuitry. In case the harvested voltage goes below a certain level (which is programmable by the voltage divider described above and is set close to 1.0 V upon startup), the system enters standby mode and waits until enough energy is available for another transmit cycle. A safer approach would be to separate the storage capacitors for the LED driver and the rest of the circuitry in the system which is not implemented in this work.

The total internal boosting capacitance is approximately 4.5 nF, 1.5 nF assigned to each triple cluster of pulser. As the value of the external storage capacitor becomes an order of magnitude greater than that of the internal boosting capacitor, the energy content of the first pulse becomes a linear function of the steady state supply voltage,

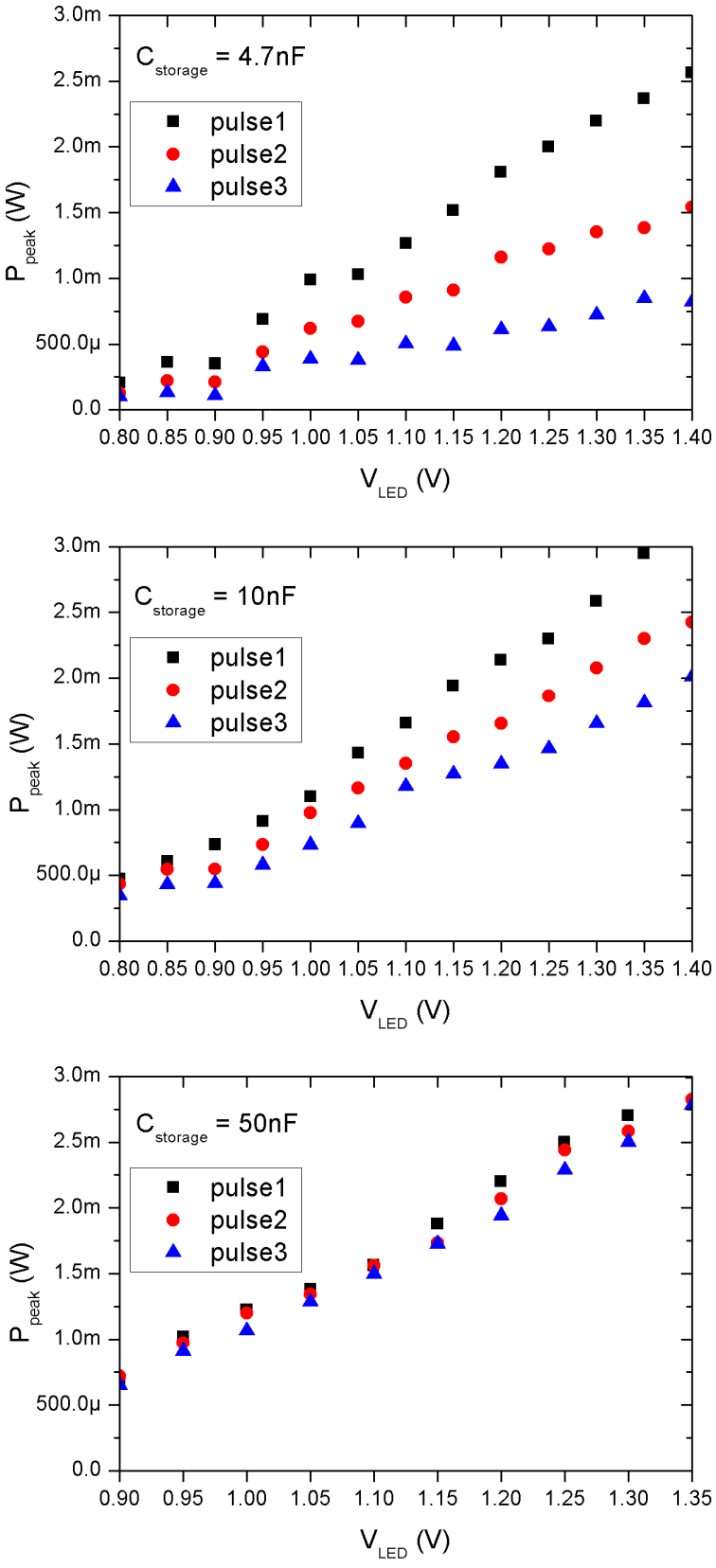

Figure 6.7. Peak pulse powers for the consecutive pulses in a preamble signal, plotted for varying storage capacitor values.

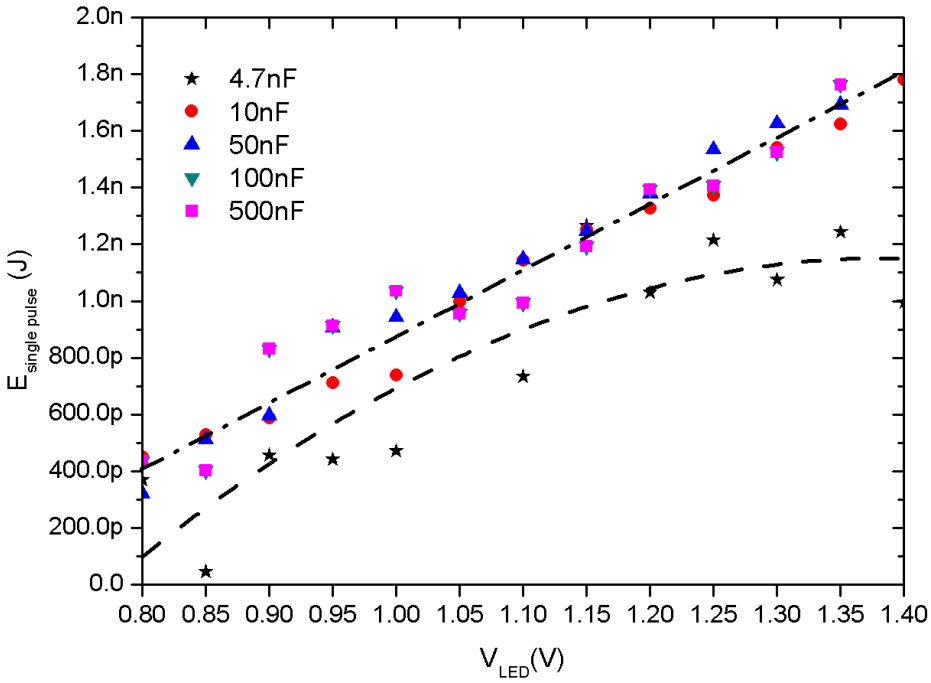

Figure 6.8. Single pulse energy delivered to the LED as a function of LED open circuit voltage and capacitor size

i.e. the LED voltage prior to the boosting transmission, as seen in Figure 6.8. Under these conditions, the size of the external boosting capacitors does not have an effect on the initial pulse of a transmitted symbol, although the following pulses experience drastic drops as the storage capacitor becomes slower. This is attributed to the switch resistance being the limiting factor in current discharge, as the PMOS discharge path is estimated to have a resistance of 800 Ω.

6.3. Detection of Optical Transmissions

The requirements for the optical detection circuitry are as follows.

- Considering 1 to 2.5 mW peak power and 20% electrical to optical conversion ratio, the receiver must be able to pick up 1 μs wide pulses of light having a peak power of 0.2 to 0.5 mW at contact distance. The receiver is to operate at near field (> 1 cm) or beyond (1 cm – 10 cm) to be practical. The expected reception

will result in around 10 nA - 100 nA photocurrent to be generated within the receiving PIN photodiode.

- The chip is intended for operation under sunlight where ambient illumination levels are multiple orders of magnitude greater than the optical signal coming from the LED. Therefore the photodiode receiver must have very high DC rejection. Indoor operation requires the rejection of power line frequencies carried by fluorescent lights.
- The detector must be low cost and easy to integrate with a readout scheme, such as an FPGA.

As a solution, a DC servo loop is implemented to cancel the DC-low frequency photocurrent in current mode. The response bandwidth of the photodiode is maximized by bootstrapping it with a unity gain follower, which equates the voltage between its terminals, ideally nullifying the junction capacitance. To do so, the bandwidth of the unity gain amplifier must be a few orders of magnitude greater than that of the photodiode, the input capacitance of the buffer must be an order of magnitude smaller, and the output resistance must be very small. Two Texas Instruments OPA 656 amplifiers are used to meet the bandwidth and input capacitance requirements, one serving as the bootstrap, and one serving as the transimpedance amplifier. A DC servo amplifier with a large integration time constant cancels out the effects of large ambient illumination levels by injecting current into the summing junction if the average voltage level of the main amplifier deviates from ground level. A T-network feedback topology is employed to maximize bandwidth. LED is connected to the microsystem with a wire and mounted outside the chamber. It is powered with the mentioned 680 nm laser giving power density of 6 mW/mm^2. Optical receiver is positioned 10 cm away from the LED to pick up the transmitted data. This range is similar to the ultra-low power microsystems that use RF transmission reported before, where reception is made with dedicated receivers. The in-house designed optical receiver consists of a PIN photodiode (OP999) and its bootstrapped transimpedance amplifier configured to have a high gain at the passband of the optical signal with transimpedance gain of 10 MΩ (Figure 6.9).

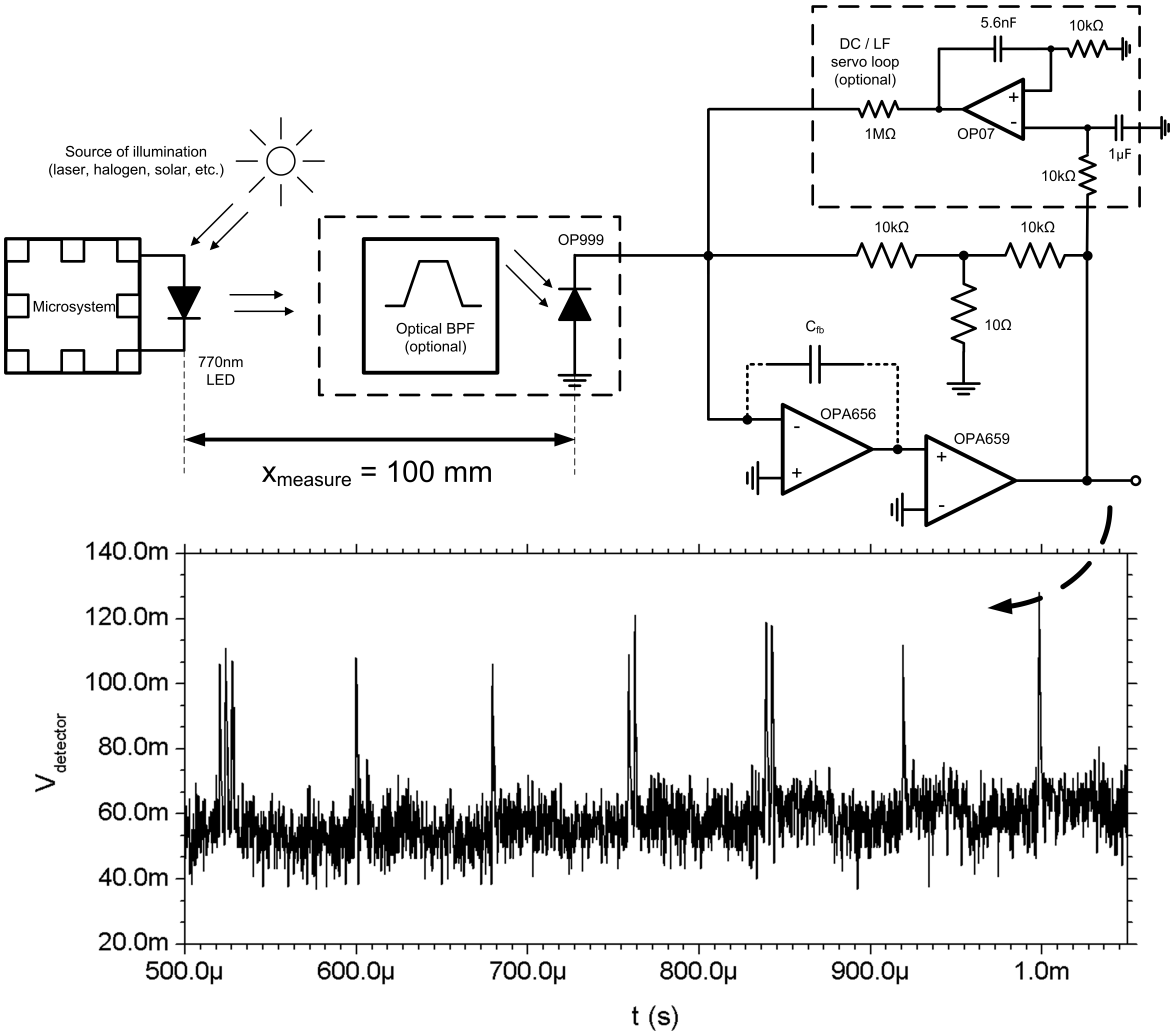

Figure 6.9. Demonstration of the optical transmission of the optically powered microsystem: optical wireless link setup with in-house built photodiode transimpedance amplifier (top) and received data at its output (bottom)

6.3.1. Energy Expenditure During Transmission

From the plot in Figure 6.9, approximately 80 μs elapses after a symbol is transmitted. In other words, the charge within the 100 nF storage capacitor is restored within this time interval and as the signal peaks are very close to one another, the assumption that the charge is restored is reasonable. The experiments were conducted under strong illumination intensities, so 50 μA recharge current is assumed to restore the capacitor charge. These figures point at an estimated voltage change of 40 mV oer

the storage capacitor, which in turn corresponds to 80 pJ expended from the storage capacitor, as opposed to 1 to 1.5 nJ recorded during the transmission of a single pulse in prior experimental steps. As the goal of the transmitter is to ideally deplete the charge from the boosting capacitor and to retain the charge of the storage capacitor, the energy efficiency of the switched capacitor boosting transmitter can be found by:

$$\eta = \frac{E_{transmit}}{E_{lost} + E_{transmit}} = 0.926 \tag{6.1}$$

6.4. Temperature Sensor Characterization

For testing the temperature sensor, the chip is placed into the thermal chamber and the DUT setting register is programmed by an FPGA. As the temperature is set by the operator, waiting for the chamber temperature to settle is crucial to minimize fluctuations and also to allow the die temperature to settle to a final value. A reasonable time for the control loop to settle to within ±0.05 °C of the desired temperature point is 10 seconds for step sizes of ∼1 °C. The readout process can then start, where the FPGA requests measurements and extracts the data serially for 100 consecutive cycles, calculates the average and standard deviation of these measurements, and displays the results at the end of the process.

The implemented SAR ADC does not support the ability to directly read or write to its register, complicating characterization. Furthermore, a silicon bug in the digital error correction logic causes the data to be corrupted if the conversion is not stopped within 1 clock cycle after the conversion is completed, and the ADC clock is unobservable from the outside. While direct control of the ADC is not possible in this implementation, a workaround was devised to extract uncorrupted data. The state-machine of the design ensures the serial output pin to be high upon reset. The conversion starts when the enable signal is pulled to high from low by the readout FPGA. As the conversion is completed, the serial output signal will fall low, as long

as the MSB of the measurement is 0, which is expected for the vast majority of the temperature range. The time between the low to high transition of the enable signal and the high to low transition of the serial output signal can be measured to calculate the average clock frequency across the 30 cycles it takes for the conversion time to complete (Figure 6.10). This process was automated within the readout FPGA to stop a faulty operation in the offset calibration logic from executing.

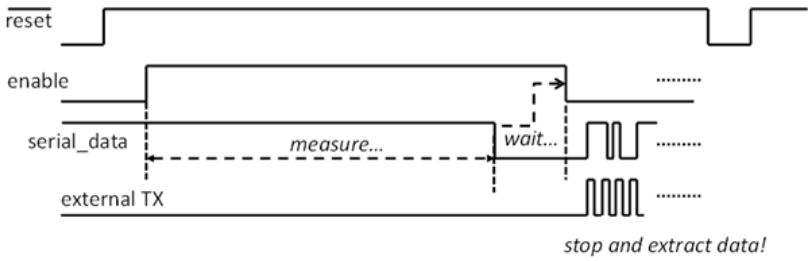

Figure 6.10. Data extraction scheme for working around the silicon bug

Each point was sampled 100 times; the mean values are displayed as a solid symbol and standard deviations for measurements are represented by an error bar. The resolutions and standard deviations from the mean measurements are tabulated in Table 6.1. Certain data points were measured at much higher standard deviations, implying that a thermometer coded current source is switching into and out of the ladder around that temperature point, causing fluctuations in individual measurements. The assumption of uniformly settled temperature does not always hold, as the temperature control loop in itself has a minimum variation of ± 0.1 °C within the insulated chamber. Outside the chamber, factors such as air flow are expected to affect the package temperature, and the thermal chamber built in-house was not tested rigorously for its insulation qualities either.

Examining the data in Table 6.1, an effective resolution of 0.5 °C on average can be determined. While the PSRR is poor in some operation modes and samples, the harvested voltage changes logarithmically with received light intensity, i.e. such supply variation is not expected under nominal lighting conditions, i.e. under sunlight or constant halogen illumination. Untrimmed temperature sensing readouts under

Table 6.1. Measured samples and average effective resolution

sample	mode	points/°C	σ	effective resolution
3	self-bias	75	50	0.66°C
	programmed	56	24	0.43°C
4	self-bias	63	51	0.81°C
	programmed	91	60	0.66°C
6	self-bias	35	16	0.46°C
	programmed	86	57	0.66°C
7	self-bias	n/a	n/a	n/a
	programmed	96	47	0.49°C
8	self-bias	74	27	0.37°C
	programmed	n/a	n/a	n/a
10	self-bias	n/a	n/a	n/a
	programmed	82	30	0.37°C
19	self-bias	n/a	n/a	n/a
	programmed	68	26	0.38°C
20	self-bias	n/a	n/a	n/a
	programmed	91	39	0.43°C

varying supply voltages for various samples are as presented in Figures 6.11, 6.12, 6.13 and 6.14.

6.5. Conclusions

The fabricated samples were tested to be functional at the system level, consuming total currents closely predicted by simulation models in self-biased mode. Systematically larger bias currents are observed in digitally programmable current setting mode that was not predicted by neither corner simulations nor Monte Carlo simulations. Transmitter oscillator works slower than expected, though adequate for the

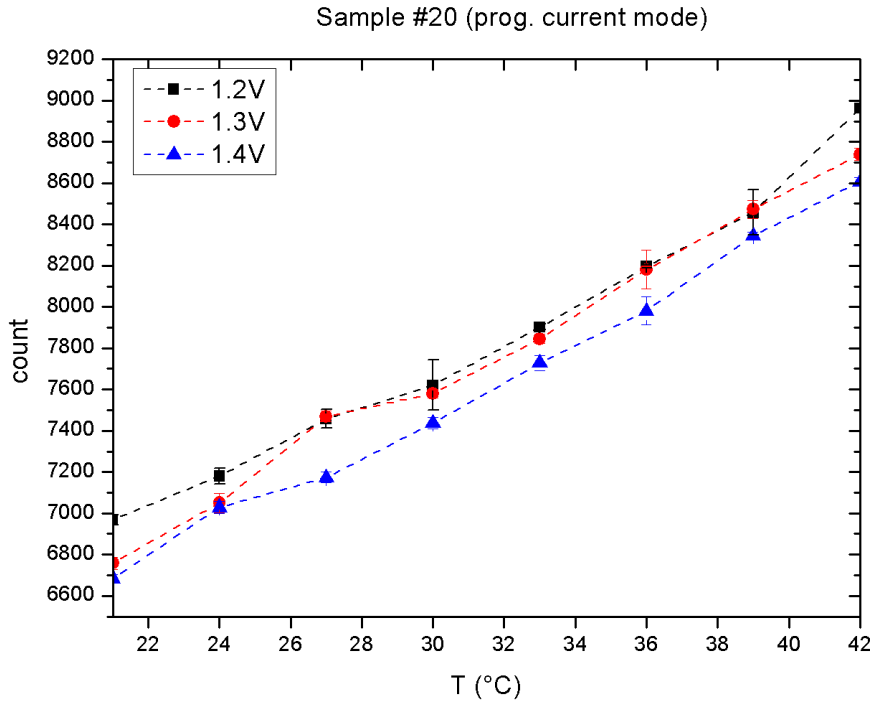

Figure 6.11. Results for sample 4, user programmed bias current settings (C000 1800)

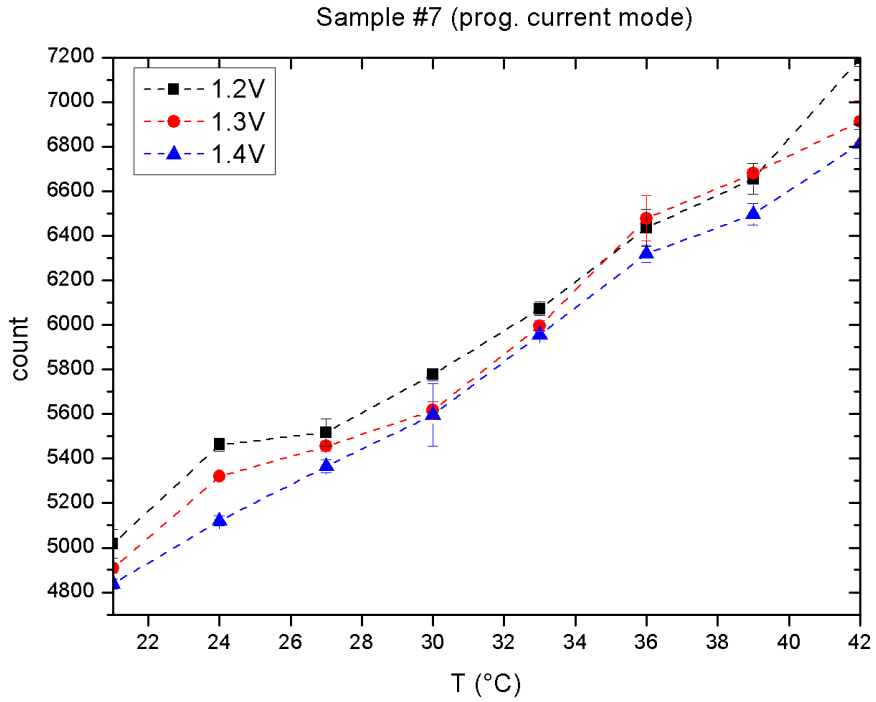

Figure 6.12. Results for sample 7, user programmed bias current settings (C000 1800)

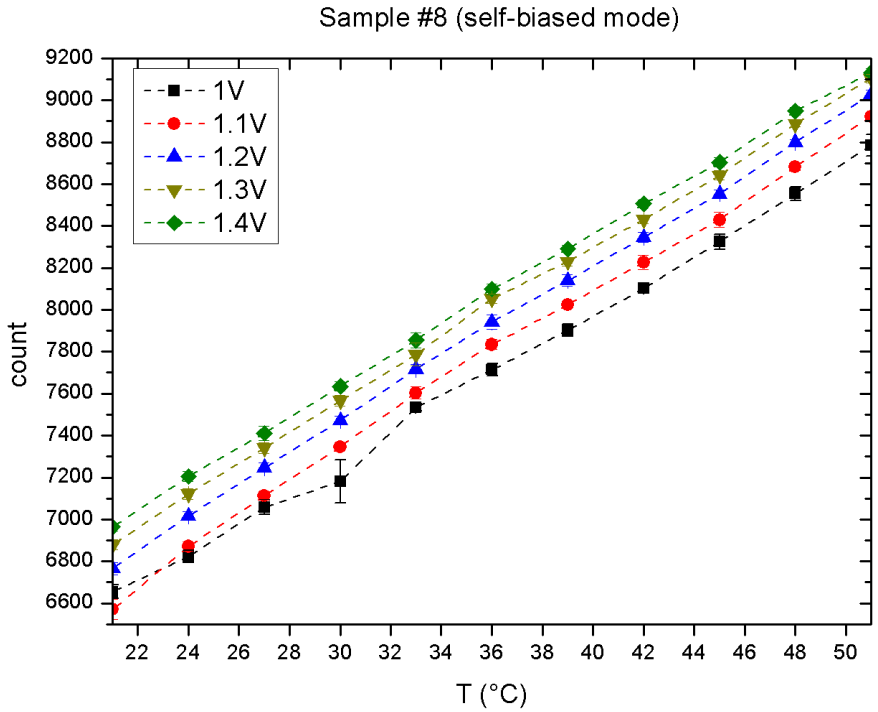

Figure 6.13. Results for sample 8, self-biased current setting (C000 0000)

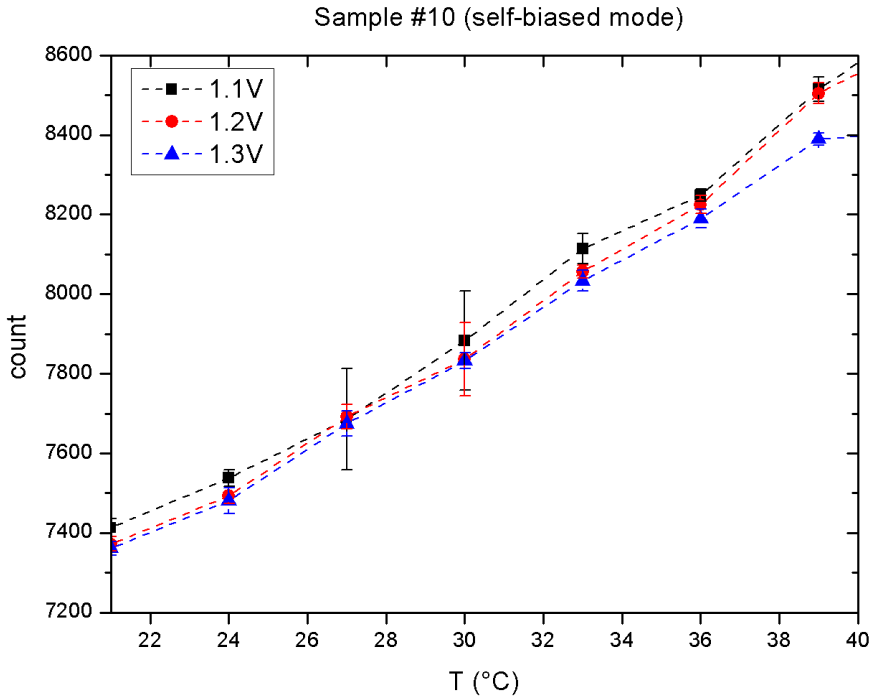

Figure 6.14. Results for sample 10, self-biased current setting (C000 0000)

purposes of our design. About 6 μW total power consumption is measured, enabling the device to be able to operate under illumination conditions equivalent to direct sunlight exposure. Optical power was delivered with laser and halogen light sources, under which the device was able to sense temperature and transmit the recorded sensor data optically. The optical emissions were detected by a photodetector circuit built in-house from a distance up to 10 cm for an energy consumption of 1 nJ/bit, which is comparable to or better than transmitter designs published for energy harvesting designs confined to millimeter-scale dimensions. A more sensitive, commercially built receiver may extend the reception range. The integrated smart temperature sensor can have a resolution of as low as 0.4 °C as expected from system level noise simulations, but device to device variations result in an average resolution of 0.5 °C. Supply rejection of the design may be improved by incorporating an low drop-out (LDO) voltage regulator, which would require additional area and power consumption. As a result of the improvements introduced in Chapter 5, a functional and efficient energy harvesting millimeter-scaled integrated smart temperature sensor is achieved, proving the use of the LED highly suitable for the purpose.

7. CONCLUSION

7.1. Overview

Miniaturization of smart sensors requires batteryless, energy harvesting operation if the aim is to realize millimeter-scaled devices, as the inclusion of batteries increases the overall system size drastically, drives up the costs and limits the lifetime of the device to that of the battery. The most severe impact of miniaturization is on the reduction in the overall area of the energy harvesting facilities incorporated into the microsystem, imposing a hard limit to what can be done within the design by limiting the power and energy available to the device. Delivering the most power per area and volume compared to other alternatives, photovoltaic energy harvesting is a first choice in maximizing the harvested energy at the smallest area. However, this occupies expensive on-chip resources that could be used for enhancing the functionalities of the design. As a result, dedicated, separate dies consisting of functional blocks and photodiode arrays for harvesting optical energy are proposed. Photovoltaic energy harvesting in standard CMOS processes is severely limited by suboptimal process parameters, such as inadequate junction depths, as well as physical limitations, such as the low bandgap energy of silicon. The low voltage problem is particularly limiting if the microsystem is to interface with the outside world by means of sensors, where analog quantities must be converted to digital in order to be processed, stored and/or transmitted. The low voltage can be boosted to adequate levels at severely reduced conversion efficiencies, wasting the precious, scarce energy resources available to the system that was gained by maximizing the area of the energy harvester in the first place. Therefore, moving away from relying on on-chip or off-chip silicon photodiodes to other semiconductors that can harvest energy more efficiently becomes a rational choice as the demands on the microsystem becomes non-trivial, such as sensing, processing and transmitting data on environmental variables. In addition, as the microsystem is limited to millimeter-scale, RF domain transmission tends to be inefficient since the antenna sizes realizable on chip are much smaller than half the wavelength of the transmission frequency. Off-chip antennas can be realized with optimal sub-

strates and metallization as opposed to on-chip antennas, but the size limitation is still a problem if the transmission wavelength is much greater than the antenna size. The proposed approach in this work aims to circumvent the obstacles imposed by miniaturization by using a single light emitting diode to harvest optical energy and transmit optical data. The AlGaAs LED die has an area of 0.1 mm2, very suitable for data transmission, much more efficient than standard CMOS photodiodes in terms of optoelectronic conversion efficiency, and provides higher voltages at its output that can be used directly, without having to boost it and sacrifice energy in doing so. The first generation design was built to prove that the LED under sustained illumination can be switched from energy harvesting mode to transmission mode, using a charge pump based transmitter. The second generation design integrates a temperature sensor into the existing energy management design, proving that essential analog blocks for sensor design, such as bandgap references, amplifiers, oscillators, can be powered directly from the voltage harvested from the LED. The third generation design features an inverter based, scalable switched capacitor voltage boosting transmitter that can transmit trains of optical pulses in rapid succession in an efficient manner. The capacitors are charged directly from the LED current, which means that efficiency wasting intermediary stages can be thrown out. Moreover, an ultra low power, ultra low energy temperature sensor is devised, creating a smart temperature sensing microsystem that consumes 6 μW during measurement, with an energy consumption in the order of 1 nJ/conversion, and transmit sensor data with 1 nJ/bit for ranges up to 10 cm, which are all comparable to or better than published energy harvesting miniaturized designs. The design features digital offset correction and partial measurements that update the changes from the last full measurement. The partial update scheme relies on the fact that the environmental temperature is a quantity that changes slowly and therefore needs only small updates that signify deviations from the original measurement. This reduces the number of conversion cycles, effectively reducing the energy consumption per measurement. The transmission of the partial updates is also critical in saving energy, as it takes comparable amounts of energy for one full conversion and the transmission of one bit of the converted word, it is important to save on the amount of bits transmitted.

7.2. Future Work

The proposed solutions to the problems faced in the realization of miniaturized energy harvesting microsystems can be taken one step further by analyzing the light spectrum of the targeted source of optical power and choosing a LED with an absorption spectrum that matches closely to that of the light source. As the CMOS die occupies an area of 1.5 mm $\times$ 1.5 mm, the LED die size can be increased to similar magnitudes, in effect reducing the minimum level of illumination necessary for device operation. The temperature sensor architecture can be modified to realize a hybrid "zoom ADC" architecture, where a SAR converter quickly completes the coarse conversion after which a fine ADC, such as an incremental or dual slope design, can produce more precise measurements at a slower rate. The coarse conversion would dramatically reduce total time as well as the dynamic range necessary for the converter, and optimizing the division of bits between coarse and fine converters can yield a very high performance design. The transmitter consists of individual transmission units with adjustable signal strengths and outputs that can be summed in current mode, which means that consecutive pulses with variable amplitudes can be transmitted. This allows not only pulse coding schemes in transmission, but also amplitude modulation schemes; therefore bits carried by each train of pulses can be improved significantly, further increasing the energy efficiency of the transmitter.

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APPENDIX A: TRANSMITTER DESIGN DETAILS

In order to force current into a LED it has to be forward biased; i.e. its open circuit voltage must be exceeded. Open circuit voltage is defined as the potential at the p-n junction where no current flow into or out of the junction occurs. In an ideal diode, the current values for conditions below open circuit voltage would be zero, however thermal and optical electron-hole pair generation processes ensure that there exists a small current generated by the diode depending on the energy absorbed from external sources. Under illumination, additional electron-hole pairs are generated and are swept away from the space charge region by the built-in potential, which results in a net current flow. This net current flow, which is in direct relation to the optical generation process, pushes the open circuit voltage further away as the illumination increases which means that the point where the net current into or out of the junction becomes zero occurs further away from the dark conditions. Below the open circuit voltage the LED supplies current into the circuit whereas above it drains current from the circuit. In order to go from supply regime to drain regime the open circuit voltage has to be exceeded, but as the LED can only supply as much as its open circuit voltage assuming zero current load this requires the necessity of a voltage boosting scheme. The potential barrier of the LED under illumination has to be exceeded in order to forward bias the LED strongly enough to conduct appreciably large amounts of current that will allow practical detection. A switched capacitor voltage booster is very similar to charge pump in principle, but different in execution that it provides an instantaneous voltage pulse instead of sustained delivery of current as in conventional charge pumps. The conventional charge pump takes numerous cycles of switching small capacitances to transfer small amounts of charge to a large capacitor or a current load at each cycle. The switched capacitor voltage booster allows the charge to trickle from the photovoltaic cell into relatively larger capacitors connected in parallel, and connects them serially in a single cycle to create an instantaneous boost in output voltage. In a sense, the proposed architecture resembles a charge pump operated at diametrically opposite parameters to a conventional charge pump.

The current load limited voltage peaking will now be explored. The conductivity of the switches connecting the capacitors change at a finite rate, as a result the effective capacitance. Considering the switched capacitor boosting transmitter as a parametric amplifier where the capacitance parameter of a passive circuit is varied to create signal amplification, the capacitance can be modeled as:

$$C(t) = C_{harvest}\,(1 - k \cdot x(t)) \tag{A.1}$$

In Eq.(A.1), $x(t)$ is a switching function that describes the time related change in the capacitance, and k is the factor by which the total capacitance changes;

$$\begin{aligned} k &= 1 - \frac{C_{transmit}}{C_{harvest}}; \\ C_{harvest} &= C_{storage} + C_{boost}, \\ C_{transmit} &= \frac{C_{storage} \cdot C_{boost}}{C_{storage} + C_{boost}} \end{aligned} \tag{A.2}$$

$x(t)$ can simply be modeled as a step function, or as a ramp function $r(t)$ with a rise time of T_0 to model a more graded transition form $C_{harvest}$ to $C_{transmit}$;

$$x(t) = \frac{r(t) - r(t - T_0)}{T_0} \tag{A.3}$$

In addition, the LED current switches directions when the open circuit voltage is exceeded. As a result, a certain amount of charge has to accumulate within the depletion region before the voltage of the diode starts to change. Assuming a step input current I_F is applied, the transient diode voltage behaves as follows:

$$v_D(t) = \frac{kT}{q} \ln\left(1 + \frac{I_F}{I_0}\left(1 - \exp\frac{-t}{\tau_c}\right)\right) \tag{A.4}$$

As a result, we have time dependent capacitor and voltage quantities determining the current flowing into the diode:

$$i(t) = \frac{\partial C(t)}{\partial t} \cdot v_D(t) + C(t) \cdot \frac{\partial v_D(t)}{\partial t} \tag{A.5}$$

Recognizing that $i(t)$ is defined by the diode equation we get:

$$I_0\left[\exp\left(\frac{v_D(t)}{V_T}\right) - 1\right] = \frac{\partial C(t)}{\partial t} \cdot v_D(t) + C(t) \cdot \frac{\partial v_D(t)}{\partial t} \tag{A.6}$$

Plugging Eq.(A.1) and Eq.(A.4) into Eq.(A.6) gives a solution to the current injected into the diode during the transmission of a single pulse. Approximating the current-voltage relationship of the diode as a resistive one can simplify calculations, and as $v_D(t)$ becomes much larger than V_T, the effective series resistance of the diode determines the current flow. As a first order analysis, the nonidealities such as wire inductance, junction capacitance, and parallel diode resistance is neglected. Now considering a purely resistive load, the transmit voltage becomes

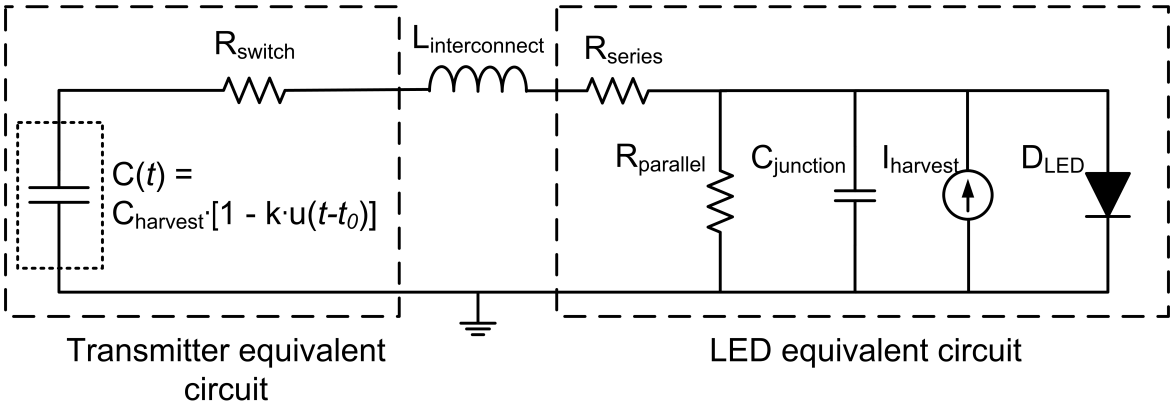

Figure A.1. Equivalent model of the switched capacitor booster and LED during transmission cycle

$$V_{transmit}(t) = V_{harvest}\left[1 - \left(1 - \frac{C_{harvest}}{C(t)}\right)\exp\left(\frac{-t}{R_{eq}\cdot C(t)}\right)\right] \tag{A.7}$$

The LED current is approximated as a resistive relationship within the forward bias region to obtain an expression in closed form and also following the fact that the voltage across the LED is much greater than thermal voltage, therefore the signals across the diode are considered as large signal quantities. Intuitively, the switch from parallel to series boosts the voltage, and as the transmitters output rises from the harvested voltage to its boosted voltage, current flows from capacitors to the diode due to the increasing potential difference, removing charge from the capacitors, which snubs the peak value of the boosted voltage (Figure A.2).

The implementation of the boosting transmitter is based on inverters. Up to three boosters can transmit a pulse in parallel, and each group of boosters is responsible for transmitting one pulse of a stream of up to three pulses. The fixed terminal of the boosting capacitor is connected to the LED while the floating terminal is either grounded or connected to supply voltage, by means of an inverter. During charge-

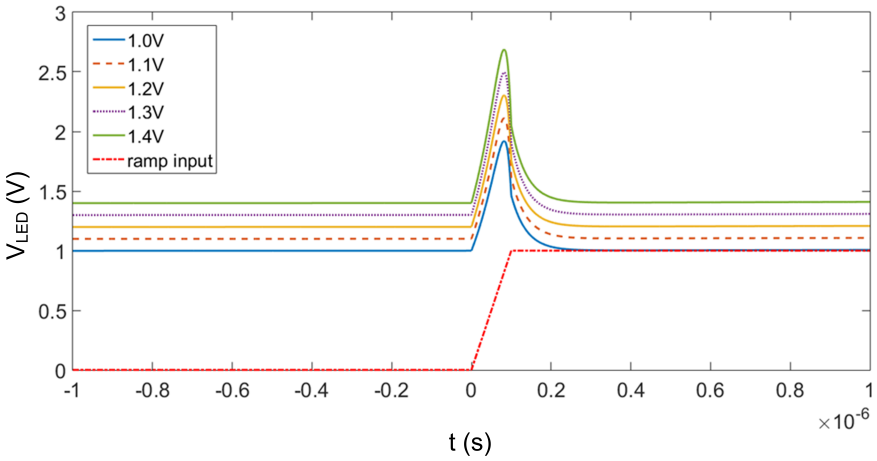

Figure A.2. MATLAB simulation of the simplified, RC discharge model

up, the LED is connected to the microsystem, and the LED current directly charges the (external) storage and (internal) boosting capacitors. To transmit, the LED is disconnected from the microsystem, and the inverter switches the floating terminal of the boosting capacitor from ground to supply rail, which is now essentially the external storage capacitor, to create the voltage boost discussed above. Each boosting capacitor consists of p-type MOS capacitor arrays with a total of approximately 430 pF, and a MIM capacitor array of 60 pF, a total of about 500 pF is available for each one of the nine booster units. The supply switch is a PMOS pass transistor drawn to 200 μm / 0.2 μm width and length respectively, and consists a low resistance path during charge-up. The inverter is heavily low skewed, using a 10 μm / 0.2 μm PMOS to 100 μm / 0.2 μm NMOS ratio. The wide NMOS again ensures a low resistance path during charge up whereas the narrower PMOS provides a certain limit to the current flowing into the LED during transmission, stretching the pulse duration.

APPENDIX B: TEMPERATURE SENSOR DESIGN DETAILS

The temperature sensor is desired to resolve 0.1 °C within a range of 0 °C to 100 °C. At that range, with a junction ratio of 1:24 and 1:1 bias current ratio, the V_{BE} ranges from 79 mV to 108 mV; with V_{BE1} ranging from 620 mV to 380 mV, and V_{BE2} from 700 mV to 490 mV. The LSB voltage the DAC has to produce is therefore approximately 30 μV to achieve 0.1 °C resolution. Note that the minimum necessary resolution goes from 10-bits to 14-bits if the 700 mV to 380 mV range is to be resolved directly with the same resolution, forcing architectural changes to be made, complicating the design further and increasing the power consumption of the system. The proposed design reduces the necessary dynamic range by more than 10 times achieving the same absolute LSB at 3.5 bits less than what is necessary for a conventional design for the temperature range in question. For the military grade temperature range the reduction in dynamic range necessities is 24 times, a 4.6 bit improvement. The drastic drop in necessary bits allows ADC architectures other than integrator based designs to be used for the purpose of high resolution temperature sensing, for example, a SAR ADC as featured in this work. The advantage gained is also in terms of conversion speed, taking N cycles long instead of $2N$ cycles, and the resulting energy/conversion efficiency. The proposed architecture can be extended to measure multiple p-n junction arrays distributed across a die in quick succession, routing the base currents to desired p-n junction arrays, respectively. This would allow rapid thermal monitoring of multiple on-chip sites using a single ADC which may be desirable for designs with very high density of integration such as processors, where temperature monitoring has to be fast enough to follow the rapid changes of local temperatures of different blocks. A high resolution integrating temperature sensor would take measurement times in the order of 10th of seconds to seconds to do so, which is not fast enough. Another field of application would be solid state wind direction sensors, where the temperature gradient of the chip is measured by multiple sensors. Instead of having multiple ADCs for each site, the p-n junction arrays can be

multiplexed to interface with the SAR ADC one at a time, measuring each site at a kHz rate, producing high resolution, high data rate output using a single ADC.

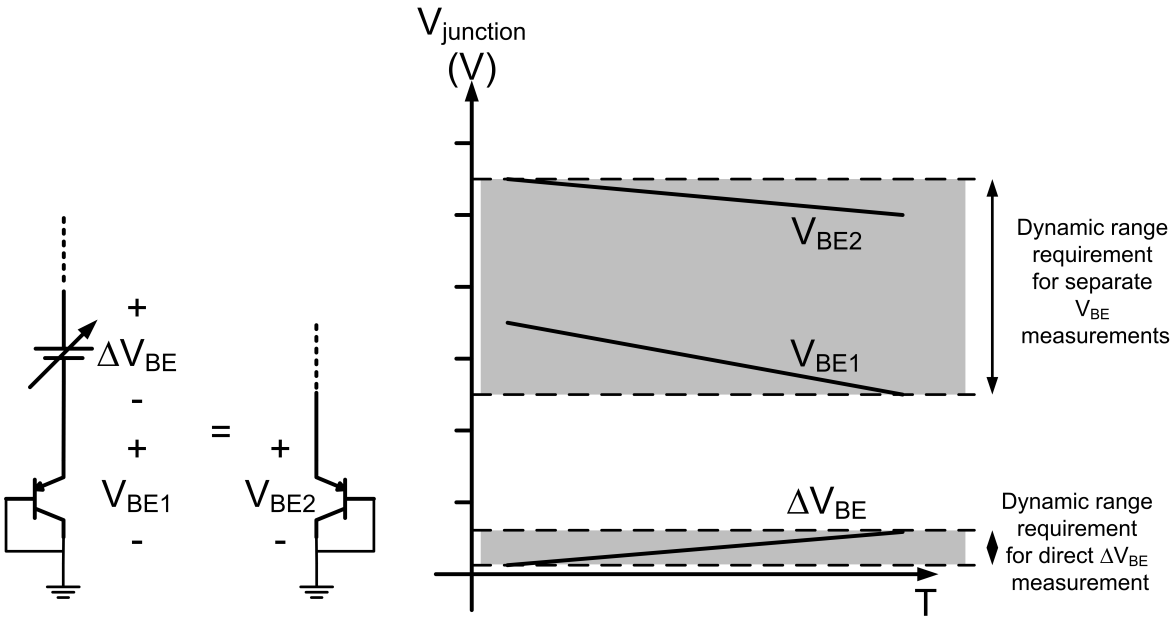

Figure B.1. Sensor concept described in this work

Biasing the bipolar junctions at ∼1 μA reduces the errors introduced by base resistance along with keeping the power consumption low, which are both desirable goals. The proposed current DAC should steer 0-1 μA to the reference resistor in series with the Q_1 junction. The voltage drop across the reference resistor should be kept in mind as a primary design constraint because that is where the V_{BE} is generated. Using the same type of resistors on chip and arranging the resistors so that they are in close vicinity and track with gradient variations, the voltage across the reference resistor can be ensured to be inside a certain range. Thus, the design starts with this parameter in mind, starting from the design of the sub-bandgap generator and bias generation circuit, and the total current that is to be drawn by the circuit blocks.

B.0.1. Sub-bandgap Reference

Starting from a sub-bandgap reference architecture that will provide the reference bias current for the remaining of the system, the junctions are biased at 500 nA at a junction ratio of 1:48 (Figure B.2).

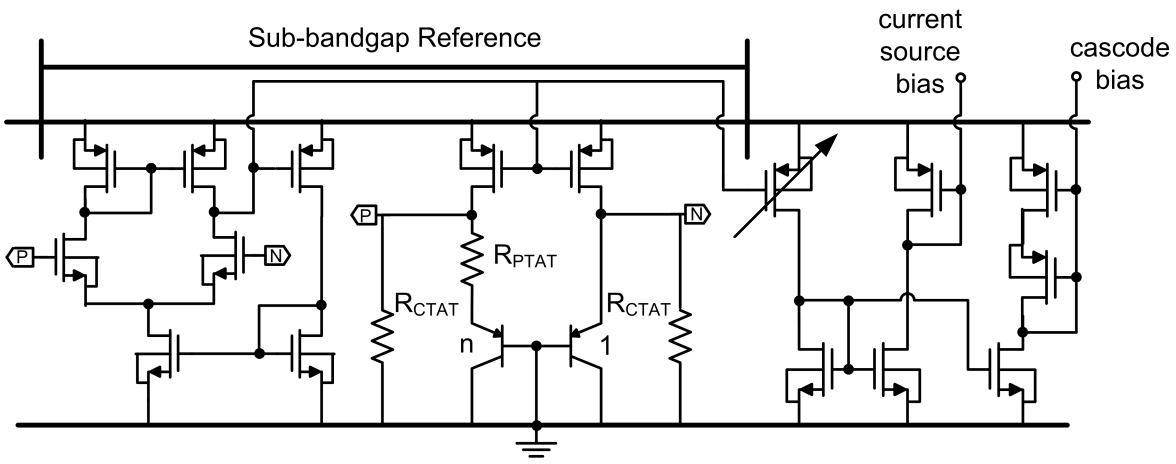

Figure B.2. Subbandgap reference used in this work

By inspection, the current generated by the subbandgap reference is dependent on the potential of the narrow junciton V_{BE2}, V_{BE}, the ratio of R_{CTAT} to R_{PTAT} m, and the absolute value of R_{PTAT}:

$$\begin{aligned} I_{ref} &= \frac{\Delta V_{BE}}{R_{PTAT}} + \frac{V_{BE2}}{R_{CTAT}} \\ &= \frac{m \cdot \Delta V_{BE} + V_{BE2}}{R_{PTAT}} \end{aligned} \tag{B.1}$$

The choice of R_{PTAT} depends on the practical limits of the R_{CTAT}; to bias the Q_1 junction at the desired current levels and have it function at the low ends of the temperature range, the R_{CTAT} and R_{PTAT} cannot be too large. Too small R_{CTAT} and R_{PTAT} values increase the current consumption. The space taken up by the resistors

is another consideration as poly resistors that are not specially treated do not exhibit huge resistances. Random variations with respect to the absolute resistance are minimized by drawing the layout at a few multiples of the minimum size allowed by the technology node. As in this design a stable current reference is desired, the R_{CTAT} to R_{PTAT} ratio m is adjusted to minimize the temperature coefficient of the reference current, resulting in an (ideally) temperature independent voltage that is determined by the projected bandgap energy of the semiconductor material at absolute zero that the architecture was used in (1.22 V in silicon):

$$V_{BG} = m \cdot \Delta V_{BE} + V_{BE2} \tag{B.2}$$

Note that the 1.22 V reference voltage requires at least 1.4 V in a classical implementation, but generating a current proportional to the reference voltage and dumping it on a resistor smaller than the reference resistor allows the designer to operate the bandgap reference circuit at lower voltages, hence the name "sub-bandgap" reference.

In addition, in the bias generation circuit the secondary effects due to the temperature dependence of the resistors are corrected for, so that the resistors within the DAC and the reference resistor have as low temperature coefficient as possible. The PMOS bias voltage from the sub-bandgap generator is used to bias comparators and oscillators in other sections of the circuit. R_{PTAT}, $R_{CTAT,1}$ and $R_{CTAT,2}$ arrays are laid out in common centroid arrangement to ensure cross-chip gradient variation tolerance, consisting of 12 units of 10:1:10 resistors in series folded in a serpentine fashion, with a unit resistance of 36 kΩ. As a result, R_{PTAT} becomes 432 kΩ and R_{CTAT} resistors are 4.32 MΩ each.

B.0.2. Hybrid DAC

Using a fraction k of the reference current generated by the subbandgap reference on the DAC that uses the same type of poly resistors as the reference generator does should give a voltage output that can be described as:

$$\begin{aligned} V_{DAC} &= k \cdot I_{ref} \cdot R_{unit} \cdot \sum_{0}^{n} b_n \cdot 2^{-n} \\ &= k \cdot V_{BG} \cdot \frac{R_{unit}}{R_{PTAT}} \sum_{0}^{n} b_n \cdot 2^{-n} \end{aligned} \tag{B.3}$$

Since R_{PTAT} used in the sub-bandgap reference generator and the unit resistor R_{unit} used in the DAC are of the same type, process, voltage and temperature related variations are cancelled out. The DAC consists of two subsections; a unary weighted section generating the 4 MSBs of the converter implemented as thermometer coded identical current sources, and a binary weighted section that generates the remaining 10 LSB implemented as an R-2R ladder (Figure B.3). Each junction of the R-2R array is supplied with current sources identical to the unary weighted section, simplifying design, introducing consistency and making it easier to match current sources as an array. By routing current into the junctions or bypassing the R-2R network to feed the current directly to the emitter of Q_1, a fine tuned voltage is generated at the output of the DAC. All current sources are identical, cascaded sources with a nominal bias current of 30 nA. The output resistance of the cascode transistor is around 4 GΩ.

The coarse steps are generated by the unary weighted current sources, while the fine steps are generated by the R-2R ladder (Figure B.4). At the end of the process, the potential across the reference resistor in series with Q_1 is approximated to the potential of Q_2, outputting a digital code that maps to the V_{BE} voltage. The DAC is designed to have an excess dynamic range to ensure that process variations do not leave the V_{BE} values of either junction beyond the dynamic range of the DAC.

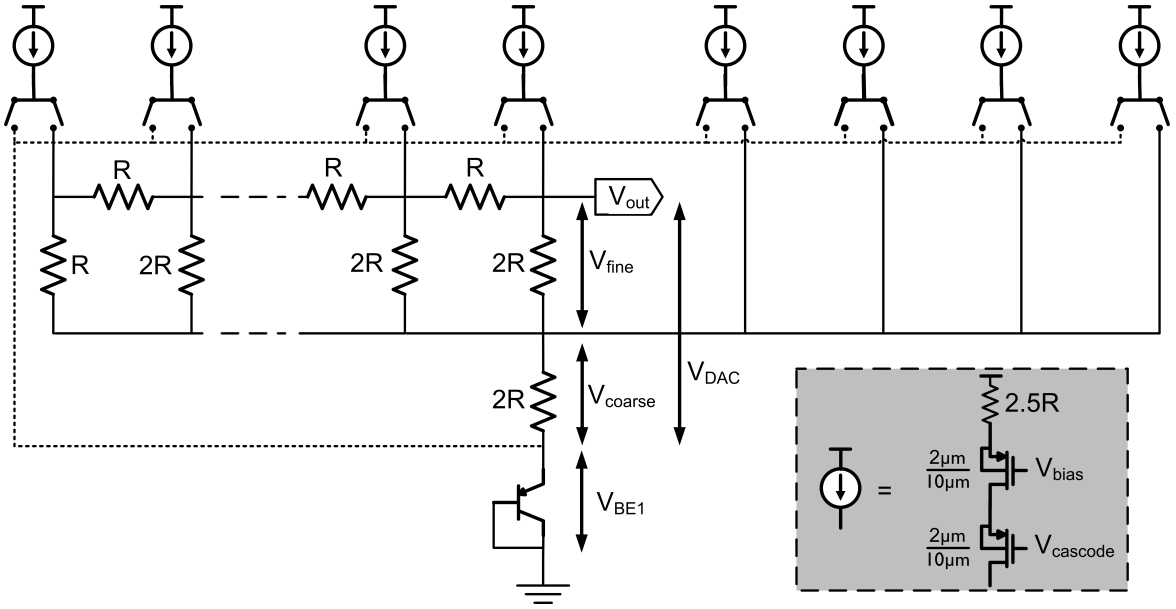

Figure B.3. DAC portion of the temperature sensor

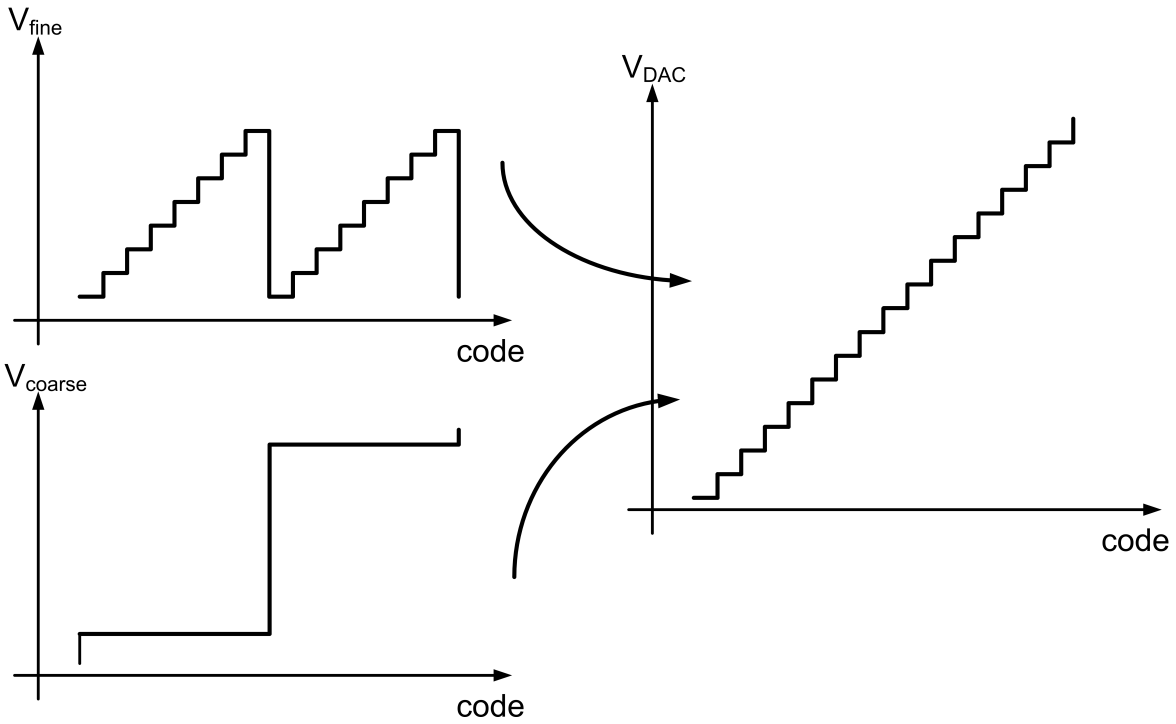

Figure B.4. Fine and coarse voltages generated by the thermometer-coded and R-2R sections are combined to cver a wide range of V_{BE} voltages

DAC biasing circuit has two modes that can be selected by writing the correct control word into the program register. The digitally adjustable mode enables the user to bias the DAC with a programmable fraction of the reference current generated by the bandgap. The alternative mode ensures that the bias current of the DAC is adjusted such that the voltage drop across the sense resistor embedded into the DAC tracks a reference voltage that is curvature corrected for temperature effects. While the bias current generated in the bandgap is dependent on the same type of resistors used in the DAC, the feedback mode is an additional measure intended for reducing nonlinearities and improving PVT tolerance (Figure B.5).

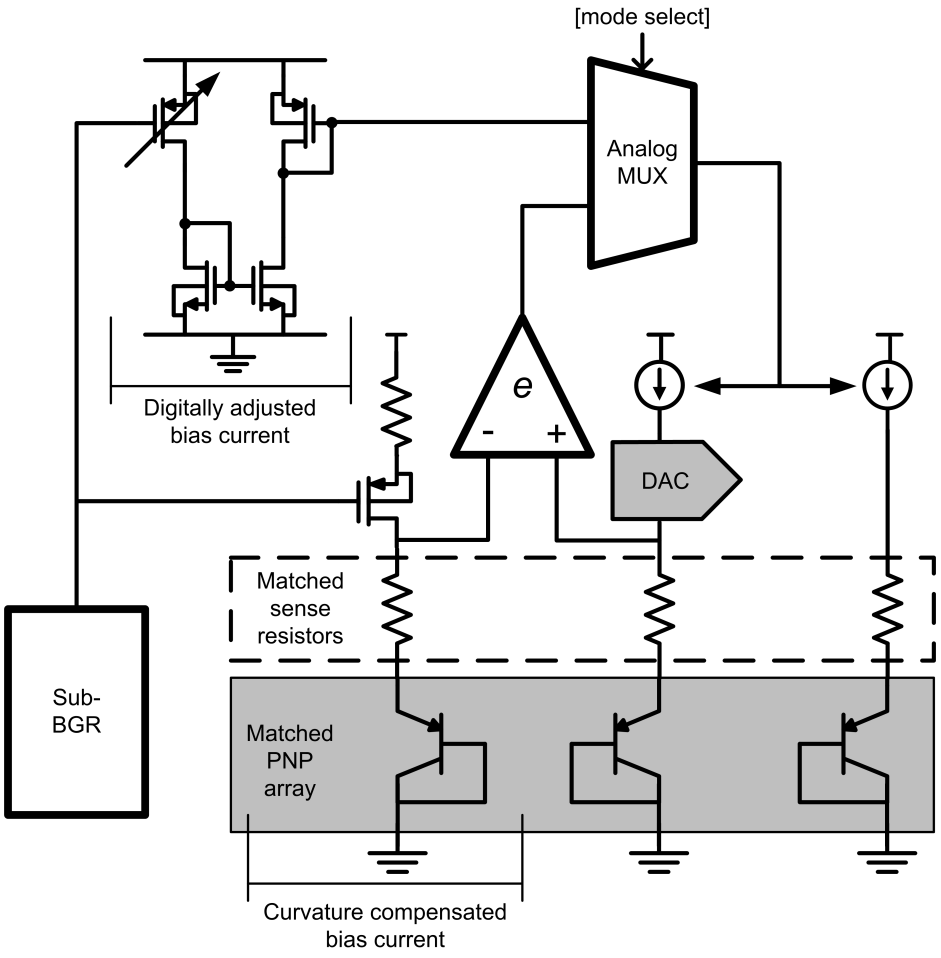

Figure B.5. Selective mode DAC biasing scheme implemented in this work

The reliance on resistors brings forward the question of noise, and therefore the architecture must be evaluated with this in mind. For starters, the noise introduced by the resistors in the DAC and the current sources will be compared. At 300 K, the noise contribution to the output of the DAC can be evaluated as follows;

- MOS channel noise contribution: g_m=550·10^{-9};
  $\overline{i^2}_{\text{n,MOS}} = 4kT\Delta f\frac{2g_m}{3} = 6.1 \cdot 10^{-27}$ A^2/Hz
- Noise contribution from R-2R network [75]: R=65 kΩ;
  $\overline{i^2}_{\text{n,R-2R}} = \frac{2kT\Delta f}{R} = 1.3 \cdot 10^{-23}$ A^2/Hz
- DAC unit current source: $I_D = 30$ nA; current noise contribution:
  $\overline{i^2}_{\text{n},I_D} = 2qI_D\Delta f = 9.6 \cdot 10^{-23}$ A^2/Hz

The total current noise power at the output of the DAC can be estimated as the sum of the contribution of resistors in the R-2R ladder, the LSB current sources biasing the R-2R ladder, and the thermometer coded MSB current sources. Noise contribution from the LSB R-2R bias sources is estimated to be similar to the R-2R resistor case [75], whereas the MSB unary weighted current sources contribute with a factor of N, where N is the number of MSB current sources routed into the DAC by the SAR algorithm.

$$\begin{aligned}\overline{i^2}_{\text{n,total}} &= \overline{i^2}_{\text{n,R-2R}} + \overline{i^2}_{\text{n},I_{MSB}} + \overline{i^2}_{\text{n},I_{LSB}} \\ &= \overline{i^2}_{\text{n,R-2R}} + N \cdot \left(\overline{i^2}_{\text{n},I_D} + \overline{i^2}_{\text{n,MOS}}\right) + 2 \cdot \left(\overline{i^2}_{\text{n},I_D} + \overline{i^2}_{\text{n,MOS}}\right)\end{aligned} \tag{B.4}$$

As evident from the above, resistor noise from R-2R network tends to dominate the total noise power. Let us further assume three temperature points, -25 °C, 50 °C and 125 °C (248 K, 320 K and 398 K respectively) to cover a wide range of temperatures not only limited to environmental and/or biomedical measurements, but also for wider, industrial range applications. Worst case noise will be for the high end range, where all MSB (thermometer-coded) DAC sources contribute to noise (4 MSB=1111)

$$\begin{aligned}\overline{i^2}_{\text{n,total}} &= \overline{i^2}_{\text{n,R-2R}} + 15 \cdot \left(\overline{i^2}_{\text{n},I_D} + \overline{i^2}_{\text{n,MOS}}\right) + 2 \cdot \left(\overline{i^2}_{\text{n},I_D} + \overline{i^2}_{\text{n,MOS}}\right) \\ &= 4.7 \cdot 10^{-25}\ \text{A}^2/\text{Hz}\end{aligned} \tag{B.5}$$

For the mid-range, the temperature is at an intermediate level and the number of MSB current sources contributing to the noise are halved (4MSB=0011)

$$\begin{aligned}\overline{i^2}_{\text{n,total}} &= \overline{i^2}_{\text{n,R-2R}} + 7 \cdot \left(\overline{i^2}_{\text{n},I_D} + \overline{i^2}_{\text{n,MOS}}\right) + 2 \cdot \left(\overline{i^2}_{\text{n},I_D} + \overline{i^2}_{\text{n,MOS}}\right) \\ &= 2.8 \cdot 10^{-25}\ \text{A}^2/\text{Hz}\end{aligned} \tag{B.6}$$

Finally at the end range, all MSB current sources are routed away from the R-2R ladder, leaving only the contributions from R-2R resistors and current sources (4MSB=0000)

$$\begin{aligned}\overline{i^2}_{\text{n,total}} &= \overline{i^2}_{\text{n,R-2R}} + 2 \cdot \left(\overline{i^2}_{\text{n},I_D} + \overline{i^2}_{\text{n,MOS}}\right) \\ &= 1.4 \cdot 10^{-25}\ \text{A}^2/\text{Hz}\end{aligned} \tag{B.7}$$

For the output resistor with a value of 2·R=130 kΩ, the above current noise will act upon this resistor in addition to its own voltage noise. The total equivalent voltage noise at the output of the DAC ranges are tabulated in Table B.1, according to ADC clock values of f_{min} = 30 kHz and f_{max} =150 kHz:

Table B.1. Total voltage noise at the output of the DAC.

	T=248 K	**T=320 K**	**T=398 K**
f_{min} = **30 kHz**	15 μV_{RMS}	19 μV_{RMS}	24 μV_{RMS}
f_{max} = **150 kHz**	37 μV_{RMS}	46 μV_{RMS}	56 μV_{RMS}

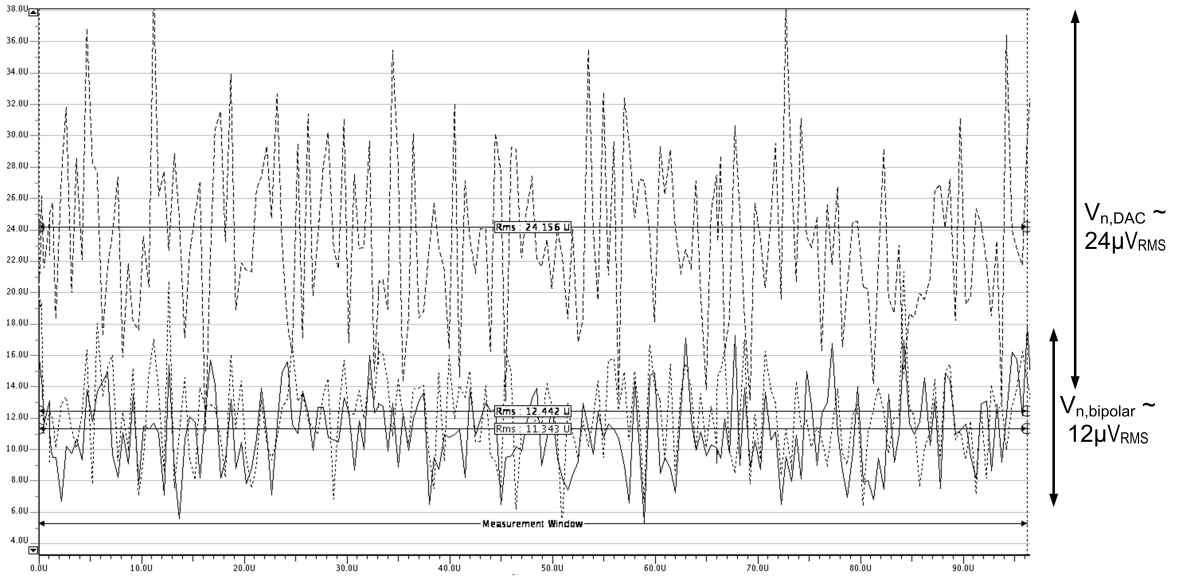

Figure B.6. Noise simulations for DAC output, V_{BE2} and V_{BE1}, showing equivalent voltage noises of 24 μV_{RMS}, 12 μV_{RMS} and 11 μV_{RMS} respectively.

With the requirement of a minimum voltage step of ~30 μV for the DAC, 0.1 °C sized bins appear viable at reduced conversion rates according to calculation results in Table B.1 and also in noise simulation results of the DAC presented in Figure B.6. However, the above calculations are performed assuming only the resistors and the current sources. The bias voltages of the current sources also have a noise component, generated within the subbandgap reference. Including the influence of bandgap reference noise worsens the effective resolution to 0.3 °C or worse, as displayed in Figure B.7.

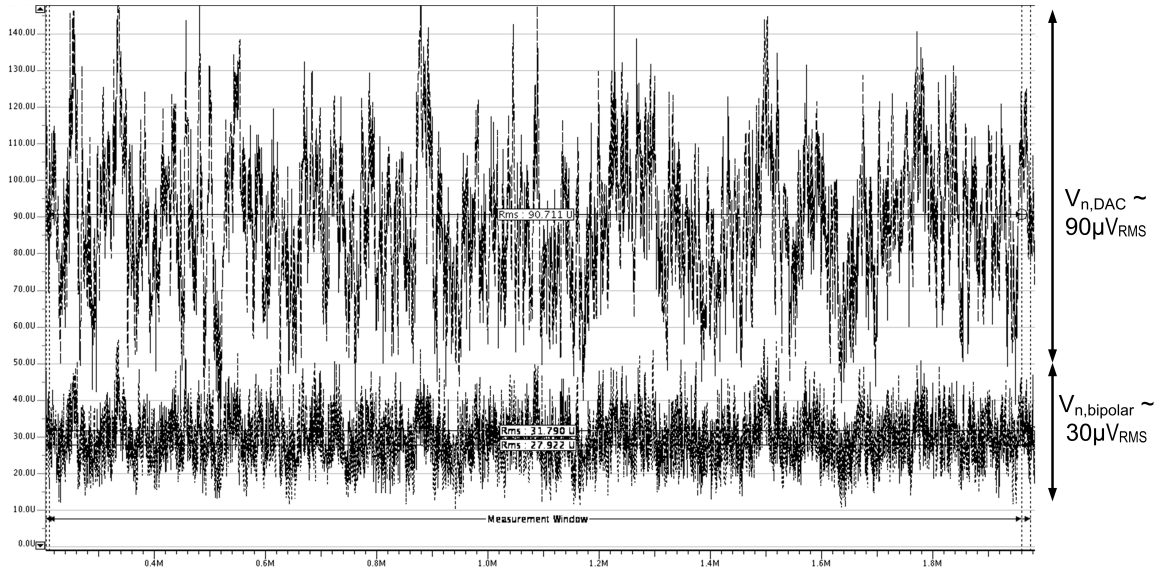

Figure B.7. Noise simulations for DAC output,V_{BE2} and V_{BE1}, showing equivalent voltage noises of 91 μV_{RMS}, 32 μV_{RMS} and 23 μV_{RMS} respectively.

Since the DAC output ranges up to $16 \times I_D \times 2R$, or about 62.4 mV, an 11-bit resolution will suffice for our purposes. However, to cover for process variations that could result in offsets or reduce the range of the DAC, more bits were implemented as a measure. Next, the proposed temperature sensor will be examined using the resolution figure of merit proposed by Kofi Makinwa, which evaluates smart temperature sensors by

$$FoM = \frac{Energy}{Conversion} \cdot Resolution^2 \tag{B.8}$$

A full conversion involves 30 ADC cycles, completing two full range measurements to obtain a digital offset correction data, whereas a partial conversion takes 7 cycles to complete. Assuming adjustable ADC clock frequencies from 30 kHz to 150 kHz, the conversion time for a full measurement is 0.2 to 1 ms, and 47 to 230 μs to for a partial measurement. The PNP core and ADC draw 1.5 μA, and the comparator uses 0.8 μA; at the nominal design voltage of 1.2 V we have 2.8 μW. For a resolution of 0.1 °C, we have 5.5 pJ/K^2 to 27.6 pJ/K^2 for full conversion, and 1.3 pJ/K^2 to 6.4 pJ/K^2 for partial updates. For more pessimistic results, assuming 0.3 °C effective resolution, the figures become 50 pJ/K^2 to 250 pJ/K^2 in full measurements and 11.7 pJ/K^2 to 57.6 pJ/K^2. For comparison purposes, 10-30 pJ/K^2 is observed in cutting edge designs, not including the power consumption of the digital back end and decimation filters used in high resolution examples, which are implemented off-chip in many examples [29].

B.0.3. Comparator

As the V_{BE} becomes smaller, the comparator requires longer time in a logarithmic relation [76]. Also, the settling time requirements increase as smaller amount of current flows into the sense node, which slows the charging/discharging of node capacitances. The comparator clocking is designed to have a certain level of self-timing where the arrival of the next clock cycle is delayed until the comparator arrives at a decision. This is implemented by gating the enable signal of the SAR register, which is propagated when the XOR of the differential outputs of the comparator becomes logic high. Since the latched comparator outputs start from ground level and converge to voltage rails upon the completion of the decision, the XOR of the two outputs go from 0 to 1. The block diagram of the multi-stage comparator is depicted in Figure B.8.

Folded cascode preamplifier consists of an input pair, a cascode stage (Figure B.9) and the bias generator that is necessary for the cascode transistors (Figure B.10). The design is fully differential, and the output node of the folded cascode is stabilized by a continuous time CMFB, adjusting the bias of the NMOS current sources of the cascode stage. Overall, the comparator draws around 700 nA, capable of operating down to 1.0 V. Designed using g_m/I_D methodology, the inversion coefficient is chosen

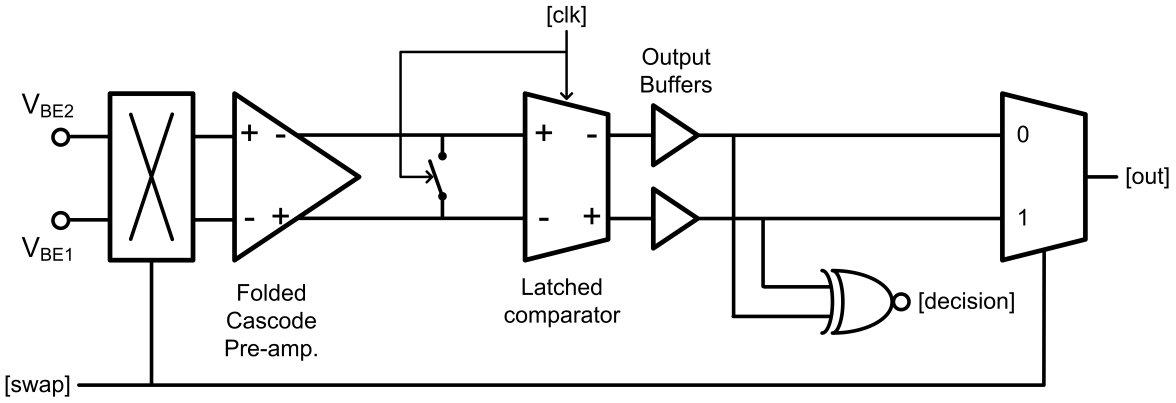

Figure B.8. Comparator chain used in the design, including the input swapping block, high gain preamplifier, latched comparator and decision logic

to be approximately 1, putting the transistors biased in moderate inversion regime [77]. The NMOS pair of the CMFB circuit that adjusts the bottom transistors of the NMOS cascode are an exception; they are designed as voltage dependent resistors and therefore in linear region.

Latched comparator follows the folded cascode preamplifier. The differential outputs of the preamplifier are shorted together during the low phase of a clock cycle, discharging the parasitic capacitances that would otherwise introduce a memory effect to the latched comparator. As the shorted differential outputs are let go, the respective nodes charge up/down to their respective levels. The latched comparator has the similar requirement of discharging the output nodes, as a mismatch of 1 fF can result in a 1 mV offset [78], in fact offset trimming for comparators regularly features digitally adjustable capacitor banks at the output nodes.

System level noise simulations for 27 °C, 28 °C and 29 °C, showing the digital outputs for each simulated point are presented in Figure B.12. 10 simulations are conducted for each temperature point, and the digital outputs are plotted. An average of 90 points per 1 °C is evident in the 14-bit measurements, with an error of 16 points on average. Following from these results, a 0.3-0.4 °C bin size can be expected from the design, placing it in the moderate resolution - ultra low energy corner of the FoM

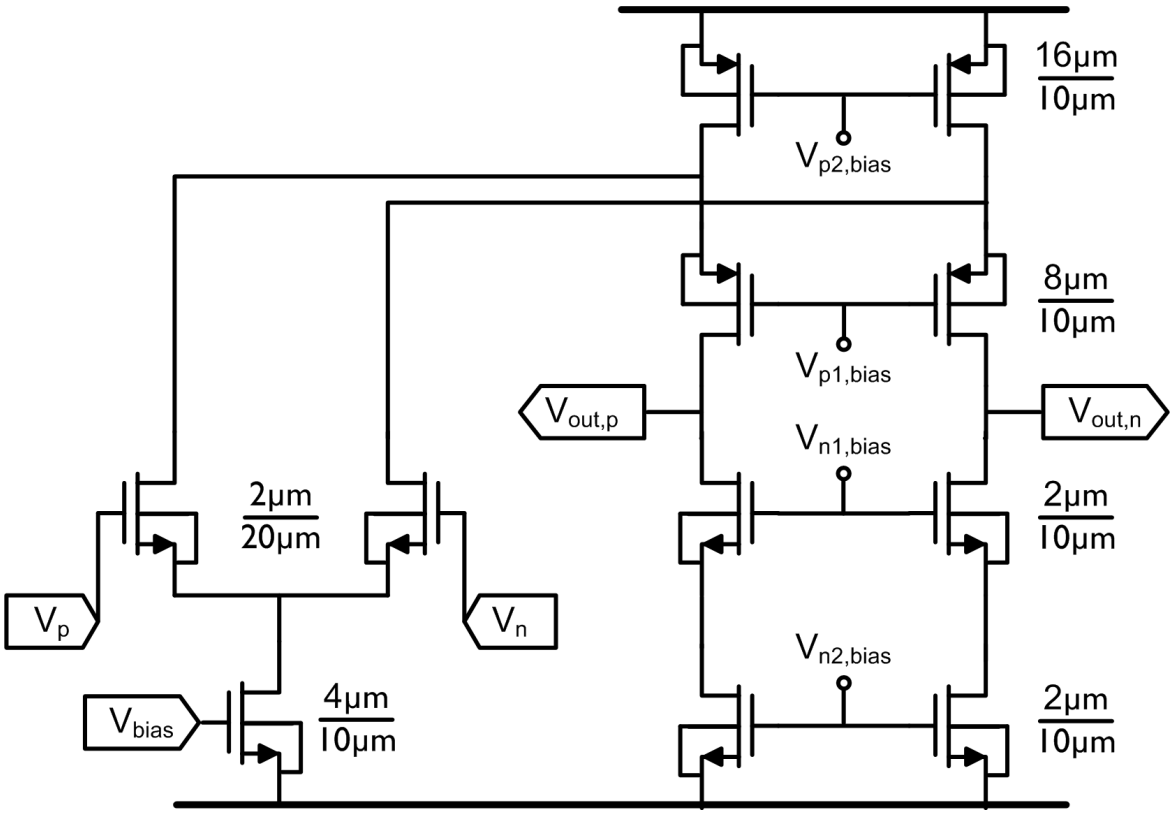

Figure B.9. Fully differential folded cascode amplifier

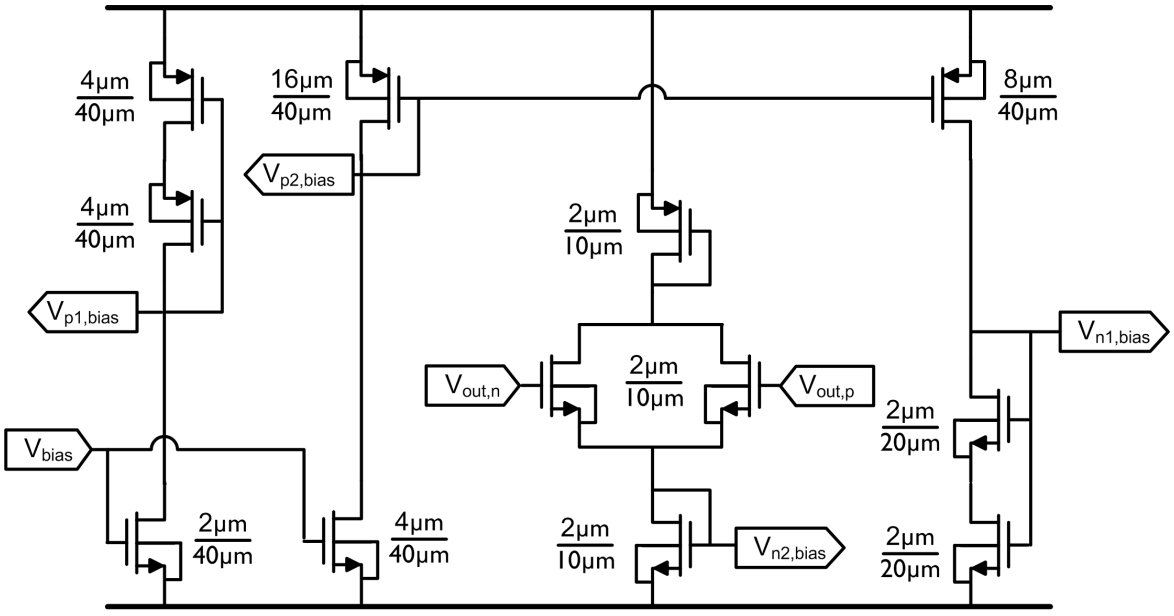

Figure B.10. Bias generator for cascode transistors, including CMFB.

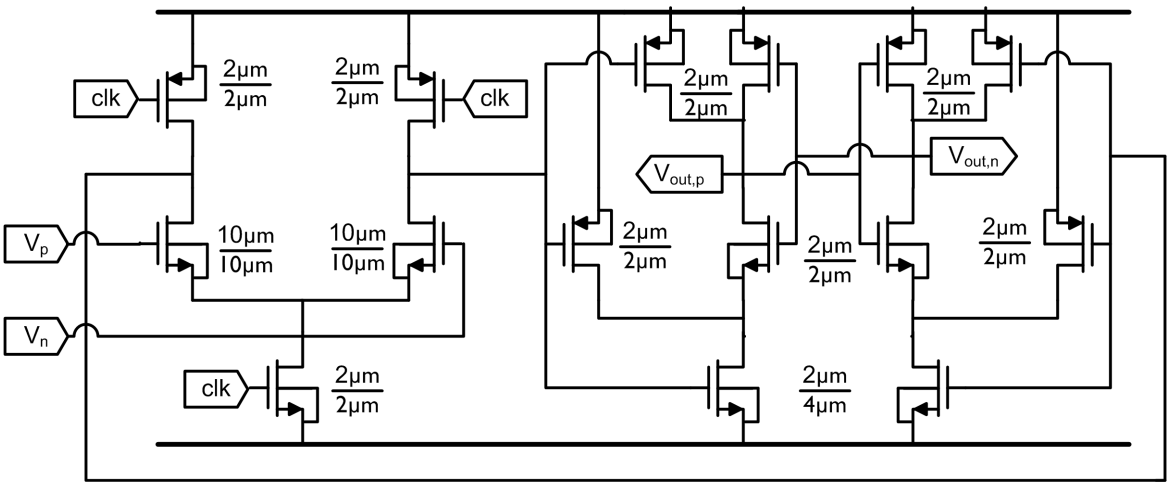

Figure B.11. Latched comparator used in the comparator chain

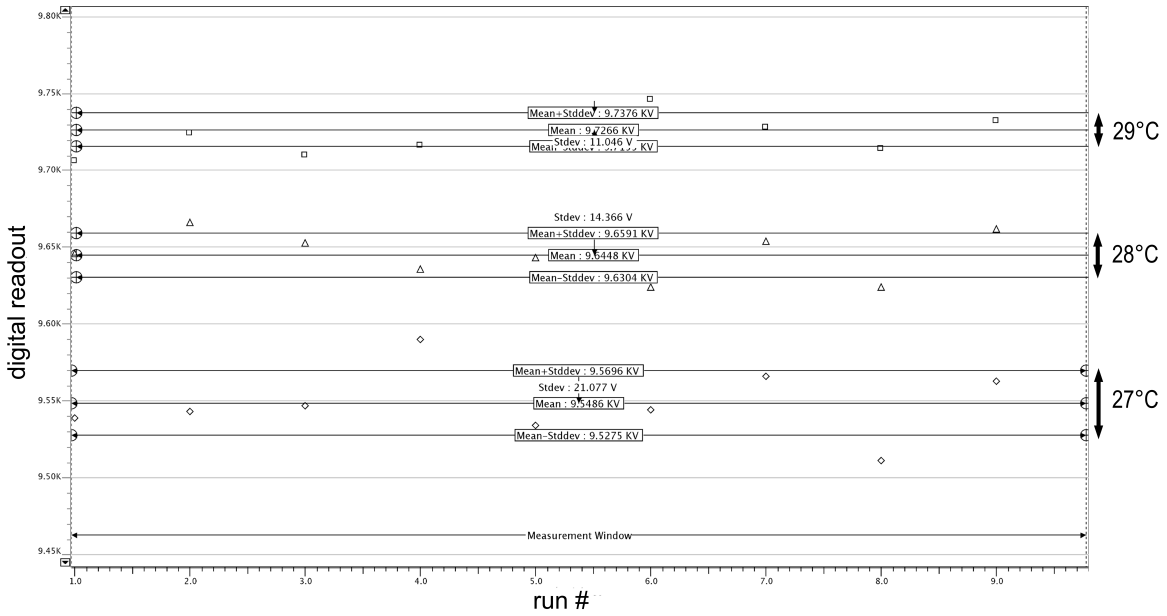

Figure B.12. Digital output of the smart sensor for system level noise simulations under 27 °C, 28 °C and 29 °C

map of published smart temperature sensors as presented in Figure B.13 [26].

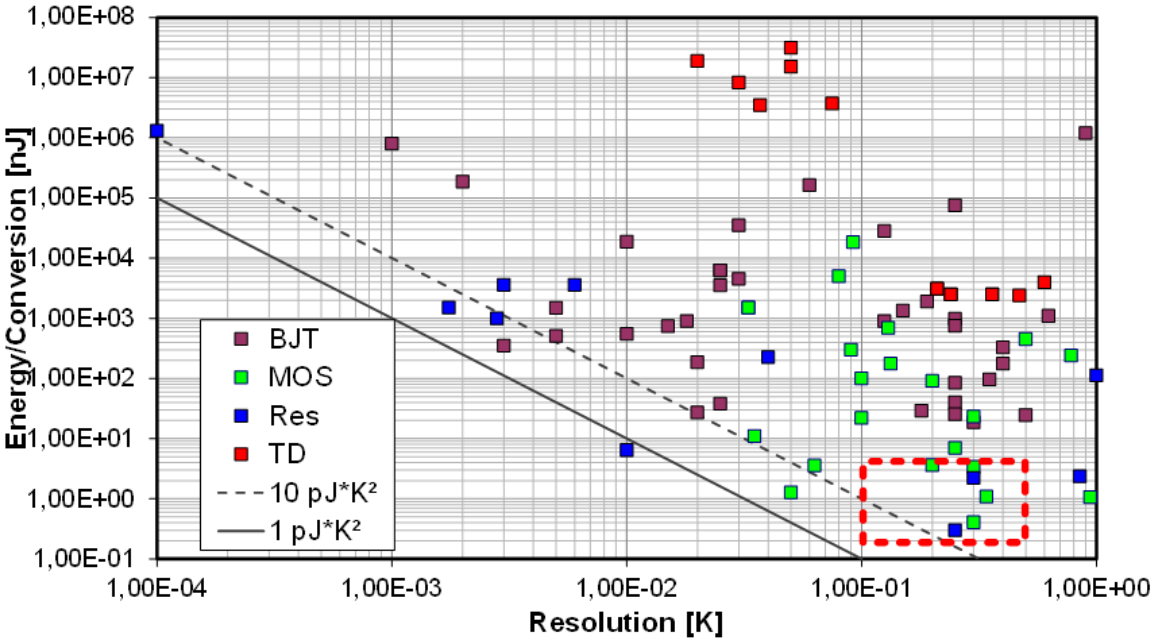

Figure B.13. FoM map of smart temperature sensors. The presented design resides within the range marked with the dashed box

APPENDIX C: DESIGN OF EXPERIMENTAL SETUP

The temperature control scheme is illustrated in Figure C.1. The high accuracy temperature measurement capabilities of the HP 34410 6 $\frac{1}{2}$ point digital multimeter (DMM) is fully exploited to provide a feedback to the PID control loop implemented in software as a LabVIEW application. The software control of PID loop parameters enhances flexibility and drastically reduces design time.

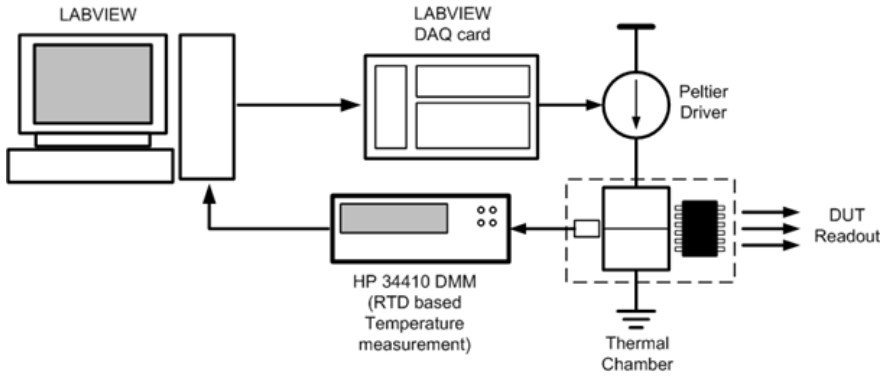

Figure C.1. Temperature control loop block diagram

The thermoelectric generator (TEG) driver is implemented as a bipolar voltage to current converter based on a Texas Instruments OPA 541, a high power FET input audio op-amp that is capable of supplying ±5 A of continuous current to the load (Figure C.2). The feedback loop of the featured bidirectional current source, also known as Howland current pump, ensures that the applied voltage is converted to a current proportioanl to the sense resistor.

The voltage to current converter is driven by the 12-bit bipolar output from the DAQ card controlled by the LabVIEW application, closing the loop. The voltage to current converter was elected to be built from scratch instead of using purpose made PWM controllers available off the shelf. The reasoning behind this is that both linear and bang-bang control of the TEG is possible by adjusting the gain of the PID loop through software, whereas with purpose built ICs the designer is limited to bang-

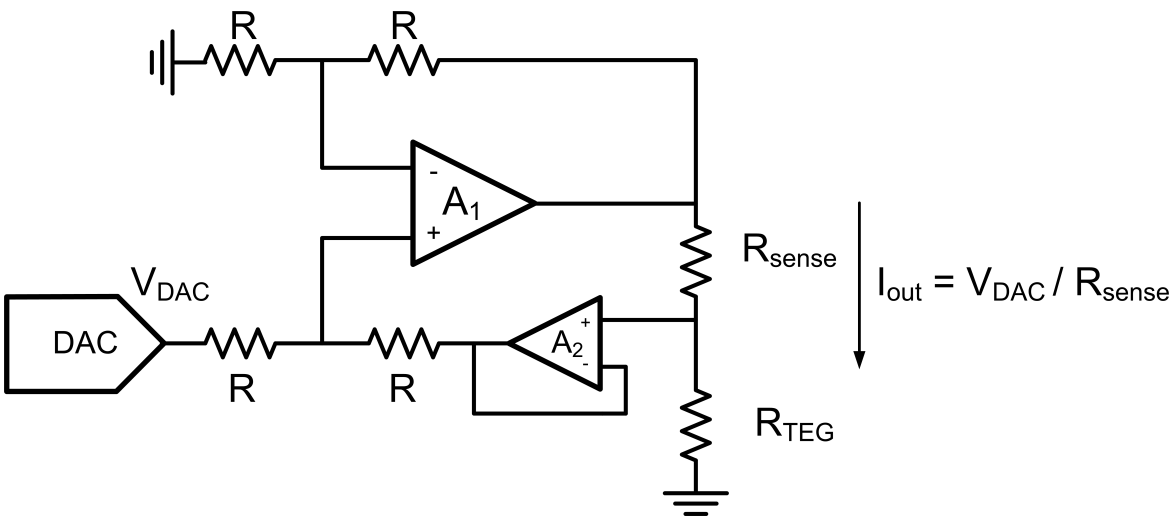

Figure C.2. OPA 541 based bidirectional current source

bang control only. Nevertheless, thermal control loop design principles hold for both discrete and integrated designs, whether the control loop is implemented in software or hardware. Valuable information pertinent to TEG control loop design is provided by various semiconductor manufacturers [79].

Thermal runaway is a problem in TEG cooler stacks; as the heat removed from the cold side is proportional to the applied current and the internal heat generation is determined by $I^2 \cdot R$. As a result, there is a bias point where the applied current heats up the device more than it removes heat form the cold side. To compensate, the PID loop applies more current in the same polarity to cool down the device, causing even more heating as $I^2 \cdot R$ heating is now dominant. A practical solution is to impose a hard limit to the swing of the current source, which is easily achievable and precisely controlled using a DAC driven voltage to current converter as opposed to a purely analog solution.

A stack of three identical TEG units is situated on top of a thick copper slab, which is placed on a fan-cooled heat sink designed for CPU cooling. On top of the TEG stack an aluminum pedestal is placed, to which the RTD sensor head is screwed tightly and the device under test (DUT) is coupled by thermal grease (OmegaTherm

OT-201). A thermally insulating block fashioned out of low density polyurethane foam covers around the TEG stack so that only the aluminum pedestal holding the DUT is exposed to the inner chamber, insulating the inside from the TEG stack and the rest of the environment. While the stacking of the TEG units is inefficient in terms of thermoelectric conversion, reaching low temperatures can only be achieved in such manner as the temperature difference between the two sides of the TEG devices can only be around 20 °C (Figure C.3) shows the temperature measurement setup used in this work.

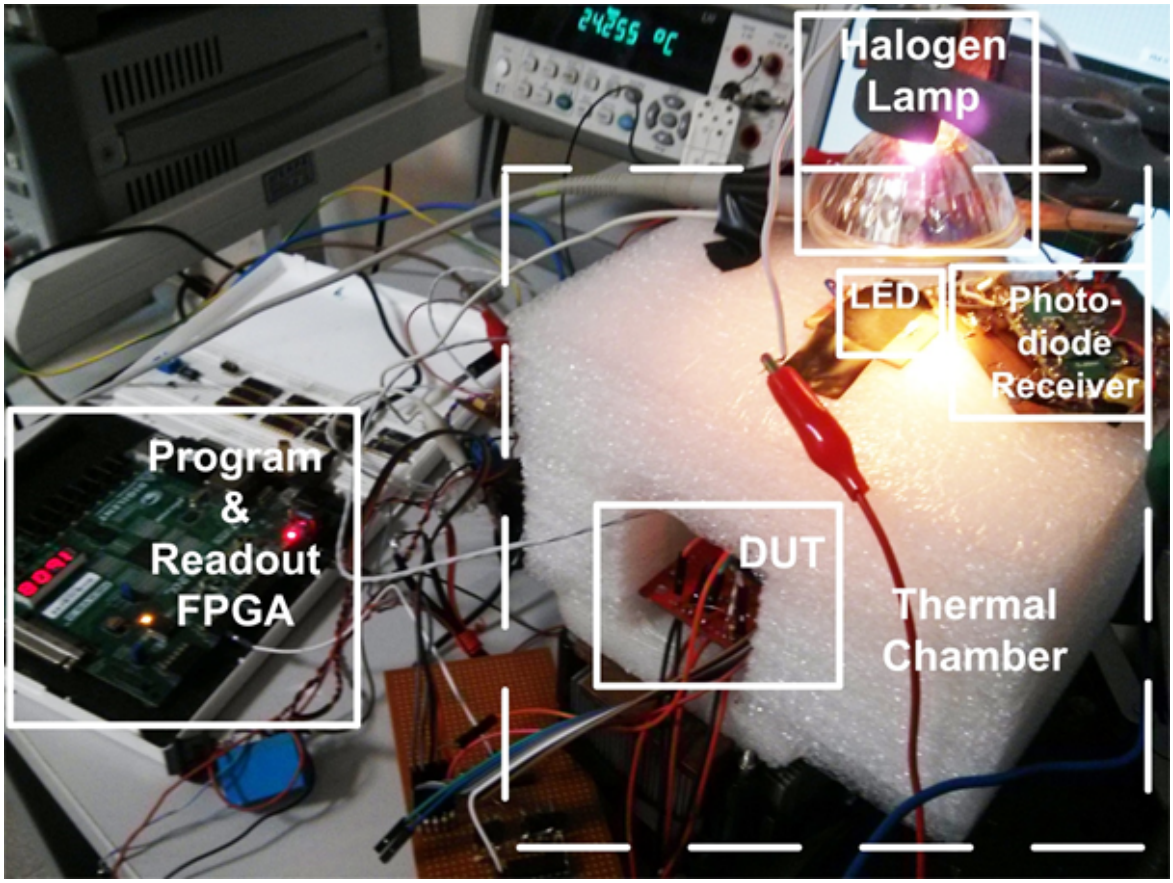

Figure C.3. Test setup